RN821X User Manual

New: 2015-05-20

Rev: 2.2

2019-07-26

Rev:2.3

2020-11-13

Rev：2.4

Renergy Technology Co., Ltd. of Shenzhen

Release Notes:

Updates in Version 1.2:

A supplement for the RN8211's unsupported functions which are explained detailedly in each module;

Corrected the default value of PC50/PC51 register in section GPIO, changed from 0 to 1;

Updates in Version 1.3:

Fixed the RSTN pin number error in the Pinout;

Deleted the description that 3v battery is not supported by VBAT in the electrical characteristics;

Modified the description of OSC_CTL2 register;

Modified the description of chapter 3.3 Clock Switching;

Modified the description of MODE1_EN and reset values, recommends that customers do not close WDT_EN and RTC_EN bit;

Increasing the description of Chapter 18 Programmable Support, advising clients to achieve IAP function by calling the library function, use Renergy's programmer to implement the ISP;

Descriptions that EEPROM and FLASH are applied to low-power conditions was added separately in section 4.3.4 and 4.3.5;

The default value of LBGR_PD register bit was changed from 0 to 1 in chapter 3.6;

Description of Package Type was added in section 1.2.8;

Description of wide operating voltage range is added in section 1.2.1;

Increasing section 1.2.8 card meter isolation scheme;

Updates in Version 1.4:

Capacity of RN8211'EEPROM was upgraded from 16KBytes to 32KBytes;

Updates in Version 1.5:

Description of LBGR operating voltage range was added in chapter 2;

Modified the description of LCD output voltage range;

Description of LBGR voltage value was added in section 8.1.4(about LCD)

Updates in Version 1.6:

Refined the definition of RN821x series model in sections 1.2.9;

Fixed the register defined error in chapter 12;

Updates in Version 1.7:

Fixed the incorrect description of TC_CCFG(the clock configuration register) bit8~bit14 in chapter 9 Timer;

Updates in Version 1.8:

Increasing the description of section about 'option byte';

Modified the description of section about WDT;

Refined the description of EEPROM and FLASH section;

Updates in Version 1.9:

The specific indicators of cpu's minimum operating voltage in the whole temperature range was added in chapter 2 electrical characteristics;

Updates in Version 2.0:

Timer Instructions were added in chapter 9;

Modified LVD_STA register in chapter 10 Analog Peripherals;

Updates in Version 2.1:

Deleted the incorrect description of P05 in chapter 11 GPIO.

Updates in Version 2.2:

Based on Chinese version V2.5, updated “1.2.9 RN821X Model Division” and “1.4 Pin Configuration” by adding information of model RN8211B and RN8213B, and “11 GPIO” on PC port configuration registers.

Updates in Version 2.2:

Add Chip Packaging Instructions

Updates in Version 2.4

Add description of Chip RN8217 and RN8213B(D)

CONTENTS

1 OVERVIEW

1.1 Summary

RN821X is a low power, high performance, highly integrated, highly reliable single-phase SOC chip, in which an 32-bit ARM Cortex-M0 core is embedded, and this product is able to meet the growing requirements for functions and performance of single-phase smart meter.

1.2 Product Features

1.2.1 Fundamental Features

- Highly integrated: 32bit ARM Cortex-M0,Measurement module, Hardware temperature compensation (RTC), The controller of LCD,EEPROM;
- Wide voltage range: Voltage range of 2.8V~5.5V to ensure the measurement's accuracy;
  Typical voltage range of CPU system is 2.2V ~ 5.5V;
  GPIO supports docking devices having different operating voltages.
- High performance: Typical CPU operating frequency is 3.6864MHz (Maximum up to 29.4912MHz);
- Low power: Typical power consumption is about 3.5mA during the single-phase Smart Meter normal operation;
  Power consumption is about 18uA when the system operates at 32KHz;
  Power consumption of the overall chip is about 10uA in sleep mode.
- High precision: The active energy accuracy is less than 0.1% over a dynamic range of 5000:1;
  Typical reference temperature coefficient through the measurement is 5ppm;
  The second pulse error of RTC is less than ± 5ppm within -25 ℃ ~ 70 ℃ and the minimum calibration scale is 0.068ppm;
- Package Type: LQFP100

1.2.2 Processor-related

- ARM Cortex-M0 core;
- The maximum operating frequency is up to 29.4812Mhz, 3.6864MHz is recommended for the single-phase smart meter applications;
- Maximum support 512Kbytes FLASH memory,100000 Programming Cycles, More than 20 years of data retention;
- Maximum support 48Kbytes SRAM,Among them, 2kbytes is used for internal cache, and 46kbytes is open to customers
- Maximum support 32KbytesEEPROM,1000000 Programming Cycle, support for byte operation, more than 20 years of data retention;（RN8217/RN8213B(D) none ）.
- Single-cycle multiplier(32bit*32bit);
- System timer is embedded in the CM0;
- 2 DMA controllers;
- Support for external interrupts and other ways to wake up;
- Complete hardware and software for the integrated development environment is provided.

1.2.3 Measure

- The active energy accuracy is less than 0.1% over a dynamic range of 5000:1;
- Typical reference temperature coefficient is 5ppm;
- Support Neutral Wire and Fire Wire dual-channel's active power, reactive power, apparent power and current

RMS simultaneously measuring;

- Support Neutral Wire and Fire Wire dual-channel's active energy, reactive energy and apparent energy simultaneously measuring;
- Measurement are provided for RMS voltage and frequency of voltage line;
- Providing calibration of sampling channel's gain and offset;
- Providing power factor;

1.2.4 RTC

- Hardware's automatic temperature compensation, precision and power consumption meet the national standard;
- Temperature Sensor: Provide accurate temperature, temperature measurement accuracy is ± 1 ℃ in the range of -25 ℃ ~ 70 ℃; Power consumption less than 2uA;

1.2.5 LCD

- Support 4*34,6*32,8*30;
- Support DMA automatic loop display without CPU operating;
- Charge pump provides LCD voltage, supporting clearly display over wide voltage range and the full temperature range;
- Power consumption of automatic loop display is less than 20uA.

1.2.6 Other Peripherals

- High speed GPIO, supports interface of peripheral devices with different voltage;
- 10bit ADC: Temperature sensor / battery voltage detection / generic ADC time division multiplexing;
- Voltage detecting LVD: chip supply voltage detection; external voltage detection.
- Two comparator CMP1and CMP2: external voltage detection, among which the CMP2's power consumption is less than 1uA,supporting low power supply monitoring under power failure.
- Timer:2 32bit extended timer,2 RTC timer,1 CM0 embedded system timer;
- UART:5 at most, supports automatic baud rate, support infrared modulation, supports UART wake up;
- 7816 port:2
- I2C:1
- SPI:2
- Watchdog: Hardware watchdog;
- Button Interrupts: 2, pin multiplexing;
- External interrupts: 4, pin multiplexing;

1.2.7 Encryption

- Hardware true random number generator meets the U.S. NIST FIPS140-2 standard;
- AES128/192/256 hardware encryption meets the FIPS197 standards, supporting EBC / CBC / CTR / GCM / GMAC mode;
- ECC192 hardware accelerators;
- Encryption documentation refers to Renergy application notes.

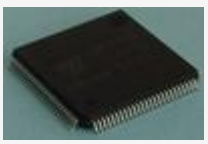
1.2.8 Card Meter Isolation

Provide high reliable and low cost card meter isolation solutions which can be seen in detail in Renergy RN8501 card meter isolation scheme explains;

1.2.9 RN821x Model Division

single-phase SOC series	RN8211	RN8211B	RN8213	RN8213B	RN8215	RN8217	RN8213B(D)
FLASH	64KBytes	64KBytes	128KBytes	128KByte	192KBytes	512KByte	512KBytes

				s		s	
EEPROM	32KBytes	32KBytes	32KBytes	32KBytes	32KBytes		
RAM	8KBytes	8KBytes	8KBytes	8KBytes	16KBytes(cache disable) 14KBytes(cache enable)	48KBytes	48KBytes
Measure	No zero line	Both fire wire and zero line	Both fire wire and zero line	Both fire wire and zero line	Both fire wire and zero line	Both fire wire and zero line	Both fire wire and zero line
DMA	No	No	No	No	Yes	Yes	Yes
32-bit general-purpose timer	1	1	2	2	2	2	2
Measurement of total voltage loss	No	No	No	No	**Yes, Refer to Application Note**	Yes	Yes
Encryption	No	No	No	No	**Yes, Refer to Application Note**	Yes	Yes
Hardware SPI	No	No	1	1	1	2	2
7816	No	No	2	2	2	2	2
UART	4	4	5	6	5	5	6
I2C	1	1	1	1	1	1	1
Package	LQFP64	LQFP64	LQFP100	LQFP128	LQFP100	LQFP100	LQFP128
Application fields	Rural Power Meter	Low-cost overseas Meter	State Grid Meter	Overseas Meter	Overseas Meter	Overseas Meter	Overseas Meter

LQFP64L (0707×1.4)			
LQFP100L (1414×1.4)			
LQFP128L (1414×1.4)			

Specific package size refer to Chapter 19 Package Dimensions.

1.3 System Block Diagram

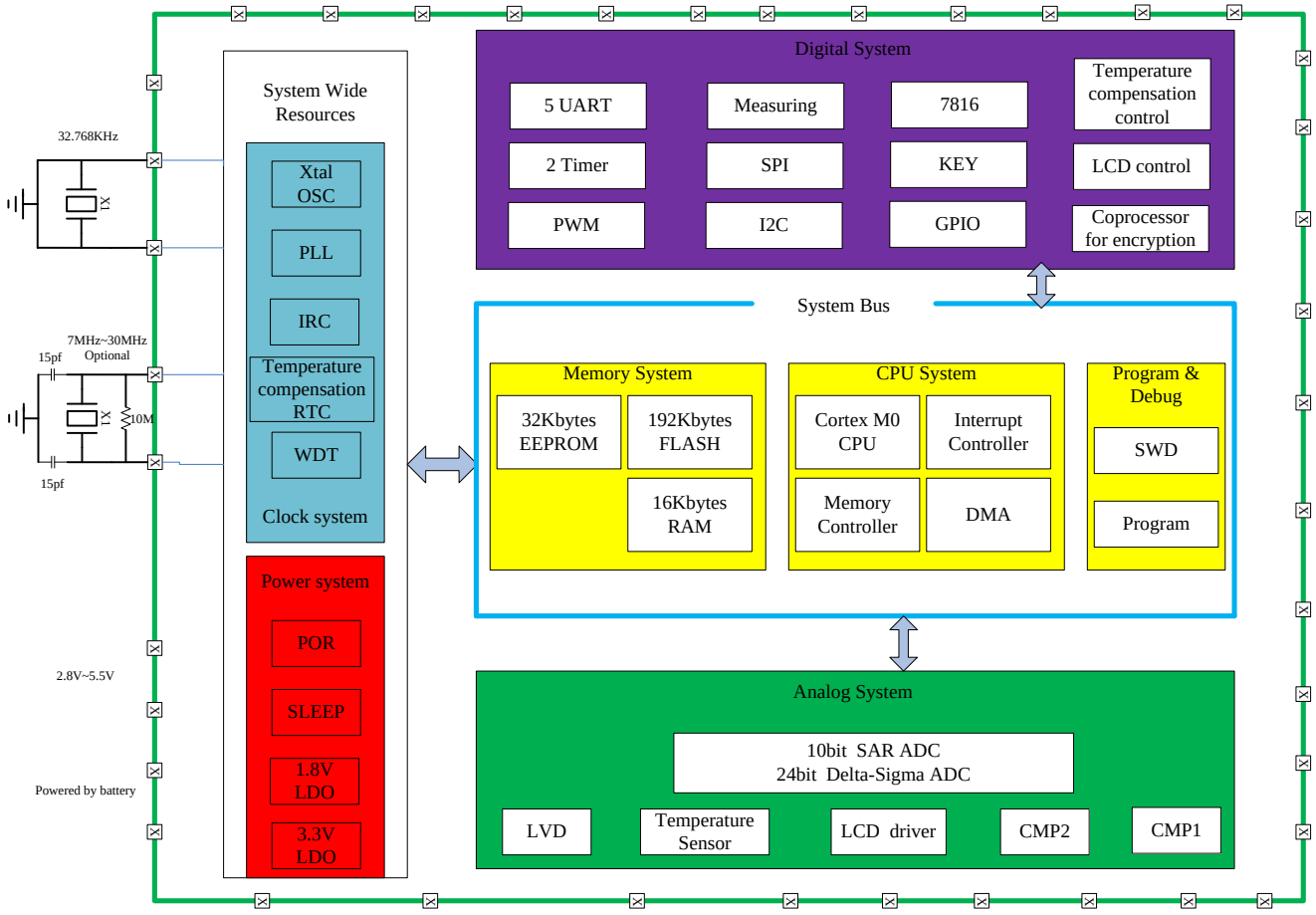
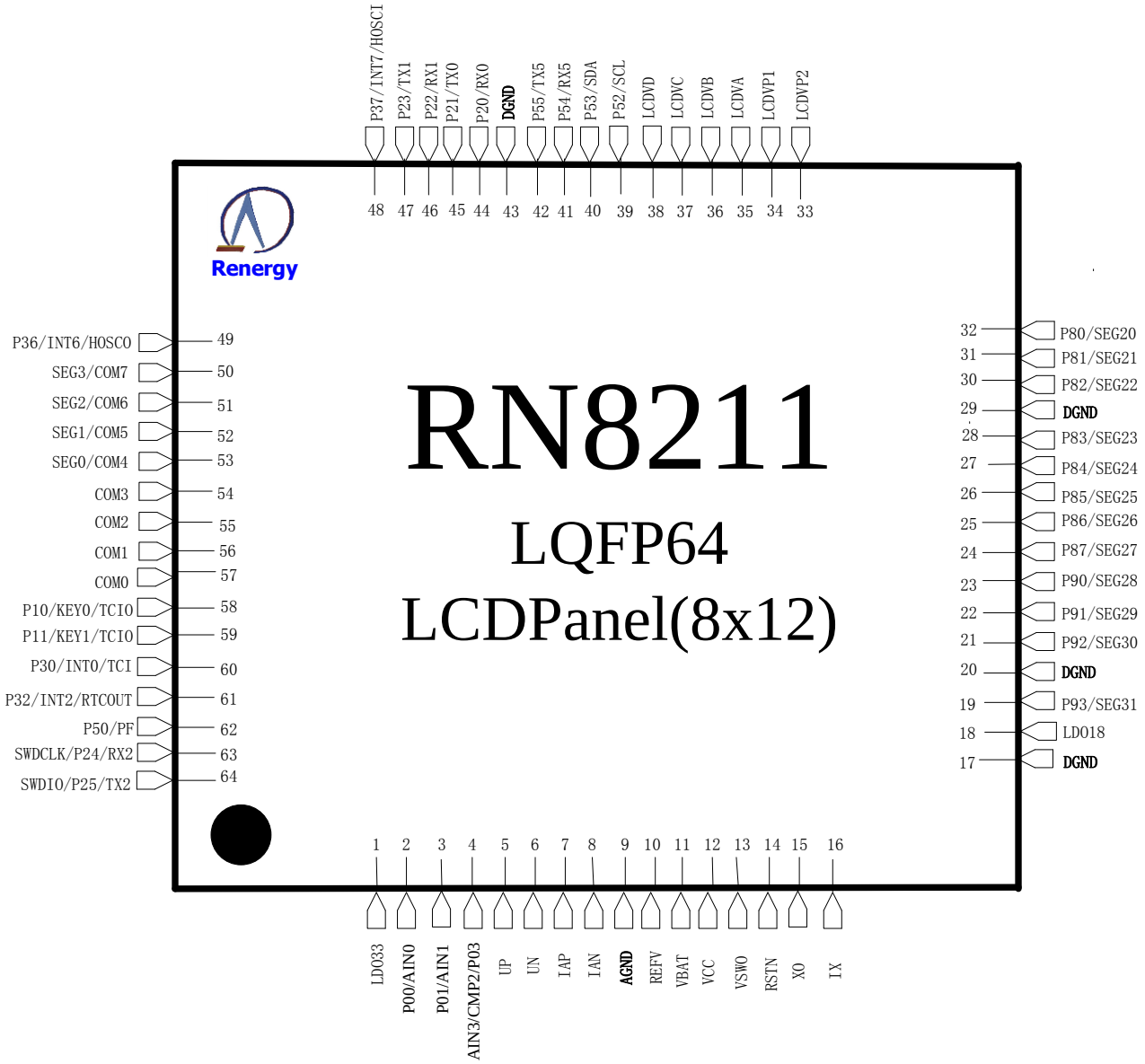
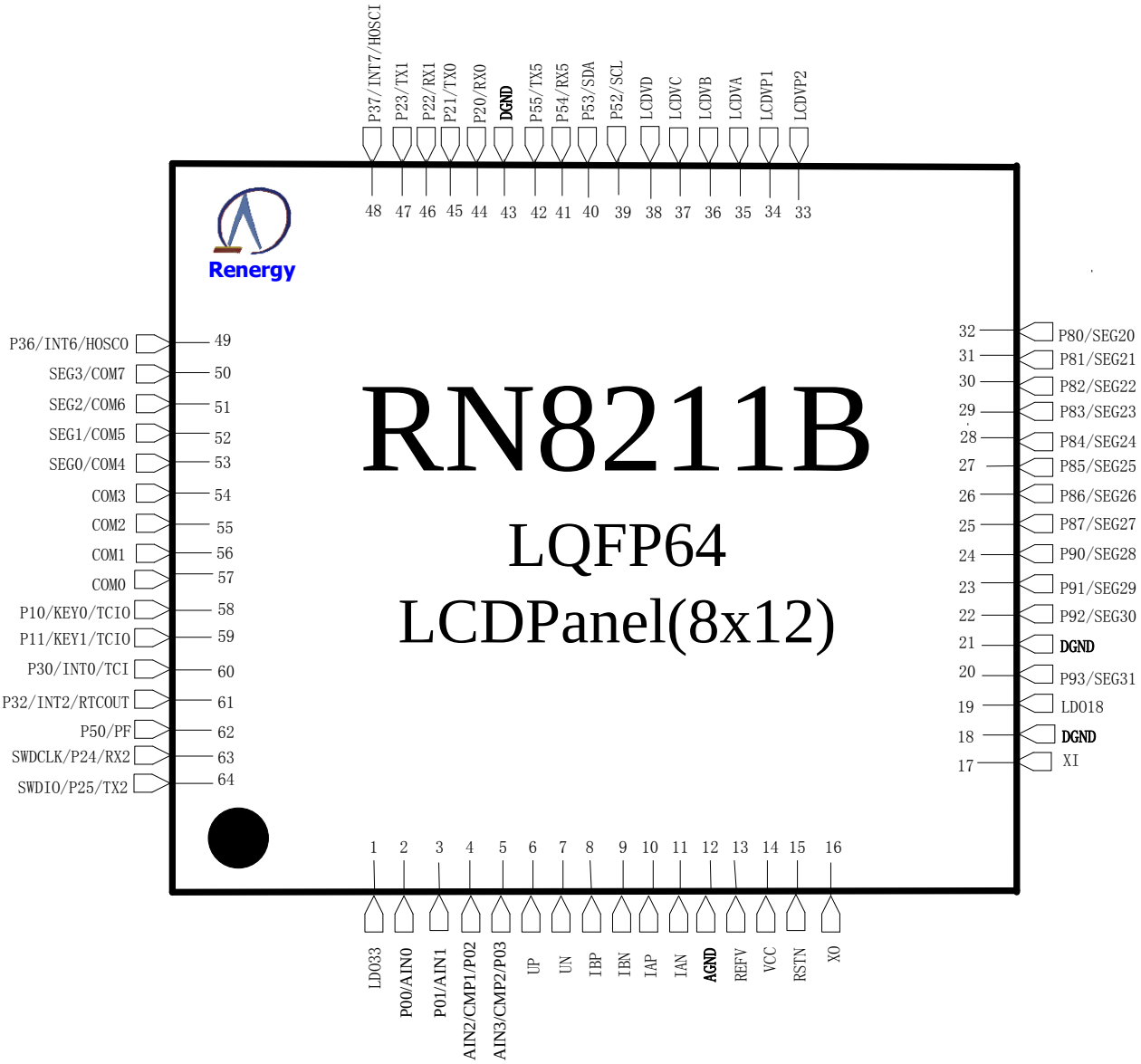
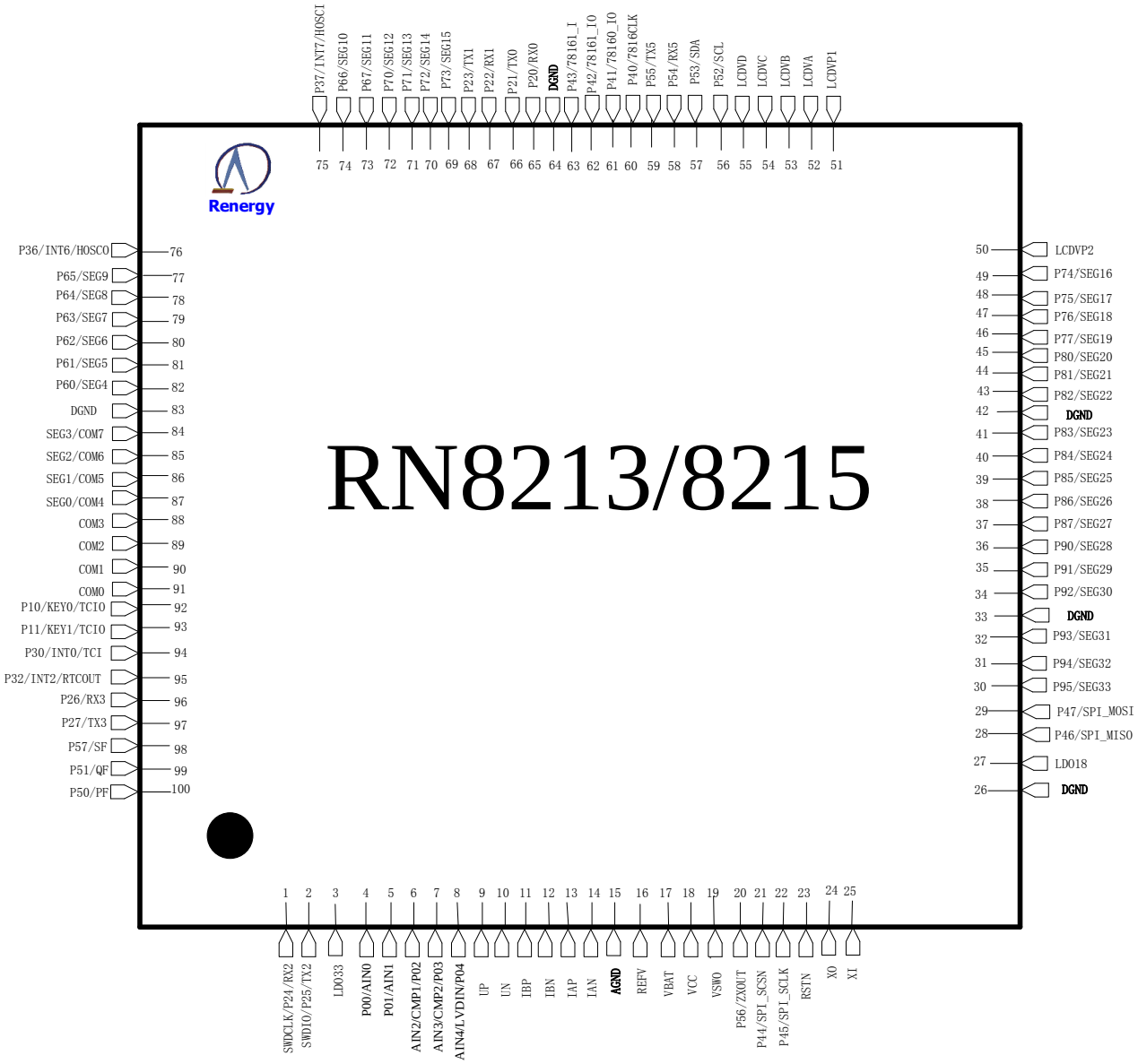


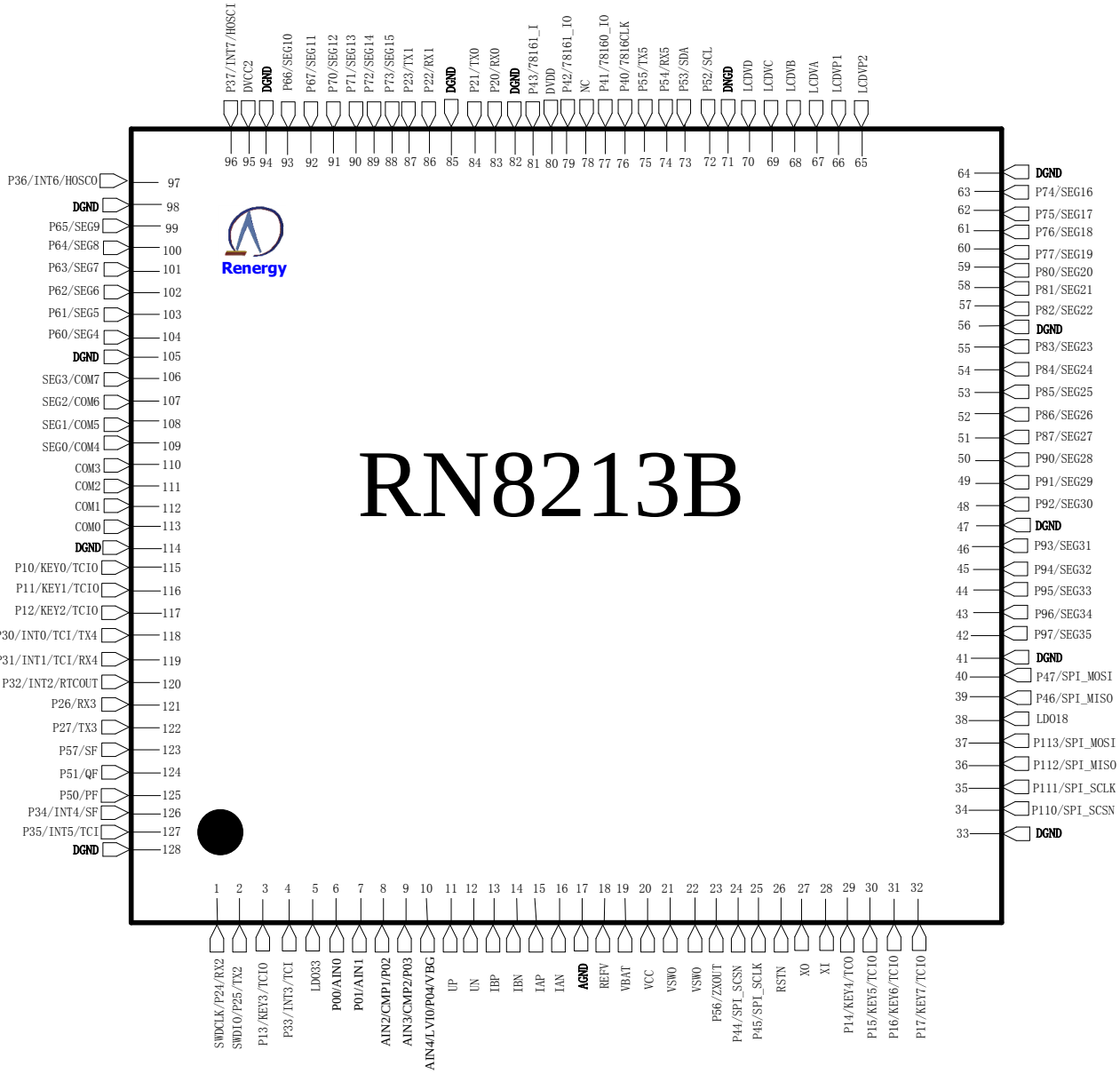
Figure 1.1 RN821X System Block Diagram

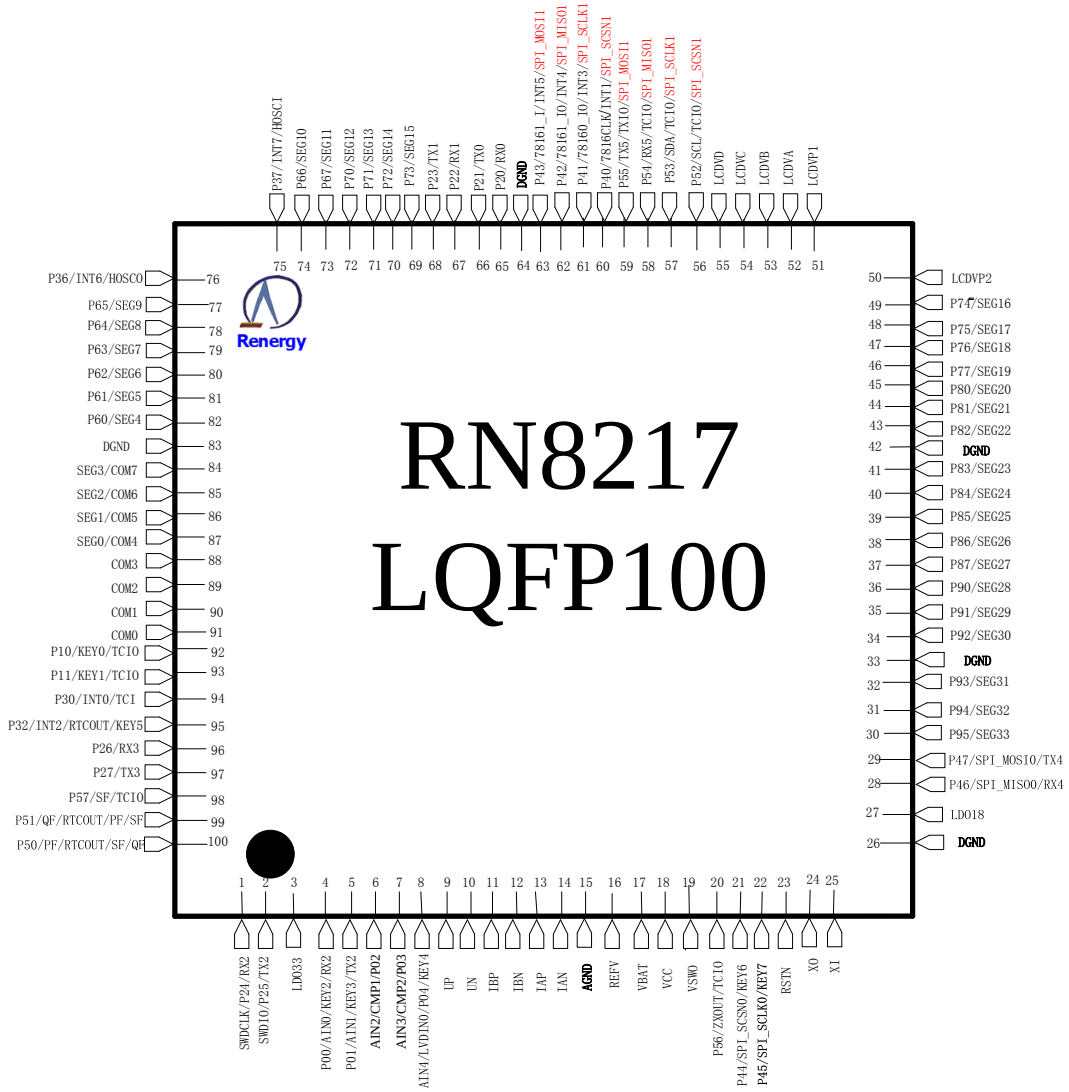
1.4 Pin Configuration




P37/INT7/HOSCI
P23/TX1
P22/RX1
P21/TX0
P20/RX0
DGND
P55/TX5
P54/RX5
P53/SDA
P52/SCL
LCDVD
LCDVC
LCDVB
LCDVA
LCDVP1
LCDVP2
48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33
Renergy
P36/INT6/HOSCO 49
SEG3/COM7 50
SEG2/COM6 51
SEG1/COM5 52
SEG0/COM4 53
COM3 54
COM2 55
COM1 56
COM0 57
P10/KEY0/TCIO 58
P11/KEY1/TCIO 59
P30/INT0/TCI 60
P32/INT2/RTCOUT 61
P50/PF 62
SWDCLK/P24/RX2 63
SWDIO/P25/TX2 64
RN8211B
LQFP64
LCDPanel(8x12)
32 P80/SEG20
31 P81/SEG21
30 P82/SEG22
29 P83/SEG23
28 P84/SEG24
27 P85/SEG25
26 P86/SEG26
25 P87/SEG27
24 P90/SEG28
23 P91/SEG29
22 P92/SEG30
21 DGND
20 P93/SEG31
19 LDO18
18 DGND
17 XI
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
LDO33
P00/AIN0
P01/AIN1
AIN2/CMP1/P02
AIN3/CMP2/P03
UP
UN
IBP
IBN
IAP
IAN
AGND
REFV
VCC
RSTN
XO


RN8213/8215
Renergy
P37/INT7/HOSCI 75
P66/SEG10 74
P67/SEG11 73
P70/SEG12 72
P71/SEG13 71
P72/SEG14 70
P73/SEG15 69
P23/TX1 68
P22/RX1 67
P21/TX0 66
P20/RX0 65
DGND 64
P43/7816I_I 63
P42/7816I_IO 62
P41/7816O_IO 61
P40/7816CLK 60
P55/TX5 59
P54/RX5 58
P53/SDA 57
P52/SCL 56
LCDVD 55
LCDVC 54
LCDVB 53
LCDVA 52
LCDVP1 51
P36/INT6/HOSCO 76
P65/SEG9 77
P64/SEG8 78
P63/SEG7 79
P62/SEG6 80
P61/SEG5 81
P60/SEG4 82
DGND 83
SEG3/COM7 84
SEG2/COM6 85
SEG1/COM5 86
SEG0/COM4 87
COM3 88
COM2 89
COM1 90
COM0 91
P10/KEY0/TCIO 92
P11/KEY1/TCIO 93
P30/INT0/TCI 94
P32/INT2/RTCOUT 95
P26/RX3 96
P27/TX3 97
P57/SF 98
P51/QF 99
P50/PF 100
50 LCDVP2
49 P74/SEG16
48 P75/SEG17
47 P76/SEG18
46 P77/SEG19
45 P80/SEG20
44 P81/SEG21
43 P82/SEG22
42 DGND
41 P83/SEG23
40 P84/SEG24
39 P85/SEG25
38 P86/SEG26
37 P87/SEG27
36 P90/SEG28
35 P91/SEG29
34 P92/SEG30
33 DGND
32 P93/SEG31
31 P94/SEG32
30 P95/SEG33
29 P47/SPI_MOSI
28 P46/SPI_MISO
27 LDO18
26 DGND
1 SWDCLK/P24/RX2
2 SWDIO/P25/TX2
3 LDO33
4 P00/AIN0
5 P01/AIN1
6 AIN2/CMP1/P02
7 AIN3/CMP2/P03
8 AIN4/LVDIN/P04
9 UP
10 UN
11 IBP
12 IBN
13 IAP
14 IAN
15 AGND
16 REFV
17 VBAT
18 VCC
19 VSWO
20 P56/ZXOUT
21 P44/SPI_SCSN
22 P45/SPI_SCLK
23 RSTN
24 XO
25 XI


RN8213B
Renergy
1 SWDCLK/P24/RX2
2 SWDIO/P25/TX2
3 P13/KEY3/TCI0
4 P33/INT3/TCI
5 LDO33
6 P00/AIN0
7 P01/AIN1
8 AIN2/CMP1/P02
9 AIN3/CMP2/P03
10 AIN4/LVI0/P04/VBG
11 UP
12 UN
13 IBP
14 IBN
15 IAP
16 IAN
17 AGND
18 REFV
19 VBAT
20 VCC
21 VSW0
22 VSW0
23 P56/ZXOUT
24 P44/SPI_SCSN
25 P45/SPI_SCLK
26 RSTN
27 XO
28 XI
29 P14/KEY4/TCO
30 P15/KEY5/TCI0
31 P16/KEY6/TCI0
32 P17/KEY7/TCI0
33 DGND
34 P110/SPI_SCSN
35 P111/SPI_SCLK
36 P112/SPI_MISO
37 P113/SPI_MOSI
38 LDO18
39 P46/SPI_MISO
40 P47/SPI_MOSI
41 DGND
42 P97/SEG35
43 P96/SEG34
44 P95/SEG33
45 P94/SEG32
46 P93/SEG31
47 DGND
48 P92/SEG30
49 P91/SEG29
50 P90/SEG28
51 P87/SEG27
52 P86/SEG26
53 P85/SEG25
54 P84/SEG24
55 P83/SEG23
56 DGND
57 P82/SEG22
58 P81/SEG21
59 P80/SEG20
60 P77/SEG19
61 P76/SEG18
62 P75/SEG17
63 P74/SEG16
64 DGND
65 LCDVP2
66 LCDVP1
67 LCDVA
68 LCDVB
69 LCDVC
70 LCDVD
71 DNGD
72 P52/SCL
73 P53/SDA
74 P54/RX5
75 P55/TX5
76 P40/7816CLK
77 P41/78160_IO
78 NC
79 P42/78161_IO
80 DVDD
81 P43/78161_I
82 DGND
83 P20/RX0
84 P21/TX0
85 DGND
86 P22/RX1
87 P23/TX1
88 P73/SEG15
89 P72/SEG14
90 P71/SEG13
91 P70/SEG12
92 P67/SEG11
93 P66/SEG10
94 DGND
95 DVCC2
96 P37/INT7/HOSC1
97 P36/INT6/HOSCO
98 DGND
99 P65/SEG9
100 P64/SEG8
101 P63/SEG7
102 P62/SEG6
103 P61/SEG5
104 P60/SEG4
105 DGND
106 SEG3/COM7
107 SEG2/COM6
108 SEG1/COM5
109 SEG0/COM4
110 COM3
111 COM2
112 COM1
113 COM0
114 DGND
115 P10/KEY0/TCI0
116 P11/KEY1/TCI0
117 P12/KEY2/TCI0
118 P30/INT0/TCI/TX4
119 P31/INT1/TCI/RX4
120 P32/INT2/RTCOUT
121 P26/RX3
122 P27/TX3
123 P57/SF
124 P51/QF
125 P50/PF
126 P34/INT4/SF
127 P35/INT5/TCI
128 DGND


RN8217
LQFP100
P36/INT6/HOSCO 76
P65/SEG9 77
P64/SEG8 78
P63/SEG7 79
P62/SEG6 80
P61/SEG5 81
P60/SEG4 82
DGND 83
SEG3/COM7 84
SEG2/COM6 85
SEG1/COM5 86
SEG0/COM4 87
COM3 88
COM2 89
COM1 90
COM0 91
P10/KEY0/TCI0 92
P11/KEY1/TCI0 93
P30/INT0/TC1 94
P32/INT2/RTCOUT/KEY5 95
P26/RX3 96
P27/TX3 97
P57/SF/TCI0 98
P51/QF/RTCOUT/PF/SF 99
P50/PF/RTCOUT/SF/QF 100
P37/INT7/HOSC1 75
P66/SEG10 74
P67/SEG11 73
P70/SEG12 72
P71/SEG13 71
P72/SEG14 70
P73/SEG15 69
P23/TX1 68
P22/RX1 67
P21/TX0 66
P20/RX0 65
DGND 64
P43/7816I_1/INT5/SPI_MOSI1 63
P42/7816I_IO/INT4/SPI_MISO1 62
P41/7816O_IO/INT3/SPI_SCLK1 61
P40/7816CLK/INT1/SPI_SCSN1 60
P55/TX5/TX10/SPI_MOSI1 59
P54/RX5/TC10/SPI_MISO1 58
P53/SDA/TC10/SPI_SCLK1 57
P52/SCL/TC10/SPI_SCSN1 56
LCDVD 55
LCDVC 54
LCDVB 53
LCDVA 52
LCDVP1 51
50 LCDVP2
49 P74/SEG16
48 P75/SEG17
47 P76/SEG18
46 P77/SEG19
45 P80/SEG20
44 P81/SEG21
43 P82/SEG22
42 DGND
41 P83/SEG23
40 P84/SEG24
39 P85/SEG25
38 P86/SEG26
37 P87/SEG27
36 P90/SEG28
35 P91/SEG29
34 P92/SEG30
33 DGND
32 P93/SEG31
31 P94/SEG32
30 P95/SEG33
29 P47/SPI_MOSI0/TX4
28 P46/SPI_MISO0/RX4
27 LDO18
26 DGND
1 SWDCLK/P24/RX2
2 SWDIO/P25/TX2
3 LDO33
4 P00/AIN0/KEY2/RX2
5 P01/AIN1/KEY3/TX2
6 AIN2/CMP1/P02
7 AIN3/CMP2/P03
8 AIN4/LVDIN0/P04/KEY4
9 UP
10 UN
11 IBP
12 IBN
13 IAP
14 IAN
15 AGND
16 REFV
17 VBAT
18 VCC
19 VSW0
20 P56/ZXOUT/TC10
21 P44/SPI_SCSN0/KEY6
22 P45/SPI_SCLK0/KEY7
23 RSTN
24 XO
25 XI

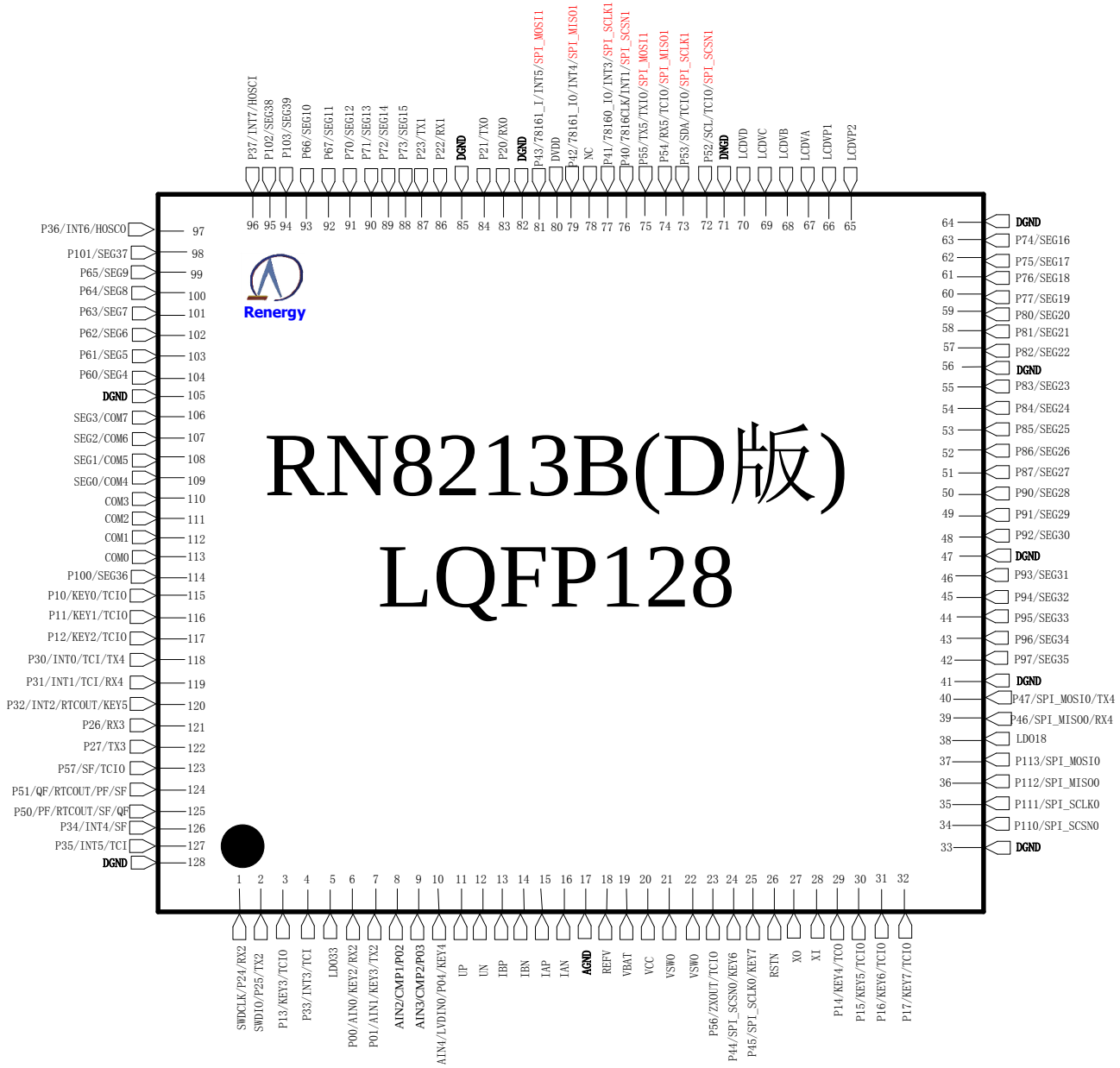


Figure 1.2 Single-phase SOC Pin Configuration

Pin Type Description:

Type	A	B	I	O	U	S	L	D	X	G	M	Drive
PBUS6		√			√	√						6mA
PBULD3		√			√		√	√				3mA
PABUS3	√	√				√						3mA
PUXI			√						√			
PBUSG3		√			√	√				√		3mA
PAM	√										√	
PAGM	√									√	√	

Notes: A-analog, B-Bilateral, I-input, O-output, U-pull up, S-Schmidt, L-TTL/CMOS, X-Crystal oscillator, G-SEG, M-COM.

Pin Description:

Number					
8213/5	8211	8211B	Name	Pin Type	Function Description
1	63	63	SWDCLK/P24/RX2	PBULD3	SWD clock,UART2 input,P24 multiplexing; Optional pull up,TTL/CMOS voltage and open drain.
2	64	64	SWDIO/P25/TX2	PBULD3	SWD data port,UART2 output,P25 multiplexing; Optional pull up,TTL/CMOS voltage and open drain.
3	1	1	LDO33	LDO output	3.3V measure LDO output,supply for measure ADC; External connected 0.1uF and 10uF capacitors;
4	2	2	P00/AIN0	PABUS3	P00 port,SAR-ADC input multiplexing PAD
5	3	3	P01/AIN1	PABUS3	P01 port,SAR-ADC input multiplexing PAD
6			AIN2/CMP1/P02	PABUS3	SAR-ADC input,comparator 1 input, P02multiplexing;
7	4	4	AIN3/CMP2/P03	PABUS3	SAR-ADC input,low power comparator 2 input,P03 multiplexing;
8		5	AIN4/LVDIN/P04	PABUS3	SAR-ADC input,LVDIN input,P04 multiplexing;
9	5	6	UP	Analog input	Positive analog input pin of voltage channel
10	6	7	UN	Analog input	Negative analog input pin of voltage channel
11		8	IBP	Analog input	Positive analog input pin of current channel B
12		9	IBN	Analog input	Negative analog input pin of current channel B

13	7	10	IAP	Analog input	Positive analog input pin of current channel A,Maximum gain 16,External connect manganese bronze sampling circuit.Maximum input signal ±1V(signal after differential);
14	8	11	IAN	Analog input	Negative analog input pin of current channel A,Maximum gain 16,External connect manganese bronze sampling circuit.
15	9	12	AGND	Ground	Analog ground
16	10	13	REFV	Reference voltage	Measure ADC input,,should connect external 0.1uF and 10uF capacitors;
17	11		VBAT	Source	3.6V battery input Pin,meanwhile SAR-ADC input.
18	12	14	VCC	Source	2.8V~5.5V source input, should connect external 0.1uF and 10uF capacitors for decoupling;
19	13		VSWO	Source	Output after the switching of main power and battery power, should connect external 0.1uF and 10uF capacitors for decoupling;
20			P56/ZXOUT	PBULD3	P56/Zero-crossing output multiplexing
21			P44/SPI_SCSN	PBULD3	P4/SPI multiplexing Optional pull up, TTL/CMOS voltage and open drain.
22			P45/SPI_SCLK	PBULD3	
23	14	15	RSTN	Reset	Low voltage reset, internal pull-up resistor;
24	15	16	XO	Clock	32.768KHz passive crystal output and input; Should be isolated by ground wire, external resistor and capacitor are not needed;
25	16	17	XI	Clock	
26	17	18	DGND	Ground	Digital ground
27	18	19	LDO18	LDO	Output of 1.8V LDO, should connect external 0.1uF and 10uF capacitors for decoupling;
28			P46/SPI_MISO	PBULD3	P4/SPI multiplexing; Optional pull up, TTL/CMOS voltage and open drain.
29			P47/SPI_MOSI	PBULD3	
30			P95/SEG33	PBUSG3	LCD/GPIO multiplexing
31			P94/SEG32	PBUSG3	LCD/GPIO multiplexing
32	19	20	P93/SEG31	PBUSG3	LCD/GPIO multiplexing
33	20	21	DGND	Ground	Digital ground
34	21	22	P92/SEG30	PBUSG3	LCD/GPIO multiplexing
35	22	23	P91/SEG29	PBUSG3	LCD/GPIO multiplexing

36	23	24	P90/SEG28	PBUSG3	LCD/GPIO multiplexing
37	24	25	P87/SEG27	PBUSG3	LCD/GPIO multiplexing
38	25	26	P86/SEG26	PBUSG3	LCD/GPIO multiplexing
39	26	27	P85/SEG25	PBUSG3	LCD/GPIO multiplexing
40	27	28	P84/SEG24	PBUSG3	LCD/GPIO multiplexing
41	28	29	P83/SEG23	PBUSG3	LCD/GPIO multiplexing
42	29		DGND	Ground	Digital ground
43	30	30	P82/SEG22	PBUSG3	LCD/GPIO multiplexing
44	31	31	P81/SEG21	PBUSG3	LCD/GPIO multiplexing
45	32	32	P80/SEG20	PBUSG3	LCD/GPIO multiplexing
46			P77/SEG19	PBUSG3	LCD/GPIO multiplexing
47			P76/SEG18	PBUSG3	LCD/GPIO multiplexing
48			P75/SEG17	PBUSG3	LCD/GPIO multiplexing
49			P74/SEG16	PBUSG3	LCD/GPIO multiplexing
50	33	33	LCDVP2	Analog	Analog output, 100nF capacitor should be connected between LCDVP2 and LCDVP1.
51	34	34	LVDVP1	Analog	Analog output, 100nF capacitor should be connected between LCDVP2 and LCDVP1.
52	35	35	LCDVA	Analog	LCD voltage output, need for external capacitors 470nF
53	36	36	LCDVB	Analog	LCD voltage output, need for external capacitors 470nF
54	37	37	LCDVC	Analog	LCD voltage output, need for external capacitors 470nF
55	38	38	LCDVD	Analog	LCD voltage output, need for external capacitors 470nF
56	39	39	P52/SCL	PBULD3	P5/I2C port multiplexing. Optional pull-up resistor, optional TTL/CMOS input, optional open drain
57	40	40	P53/SDA	PBULD3	
58	41	41	P54/ RX5	PBULD3	P54/UART5input multiplexing

59	42	42	P55/ TX5	PBULD3	P55/UART5output multiplexing
60			P40/7816CLK	PBULD3	Pins that IO ports multiplex with 7816. Optional pull-up resistor, optional TTL/CMOS input, optional open drain; Notes: supports two interfaces of 7861. 78160_IO is bidirectional data port of 7816 0; 78161_IO is bidirectional data port of 7816 1; Besides,7816 1 can be configured by register as follows: 78161_IO as 7816 1 data output; 78161_I as 7816 1 data input.
61			P41/78160_IO	PBULD3	
62			P42/78161_IO	PBULD3	
63			P43/78161_I/TCI	PBULD3	
64	43	43	DGND	Ground	Digital ground
65	44	44	P20/RX0	PBULD3	P2/UART0/UART1 multiplexing; Optional pull up, TTL/CMOS voltage and open drain.
66	45	45	P21/TX0	PBULD3	
67	46	46	P22/RX1	PBULD3	
68	47	47	P23/TX1	PBULD3	
69			P73/SEG15	PBUSG3	LCD/GPIO multiplexing
70			P72/SEG14	PBUSG3	LCD/GPIO multiplexing
71			P71/SEG13	PBUSG3	LCD/GPIO multiplexing
72			P70/SEG12	PBUSG3	LCD/GPIO multiplexing
73			P67/SEG11	PBUSG3	LCD/GPIO multiplexing
74			P66/SEG10	PBUSG3	LCD/GPIO multiplexing
75	48	48	P37/INT7/HOSCI	PUXI	P3/ interrupt port / high-frequency crystal multiplexing high-frequency crystal port should connect a 10Mresistor in serial and 2 15pf capacitors in parallel.
76	49	49	P36/INT6/HOSCO	PUXI	
77			P65/SEG9	PBUSG3	LCD/GPIO multiplexing
78			P64/SEG8	PBUSG3	LCD/GPIO multiplexing
79			P63/SEG7	PBUSG3	LCD/GPIO multiplexing
80			P62/SEG6	PBUSG3	LCD/GPIO multiplexing
81			P61/SEG5	PBUSG3	LCD/GPIO multiplexing
82			P60/SEG4	PBUSG3	LCD/GPIO multiplexing
83			DGND	Ground	Digital ground
84	50	50	SEG3/COM7	PAM	SEG/COM multiplexing
85	51	51	SEG2/CO	PAM	SEG/COM multiplexing

			M6		
86	52	52	SEG1/COM5	PAM	SEG/COM multiplexing
87	53	53	SEG0/COM4	PAM	SEG/COM multiplexing
88	54	54	COM3	PAM	COM port
89	55	55	COM2	PAM	COM port
90	56	56	COM1	PAM	COM port
91	57	57	COM0	PAM	COM port
92	58	58	P10/KEY0/TC0OUTn0/TCIN	PBULD3	IO/KEY input/timer input output multiplexing; Optional pull up, TTL/CMOS voltage and open drain.
93	59	59	P11/KEY1/TC0OUTp0/TCIN	PBULD3	
94	60	60	P30/INT0/TCIN	PBUS6	IO/external interrupt input/timer input multiplexing; Optional pull-up, Schmitt input,6mA drive capability.
95	61	61	P32/ INT2/RTCOUT	PBUS6	IO/external interrupt input/RTC pulse output multiplexing; Optional pull-up, Schmitt input,6mA drive capability.
96			P26/RX3	PBULD3	UART3/P2 multiplexing; Optional pull up, TTL/CMOS voltage and open drain.
97			P27/TX3	PBULD3	
98			P57/SF	PBULD3	P57/SF apparent power pulse output multiplexing; Optional pull up, TTL/CMOS voltage and open drain.
99			P51/QF	PBUS6	P51/reactive energy pulse output multiplexing; Optional pull-up, Schmitt input,6mA drive capability.
100	62	62	P50/PF	PBUS6	P50/active energy pulse output multiplexing; Optional pull-up, Schmitt input,6mA drive capability.

RN8213B Number	Name	Pin Type	Function Description
1	SWDCLK/ P24/RX2	PBULD3	SWD clock,UART2 input,P24 multiplexing; Optional pull up,TTL/CMOS voltage and open drain.
2	SWDIO/P25/TX2	PBULD3	SWD data port,UART2 output,P25 multiplexing; Optional pull up,TTL/CMOS voltage and open drain.
3	P13/KEY3/TCIO	PBULD3	IO/KEY input/timer input output multiplexing; Optional pull up, TTL/CMOS voltage and open drain.
4	P33/ INT3/ TCI	PBUS6	IO/external interrupt input/timer input multiplexing; Optional pull-up, Schmitt input,6mA drive capability.
5	LDO33	LDO output	3.3V measure LDO output; External connected 0.1uF and 10uF capacitors;
6	P00/AIN0	PABUS3	P00 port,SAR-ADC input multiplexing PAD
7	P01/AIN1	PABUS3	P01 port,SAR-ADC input multiplexing PAD
8	AIN2/CMP1/P02	PABUS3	SAR-ADC input,comparator 1 input, P02multiplexing;
9	AIN3/CMP2/P03	PABUS3	SAR-ADC input,low power comparator 2 input,P03 multiplexing;
10	AIN4/LVDIN/P04	PABUS3	SAR-ADC input,LVDIN input,P04 multiplexing;
11	UP	Analog input	Positive analog input pin of voltage channel
12	UN	Analog input	Negative analog input pin of voltage channel
13	IBP	Analog input	Positive analog input pin of current channel B
14	IBN	Analog input	Negative analog input pin of current channel B
15	IAP	Analog input	Positive analog input pin of current channel A,Maximum gain 16,External connect manganese bronze sampling circuit.Maximum input signal ±1V(signal after differential);
16	IAN	Analog input	Negative analog input pin of current channel A,Maximum gain 16,External connect manganese bronze sampling circuit.
17	AGND	Ground	Analog ground
18	REFV	Reference voltage	Measure ADC input,,should connect external 0.1uF and 10uF capacitors;
19	VBAT	Source	3.6V battery input Pin,meanwhile SAR-ADC input.
20	VCC	Source	main power input, should connect external 0.1uF and 10uF capacitors for decoupling;
21	VSWO	Source	Output after the switching of main power and battery power, should connect external 0.1uF and 10uF capacitors for decoupling;

22	VSWO	Source	It has the same function with pin 21; could connect with pin 21 externally.
23	P56/ZXOUT	PBULD3	P56/Zero-crossing output multiplexing
24	P44/SPI_SCSN	PBULD3	P4/SPI multiplexing
25	P45/SPI_SCLK	PBULD3	Optional pull up, TTL/CMOS voltage and open drain.
26	RSTN	Reset	Low voltage reset, internal pull-up resistor;
27	XO	Clock	32.768KHz passive crystal output and input;
28	XI	Clock	Should be isolated by ground wire, external resistor and capacitor are not needed;
29	P14/KEY4/TCO	PBULD3	IO/KEY input/timer input output multiplexing;
30	P15/KEY5/TCIO	PBULD3	Optional pull up, TTL/CMOS voltage and open drain.
31	P16/KEY6/TCIO	PBULD3	
32	P17/KEY7/TCIO	PBULD3	
33	DGND	Ground	Digital ground
34	P110/SPI-SCSN	PBULD3	P11/SPI multiplexing
35	P111/SPI-SCLK	PBULD3	The SPI of P11 and P4 can't be used at the same time.
36	P112/SPI-MISO	PBULD3	
37	P113/SPI-MOSI	PBULD3	Optional pull up, TTL/CMOS voltage and open drain.
38	LDO18	LDO	Output of 1.8V LDO, should connect external 0.1uF and 10uF capacitors for decoupling;
39	P46/SPI_MISO	PBULD3	P4/SPI multiplexing;
40	P47/SPI_MOSI	PBULD3	Optional pull up, TTL/CMOS voltage and open drain.
41	DGND	Ground	Digital ground
42	P97/SEG35	PBUSG3	LCD/GPIO multiplexing
43	P96/SEG34	PBUSG3	LCD/GPIO multiplexing
44	P95/SEG33	PBUSG3	LCD/GPIO multiplexing
45	P94/SEG32	PBUSG3	LCD/GPIO multiplexing
46	P93/SEG31	PBUSG3	LCD/GPIO multiplexing
47	DGND	Ground	Digital ground
48	P92/SEG30	PBUSG3	LCD/GPIO multiplexing
49	P91/SEG29	PBUSG3	LCD/GPIO multiplexing
50	P90/SEG28	PBUSG3	LCD/GPIO multiplexing
51	P87/SEG27	PBUSG3	LCD/GPIO multiplexing
52	P86/SEG26	PBUSG3	LCD/GPIO multiplexing
53	P85/SEG25	PBUSG3	LCD/GPIO multiplexing
54	P84/SEG24	PBUSG3	LCD/GPIO multiplexing
55	P83/SEG23	PBUSG3	LCD/GPIO multiplexing
56	DGND	Ground	Digital ground
57	P82/SEG22	PBUSG3	LCD/GPIO multiplexing
58	P81/SEG21	PBUSG3	LCD/GPIO multiplexing
59	P80/SEG20	PBUSG3	LCD/GPIO multiplexing
60	P77/SEG19	PBUSG3	LCD/GPIO multiplexing
61	P76/SEG18	PBUSG3	LCD/GPIO multiplexing

62	P75/SEG17	PBUSG3	LCD/GPIO multiplexing
63	P74/SEG16	PBUSG3	LCD/GPIO multiplexing
64	DGND	Ground	Digital ground
65	LCDVP2	Analog	Analog output, 100nF capacitor should be connected between LCDVP2 and LCDVP1.
66	LVDVP1	Analog	Analog output, 100nF capacitor should be connected between LCDVP2 and LCDVP1.
67	LCDVA	Analog	LCD voltage output, need for external capacitors 470nF
68	LCDVB	Analog	LCD voltage output, need for external capacitors 470nF
69	LCDVC	Analog	LCD voltage output, need for external capacitors 470nF
70	LCDVD	Analog	LCD voltage output, need for external capacitors 470nF
71	DGND	Ground	Digital ground
72	P52/SCL	PBULD3	P5/I2C port multiplexing. Optional pull-up resistor, optional TTL/CMOS input, optional open drain
73	P53/SDA	PBULD3	
74	P54/ RX5	PBULD3	P54/UART5input multiplexing
75	P55/ TX5	PBULD3	P55/UART5output multiplexing
76	P40/7816CLK	PBULD3	Pins that IO ports multiplex with 7816. Two interfaces of 7861 are supported. 78160_IO is bidirectional data port of 7816 0; Optional pull-up resistor, optional TTL/CMOS input, optional open drain;
77	P41/78160_IO	PBULD3	
78	NC	Not connect	
79	P42/78161_IO	PBULD3	78161_IO is bidirectional data port of 7816 1; Optional pull-up resistor, optional TTL/CMOS input, optional open drain;
80	DVDD	source	Back up of 1.8V power supply; can be connected with pin 38 or not connected when using.
81	P43/78161_I	PBULD3	There is a register of module 7816 1 to configure that: 78161_IO as 7816 1 data output; 78161_I as 7816 1 data input.
82	DGND	Ground	Digital ground
83	P20/RX0	PBULD3	P2/UART0 multiplexing; Optional pull up, TTL/CMOS voltage and open drain.
84	P21/TX0	PBULD3	
85	DGND	Ground	Digital ground
86	P22/RX1	PBULD3	P2/UART1 multiplexing;

87	P23/TX1	PBULD3	Optional pull up, TTL/CMOS voltage and open drain.
88	P73/SEG15	PBUSG3	LCD/GPIO multiplexing
89	P72/SEG14	PBUSG3	LCD/GPIO multiplexing
90	P71/SEG13	PBUSG3	LCD/GPIO multiplexing
91	P70/SEG12	PBUSG3	LCD/GPIO multiplexing
92	P67/SEG11	PBUSG3	LCD/GPIO multiplexing
93	P66/SEG10	PBUSG3	LCD/GPIO multiplexing
94	DGND	Ground	Digital ground
95	DVCC	Source	Back up of 5V power supply; can be connected with VSWO or not connected when using.
96	P37/INT7/HOSCI	PUXI	P3/ interrupt port / high-frequency crystal multiplexing high-frequency crystal port should connect a 10Mresistor in serial and 2 15pf capacitors in parallel.
97	P36/INT6/HOSCO	PUXI	
98	DNGD	Ground	Digital ground
99	P65/SEG9	PBUSG3	LCD/GPIO
100	P64/SEG8	PBUSG3	LCD/GPIO
101	P63/SEG7	PBUSG3	LCD/GPIO
102	P62/SEG6	PBUSG3	LCD/GPIO
103	P61/SEG5	PBUSG3	LCD/GPIO
104	P60/SEG4	PBUSG3	LCD/GPIO
105	DGND	Ground	Digital ground
106	SEG3/COM7	PAM	SEG/COM
107	SEG2/COM6	PAM	SEG/COM
108	SEG1/COM5	PAM	SEG/COM
109	SEG0/COM4	PAM	SEG/COM
110	COM3	PAM	COM port
111	COM2	PAM	COM port
112	COM1	PAM	COM port
113	COM0	PAM	COM port
114	DGND	Ground	Digital ground
115	P10/KEY0/ TCIO	PBULD3	O/KEY input/timer input output multiplexing; Optional pull up, TTL/CMOS voltage and open drain.
116	P11/KEY1/TCIO	PBULD3	
117	P12/KEY2/TCIO	PBULD3	
118	P30/INT0/ TCI/TX4	PBUS6	IO/external interrupt input/timer input / TX4 multiplexing; Optional pull-up, Schmitt input,6mA drive capability.
119	P31/ INT1/TCI/RX4	PBUS6	IO/external interrupt input/timer input / RX4 multiplexing; Optional pull-up, Schmitt input,6mA drive capability.
120	P32/ INT2/ RTCOUT	PBUS6	IO/external interrupt input/RTC pulse output multiplexing; Optional pull-up, Schmitt input,6mA drive capability.
121	P26/RX3	PBULD3	UART3/P2 multiplexing;

122	P27/TX3	PBULD3	Optional pull up, TTL/CMOS voltage and open drain.
123	P57/SF	PBULD3	P57/SF apparent power pulse output multiplexing; Optional pull up, TTL/CMOS voltage and open drain.
124	P51/QF	PBUS6	P51/reactive energy pulse output multiplexing; Optional pull-up, Schmitt input,6mA drive capability.
125	P50/PF	PBUS6	P50/active energy pulse output multiplexing; Optional pull-up, Schmitt input,6mA drive capability.
126	P34/INT4/SF	PBUS6	P34/external interrupt input/SF apparent power pulse output multiplexing;
127	P35/ INT5/ TCI	PBUS6	P35/external interrupt input/ timer input multiplexing; Optional pull-up, Schmitt input,6mA drive capability.
128	DGND	Ground	Digital ground

RN8217	Name	Pin Type	Function Description
1	SWDCLK/ P24/RX2	PBULD3	SWD clock, UART2 input, p24 multiplexing; Pull up, TTL / CMOS level and drain open circuit are available.
2	SWDIO/ P25/TX2	PBULD3	SWD data port, UART2 output, P25 multiplexing;Pull up, TTL / CMOS level and drain open circuit are available.
3	LDO33	LDO output	3.3V metering LDO output to supply power to metering ADC; external parallel connected with 0.1uF and 1uF capacitors;
4	P00/AIN0/KEY2/RX2	PABUS3	P00 port, sar-adc input, key2, rx2 multiplexed pad
5	P01/AIN1/KEY3/TX2	PABUS3	P01 port, sar-adc input, Key3, TX2 multiplexing pad
6	AIN2/CMP1/P02	PABUS3	Sar-adc input, comparator 1 input, P02 multiplexing;
7	AIN3/CMP2/P03	PABUS3	Sar-adc input, low power comparator 2 input, P03 multiplexing;
8	AIN4/LVDIN0/P04/KEY4	PABUS3	Sar-adc input, lvdin input, P04, key4 multiplexing;
9	UP	Analog input	Positive analog input pin of voltage channel
10	UN	Analog input	Negative analog input pin of voltage channel
11	IBP	Analog input	Positive analog input pin for current channel B
12	IBN	Analog input	Negative analog input pin for current channel B
13	IAP	Analog input	Positive analog input pin of current channel a, with maximum gain of 16 times, and external manganese copper sampling circuit. The

			maximum input signal is ± 1V (differential signal);
14	IAN	Analog input	The negative analog input pin of current channel a has a maximum gain of 16 times and an external manganese copper sampling circuit.
15	AGND	GND	AGND
16	REFV	Vreference	The reference input of ADC should be connected with 0.1uF and 1uF capacitors in parallel
17	VBAT	Power Supply	3.6V battery input pin; it is also the input of internal sar-adc.
18	VCC	Power Supply	2.8v-5.5v power input, 4.7uf capacitor shall be connected in parallel with 0.1uF capacitance decoupling.
19	VSWO	Power Supply	The power output after switching between main power and battery should be connected with external 1uF capacitor in parallel with 0.1uF capacitor for decoupling.
20	P56/ZXOUT/TCIN/TC1_N[1]	PBULD3	P56 port, zero crossing output, tcio multiplexing
21	P44/SPI_SCSN0/KEY6	PBULD3	P4 port, spi0 and key are multiplexed; Pull up, TTL / CMOS level and drain open circuit are available.
22	P45/SPI_SCLK0/KEY7	PBULD3	
23	RSTN	reset	Low level reset circuit with pull-up resistor inside;
24	XO	Clock	32.768KHz passive crystal oscillator output and input. No external resistance and capacitance are required, and it needs to be isolated by ground wire. It is suggested that the crystal vibration with load capacitance of 12.5pF should be used.
25	XI	Clock	
26	DGND	GND	DGND
27	LDO18	LDO	The output of 1.8V LDO should be connected with external 1uF capacitor in parallel with 0.1uF capacitor to decouple;
28	P46/SPI_MISO0/RX4	PBULD3	P4 port, spi0 and uart4 are multiplexed; Pull up, TTL / CMOS level and drain open circuit are available.
29	P47/SPI_MOSI0/TX4	PBULD3	
30	P95/SEG33	PBUSG3	LCD / GPIO multiplexing
31	P94/SEG32	PBUSG3	LCD / GPIO multiplexing
32	P93/SEG31	PBUSG3	LCD / GPIO multiplexing
33	DGND	GND	DGND
34	P92/SEG30	PBUSG3	LCD/GPIO multiplexing

35	P91/SEG29	PBUSG3	LCD/GPIO multiplexing
36	P90/SEG28	PBUSG3	LCD/GPIO multiplexing
37	P87/SEG27	PBUSG3	LCD/GPIO multiplexing
38	P86/SEG26	PBUSG3	LCD/GPIO multiplexing
39	P85/SEG25	PBUSG3	LCD/GPIO multiplexing
40	P84/SEG24	PBUSG3	LCD/GPIO multiplexing
41	P83/SEG23	PBUSG3	LCD/GPIO multiplexing
42	DGND	GND	DGND
43	P82/SEG22	PBUSG3	LCD/GPIO multiplexing
44	P81/SEG21	PBUSG3	LCD/GPIO multiplexing
45	P80/SEG20	PBUSG3	LCD/GPIO multiplexing
46	P77/SEG19	PBUSG3	LCD/GPIO multiplexing
47	P76/SEG18	PBUSG3	LCD/GPIO multiplexing
48	P75/SEG17	PBUSG3	LCD/GPIO multiplexing
49	P74/SEG16	PBUSG3	LCD/GPIO multiplexing
50	LCDVP2	simulation	For analog output, a capacitance of 100nF should be connected between lcdvp2 and lcdvp1.
51	LVDVP1	simulation	For analog output, a capacitance of 100nF should be connected between lcdvp2 and lcdvp1.
52	LCDVA	simulation	LCD voltage output, need external 470nf capacitor
53	LCDVB	simulation	LCD voltage output, need external 470nf capacitor
54	LCDVC	simulation	LCD voltage output, need external 470nf capacitor
55	LCDVD	simulation	LCD voltage output, need external 470nf capacitor
56	P52/SCL/TCIN/TC0_N[1]/ SPI_SCSN1	PBULD3	P5 port, I2C, tcio and SPI1 are multiplexed. Pull up resistor, TTL / CMOS input and drain open circuit are optional; P52 ~ p55 can be reused as SPI1 ports, and the priority of SPI1 is lower than that of P40 ~ p43
57	P53/SDA/TCIN/TC0_P[1]/ SPI_SCLK1	PBULD3	
58	P54/RX5/TCIN/TC1_N[0]/ SPI_MISO1	PBULD3	P54, uart5 input, tcio, SPI2 multiplexing
59	P55/TX5/TCIN/TC1_P[0]/ SPI_MOSI1	PBULD3	P55, uart5 output, tcio, SPI2 multiplexing
60	P40/7816CLK/INT1/ SPI_SCSN1	PBULD3	The IO port is multiplexed with 7816, int and SPI2. Pull up resistor, TTL / CMOS input and drain open circuit are optional; P40 ~ p43 can be reused as SPI1 port, and the
61	P41/78160_IO/INT3/ SPI_SCLK1	PBULD3	
62	P42/78161_IO/INT4/	PBULD3	

	SPI_MISO1		priority of SPI1 is higher than that of p52 ~ p55.
63	P43/78161_I/INT5/ SPI_MOSI1	PBULD3	Note: two 7816 interfaces are supported. 78160_ IO is the bidirectional data port of 78160; 78161_ IO is the bidirectional data port of 78161; In addition, 78161 has registers that can be configured as: 78161_ IO is used as the data output of 78161; 78161_ I as the data input of 7816 1.
64	DGND	GND	DGND
65	P20/RX0	PBULD3	P2 port is multiplexed with UART0 and uart1; Pull up, TTL / CMOS level and drain open circuit are available.
66	P21/TX0	PBULD3	
67	P22/RX1	PBULD3	
68	P23/TX1	PBULD3	
69	P73/SEG15	PBUSG3	LCD / GPIO multiplexing
70	P72/SEG14	PBUSG3	LCD / GPIO multiplexing
71	P71/SEG13	PBUSG3	LCD / GPIO multiplexing
72	P70/SEG12	PBUSG3	LCD / GPIO multiplexing
73	P67/SEG11	PBUSG3	LCD / GPIO multiplexing
74	P66/SEG10	PBUSG3	LCD / GPIO multiplexing
75	P37/INT7/HOSCI	PUXI	P3 port / interrupt / high frequency crystal multiplexing A 10 m ohm resistor and two 15pF capacitors should be connected in series outside the high frequency crystal port.
76	P36/INT6/HOSCO	PUXI	
77	P65/SEG9	PBUSG3	LCD / GPIO multiplexing
78	P64/SEG8	PBUSG3	LCD / GPIO multiplexing
79	P63/SEG7	PBUSG3	LCD / GPIO multiplexing
80	P62/SEG6	PBUSG3	LCD / GPIO multiplexing
81	P61/SEG5	PBUSG3	LCD / GPIO multiplexing
82	P60/SEG4	PBUSG3	LCD / GPIO multiplexing
83	DGND	GND	DGND
84	SEG3/COM7	PAM	Ports multiplexed by SEG and com
85	SEG2/COM6	PAM	Ports multiplexed by SEG and com
86	SEG1/COM5	PAM	Ports multiplexed by SEG and com
87	SEG0/COM4	PAM	Ports multiplexed by SEG and com
88	COM3	PAM	COM port
89	COM2	PAM	COM port
90	COM1	PAM	COM port
91	COM0	PAM	COM port
92	P10/KEY0/TC0_N[0]/TCIN	PBULD3	IO port, key input and timer input and output are multiplexed;
93	P11/KEY1/TC0_P[0]/TCIN	PBULD3	

			Pull up, TTL / CMOS level and drain open circuit are available.
94	P30/INT0/ TCIN	PBUS6	IO port, external interrupt input and timer input are multiplexed; Pull up optional, Schmidt input, 6mA drive capability.
95	P32/ INT2/ RTCOUT / KEY5	PBUS6	IO port, external interrupt input, RTC pulse output, key input multiplexing; Pull up optional, Schmidt input, 6mA drive capability.
96	P26/RX3	PBULD3	Uart3 is multiplexed with P2 port; Pull up, TTL / CMOS level and drain open circuit are available.
97	P27/TX3	PBULD3	
98	P57/SF/TCIN/TC1_P[1]	PBULD3	P57 port, SF apparent power pulse output, tcio multiplexing; Pull up, TTL / CMOS level and drain open circuit are available.
99	P51/QF/RTCOUT/PF/SF	PBUS6	P51 port, reactive pulse output, RTC output, active pulse output and apparent pulse output are multiplexed; Pull up optional, Schmidt input, 6mA drive capability
100	P50/PF/RTCOUT/SF/QF	PBUS6	P50 port, active pulse output, RTC output, apparent pulse output and reactive power pulse output are multiplexed; Pull up optional, Schmidt input, 6mA drive capability

RN8213B（D）	Name	Pin Type	Function Description
1	SWDCLK/ P24/RX2	PBULD3	SWD clock, UART2 input, p24 multiplexing; Pull up, TTL / CMOS level and drain open circuit are available.
2	SWDIO/P25/TX2	PBULD3	SWD data port, UART2 output, P25 multiplexing; Pull up, TTL / CMOS level and drain open circuit are available.
3	P13/KEY3/TCIO	PBULD3	IO port, key input, timer output and timer input are multiplexed; Pull up, TTL / CMOS level and drain open circuit are available.
4	P33/ INT3/ TCI	PBUS6	P3 port is multiplexed with external interrupt and timer input; Pull up optional, Schmidt input, 6mA drive capability.

5	LDO33	LDOOUTPUT	3.3v-ldo output, 0.1uF and 1uF capacitors need to be connected externally;
6	P00/AIN0/KEY2/RX2	PABUS3	P00 port, sar-adc input, key2, rx2 multiplexed pad
7	P01/AIN1/KEY3/TX2	PABUS3	P01 port, sar-adc input, Key3, TX2 multiplexing pad
8	AIN2/CMP1/P02	PABUS3	Sar-adc input, comparator 1 input, P02 multiplexing;
9	AIN3/CMP2/P03	PABUS3	Sar-adc input, low power comparator 2 input, P03 multiplexing;
10	AIN4/LVDIN0/P04/KEY4	PABUS3	Sar-adc input, lvdin input, P04, key4 multiplexing;
11	UP	Analog input	Positive analog input pin of voltage channel
12	UN	Analog input	Negative analog input pin of voltage channel
13	IBP	Analog input	Positive analog input pin for current channel B
14	IBN	Analog input	Negative analog input pin for current channel B
15	IAP	Analog input	Positive analog input pin of current channel a, with maximum gain of 16 times, and external manganese copper sampling circuit. The maximum input signal is ± 1V (differential signal);
16	IAN	Analog input	The negative analog input pin of current channel a has a maximum gain of 16 times and an external manganese copper sampling circuit.
17	AGND	GND	AGND
18	REFV	Vreference	The reference input of ADC should be connected with 0.1uF and 1uF capacitors in parallel
19	VBAT	Power Supply	3.6V battery input pin; it is also the input of internal sar-adc.
20	VCC	Power Supply	The main power input shall be connected with 4.7uf capacitor in parallel with 0.1uF capacitance decoupling.
21	VSWO	Power Supply	The power output after switching between main power and battery should be connected with external 1uF capacitor in parallel with 0.1uF capacitor for decoupling.
22	VSWO	Power Supply	It has the same function as 21 pin, and can be short circuited with 21 pin externally.
23	P56/ZXOUT/TCIN/TC1_N[1]	PBULD3	P56 port, zero crossing output, tcio multiplexing
24	P44/SPI_SCSN0/KEY6	PBULD3	P4 port, spi0 and key are multiplexed;

25	P45/SPI_SCLK0/KEY7	PBULD3	Pull up, TTL / CMOS level and drain open circuit are available.
26	RSTN	reset	Low level reset circuit with pull-up resistor inside;
27	XO	Clock	32.768KHz passive crystal oscillator output and input. It does not need external resistance and capacitance, but needs to be isolated by ground wire. It is suggested to use a crystal oscillator with a load capacitance of 12.5pF.
28	XI	Clock	
29	P14/KEY4/TCO	PBULD3	IO port, key input, timer output and timer input are multiplexed; Pull up, TTL / CMOS level and drain open circuit are available.
30	P15/KEY5/TCIO	PBULD3	
31	P16/KEY6/TCIO	PBULD3	
32	P17/KEY7/TCIO	PBULD3	
33	DGND	GND	DGND
34	P110/SPI-SCSN0	PBULD3	P11 is multiplexed with spi0; Spi0 of port P11 and spi0 of port P4 cannot be used at the same time; Pull up, TTL / CMOS level and drain open circuit are available.
35	P111/SPI-SCLK0	PBULD3	
36	P112/SPI-MISO0	PBULD3	
37	P113/SPI-MOSI0	PBULD3	
38	LDO18	LDO	The output of 1.8V LDO should be connected with external 1uF capacitor in parallel with 0.1uF capacitor to decouple;
39	P46/SPI_MISO0/RX4	PBULD3	P4 port, spi0 and uart4 are multiplexed; Pull up, TTL / CMOS level and drain open circuit are available.
40	P47/SPI_MOSI0/TX4	PBULD3	
41	DGND	GND	DGND
42	P97/SEG35	PBUSG3	LCD / GPIO multiplexing
43	P96/SEG34	PBUSG3	LCD / GPIO multiplexing
44	P95/SEG33	PBUSG3	LCD / GPIO multiplexing
45	P94/SEG32	PBUSG3	LCD / GPIO multiplexing
46	P93/SEG31	PBUSG3	LCD / GPIO multiplexing
47	DGND	GND	DGND
48	P92/SEG30	PBUSG3	LCD / GPIO multiplexing
49	P91/SEG29	PBUSG3	LCD / GPIO multiplexing
50	P90/SEG28	PBUSG3	LCD / GPIO multiplexing
51	P87/SEG27	PBUSG3	LCD / GPIO multiplexing
52	P86/SEG26	PBUSG3	LCD / GPIO multiplexing
53	P85/SEG25	PBUSG3	LCD / GPIO multiplexing
54	P84/SEG24	PBUSG3	LCD / GPIO multiplexing
55	P83/SEG23	PBUSG3	LCD / GPIO multiplexing
56	DGND	GND	DGND
57	P82/SEG22	PBUSG3	LCD / GPIO multiplexing
58	P81/SEG21	PBUSG3	LCD / GPIO multiplexing

59	P80/SEG20	PBUSG3	LCD / GPIO multiplexing
60	P77/SEG19	PBUSG3	LCD / GPIO multiplexing
61	P76/SEG18	PBUSG3	LCD / GPIO multiplexing
62	P75/SEG17	PBUSG3	LCD / GPIO multiplexing
63	P74/SEG16	PBUSG3	LCD / GPIO multiplexing
64	DGND	GND	DGND
65	LCDVP2	simulation	For analog output, a capacitance of 100nF should be connected between lcdvp2 and lcdvp1.
66	LVDVP1	simulation	For analog output, a capacitance of 100nF should be connected between lcdvp2 and lcdvp1.
67	LCDVA	simulation	LCD voltage output, need external 470nf capacitor
68	LCDVB	simulation	LCD voltage output, need external 470nf capacitor
69	LCDVC	simulation	LCD voltage output, need external 470nf capacitor
70	LCDVD	simulation	LCD voltage output, need external 470nf capacitor
71	DGND	GND	DGND
72	P52/SCL/TCIN/TC0_N[1]/ SPI_SCSN1	PBULD3	P5 port, I2C, tcio and SPI1 are multiplexed. Pull up resistor, TTL / CMOS input and drain open circuit are optional; P52 ~ p55 can be reused as SPI1 ports, and the priority of SPI1 is lower than that of P40 ~ p43.
73	P53/SDA/TCIN/TC0_P[1]/ SPI_SCLK1	PBULD3	
74	P54/RX5/TCIN/TC1_N[0]/ SPI_MISO1	PBULD3	P5 port, uart5, tcio, SPI1 multiplexing
75	P55/TX5/TCIN/TC1_P[0]/ SPI_MOSI1	PBULD3	
76	P40/7816CLK/INT1/ SPI_SCSN1	PBULD3	IO port, 7816, int, SPI1 multiplexing pin. It can support two 7816 interfaces. 78160_ IO is the bidirectional data port of 78160; Pull up resistor, TTL / CMOS input and drain open circuit are optional; P40 ~ p43 can be reused as SPI1 port, and the priority of SPI1 is higher than that of p52 ~ p55
77	P41/78160_IO/INT3/ SPI_SCLK1	PBULD3	
78	NC	Not connected	
79	P42/78161_IO/INT4/ SPI_MISO1	PBULD3	78161_ IO is the bidirectional data port of 78161; Pull up resistor, TTL / CMOS input and drain open circuit are optional;
80	DVDD	Power	1.8V standby power supply, suspended.

		Supply	
81	P43/78161_I/INT5/ SPI_MOSI1	PBULD3	7816 1 has registers that can be configured as: 78161_ IO is used as the data output of 78161; 78161_ I as the data input of 7816 1.
82	DGND	GND	DGND
83	P20/RX0	PBULD3	P2 port is multiplexed with UART0; Pull up, TTL / CMOS level and drain open circuit are available.
84	P21/TX0	PBULD3	
85	DGND	GND	DGND
86	P22/RX1	PBULD3	P2 port is multiplexed with uart1; Pull up, TTL / CMOS level and drain open circuit are available.
87	P23/TX1	PBULD3	
88	P73/SEG15	PBUSG3	LCD / GPIO multiplexing
89	P72/SEG14	PBUSG3	LCD / GPIO multiplexing
90	P71/SEG13	PBUSG3	LCD / GPIO multiplexing
91	P70/SEG12	PBUSG3	LCD / GPIO multiplexing
92	P67/SEG11	PBUSG3	LCD / GPIO multiplexing
93	P66/SEG10	PBUSG3	LCD / GPIO multiplexing
94	P103/SEG39	PBUSG3	LCD / GPIO multiplexing
95	P102/SEG38	PBUSG3	LCD / GPIO multiplexing
96	P37/INT7/HOSCI	PUXI	P3 port / interrupt / high frequency crystal multiplexing A 10 m ohm resistor and two 15pF capacitors should be connected in series outside the high frequency crystal port.
97	P36/INT6/HOSCO	PUXI	
98	P101/SEG37	PBUSG3	LCD / GPIO multiplexing
99	P65/SEG9	PBUSG3	LCD / GPIO multiplexing
100	P64/SEG8	PBUSG3	LCD / GPIO multiplexing
101	P63/SEG7	PBUSG3	LCD / GPIO multiplexing
102	P62/SEG6	PBUSG3	LCD / GPIO multiplexing
103	P61/SEG5	PBUSG3	LCD / GPIO multiplexing
104	P60/SEG4	PBUSG3	LCD / GPIO multiplexing
105	DGND	GND	DGND
106	SEG3/COM7	PAM	Ports multiplexed by SEG and com
107	SEG2/COM6	PAM	Ports multiplexed by SEG and com
108	SEG1/COM5	PAM	Ports multiplexed by SEG and com
109	SEG0/COM4	PAM	Ports multiplexed by SEG and com
110	COM3	PAM	COM port

111	COM2	PAM	COM port
112	COM1	PAM	COM port
113	COM0	PAM	COM port
114	P100/SEG36	PBUSG3	LCD / GPIO multiplexing
115	P10/KEY0/ TCIO	PBULD3	IO port, key input and timer input and output are multiplexed; Pull up, TTL / CMOS level and drain open circuit are available.
116	P11/KEY1/TCIO	PBULD3	
117	P12/KEY2/TCIO	PBULD3	
118	P30/INT0/ TCI/TX4	PBUS6	IO port, external interrupt input, timer input, TX4 multiplexing; Pull up optional, Schmidt input, 6mA drive capability.
119	P31/ INT1/TCI/RX4	PBUS6	IO port, external interrupt input, timer input, RX4 multiplexing; Pull up optional, Schmidt input, 6mA drive capability.
120	P32/ INT2/ RTCOUT / KEY5	PBUS6	IO port, external interrupt input, RTC pulse output, key input multiplexing; Pull up optional, Schmidt input, 6mA drive capability.
121	P26/RX3	PBULD3	Uart3 is multiplexed with P2 port; Pull up, TTL / CMOS level and drain open circuit are available.
122	P27/TX3	PBULD3	
123	P57/SF/TCIN/TC1_P[1]	PBULD3	P57 port, SF apparent power pulse output, tcio multiplexing; Pull up, TTL / CMOS level and drain open circuit are available.
124	P51/QF/RTCOUT/PF/SF	PBUS6	P51 port, reactive pulse output, RTC output, active pulse output and apparent pulse output are multiplexed; Pull up optional, Schmidt input, 6mA drive capability
125	P50/PF/RTCOUT/SF/QF	PBUS6	P50 port, active pulse output, RTC output, apparent pulse output and reactive power pulse output are multiplexed; Pull up optional, Schmidt input, 6mA drive capability
126	P34/INT4/SF	PBUS6	P34 is multiplexed with external interrupt and apparent pulse SF;
127	P35/ INT5/ TCI	PBUS6	P35 is multiplexed with external interrupt and timer input;

			Pull up optional, Schmidt input, 6mA drive capability.
128	DGND	GND	DGND

RN821X Key Pin Description:

1.LDO33 is output of 3.3V LDO, power supply for ADC; external connects 0.1uf and 10uf capacitor;

2.UP,UN,IBP,IBN,IAP,IAN use a conventional measure chip connection;

3.AGND is analog ground, DGND is digital ground; which can be rationally distributed according to the actual use experience;

4.REFV is the reference input of measure ADC, external connects both 0.1uf and 10uf capacitor;

5.VBAT is the input of 3.6V battery;

6.VCC is the main power input, the normal operating range2.8V~5.5V,external connects both 10uf and 0.1uf for decoupling;

7.VSWO is the power output after switching VCC and VBAT, external connects both 10uf and 0.1uf for decoupling;

8.32.768KHz crystal connects crossover between XO and XI, which should be isolated by the ground wire, external resistors and capacitors are not necessary;

9.LDO18 is the output of 1.8V LDO, supplying power to the 1.8V digital domain of chip, external connects both 10uf and 0.1uf for decoupling;

10.LCDVD,LCDVC,LCDVB,LCDVA is the voltage output of LCD, which should be connected external 470nf capacitor;

11.An 100nf capacitor is connected between LCDVP1 and LCDVP2.

12.When LCD/GPIO multiplexing PAD is chosen to GPIO, it's structure is open drain; only LCD is selected to 5V, GPIO is selectable, and if LCD is selected to 3.3V,GPIO is not available.

2 Electrical Characteristics

Measurement Parameters (VCC=3V~5.5V,room temperature)						
Measurement Items	Symbol	Min	Typical	Max	Unit	Test Conditions, Notes
Active energy measure error	Err			±0.1%		1000:1 dynamic range at normal temperature
Active energy measure bandwidth	BW		7		kHz	
reactive energy measure error	Err			±0.1%		1000:1 dynamic range at normal temperature
Apparent energy measure error	Err			±0.1%		1000:1 dynamic range at normal temperature
RMS measure error	Err			±0.2%		1000:1 dynamic range at normal temperature
Power measure error	Err			±0.1%		1000:1 dynamic range at normal temperature
Energy pulse output Max Frequency Duty Cycle High Pulse Width	 Hz % ms		 50% 84ms	20KHz		When Pulse Width less than 84ms
Sigma-Delta ADC Performance						
The maximum signal level	V_{xn}			±1000	mV	the differential signal
ADC Offset error	DC_{off}		1		mV	
-3dB Bandwidth	B_{-3dB}		7		kHz	
Reference voltage (VCC=3V~5.5V,temperature range:-40℃～+85℃)						
Output Voltage	V_{ref}	1.25	1.26	1.27	V	
Temperature Coefficient	T_c		5	15	ppm/℃	
Analog Peripherals						
Low power comparator CMP2 Threshold	CMP2	1.1	1.22	1.35	V	It is threshold of CMP2's output low comparison results Threshold of output high comparison results is 200mv higher than this.
SAR ADC input range	SAR-IN	0		LBGR	V	LBGR is internal low-power reference, typical value :1.25V
Switch to the main power Threshold	Power-on switch threshold	2.6	2.8	3.0	V	When VCC is higher than this threshold or VBAT, power switch to VCC. It is suggested that when the

						main power supply is 3.3V, the power supply voltage range should be 3.3V ±5%.
Switch to the battery Threshold	Power-off switch threshold	2.5	2.7	2.9	V	When VCC is lower than this threshold and VBAT, power switch to VBAT.
LCD output voltage	LCDVD	4.85	5.05	5.25	V	Full temperature range test;
VBAT measure	VBATD	0	3.6	3.8	V	Measure range of VBAT by SAR ADC;
LBGR voltage	LBGR	1.22	1.27	1.32	V	Full temperature range test;
Clock Parameters						
Clock frequency range at low-frequency input	XI		32.768		KHz	
Clock frequency range at low-frequency input	HOSI	3.6864	7.3728	29.4912	Mhz	
Internal PLL clock frequency range	PLL		7.3728		MHz	
Internal high frequency RC	RCH	1.4	1.6	1.8	MHz	The typical value of internal RCH is 3.2mhz, and the default clock is used for chip reset after dichotomy
Internal low frequency RC	RCL	20	30	40	KHz	Clock for WDT
Power supply						
Main source	VCC	2.8	5/3.3	5.5	V	
Minimum cpu operating voltage	Vil	2.1	2.2	2.35	V	Normal temperature
	Vil	2	2.15	2.3	V	Low temperature:-40 ℃
	Vil	2.2	2.3	2.45	V	High temperature:85 ℃
Battery	VBAT		3.6			
Analog current	AIdd		2		mA	Three-way ADC are open
Digital current	DIdd		1.5		mA	CPU operating at 3.6864MHz,Measurement open
Sleep Power Consumption	SIdd		10		μA	RTC Automatic temperature compensation, RAM hold; CPU and digital peripherals are power on; WDT open; Source monitor open; interrupt wake up
LDO33	V33	3.2	3.3	3.4	V	
LDO18	V1P8	1.62	1.8	1.98	V	
Limit Parameters						
Main source voltage	Vvcc	-0.3	--	＋7	V	
Battery input voltage	Vvbat	-0.3	--	＋7	V	
DV_{DD} to DGND		-0.3	--	＋7	V	
DV_{DD} to AV_{DD}		-0.3		+0.3	V	

V1P,V1N,V2P,V2N,V3P,V3N		-6		+6	V	
Digital IO output high voltage	VOH		--	DV_{DD} +0.3	V	
Digital IO output low voltage	VOL	-0.3	--		V	
Digital IO input high voltage	VIH		0.7VCC			CMOS
Digital IO input low voltage	VIL		0.3VCC			CMOS
Digital IO input high voltage	VIH		0.4VCC			TTL
Digital IO input low voltage	VIL		0.2VCC			TTL
Isource of digital IO	Isource	5		10	mA	6mA Type
Isink of digital IO	Isink	7		15	mA	6mA Type
Isource of digital IO	Isource	3		5	mA	3mA Type
Isink of digital IO	Isink	5		10	mA	3mA Type
Analog input voltage with respect to AGND	V_{INA}	-0.3	--	AV_{DD} +0.3	V	
Operate temperature range	T_A	-40	--	85	℃	
Storage Temperature Range	T_{stg}	-65	--	150	℃	

3 System Control

3.1 Power Management Solutions

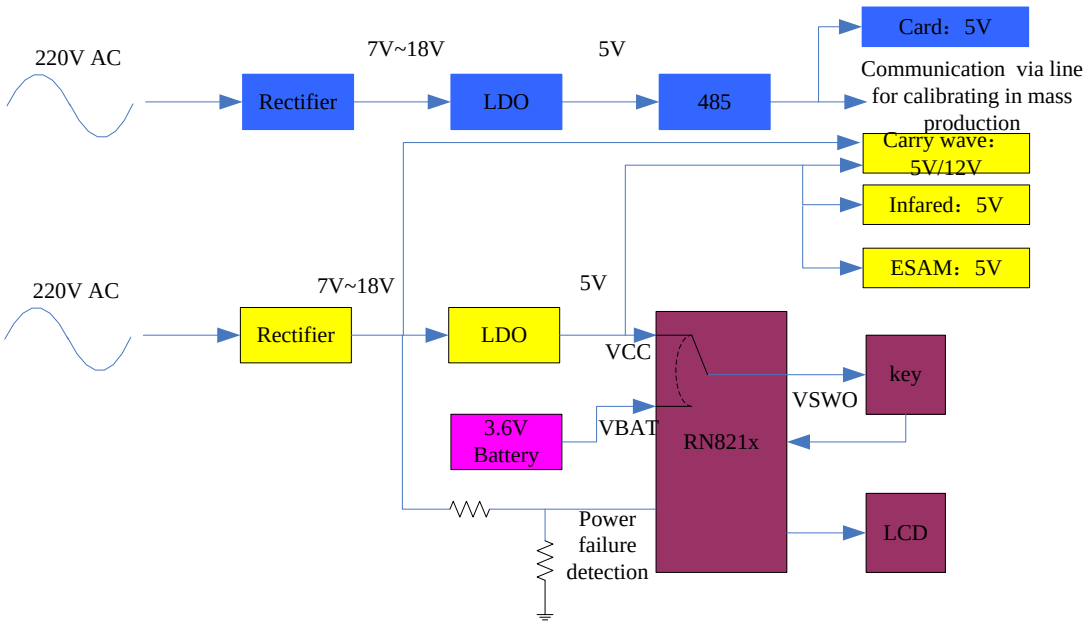


Figure 3.1 single-phase meter power management solution:internal battery switch

3.2 Clock Source

- Two external clock:
  32.768KHz crystal, supply for RTC and CPU low frequency operation, never turn off;
  External clock, support 3.6864Mhz and *2/*4/*8 four frequency, using for CPU main system;
- 3 internal clock :
  1.6MHz RC supply for CPU after chip power-on reset, default clock of CPU is IRC after power-on reset.
  32KHz RC clock, using for WDT clock.
  7.3728MHz PLL output, which is the system main clock, CPU switch clock from low frequency to high frequency by command.

3.3 Clock Switch

Include switchings as follows:

1. Default select IRC after first power-on reset;
2. Switch between high-frequency mode and IRC, which is completed by CPU command;
3. Switch between high-frequency mode and LOSC, which is completed by CPU command;
4. Switch between LOSC and IRC, which is completed by CPU command;

Please call the library function provided by Renergy to complete clock switching.
Renergy clock switching library function complete FLASH and EEPROM parameter configuration firstly, then run mode switch command.
If external high-frequency crystal HOSC is selected as system main clock,OSC_CTL2 register should be configured before calling library function.
If PLL is selected as system main clock at first power-on, calling the clock switching library function need to wait for 32KHz crystal oscillator start-up(start-up time is approximately 1.5s).

3.4 Soc Low-power Mode

Two low-power mode of M0:
Sleep and DeepSleep. For RN821x, the difference between Sleep and DeepSleep is only that the clock of some modules will automatically turn off when DeepSleep, Using only Sleep without using DeepSleep is recommended to users. Module clock using software turn off without using DeepSleep auto-off.
Besides low-power mode of M0,SOC providing a flexible mechanism to realize the needs of users in different power modes:

1. Providing high frequency clock mode HCM,internal RC mode RCM,low frequency clock mode LCM,CPU can switch between any of the three modes by instructions;
2. CPU,peripheral clock or power supply can be turned off;
3. Minimum power mode(CPU sleep,SRAM and digital peripherals does not power down,RTC run,main power monitor open)power consumption is about 8uA;

Users can flexibility achieve low power mode they need according to the mechanism SOC provides above. The main module's default state after power-up:

Main Module	Default State
1.8V voltage domain	
M0 core	Open, closable clock, never power down

Interrupt system	Open, closable clock, never power down
SRAM	Open, closable clock, never power down
ROM	Open, closable clock, never power down
FLASH	Open, automatically power off after CPU sleep
EEPROM	Open, power down need to call Renergy library functions when CPU sleep;
RTC	Open, calendar can not be closed, no reset
EMM(normal measure)	Open, closable clock, never power down
Other peripherals	Open, closable clock, never power down
5V voltage domain	
Measurer ADC	Close, closable power supply
Measure ref	Close, closable power supply
3.3V LDO	Close, closable power supply
1.8V LDO	Open, can not be closed
RC	Open ,closable power supply
Comparator CMP2	Open ,closable power supply
Comparator CMP2	Close, closable power supply
LCD	Close, closable power supply
Temperature ADC	Timing open
LVD	Close, closable power supply
Comparator	Close, closable power supply
Power reset system	Always open
PLL	Close, closable power supply
HOSC	Close, closable power supply
LOSC	Always open

The default closed modules can be choose to open or close under the three clocks.

3.5 Reset

Reset source:

External PIN reset, global reset;

Power-on and power-down reset, global reset;

Mode switch reset, only reset partial modules(measure);

Software reset, global reset;

Watchdog, global reset;

3.6 Register Description

The base address of system control module:

Module Name	**Physical Address**	**Mapping Address**
SYSC	0x40034000	0x40034000
Register Name	**Address Offset**	**Description**
OSC_CTL1	0x0	System OSC control register1
SYS_MODE	0x4	System mode switch register

SYS_PD	0x8	System power down control register
ADC_CTL	0xC	ADC control register
OSC_CTL2	0x10	System OSC control register2
SYS_RST	0x14	System reset register
MAP_CTL	0x18	Address Mapping control register
MOD0_EN	0x1C	Module enable 0 register
MOD1_EN	0x20	Module enable 1 register
INTC_EN	0x24	INTC enable register
KBI_EN	0x28	KBI enable register
CHIP_ID	0x2C	Chip version number
SYS_PS	0x30	**System register password protection bit, write is 0x82,0x00~0x28 writable register**

- System OSC control register1 OSC_CTL1(0x0)

Bit	Name	Description	write/read flag	Reset value
31:16	Reserve	Reserve	R	0
15:11	CLOCK_FLAG	System clock open flag: if clock opened, this bit is 1: { HOSC,RCL,RCH,PLL, LOSC}	R	01101
10:8	SYSCLK_STAT	System main clock frequency instruction: 000:current system master clock is 7.3728MHz; 001:current system master clock is 3.6864MHz; 010:current system master clock is 1.8432MHz; 011:current system master clock is 32.768KHz; 100:current system master clock is 14.7456Mhz; (only support external crystal oscillator) 101:current system master clock is 29.4912Mhz; (only support external crystal oscillator)	R	010
7	PLL_LOCK	PLL Lock Status 0:Unlocked 1:locked	R	0
6	PLL_HOSC_ON	System operating at external high frequency or internal PLL clock, this bit is 1; System operating at other clocks, this bit is 0.	R	0
5	IRCH_ON	System operating at internal high frequency clock, this bit is 1; System operating at other clocks, this bit is 0.	R	1

4	LOSC_ON	System operating at external low frequency clock, this bit is 1; System operating at other clocks, this bit is 0.	R	0
3:2	PLL_HOSC_DIV	System master clock divide select:(Only valid for high frequency clock mode) 00:PLL,HOSC as CPU master clock; 01:Two Division of PLL,HOSC as CPU master clock; 10:Four division of PLL,HOSC as CPU master clock; 11:Eight division of HOSC(clock select as 14MHz and 29MHz) as CPU master clock; Note: Can only be changed under RC or LC mode. Note: These registers only decide division factor, and specific system master frequency is determined by the frequency division factor and current clock source.	R/W	01
1	IRCH_PD	1.6MHz internal RC enable bit: 0:open; 1:close.	R/W	0
0	PLL_PD	PLL module enable bit (32.768KHz---7.3728MHz) 0:open; 1:close.	RW	1

When users switch clock, it is recommended to call Renergy library functions. And it is not recommended write OSC_CTL1 (0x0) register in applications.

- System Mode Setting Register SYS_MODE(0x4)

Bit	Name	Description	Read /write flag	Reset value
31:6	---	Reserve	R	0
5	FLASH_BUSY	Flash busy status, can not enter the mode switch: 0:idle 1:busy	R	0
4	EEPROM_BUSY	eeprom busy status, can not enter the mode switch: 0:idle 1:busy	R	0
3:0	MODE	Write D,set enter high frequency mode HCM,bit2 read is 1; Write E, set enter RC mode RCM,bit1 read is1; Write F, set enter 32.768KHz mode LCM,bit0	R/W	2

		read is1. The register read value is: {0,HCM,RCM,LCM}		

Note: The instructions of current mode status should be read from LOSC_ON,IRCH_ON,PLL_HOSC_ON(OSC_CTL register bit4~6) these three status. But not from this register. This register represents the mode switch command is written, which does not mean that has been switched to the desired mode.

When users switch clock, it is recommended to call Renergy library functions. And it is not recommended write SYS_MODE(0x4) register in applications.

- System Power Down Control Register SYS_PD(0x8)

Bit	Name	Description	Read/write flag	Reset value
31:8	---	Reserve	R	0
7	LBGR_PD	LBGR power switch 0:power on 1:power down Note: LCD open, LVD open,CMP1 open, LBGR_PD register open, any of these is satisfied LBGR will open.	R/W	1
6	BGR_PD	BGR power switch 0:power on 1:power down Note :I1 passage ADC,I2 passage ADC,U1 passage ADC, temperature measure open,BGR_PD register open, any of these is satisfied BGR will open.	R/W	1
5	CMP2_PD	Comparator 2(low power comparator)power switch 0:power on 1:power down	R/W	0
4	CMP1_PD	comparator1 power switch 0:power on 1:power down **Note:RN8211 doesn't support, it's reset value shouldn't be changed;**	R/W	1
3	LVD_PD	LVD power switch 0:power on 1:power down	R/W	1
2	ADCU_PD	U passage ADC power switch 0:power on 1:power down	R/W	1
1	ADCI2_PD	I2 passage ADC power switch 0:power on 1:power down	R/W	1

		Note:RN8211 doesn't support, it's reset value shouldn't be changed;		
0	ADCI1_PD	I1 passage ADC power switch 0:power on 1:power down	R/W	1

- ADC Control Register ADC_CTL(0xC)

Bit	**Name**	**Description**	**Read/ write flag**	**Reset value**
31:9	---	Reserve	R	0
8:6	ADCU_PGA	U passage ADC gain configure =x00 1 =x01 2 =x10 4 =x11 4	R/W	0
5:3	ADCI2_PGA	I2 passage ADC gain configure =x00 1 =x01 2 =x10 4 =x11 4 **Note:RN8211 doesn't support, it's reset value shouldn't be changed;**	R/W	0
2:0	ADCI1_PGA	I1 passage ADC gain configure =x00 1 =x01 2 =x10 8 =x11 16	R/W	0

- System OSC Control Register 2 OSC_CTL2(0x10)

Bit	**Name**	**Description**	**Read /write flag**	**Reset value**
31:5	Reserve	Reserve		
4	PLL_HOSC_SEL	when it is running at full speed, the system master clock select: 0:select PLL output as system master clock; 1:select backup high frequency crystal as system master clock; It can only be configured under RC mode and low frequency mode.	R/W	0
3	HOSC_PD	External high frequency oscillator enable bit: 0:open 1:close	RW	1
2:0	HOSC_ FREQ	000:External high crystal is 7.3728MHz 001:External high crystal is 14.7456MHz 010:Reserve 011:External high crystal is 29.4912MHz	RW	000

If system clock is selected as external high frequency crystal, before switching clock by calling Renergy library functions, OSC_CTL2 of user's application register should be configured.

- **System Clock Configuration Truth Table:**

	PLL_HOSC_DIV=00 No division	PLL_HOSC_DIV=01 2 division	PLL_HOSC_DIV=10 4 division	PLL_HOSC_DIV=11 8 division
PLL_HOSC_SEL=0 PLL_FREQ=000	**7.3728Mhz**	**3.6864MHz**	**1.8432MHz**	**8 division is unsupported, if configured it is 1.8432Mhz**
PLL_HOSC_SEL=1 HOSC_ FREQ =000	**7.3728Mhz**	**3.6864MHz**	**1.8432MHz**	**8 division is unsupported, if configured it is 1.8432Mhz**
PLL_HOSC_SEL=1 HOSC_ FREQ =001	**14.7456Mhz**	**7.3728Mhz**	**3.6864Mhz**	**1.8432Mhz**
PLL_HOSC_SEL=1 HOSC_ FREQ =010	**29.4912Mhz**	**14.7456Mhz**	**7.3728Mhz**	**3.6864Mhz**

- System Reset Register SYS_RST(0x14)

(This register's 8-5 bit can only be power on/down reset)

Bit	**Name**	**Description**	**Read/ write flag**	**Reset value**
31:9	---	Reserve	R	0
8	MCU_RST	CPU reset flag(occur software reset or LOCK UP reset): =1 represents that the reset occurred,=0 represents un happen. Write 1 to clear	R	0
7	WDT_RST	WDTreset flag: =1 represents that the reset occurred,=0 represents un happen. Write 1 to clear	R	0
6	PIN_RST	External pin reset flag: =1 represents that the reset occurred,=0 represents un happen. Write 1 to clear	R	0
5	POWEROK_RST	Source power on/down reset flag =1 represents that the reset occurred,=0 represents un happen. Write 1 to clear	R	1
4:3	Reserve	---	R	0
2	LOCKUP_ENRST	LOCKUP enable reset(CPU occurs twice Hard Fault will cause LOCKUP, if enable this bit, can cause system reset): 0: LOCKUP doesn't cause system reset 1: LOCKUP cause system reset	R/W	0
1	Reserve	---	R	0
0	EMU_RST_REQ	Software reset EMU calculate: Write 1 reset EMU calculate module; Write 0 cancel EMU calculate module. Don't reset EMU module configure register;	R/W	0

- Address Mapping Control Register MAP_CTL(0x18)

Bit	Name	Description	Read/ write flag	Reset value
31:3	---	Reserve	R	0
2:0	REMAP	Address mapping: 000:FLASH mapping to 0 address(normal mode) 001:FLASH/EEPROM mapping address exchange 010:FLASH/SRAM mapping address exchange 011: Reserve 100:FLASH mapping to 1/2 capacity address(only support half of 192K capacity) Others: Reserved.	R/W	00

- Module Enable 0 Register MOD0_EN(0x1C)

Bit	Name	Description	Read/write flag	Reset value
31:16	---	Reserve	R	0
15	SPI_EN	SPI module enable clear, clock gating,cm0 enter deepsleep synchronous close this clock: 0:Clock stop, module clear 1:Clock start, module enable **Note:RN8211 doesn't support, it's reset value shouldn't be changed;**	R/W	0
14	I2C_EN	I2C module enable clear, clock gating,cm0 enter deepsleep synchronous close this clock: 0:Clock stop, module clear 1:Clock start, module enable	R/W	0
13	ISO7816_EN	ISO7816 module enable clear, clock gating,cm0 enter deepsleep synchronous close this clock: 0:Clock stop, module clear 1:Clock start, module enable **Note:RN8211 doesn't support, it's reset value shouldn't be changed;**	R/W	0
12	UART38K _EN	UART38K infrared modulated clock open enable,cm0 enter deepsleep synchronous close this clock: 0:Clock stop, module clear 1:Clock start, module enable	R/W	0
11	UART3_EN	UART3 module enable clear, clock gating,cm0 enter deepsleep synchronous close this clock: 0:Clock stop, module clear	R/W	0

		1:Clock start, module enable **Note:RN8211 doesn't support, it's reset value shouldn't be changed;**		
10	UART2_EN	UART2 module enable clear, clock gating,cm0 enter deepsleep synchronous close this clock: 0:Clock stop, module clear 1:Clock start, module enable	R/W	0
9	UART1_EN	UART1 module enable clear, clock gating,cm0 enter deepsleep synchronous close this clock: 0:Clock stop, module clear 1:Clock start, module enable	R/W	0
8	UART0_EN	UART0 module enable clear, clock gating,cm0 enter deepsleep synchronous close this clock: 0:Clock stop, module clear 1:Clock start, module enable	R/W	0
7	UART5_EN	UART5 module enable clear, clock gating,cm0 enter deepsleep synchronous close this clock: 0:Clock stop, module clear 1:Clock start, module enable	R/W	0
6	---	Reserve	R	0
5	TC1_EN	TC1 module enable clear, clock gating,cm0 enter deepsleep synchronous close this clock: 0:Clock stop, module clear 1:Clock start, module enable **Note:RN8211 doesn't support, it's reset value shouldn't be changed;**	R/W	0
4	TC0_EN	TC0 module enable clear, clock gating,cm0 enter deepsleep synchronous close this clock: 0:Clock stop, module clear 1:Clock start, module enable	R/W	0
3	CPC_EN	Coprocessor module enable clear, clock gating,cm0 enter deepsleep synchronous close this clock: 0:Clock stop, module clear 1:Clock start, module enable **Note:RN8211 doesn't support, it's reset value shouldn't be changed;**	R/W	0
2	EEPROM_EN	EEPROM module enable clear, clock gating,cm0 enter deepsleep synchronous close this clock:	R/W	1

		0:Clock stop, module clear 1:Clock start, module enable		
1:0	---	Reserve	R	0

- Module 1 Enable Register MOD1_EN(0x20)

Bit	Name	Description	R/W	Reset value
31:16	---	Reserved	R	0
15:12	---	Reserved	R	0
11	SAR_EN	SAR Module Enable Cleared, apb Bus Clock Gating: 0:Clock Stops 1:Clock Starts	R/W	0
10	RTC_EN	RTC apb Bus Clock Gating. cm0 enters in deepsleep and closes this clock synchronously: 0:Clock Stops 1:Clock Starts **Customers are advised not to turn off the clock.**	R/W	1
9	WDT_EN	WDT apb Bus Clock Gating. cm0 enters in deepsleep and closes this clock synchronously: 0:Clock Stops 1:Clock Starts **Customers are advised not to turn off the clock.**	R/W	1
8	---	Reserved	R	0
7	EMU_EN	EMU Module Enable Cleared, clock gating: 0:Clock Stops 1:Clock Starts	R/W	0
6	LCD_EN	LCD Nodule Enable Cleared, clock gating: 0:Clock Stops, module cleared 1:Clock Starts, module enabled	R/W	0
5	GPIO_EN	GPIO Module Enable Cleared, clock gating. cm0 enters in deepsleep and closes this clock synchronously: 0:Clock Stops, module cleared 1:Clock Starts, module enabled	R/W	0
4	DMA_EN	DMA apb Clock Gating. cm0 enters in deepsleep and closes this clock synchronously: 0:Clock Stops, module cleared 1:Clock Starts, module enabled **Note: RN8211/RN8213 does not support this and the reset value should not be changed.**	R/W	0
3	---	Reserved	R	0

2	---	Reserved	R	0
1	DMA1_EN	DMA1 Module Enable Cleared, clock gating: 0:Clock Stops, module cleared 1:Clock Starts, module enabled **Note: RN8211/RN8213 does not support this and the reset value should not be changed.**	R/W	0
0	DMA0_EN	DMA0 Module Enable Cleared, clock gating: 0:Clock Stops, module cleared 1:Clock Starts, module enabled **Note: RN8211/RN8213 does not support this and the reset value should not be changed.**	R/W	0

- INTC Enable Register INTC_EN(0x24)

Bit	Name	Description	R/W	Reset value
31:16	---	Reserved	R	0
15:9	---	Reserved	R	0
8	INTC_EN	INTC apb Module Clock Gating: 0:Clock Stops 1:Clock Starts	R/W	0
7	INTC7_EN	INTC7 Module Enable Cleared, clock gating: 0:Clock Stops 1:Clock Starts	R/W	0
6	INTC6_EN	INTC6 Module Enable Cleared, clock gating: 0:Clock Stops 1:Clock Starts	R/W	0
5:3	---	Reserved	R	0
2	INTC2_EN	INTC 2 Module Enable Cleared, clock gating: 0:Clock Stops, module cleared 1:Clock Starts, module enabled	R/W	0
1	---	Reserved	R	0
0	INTC0_EN	INTC0 Module Enable Cleared, clock gating: 0:Clock Stops, module cleared 1:Clock Starts, module enabled	R/W	0

- KBI Enable Register KBI_EN(0x28)

Bit	Name	Description	R/W	Reset value
31:9	---	Reserved	R	0
8	KBI_EN	KBI apb Module Clock Gating: 0:Clock Stops 1:Clock Starts	R/W	0
7:2	---	Reserved	R	0
1	KBI1_EN	KBI1 Module Enable Cleared, clock gating: 0:Clock Stops, module cleared 1:Clock Starts, module enabled	R/W	0

0	KBI0_EN	KBI0 Module Enable Cleared, clock gating: 0:Clock Stops, module cleared 1:Clock Starts, module enabled	R/W	0

- Device ID Register CHIP_ID(0x2C)

Bit	Name	Description	R/W	Reset value
31:24	---	Reserved	R	0
15:0	CHIP_ID	Chip ID:821x	R	821x

- System Control Password Register SYS_PS(0x30)

Bit	Name	Description	R/W	Reset value
31:8	---	Reserved	R	0
7:0	SYS_PSW	When SYS_PSW=0x82, 0x00 ~ 0x28 register can be written; When SYS_PSW=other values, 0x00 ~ 0x28 register can not be written; The register's read value is its written value. Users are advised to turn off write-enable immediately after completing the write operation.	R/W	00

4 CPU System

4.1 Overview

There are three ways (three master devices) which can initiate access to SoC built-in device.

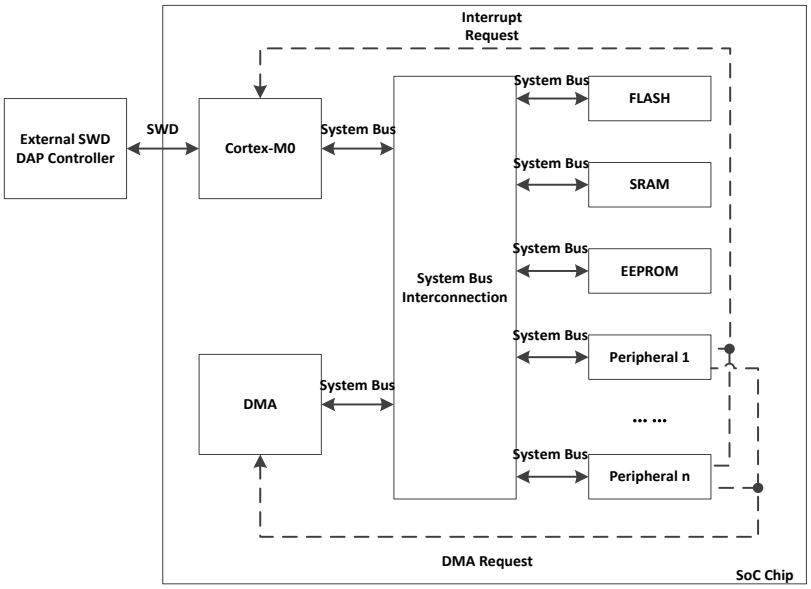
- Cortex-M0:
  - Instruction Access and Data Access;
  - Accessible to all slave devices.
- External SWD Controller(JLINK or similar function devices):
  - Debug Interface and Resource Access;
  - Accessible to all slave devices.
- DMA:
  - Data Access;
  - Accessible to all slave devices.

SoC built-in slave device resources include memory (FLASH, EEPROM and SRAM) and various peripherals (UART, Timer, Watchdog, etc.).

Part of the peripherals can initiate the interrupt request, such as UART, timer, etc.

Part of the peripherals can initiate the DMA request, such as UART, LCD, etc.

Figure 4-1 SOC device physical interconnection architecture



4.2 Cortex-M0 Processor

Cortex-M0 processor is a 32-bit processor which is designed for the embedded systems, and has the following characteristics:

- Easy-to-use programming model
- High code density, with 32-bit properties
- Tool and binary code upward compatible with cortex-m processor series, easy to upgrade and expand
- A low-power sleep mode integrated
- High efficient code execution allows that the processor clock is more low, or extend the time for sleep mode
- 32-bit single-cycle hardware multiplier
- Zero jitter interrupt handling
- Interrupt timing determination, interrupt processing efficiency
- Supporting interrupt / exception nesting and seizing
- Supporting 24-bit system beats counter
- Providing four interrupt priorities
- Supporting two observation points, four hardware breakpoints
- Supporting serial debug interface (swd), to achieve the internal state of the processor highly visible and controllable
- See the arm document for more information on the cortex-m0.

4.3 Memory Mapping

Please refer to "Figure 4 2 SoC address space mapping" for the memory mapping of SoC

Figure 4-2 SoC address space mapping

4.3.1 Memory Remapping

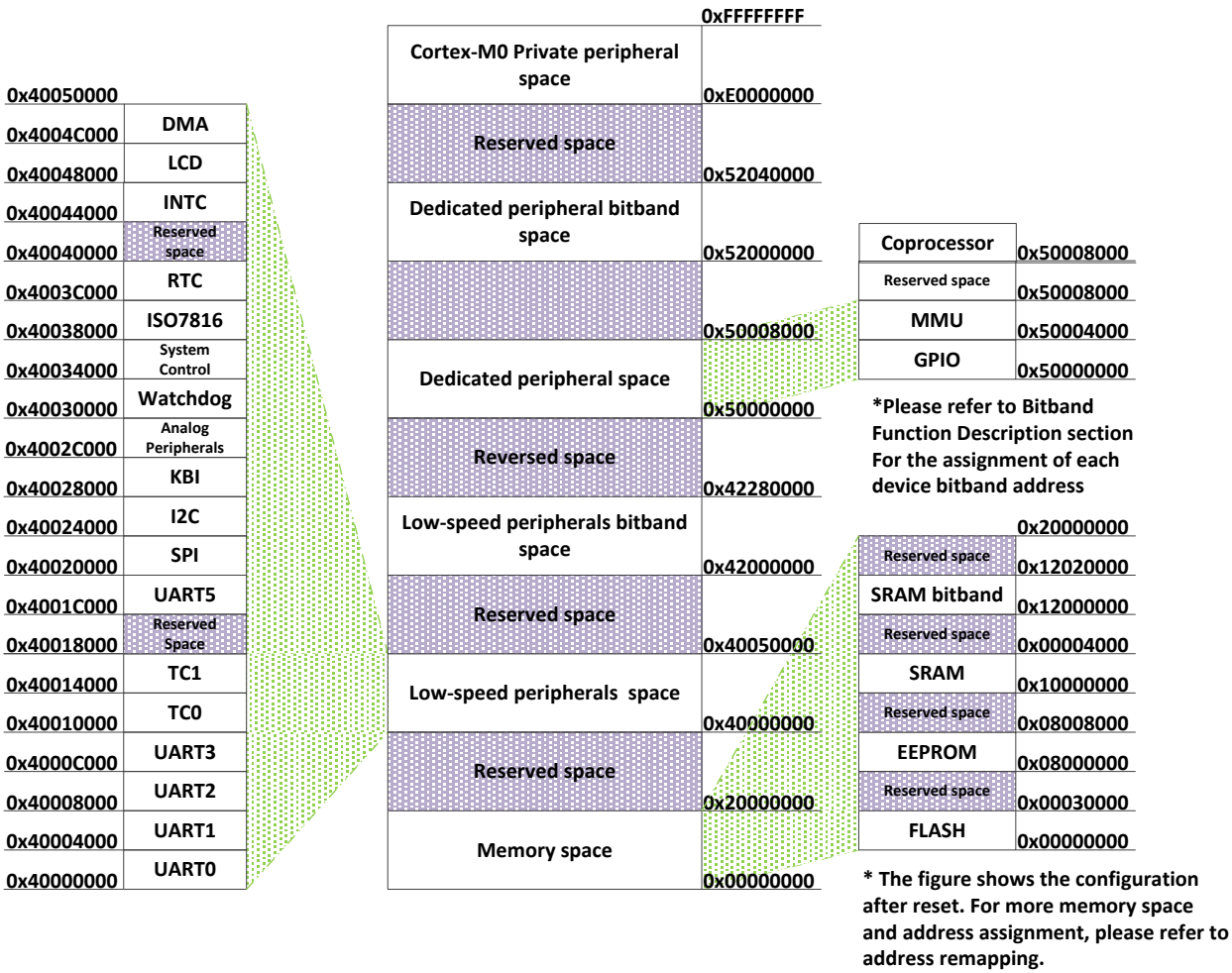
SoC supports three memory (including FLASH, EEPROM, SRAM) address space for address remapping.

The memor remapping is completed by configuring REMAP bit field of Register SYS_CTL in the system controller.

Address assignment of peripherals are not affected by mrmory remapping.

Table 4-1 Memory remapping configuration

Memory Device	REMAP	Mapping Address
FLASH	0	0x00000000~0x0001FFFF
	1	0x08000000~0x0801FFFF
	2	0x10000000~0x1001FFFF
	3	Reserved,Unavailable
EEPROM	0	0x08000000~0x08007FFF
	1	0x00000000~0x00007FFF
	2	0x08000000~0x08007FFF
	3	Reserved,Unavailable
SRAM	0	0x10000000~0x10003FFF



	1	0x10000000~0x10003FFF
	2	0x00000000~0x00003FFF
	3	Reserved,Unavailable

4.3.2 Bitband

The system supports bitband function of three address space:

SRAM Space

0x10000000~0x10003FFF mapped to 0x12000000~0x1201FFFF

0x00000000~0x00003FFF mapped to0x02000000~0x0201FFFF

0x40000000~0x4004FFFF mapped to 0x42000000~0x423FFFFF;

0x50000000~0x50007FFF mapped to 0x52000000~0x5203FFFF;

Access to bitband area is equivalent to the access to the specific bit of peripheral register.

The corresponding bitband address of the Y-th bit in the storage unit X. X is the address of the storage unit.

$$Z = (X \ \& \ 0xFC000000) + 0x02000000 + (Y << 2) + ((X << 5) \ \& \ 0x03FFFFFF)$$

4.3.3 SRAM

The maximum SRAM built in the SoC is 16KB.

- Operating frequency is the same as the processor;
- Supports 8-bit, 16-bit or 32-bit data random access and can be used code or data storage.
- Supports bitband operation.
- When Cache is enabled, Rn8215 only supports 14Kbytes maximumly. RN8211 and RN8212 is still 8Kbytes. In default, Cache is enabled.

4.3.4 EEPROM

The maximum EEPROM built in the SoC is 32KB.

- The number of erasing and writing is at least 1,000,000;
- Data can be stored for a minimum period of 20 years;
- Uses the page structure. Page size is 64 bytes, and 64 pages is one sector t. Fullly supports byte operations;
- Supports page erasing, sector erasing, bytes programming. The Specific operation needs to call library functions (nvm.a(IAR)/nvm.lib(KEIL)).
- **In low-power application, users need to call library function s to close or open EEPROM.**

EEPROM operation function interface provided by library functions(nvm.a(IAR)/nvm.lib(KEIL) follows:

uint8_t	eepromPageErase(uint32_t pg)
uint8_t	eepromSectorErase(uint32_t sec)
uint8_t	eepromProgram(uint32_t dst_addr, uint32_t src_addr, uint32_t len)
void	eepromStandby(void)
void	eepromWakeup(void)

For more details, please see “Instructions of RN821x_RN831x application note 003-library function”

4.3.5 FLASH

The maximum Flash built in the SoC is 192KB.

- The number of erasing and writing is at least 100,000;
- Data can be stored for a minimum period of 20 years;
- Uses the page structure. Page size is 128 bytes, and 32 pages is one sector;
- Supports page erasing, sector erasing, bytes programming. The Specific operation needs to call library functions

(nvm.a(IAR)/nvm.lib(KEIL)).

- **In low-power application, FLASH will close or open automatically.**

FLASH operation function interface provided by library functions(nvm.a(IAR)/nvm.lib(KEIL) follows:

uint8_t	flashPageErase(uint32_t pg)
uint8_t	flashSectorErase(uint32_t sec)
uint8_t	flashProgram(uint32_t dst_addr, uint32_t src_addr, uint32_t len)

For more details, please see "Instructions of RN821x_RN831x application note 003-library function"

4.4 Interrupt Assignment

SoC supports 32 interrupts, of which there are four open external interrupt, external interrupt 0/2/6/7 respectively.

For more information of interrupts, such as priority mask register, Nested Vectored Interrupt Controller (NVIC), etc. Please refer to ARM-M0 manual.

Table 4-2 Interrupt / exception vector table and configuration information

Abnormal Number	Interrupt Number	Vector Name	Interrupt Vector Address	Priority
-	-	MSP Initial Value	0x00	-
1	-	Reset	0x04	-3,Highest
2	-14	Non Maskable Interrupt	0x08	-2
3	-13	HARDFAULT Interrupt	0x0C	-1
4～10	-12～-6	Reserved	0x10～0x28	-
11	-5	System Call	0x2C	Configurable
12～13	-4～-3	Reserved	0x30～0x34	-
14	-2	PendSV	0x38	Configurable
15	-1	System Beat Counter	0x3C	Configurable
16	0	Reserved	0x40	Configurable
17	1	CMP1,CMP2 and LVD	0x44	Configurable
18	2	Main Power and Battery Power Switch	0x48	Configurable
19	3	RTC	0x4C	Configurable
20	4	Measure MMU	0x50	Configurable
21	5	Analog Peripherals	0x54	Configurable
22	6	UART0	0x58	Configurable
23	7	UART1	0x5C	Configurable
24	8	UART2	0x60	Configurable
25	9	UART3	0x64	Configurable
26	10	SPI	0x68	Configurable
27	11	I2C	0x6C	Configurable
28	12	7816_0	0x70	Configurable

29	13	7816_1	0x74	Configurable
30	14	TC0	0x78	Configurable
31	15	TC1	0x7C	Configurable
32	16	Reserved	0x80	Reserved
33	17	UART5	0x84	Configurable
34	18	Watchdog	0x88	Configurable
35	19	KBI	0x8C	Configurable
36	20	LCD	0x90	Configurable
37	21	Coprocessor	0x94	Configurable
38	22	DMA	0x98	Configurable
39	23	Reserved	0x9C	Reserved
40~47	24~32	External Interrupt 0~7	0xA0~0xBC	Configurable

4.5 DMA

Two-channel DMA controller, which is used to achieve data transmission without processor intervention between peripherals and memory ,is built in SoC.

Note: RN8211 and RN8213 don't support DMA function.

4.5.1 Overview

DMA has the following feature:

- Supports two independent channels;
- Supports 8-bit, 16-bit, 32-bit data transmission;
- Supports memory to memory, peripheral to memory, memory to peripheral transmission;
- Supports incremental or fixed-length transmission;
- The length of packet transmitted is up to 256;
- The length of frame transmitted is up to 256;
- Supports packet addresses wrap;
- Supports frame addresses wrap;
- Supports the transmission end and the error interrupt;
- Supports single and continuous transmission mode;
- Supports 32 peripheral DMA request;
- Support sent-length real time feedback.

4.5.2 DMA Channel Assignment

SoC supports 32 DMA channel applications, and allocates a fixed application channel number to application of each peripheral DMA.

When DMA is working, the DMA channel application need to be assigned by Register C0CTL or C1CTIL in the DMA controller.

Table 5-1 Interrupt / exception vector table and configuration information

Channel Number	TRGSEL Value	Explanation
0	0	Software Mode. Used to transfer DMA between memory
1	1	UART0 Transmission
2	2	UART0 Reception

3	3	UART1 Transmission
4	4	UART1 Reception
5	5	UART2 Transmission
6	6	UART2 Reception
7	7	UART3 Transmission
8	8	UART3 Reception
9	9	LCD Display
10	10	SPI Transmission
11	11	SPI Reception
12	12	I2C Transmission
13	13	I2C Reception
14	14	ISO7816_0 Transmission
15	15	ISO7816_0 Reception
16	16	ISO7816_1 Transmission
17	17	ISO7816_1 Reception
18	18	TC0
19	19	TC1
20	20	Reserved
21	21	Reserved
22	22	RTC
23	23	SAR
24	24	Reserved
25	25	EMU
26	26	Reserved
27	27	Reserved
28	28	UART5 Transmission
29	29	UART5 Reception
Others	Others	Reserved

4.6 Register Description

DMA Register Base Address

Module Name	Physical Address	Mapping Address
DMA	0x4004C000	0x4004C000

Register Offset Address

Register Name	Address Offset Value	Description
DMA_IE	0x0	Interrupt Enable
DMA_STA	0x4	Channel Status
DMA_C0CTL	0x10	Channel 0 Control
DMA_C0SRC	0x14	Channel 0 Source Address
DMA_C0DST	0x18	Channel 0 Destination Address
DMA_C0LEN	0x1C	Channel 0 Transmitted Length
DMA_C1CTL	0x20	Channel 1 Control
DMA_C1SRC	0x24	Channel 1 Source Address

DMA_C1DST	0x28	Channel 1 Destination Address
DMA_C1LEN	0x2C	Channel 1Transmitted Length

- Interrupt Enable Register DMA__IE(0x0)

Bit	Name	Description	R/W	Reset value
31:10	---	Reserved	R	0
9:8	C1EIE~C0EIE	Channel 1/0 Error Interrupt Enable: 0:Disable 1:Enable	R/W	0
7:6	---	Reserved	R	0
5:4	C1FIE~C0FIE	Channel 1/0 Frame Transfer End Interrupt Enable: 0:Disable 1:Enable	R/W	0
3:2	---	Reserved	R	0
1:0	C1PIE~C0PIE	Channel 1/0 Packet Transfer End Interrupt Enable: 0:Disable 1:Enable	R/W	0

- Channel Status Register DMA_STA(0x4)

Bit	Name	Description	R/W	Reset value
31:8	---	Reserved	R	0
7:6	C1ERR~C0ERR	Channel 1/0 Error Flag:(Write 1,Clear 0) 0:Transfer process without error 1:Transfer process with error	R/W	0
11:10	---	Reserved	R	0
9:8	C1FOK~C0FOK	Channel 1/0 Frame Transrer End Flag:(Write 1,Clear 0) 0:Transfer uncompleted 1:Transfer completed	R/W	0
7:6	---	Reserved	R	0
5:4	C1POK~C0POK	Channel 1/0 Packet Transfer End Flag: (Write 1,Clear 0) 0:Transfer uncompleted 1:Transfer completed	R/W	0
3:2	---	Reserved	R	0
1:0	C1BUSY~C0BUSY	Channel 1/0 Busy Status: 0: Idle 1: Busy	R	0

- Channel Control Register DMA_C0CTL and DMA_C1CTL(0x10, 0x20)

Bit	Name	Description	R/W	Reset value
31:24	FLEN	Frame Length, the length is (FLEN+1)	R/W	0
23:16	PLEN	Packet length, the length is (PLEN+1)	R/W	0
15	TERM	Stop 0:Normal stop 1:Immediately stop	R/W	0
14	---	Reserved	R	0
13	OSD	Single Transfer Ban: 0:Single Transfer 1:Continuous Transfer	R/W	0
12	TMODE	Trigger Mode: 0:A single DMA request corresponds to a single data transfer (UART)	R/W	0

		1:A single DMA request corresponds to a packet data transfer (LCD/MEN)		
11:7	TRGSEL	Trigger Chanel Selection. See "DMA Channel Assignment" section describes.	R/W	0
6:5	DMODE	Destination Address Mode: 00:Unchanged 01:Packet Wrap 10:Frame Wrap 11:Reserved(Equivalent to Frame Wrap)	R/W	0
4:3	SMODE	Source Address Mode: 00:Unchanged 01:Packet Wrap 10:Frame Wrap 11:Reserved(Equivalent to Frame Wrap)	R/W	0
2:1	SIZE	Transfer Size: 00:8 Bit 01:16 Bit 10:32 Bit 11:Reserved(Equivalent to 10,that is 32 bit)	R/W	0
0	EN	Channel Enable: 0:Disable 1:Enable	R/W	0

- Channel Source Address Register DMA_C0SRC and DMA_C1SRC(0x14,0x24)

Bit	Name	Description	R/W	Reset value
31:0	SRC	Source Address	R/W	0

- Channel Destination Address Register DMA_C0DST and DMA_C1DST(0x18,0x28)

Bit	Name	Description	R/W	Reset value
31:0	DST	Destination Address	R/W	0

- Channel Transmitted Length Register DMA_C0LEN and DMA_C1LEN(0x1C,0x2C)

Bit	Name	Description	R/W	Reset value
31:16	---	Reserved	R	0
15:8	FCNT	Frame Transmitted Length	R	0
7:0	PCNT	Packet Transmitted Length	R	0

5 Measurement

5.1 Main Features

- Active error is less than 0.1% over 5000:1 dynamic range;
- Supports the zero line (channel B) and fire wire (Channel A) dual-channel active power, reactive power, apparent power, effective value of current measured simultaneously;
- Supports the zero line (channel B) and fire wire (Channel A) dual-channel active energy, reactive energy, apparent energy measured simultaneously;
- Provides sampling channel gain and offset calibration;
- Provides power factor;

- **RN8211 only supports some features, see below register list.**

5.2 Register Description

BaseAddr is:0x50004000

Table 5-1 Measurement Section Register List

Address	Name	R/W	Effective Length	Reset Value	Function Description
Calibration Parameters and Measurement Control Register					
00H	EMUCON	R/W	3	000007h	Measurement Control Register, Write Protect
04H	EMUCON2	R/W	3	000000h	Measurement Control Register 2, Write Protect
08H	HFConst	R/W	2	1000h	Pulse Frequency Register ,Write Protect
0CH	PStart	R/W	2	0060h	Active Starting Power Setting, Write Protect
10H	Qstart	R/W	2	0120h	Reactive Starting Power Setting, Write Protect
14H	GPQA	R/W	2	0000h	Channel A Power Gain Calibration Register ,Write Protect
18H	GPQB	R/W	2	0000h	Channel B Power Gain Calibration Register ,Write Protect
1CH	PhsA	R/W	2	0000h	Channel A Phase Calibration Register, ENB 9bit, Calibration scale about 0.01 degrees, Write Protect
20H	PhsB	R/W	2	0000h	Channel B Phase Calibration Register, ENB 9bit, Calibration scale about 0.01 degrees, Write Protect
24H	QphsCal	R/W	2	0000h	Reactive Phase Compensation, Write Protect
28H	APOSA	R/W	2	0000h	Channel A Active Power Offset Calibration Register, Write Protect
2CH	APOSB	R/W	2	0000h	Channel B Active Power Offset Calibration Register, Write Protect
30H	RPOSA	R/W	2	0000h	Channel A Reactive Power Offset Calibration Register, Write Protect
34H	RPOSB	R/W	2	0000h	Channel b Reactive Power Offset Calibration Register, Write Protect
38H	IARMSOS	R/W	2	0000h	Current Channel A Effective Value Offset Compensation, Write Protect
3CH	IBRMSOS	R/W	2	0000h	Current Channel A Effective Value Offset Compensation, Write Protect
40H	URMSOS	R/W	2	0000h	Voltage Channel Effective Value Offset Compensation, Write Protect. Affecting Effective Value, Apparent Power, Apparent Energy.
44H	IAGain	R/W	2	0000h	Current Channel A Gain Setting, Write Protect; Affecting Effective Value ,POWER and Energy.
48H	IBGain	R/W	2	0000h	Current Channel A Gain Setting, Write Protect .Usage is the same as IAGain
4CH	Ugain	R/W	2	0000h	Voltage Channel Gain Setting, Write Protect; Usage is the same as IAGain. Affecting Effective Value, POWER and Energy.
50H	IADCOS	R/W	3	000000h	Current Channel A DC Offset Calibration, 24bit, Write Protect
54H	IBDCOS	R/W	3	000000h	Current Channel B DC Offset Calibration, 24bit, Write Protect

58H	UDCOS	R/W	3	000000h	Voltage Channel DC Offset Calibration, 24bit, Write Protect
5CH	UADD	R/W	3	000000h	Voltage Channel Offset Register, 24bit. It is used to write fixed value when measuring apparent energy. It Only affects apparent energy and does not affect active power, reactive power and effective value.
60H	USAG	R/W	2	0000h	Voltage Drop Threshold Setting, Write Protect; When USAG=0, this function is disabled; When USAG≠0,Drop detection starts. The detection results have interrupts reported. The number of half-cycles is determined by usag_cfg[7:0] in the measurement control register 2.
64H	IAPEAK	R/W	2	0000h	Current Channel A Peak Detection Threshold Setting, Write Protect
68H	IBPEAK	R/W	2	0000h	Current Channel B Peak Detection Threshold Setting, Write Protect
6CH	UPEAK	R/W	2	0000h	Voltage Peak Detection Threshold Setting, Write Protect
70H	D2FP	R/W	4	00000000h	Custom Power Register. When SADD=011, write the power value in this register. Through apparent channel, energy can be calculated by integrating the written power value.
Measurement Parameters and Status Register					
C0	PF2Cnt	R/W	2	0000h	Channel B Fast Active Pulse Counting, Write Protect
C4	QF2Cnt	R/W	2	0000h	Channel B Fast Reactive Pulse Counting, Write Protect
C8	SF2Cnt	R/W	2	0000h	Channel B Fast Apparent Pulse Counting, Write Protect
100	PFCnt	R/W	2	0000h	Channel A Fast Active Pulse Counting, Write Protect
104	QFCnt	R/W	2	0000h	Channel A Fast Reactive Pulse Counting, Write Protect
108	SFCnt	R/W	2	0000h	Channel A Fast Apparent Pulse Counting, Write Protect
10C	IARMS	R	3	000000h	Effective Value of Channel A current. Update rate is 13.67Hz. Settling time is about 300ms.
110	IBRMS	R	3	000000h	Effective Value of Channel B current. Update rate is 13.67Hz. Settling time is about 300ms.
114	URMS	R	3	000000h	Effective Value of Voltage. Update rate is 13.67Hz. Settling time is about 300ms.
118	Ufreq	R	2	0000h	Voltage Frequency
11C	PowerPA	R	4	00000000h	Active Power A. Update rate is 1.78Hz.
120	PowerPB	R	4	00000000h	Active Power B. Update rate is 1.78Hz.
124	PowerQA	R	4	00000000h	Reactive Power A. Update rate is 13.67Hz. Settling time is about 300ms.
128	PowerQB	R	4	00000000h	Reactive Power B. Update rate is 13.67Hz. Settling time is about 300ms.
12C	PowerSA	R	4	00000000h	Apparent Power A. Update rate is 13.67Hz. Settling time is about 300ms.
130	PowerSB	R	4	00000000h	Apparent Power B. Update rate is 13.67Hz. Settling time is about 300ms.

134	EnergyP	R	3	000000h	Active Energy. Cleared or not after reading. It is configurable. Default: Cleared after reading
138	EnergyP2	R	3	000000h	Channel B Active Energy. Cleared or not after reading. It is configurable. Default: Cleared after reading
13C	EnergyQ	R	3	000000h	Reactive Energy. Cleared or not after reading. It is configurable. Default: Cleared after reading
140	EnergyQ2	R	3	000000h	Channel B Reactive Energy. Cleared or not after reading. It is configurable. Default: Cleared after reading
144	EnergyS	R	3	000000h	Apparent Energy. Cleared or not after reading. It is configurable. Default: Cleared after reading
148	PFA	R	3	000000h	24bit. The high bit is sign bit. Channel A Power Factor.
14C	PFB	R	3	000000h	24bit. The high bit is sign bit. Channel B Power Factor.
150	ANGLEA	R	2	0000h	Calculation Method of Angle Between the voltage and Channel A:(ANGLEA/2^15)*360 Degree
154	ANGLEB	R	2	0000h	Calculation Method of Angle Between the voltage and Channel B:(ANGLEA/2^15)*360 Degree
158	EMUStatus	R	4	00FFEE78h	Measure Status and Checksum Register
15C	SPL_IA	R	3	000000h	Current Channel A Sample Value. Update rate is 7.2KHz.
160	SPL_IB	R	3	000000h	Current Channel B Sample Value. Update rate is 7.2KHz.
164	SPL_U	R	3	000000h	Voltage Channel Sample Value. Update rate is 7.2KHz.
168	PowerPA2	R	4	00000000h	Active Power A. Update rate is 13.67Hz. Settling time is about 300ms.
16C	PowerPB2	R	4	00000000h	Active Power B. Update rate is 13.67Hz. Settling time is about 300ms.
170	EnergyS2	R	3	000000h	Channel B Apparent Energy. Cleared or not after reading. It is configurable. Default: Cleared after reading
174	SPL_PA	R	3	000000h	Channel A Instantaneous Active Power. Update rate is 7.2KHz.
178	SPL_PB	R	3	000000h	Channel B Instantaneous Active Power. Update rate is 7.2KHz.
17C	SPL_QA	R	3	000000h	Channel A Instantaneous Reactive Power. Update rate is 7.2KHz.
180	SPL_QB	R	3	000000h	Channel B Instantaneous Reactive Power. Update rate is 7.2KHz.
184	TRNG	R	4	00000000h	32 Bit True Random Number Generation Register, Read-Only; bit11~bit0 is the TRNG0;bit31~bit12 is the Reserved bit; User can use the TRNG0.
188	EMUStatus2	R	4	00000000h	Measurement Status Register 2
Interrupt and DMA Register					
18C	IE	R/W	3	000000h	Interrupt Enable Register, Write Protect
190	IF	R/W	3	000000h	Interrupt Flag Register. Write 1 cleared

194	DMAEN	R/W	3	000000h	DMA Enable Register, as defined in the interrupt enable register. Write Protect
Status Register					
198	Rdata	R	4	--	Read data in the last time
19C	Wdata	R	4	--	Written data in the last time

RN8211 supports the following list of registers:

Do not operate the unsupported registers.

00H	**EMUCON---bit13/12/9/7/6/5/4/3/0**
08H	**HFConst**
0CH	**PStart**
14H	**GPQA**
1CH	**PhsA**
28H	**APOSA**
38H	**IARMSOS**
40H	**URMSOS**
100	**PFCnt**
10C	**IARMS**
114	**URMS**
118	**Ufreq**
11C	**PowerPA**
134	**EnergyP**
158	**EMUStatus---bit30/27/25:0**
18C	**IE---bit12/11/3/1/0**
190	**IF**
198	**Rdata**
19C	**Wdata**

- Measure Control Register EMUCON(0x00)

(**RN8211only supports bit13/12/9/7/6/5/4/3/0**)

Energy Measure Control Register (EMUCON) Addr:00H Default Value: 0007H		
Bit	Bit Name	Function Description
31:21	Reserved	Reserved
20	S2RUN	S2RUN=1,Enable apparent energy register 2 (EnergyS2) to accumulate; S2RUN=0,Disable apparent energy register 2 (EnergyS2) to accumulate. Default status is 1.
19	Q2RUN	Q2RUN=1,Enable reactive energy register 2 (EnergyQ2) to accumulate; Q2RUN=0,Disable reactive energy register 2 (EnergyQ2) to accumulate. Default status is 1.
18	P2RUN	P2RUN=1,Enable active energy register 2 (EnergyP2) to accumulate; P2RUN=0,Disable active energy register 2 (EnergyP2) to accumulate. Default status is 1.
17	CF3_CFG	=0:Original SF pin = SF1; =1:Original SF pin = SF2.
16	U_start	=0: When calculating apparent energy, voltage channel is involved in the calculation =1: When calculating apparent energy, voltage channel is not involved in

<table>
<tr><td></td><td></td><td>the calculation, only involved UADD.</td></tr>
<tr><td>15-14</td><td>QMOD[1:0]</td><td>Reactive Energy Accumulation Mode Selection:
<table>
<tr><td>QMOD1</td><td>QMOD0</td><td>Accumulate Power Qm</td></tr>
<tr><td>0</td><td>0</td><td>Qm=DataQ. Forward and reverse power are involved in the accumulation, and the REVQ symbol indicates a negative power.</td></tr>
<tr><td>0</td><td>1</td><td>Only foweard power is involved in the accumulation.</td></tr>
<tr><td>1</td><td>0</td><td>Qm=|DataQ|, Forward and reverse power are involved in the accumulation, and there are no negative power indicator.</td></tr>
<tr><td>1</td><td>1</td><td>Qm=DataQ(Reserved)</td></tr>
</table></td></tr>
<tr><td>13-12</td><td>PMOD[1:0]</td><td>Active Energy Accumulation Mode Selectio:
The Mode is same as the above.</td></tr>
<tr><td>11</td><td>ZXD1</td><td>The initial output of ZX is 0.According to ZXD1 and ZXD0 configuration, ZX outputs different waveforms:
ZXD1=0 indicates that the output of ZX changes only at the selected zero-crossing.
ZXD1=1 indicates that the output of ZX changes both at the positive and negative zero-crossing</td></tr>
<tr><td>10</td><td>ZXD0</td><td>ZXD0=0 indicates to choose the positive zero-crossing as zero-crossing detection signal.
ZXD0=1 indicates to choose the negative zero-crossing as zero-crossing detection signal.</td></tr>
<tr><td>9</td><td>Energy_clr</td><td>=0: all the energy registers are cleared after read.
=1: all the energy registers are not cleared after read.</td></tr>
<tr><td>8</td><td>HPFIBOFF</td><td>HPFIBOFF=0: enable IB-channel digital high-pass filter
HPFIBOFF=1: disable IB-channel digital high-pass filter</td></tr>
<tr><td>7</td><td>HPFIAOFF</td><td>HPFIAOFF=0: enable IA-channel digital high-pass filter
HPFIAOFF=1: disable IB-channel digital high-pass filter</td></tr>
<tr><td>6</td><td>HPFUOFF</td><td>HPFUOFF=0: enable U-channel digital high-pass filter
HPFUOFF=1: disable U-channel digital high-pass filter</td></tr>
<tr><td>5</td><td>CFSUEN</td><td>CFSUEN is the control bi of the PF/QF Pulse Output Acceleration Module
CFSUEN=1 enables pulse acceleration module and pulse output rate increases 2 ^ (CFSU [1:0] +1) times
CFSUEN=0 disables pulse acceleration module and the pulse outputs normally.</td></tr>
<tr><td>4,3</td><td>CFSU[1:0]</td><td>This bit is used in conjunction with CFSUEN. See CFSUEN description.</td></tr>
<tr><td>2</td><td>SRUN</td><td>SRUN=1, enable apparent energy register 1(EnergyS) accumulation;
SRUN=0, disable apparent energy register 1(EnergyS) accumulation.
Default status is 1.</td></tr>
<tr><td>1</td><td>QRUN</td><td>QRUN=1, enable reactive energy register 1(EnergyS) accumulation;
QRUN=0, disable reactive energy register 1(EnergyS) accumulation.</td></tr>
</table>

		Default status is 1.
0	PRUN	PRUN=1, enable active energy register 1(EnergyP) accumulation; PRUN=0, disable active energy register 1(EnergyP) accumulation. Default status is 1.

- Measure Control Register 2 EMUCON2(0x04)

Energy Measure Control Register 2(EMUCON2) Addr:04H Default Value: 0000H		
Bit	Bit Name	Function Description
31:24	Reserved	Reserved
23:21	SADD[2:0]	Channel A Apparent Energy Channel Power Input Selection SADD[2:0]: = 000 S=S1 or S2, determined by CHNSEL; = 001 S=S2; = 010 S=Q2; = 011 S=Custom Power; = Other Reserved.
20:18	QADD[2:0]	Channel A Reactive Energy Channel Power Input Selection QADD[2:0]: =000 Q=Q1 or Q2, determined by CHNSEL; =001 Q=P1; =010 Q=P2; =Other Reserved
17:15	PADD[2:0]	Channel A Active Energy Channel Power Input Selection PADD[2:0]: = 000 P=P1 or P2, determined by CHNSEL; =001 P=P1 =010 P=P2 =Other Reserved
14:13	CF2_CFG[1:0]	Configure Pin P51/QF Energy Pulse Output Selection =00 Original QF=QF1 =01 Original QF =QF2 =10 Original QF =SF1 =11 Original QF =SF2
12:11	CF1_CFG[1:0]	Configure Pin P50/PF Energy Pulse Output Selection =00 Original PF =PF1 =01 Original PF =PF2 =10 Original PF =QF1 =11 Original PF =QF2 Note: PF1/QF1/SF1 are correspond to energy register EnergyP/ EnergyQ /EnergyS; PF2/QF2/SF2 are correspond to energy register EnergyP2/EnergyQ2/EnergyS2.
10:3	usag_cfg[7:0]	Usag_cfg[7:0] is used to configure the number of half-cycles of the voltage drop detection.
2	u_dc_en	U_dc_en,ib_dc_en,ia_dc_en are written 1 to enable Channel DC Offset Automatic Calibration. After calibration they are cleared automatically. The calibration value is written in DC Offset Calibration Register (0x50~0x58H) automatically. The calibration time is about 1.2S.
1	ib_dc_en	
0	ia_dc_en	

- Calibration Register(0x08H~0x70H)

Address Offset	Name	Description
08H	HFConst	HFConst is a 16-bit unsigned, compared with 2 times absolute value of fast pulse counting registers. If the

		value is greater than or equal to HFConst value, then there will be a corresponding PF / QF pulse output.
0CH	PStart	Start threshold can be configured by PStart and QStart register. They are 16-bit unsigned, compared with the obsolute value of 24 high bit of PowerP and PowerQ which are 32 bit signed for starting judgment.
10H	Qstart	
14H	GPQA	GPQA is used for active / reactive power and energy gain calibration of channel A. GPQB is used for active / reactive power and energy gain calibration of channel B. Two's complement format, the highest bit is the sign bit. Correction formula: P1=P0(1+GPQS) Q1=Q0(1+GPQS) In the formula, GPQS is normalized value for the gain calibration registers.
18H	GPQB	
1CH	PhsA	Signed twos' complement, Bit0 ~ bit8 effective, in which bit8 is the sign bit. Distinguish degrees is 0.00976.
20H	PhsB	
24H	QphsCal	Reactive phase compensation register is used as phase compensation of the U-channel 90 °phase shift filters in reactive calculation. Reactive phase compensation register uses 16 bit two's complement format and the highest bit is the sign bit. Calibration formula:Q2 = Q1-QPhs*P1 In the formula, P1 is active power, Q1 is reactive power before calibration and Q2 is reactive power after calibration.
28H	APOSA	Power OFFSET calibration is fit for precision correction of small signal. Two's complement format, 16 significant digits, the highest bit is the sign bit. APOSA register is Offset value of channel A active power. APOSB register is Offset value of channel B active power. RPOSA register is Offset value of channel A reactive power. RPOSB register is Offset value of channel B reactive power.
2CH	APOSB	
30H	RPOSA	
34H	RPOSB	
38H	IARMSOS	Effective value Offset Calibration Register is used for precision calibration of small-signal current effective value. 16 significant digits, two's complement format, the highest bit is the sign bit.
3CH	IBRMSOS	
40H	URMSOS	
44H	IAGain	Triple-channel ADC gain calibration, 16-bit two's complement format
48H	IBGain	
4CH	Ugain	
50H	IADCOS	Current Channel A DC Offset Calibration, 24bit, Write Protec
54H	IBDCOS	Current Channel B DC Offset Calibration, 24bit, Write Protec
58H	UDCOS	Voltage Channel DC Offset Calibration, 24bit, Write Protect The minimum scale of the DC offset calibration register

		is 1.414 times the effective value register.
5CH	UADD	Voltage Channel Offset Register, 24bit Used to write fixed value when calculating apparent energy. It only has effect on apparent energy, and has no effect on active energy, reactive energy and the effective value. The minimum scale of UADD is 1.414 times the effective value register.
60H	USAG	Voltage Drop Threshold Setting, Write Protect When USAG=0, this function is disabled; When USAG≠0,Drop detection starts. The detection results have interrupts reported. The number of half-cycles is determined by usag_cfg[7:0] in the measurement control register 2.
64H	IAPEAK	Current Channel A Peak Detection Threshold Setting, Write Protect
68H	IBPEAK	Current Channel B Peak Detection Threshold Setting, Write Protect
6CH	UPEAK	Voltage Peak Detection Threshold Setting, Write Protect Peak detection threshold value is 16-bit, compared with the 16 high bit of the 24 bit waveform sample value.
70H	D2FP	Custom Power Register. When SADD=011, write the power value in this register. Through apparent channel, energy can be calculated by integrating the written power value. This register is 32-bit, the minimum scale is the same as power register such as active register and reactive register.

- Measure Status Register EMUStatus(0x158H)

Note: RN8211 only supports bit30/27/25:0, the other bits are meaningless.

This register includes Measure Status Register and Checksum Register

EMU STATUS Register (EMUStatus) Address:0x158 h Read-only register		
Bit	**Bit Name**	**Function Description**
31	NoSld	When apparent power is less than starting power, NoSld is set as 1; when apparent power more than/equal to starting power, NoSld is cleared.
30	WREN	Write Enable Flag: =1 allowed to write the Write Protect register =0 not allowed to write the Write Protect register. Read only
29	CHNSEL	Current Channel Selection Status Flag. Read only =1 indicates that the current channel used to calculate the active / reactive power is channel B. =0 indicates that the current channel used to calculate the active / reactive power is channel A. In default, this bit is 0.
28	Noqld	When reactive power is less than starting power, Noqd is set as 1; when reactive power more than/equal to starting power, Noqld is cleared.

27	Nopld	When active power is less than starting power, Nopld is set as 1; when active power more than/equal to starting power, Nopld is cleared.
26	REVQ	Reverse Reactive Power Indicator Signal. When detecting the negative reactive power, the signal is 1. When detecting the positive reactive power again, the signal is 0.
25	REVP	Reverse Active Power Indicator Signal. When detecting the negative reactive power, the signal is 1. When detecting the positive reactive power again, the signal is 0.
24	ChksumBusy	Calibration Data Checksum Calculation Status Register. ChksumBusy =0 indicates that Calibration Data Checksum Calculation has completed. Checksum is available. ChksumBusy =1 indicates that Calibration Data Checksum Calculation has not completed. Checksum is not available.
23:0	Chksum	Checksum Output

EMUStatus [23:0] store the 24 bit checksum of the Calibration Parameter Configuration Register. CPU can monitor is register to detect whether the calibration data is disordered or not.

The checksum algorithm is to negate the cumulative result of three bytes. For double-byte register, cumulate after extending it as three-byte. The extended byte is 00H.

According to the default value to calculate the checksum, the result is 0xFFEE78.

In the following three cases, checksum should be re-calculated: system reset, write operation occurs in one of 00H~6CH registers, read operation occurs in EMUStatus register. A checksum calculation requires 32 CPU clock.

- Measure Status Register 2 EMUStatus2(0x188H)

EMU STATUS Register (EMUStatus) Address:0x188h Read-only register		
Bit	**Bit Name**	**Function Description**
31:14	Reserved	Reserved
13	Nos2ld	When apparent power 2 is less than starting power, Nos2ld is set as 1; when apparent power 2 more than/equal to starting power, Nos2ld is cleared. Read only
12	Noq2ld	When reactive power 2 is less than starting power, Noq2ld is set as 1; when reactive power 2 more than/equal to starting power, Noq2ld is cleared. Read only
11	Nop2ld	When active power 2 is less than starting power, Nop2ld is set as 1; when active power 2 more than/equal to starting power, Nop2ld is cleared. Read only
10	Revq2	Reactive Power 2 Reverse Indicator Signal. When detecting the negative reactive power, the signal is 1. When detecting the positive reactive power again, the signal is 0. Read only
9	Revp2	Active Power 2 Reverse Indicator Signal. When detecting the negative active power, the signal is 1. When detecting the positive active power again, the signal is 0. Read only
8	Vref_flag	VREF Flag, =1: VREF normal; =0: VREF lower than drop threshold. Read only
7	Ldo_flag	Measurement LDO Flag, =1: Measurement LDO normal; =0:Measurement LDO lower than drop threshold. Read only

6	NoSld	When apparent power is less than starting power, NoSld is set as 1; when apparent power more than/equal to starting power, NoSld is cleared. Read only
5	WREN	Write Enable Flag: =1 allowed to write the Write Protect register =0 not allowed to write the Write Protect register. Read only
4	CHNSEL	Current Channel Selection Status Flag. Read only =1 indicates that the current channel used to calculate the active / reactive power is channel B. =0 indicates that the current channel used to calculate the active / reactive power is channel A. In default, this bit is 0.
3	Noqld	When reactive power is less than starting power, Noqd is set as 1; when reactive power more than/equal to starting power, Noqld is cleared.
2	Nopld	When active power is less than starting power, Nopld is set as 1; when active power more than/equal to starting power, Nopld is cleared.
1	REVQ	Reverse Reactive Power Indicator Signal. When detecting the negative reactive power, the signal is 1. When detecting the positive reactive power again, the signal is 0.
0	REVP	Reverse Active Power Indicator Signal. When detecting the negative reactive power, the signal is 1. When detecting the positive reactive power again, the signal is 0.

- Interrupt Configuration and Enable Register IE(0x18CH)

When interrupt enable bit is set as 1 and interrupt occurs, IRQ_N pin outputs low. Before configuring Write Protect Register, write enable should be enable.

Note:RN8211 only supports bit12/11/3/1/0.

Interrupt Enable Register (IE) Address: 0x18CH Default value: 0x000000H Writable and readable		
Bit	**Bit Name**	**Function Description**
Others	**Reserved**	**Reserved**
23	I2ZXIE	I2ZXIE=0: Disable channel 2 current zero-crossing interrupt; I2ZXIE=1: Enable channel 2 current zero-crossing interrupt.
22	I1ZXIE	I1ZXIE=0: Disable channel 1 current zero-crossing interrupt; I1ZXIE=1: Enable channel 1 current zero-crossing interrupt.
21	Reserved	Reserved
20	S2EOIE	S2EOIE=0: Disable apparent energy register 2 overflow interrupt; S2EOIE=1: Enable apparent energy register 2 overflow interrupt.
19	Q2EOIE	Q2EOIE=0: Disable reactive energy register 2 overflow interrupt; Q2EOIE=1: Enable reactive energy register 2 overflow interrupt.
18	P2EOIE	P2EOIE=0: Disable active energy register 2 overflow interrupt; P2EOIE=1: Enable active energy register 2 overflow interrupt.
14	SF2IE	SF2IE=0: Disable SF2 interrupt; SF2IE=1 : Enable SF2 interrupt.
16	QF2IE	QF2IE=0: Disable QF2 interrupt; QF2IE=1 : Enable QF2 interrupt.

15	PF2IE	PF2IE=0: Disable PF2 interrupt;PF2IE=1 : Enable PF2 interrupt.
14	SFIE	SFIE=0: Disable SF interrupt; SFIE=1 : Enable SF interrupt.
13	SEOIE	SEOIE=0: Disable apparent energy register overflow interrupt; SEOIE=1: Enable apparent energy register overflow interrupt;
12	VREFIE	Measurement Reference VREF Drop Interrupt Enable, =1:Enable, =0:Disable
11	LDOIE	Measurement LDO33 Drop Interrupt Enable, =1:Enable, =0:Disable
10	SPLIE	ADC Sampling Interrupt Enable, =1:Enable, =0:Disable
9	USAGIE	U Channel Drop Interrupt Enable, =1:Enable, =0:Disable
8	UpeakIE	U Channel Overload Interrupt Enable, =1:Enable, =0:Disable
7	IApeakIE	IA Channel Overload Interrupt Enable, =1:Enable, =0:Disable
6	IBpeakIE	IB Channel Overload Interrupt Enable, =1:Enable, =0:Disable
5	ZXIE	ZXIE=0: Disable zero-crossing interrupt; ZXIE=1: Disable zero-crossing interrupt
4	QEOIE	QEOIE=0: Disable reactive energy register overflow interrupt; QEOIE=1: Enable reactive energy register overflow interrupt.
3	PEOIE	PEOIE=0: Disable active energy register overflow interrupt; PEOIE=1: Enable active energy register overflow interrupt.
2	QFIE	QFIE=0: Disable QF interrupt; QFIE=1: Enable QF interrupt.
1	PFIE	PFIE=0: Disable PF interrupt; PFIE=1: Enable PF interrupt.
0	DUPDIE	DUPDIE=0: Disable data update interrupt; DUPDIE=1: Enable data update interrupt. The update frequency of data register: PowerPA/PowerPB,PowerQ,IARMS/IBRMS,URMS is 13.67HZ. When the above data updates, IRQ_N pin outputs low.

- Interrupt Status Register IF(0x190H)

Note: RN8211 only supports bit12/11/3/1/0.

Interrupt Flag Register (IF) Address: 0x190H R/W		
Bit	**Bit Name**	**Function Description**
Others	Reserved	Reserved
23	I2ZXIF	I2ZXIF=0: Current Channel 2 Zero-crossing interrupt did not occur; I2ZXIF=0: Current Channel 2 Zero-crossing interrupt occurred.
22	I1ZXIF	I1ZXIF=0: Current Channel 1 Zero-crossing interrupt did not occur; I1ZXIF=1: Current Channel 1 Zero-crossing interrupt occurred.
21	Reserved	Reserved
20	S2EOIF	S2EOIF=0: Apparent energy register 2 overflow event did not occur; S2EOIF=1: Apparent energy register 2 overflow event occurred.
19	Q2EOIF	Q2EOIF=0: Reactive energy register 2 overflow event did not occur; Q2EOIF=1: Reactive energy register 2 overflow event occurred.
18	P2EOIF	P2EOIF=0: Active energy register 2 overflow event did not occur; P2EOIF=1: Active energy register 2 overflow event occurred.
17	SF2IF	SF2IF =0: SF2 pulse output event did not occur; SF2IF =1: SF2 pulse output event occurred.
16	QF2IF	QF2IF =0: QF2 pulse output event did not occur; QF2IF =1: QF2 pulse output event occurred.

15	PF2IF	SF2IF =0: PF2 pulse output event did not occur; SF2IF =1: PF2 pulse output event occurred.
14	SFIF	SFIF =0: SF pulse output event did not occur; SFIF =1: SF pulse output event occurred.
13	SEOIF	SEOIF=0: Apparent energy register overflow event did not occur; SEOIF=1: Apparent energy register overflow event occurred.
12	VREFIF	VREF Drop; =1: The event occurred; =0: The event did not occur.
11	LDOIF	LDO Drop; =1: The event occurred; =0: The event did not occur.
10	SPLIF	ADC Sampling Interrupt; =1: The event occurred; =0: The event did not occur.
9	USAGIF	U Channel Drop Interrupt; =1: The event occurred; =0: The event did not occur.
8	UpeakIF	U Channel Overload Interrupt; =1: The event occurred; =0: The event did not occur.
7	IApeakIF	IA Channel Overload Interrupt; =1: The event occurred; =0: The event did not occur.
6	IBpeakIF	IB Channel Overload Interrupt; =1: The event occurred; =0: The event did not occur.
5	ZXIF	ZXIF =0: Zero-crossing event did not occur; ZXIF =1: Zero-crossing event occurred
4	QEOIF	QEOIF=0: Reactive energy register overflow event did not occur. QEOIF=1: Reactive energy register overflow event occurred.
3	PEOIF	PEOIF=0: Active energy register overflow event did not occur. PEOIF=1: Active energy register overflow event occurred.
2	QFIF	QFIF =0: QF pulse output event did not occur; QFIF =1: QF pulse output event occurred.
1	PFIF	PFIF =0: PF pulse output event did not occur; PFIF =1: PF pulse output event occurred.
0	DUPDIF	DUPDIF=0: Data update event did not occur; DUPDIF=1: Data update event occurred.

When an interrupt event occurs, the hardware will set the corresponding interrupt flag as 1.

The generation of IF interrupt flag is uncontrolled by interrupt enable register IE, and it is only decided by whether interrupt event occurs or not.

- Special Command

Command Name	**Command Register**	**Data**	**Description**
Write Enable Command	1A8	0xE5	Enable Measure Module Write Operation
Write Protect Command	1A8	0xDC	Disable Measure Module Write Operation
Current Channel A Select	1A8	0x5A	Current Channel A Setting Command, specifies the current used to calculate active power / reactive power of the current channel is Channel A; has no effect on the

Command			effective value and power registers. After the write enables, the system can accept the command; CHNSEL register in the Measure Status Register reflects the results of the command RN8211 don't support this command.
Current Channel B Select Command	1A8	0xA5	Current Channel B Setting Command, specifies the current used to calculate active power / reactive power of the current channel is Channel B; has no effect on the effective value and power registers. After the write enables, the system can accept the command; CHNSEL register in the Measure Status Register reflects the results of the command RN8211 don't support this command.

Scope of write protection

0x00h-0x6Ch Calibration Parameter Configure Register, Fast Pulse Register, Interrupt Enable Register can be written after using special command to enable to write. Specific command format is in the above table.

6 RTC

6.1 Overview

BaseAddr is 0x4003C000;

RTC module provides real-time clock, oscillator temperature compensated, calendar, alarm, clock pulse output, etc.

Real-time clock tracks time through swparate hour, minute, second registers. Calendar includes year, month, day and week registers with leap year and leap moth automatically calibrated. Clock pulse output has a variety of selectable frequency for clock calibration. Alarm is also provided.

Integrates a temperature sensor and provides a digital temperature measurement results.

6.2 Features

●Provides accurate temperature value, and temperature measurement accuracy is ± 1 ℃ in the range of -25 ℃ ~ 70 ℃.

●Achieves initial temperature calibration of RTC at room temperature.

●Automatically completes temperature compensation calibration of RTC without CPU involvement.

●Low Power Design

●High stability oscillator

●RTC is not closed in different modes, and still works in low power.

●Provides clock and calendar function: the output register, including seconds, minutes, hours, date, month, year and week, etc.

●Provides automatic leap year leap month adjustment function, and the time range is 100 years (00-99)

●An alarm interrupts, two timer periodic interrupts, five time interrupts (second, minute, hour, month, day)

●Can output un-calibrated frequency: 4Hz,8Hz,16Hz,32768Hz

●Can output calibrated frequency: 1Hz,1/20Hz

6.3 Register Description

Base Address of RTC

Module Name	Physical Address	Mapping Address
RTC	BaseAddr is:0x4003C000	Base1

Register Offset Address of RTC

Register Name	Address Offset Value	Description
RTC Register Group		
RTC_CTL	Offset+0x00	RTC Control Register
RTC_SC	Offset+0x04	Second Register, Write Protect
RTC_MN	Offset+0x08	Minute Register, Write Protect
RTC_HR	Offset+0x0C	Hour Register, Write Protect
RTC_DT	Offset+0x10	Day Register, Write Protect
RTC_MO	Offset+0x14	Month Register, Write Protect
RTC_YR	Offset+0x18	Year Register, Write Protect
RTC_DW	Offset+0x1C	Week Register, Write Protect
RTC_CNT1	Offset+0x20	Counter 1 Register
RTC_CNT2	Offset+0x24	Counter 2 Register
RTC_SCA	Offset+0x28	Second Alarm Register
RTC_MNA	Offset+0x2C	Minute Alarm Register
RTC_HRA	Offset+0x30	Hour Alarm Register
RTC_IE	Offset+0x34	RTC Interrupt Enable Register
RTC_IF	Offset+0x38	RTC Status Register
RTC_TEMP	Offset+0x3C	Current Temp Register, Readable and Writable, Write Protect
RTC_DMAEN	Offset+0xC0	DMA Control Register

- RTC Control Register RTC_CTL(0x00)

Bit	Name	Description	R/W	Reset value
31:11	---	Reversed	R	0
10	Cal_busy	RTC Calibration Busy. When Cal_busy=1, RTC is ongoing calibration; when Cal_busy=0, RTC has completed calibration.	R	0
9	Wr_busy	RTC Register Write Operation Busy. When Wr_busy=1,RTC register can not be written; only when Wr_busy=0, RTC register can be written. **Notice: When Wr_busy=1,don't close the APB clock of RTC; Note this matter when enter in sleep or deepsleep through WFI command.**	R	0
8	WRTC	RT Register Group Write Enable: 0:disable RTC register write operation; 1:enable RTC register write operation Notice: This bit is effective to 00~1C/3C of the RTC register group, and also effective to RTC_CTL[7:0].	R/W	0

		When writes the time register, the Second Register is written in the last. After the Second register written, time starts cumulation from the write time.		
7:6	TSE	Temperature Sensor Enable Bit 00: Disable automatic temperature compensation 01: Enable automatic temperature compensation. Periodic temperature compensation accordance with the TCP settings. 10: Enable user temperature compensation mode 0. The temperature register can be changed and the temperature value can be written by the user. Once the user writes the temperature register, the temperature compensation starts. 11: Enable user temperature compensation mode 1. The temperature register can not be changed. Once the temperature register is written, the temperature compensation starts. Temperature value can be measured by SOC. NOTICE: this register only works on power-on reset.	R/W	00
5:3	TCP	Temperature Compensation Cycle: 000:2S 001:10S Default 010:20S 011:30S 100:1M 101:2M 110:5M 111:10M	R/W	001
02:00	FOUT	000:Output Disable 001:1Hz Outputs 010:1/20Hz Outputs 011:32768Hz Outputs 100:16Hz Outputs 101:8Hz Outputs 110:4Hz Outputs 111:Output Disable NOTICE: this register only works on power-on reset.	R/W	000

- Second Register RTC_SC(0x04)

Address:0x4003C000+ 0x04

Bit	Name	Description	R/W	Reset value
31:07	---	Reversed	R	0
06:00	SC	Store the second value of the clock BCD Format, **SC[6:4]** is the tens of the second value, **SC[3:0]** is the units of the second value. The second value ranges from 0~59.	R/W	-

- Minute alarm register RTC_MNA(0x2C)

Bit	Name	Descriptions	R/W	Reset Value
31:07	---	Reserved	R	0
06:00	MNA	Minute Alarm Value	R/W	0

		BCD Format, MNA[6:4] are the tenth of minute value, MNA[3:0] are the bits of minute value, The Rang of Minute Value is 0~59		

- Hour alarm register RTC_HRA(0x30)

Bit	Name	Descriptions	R/W	Reset Value
31:06	---	Reserved	R	0
05:00	HRA	Hour Alarm Value BCD Format, HRA[5:4] are the tenth of hour value, HRA[3:0] are the bits of hour value, The Rang of Hour Value is0~23.	R/W	0

- RTC IER RTC_IE(0x34)

Bit	Name	Descriptions	R/W	Reset Value
31:09	---	Reserved	R	0
08	IECLKEN	RTC interrupt generate clock enable; When anyone of the RTC [IE 8-0] is high, the interrupt module clock would open; When anyone of the RTC [IE 8-0] is low, the interrupt module clock would close;	R/W	0
7	MOIE	Month Interrupt Enable 0 : Disable 1 : Enable	R/W	0
6	DTIE	Date Interrupt Enable 0 : Disable 1 : Enable	R/W	0
5	HRIE	Hour Interrupt Enable 0 : Disable 1 : Enable	R/W	0
4	MNIE	Minute Interrupt Enable 0 : Disable 1 : Enable	R/W	0
3	SCIE	Second Interrupt Enable 0 : Disable 1 : Enable	R/W	0
2	RTCCNT2IE	RTC Timer2 Interrupt Enable 0 : Disable 1 : Enable	R/W	0
1	RTCCNT1IE	RTC Timer1 Interrupt Enable 0 : Disable 1 : Enable	R/W	0
0	ALMIE	Alarm Event Interrupt Enable 0 : Disable 1 : Enable	R/W	0

- RTC Interrupt Flag Register RTC_IF(0x38)

Bit	Name	Descriptions	R/W	Reset Value
31:12	---	Reserved	R	0
7	MOF	Month Interrupt Flag 0 : Month Counter not plus 1 1 : Month Counter plus 1 Note: Write 1 Cleared	R/W	0
6	DTF	Date Interrupt Flag 0 : Date Counter not plus 1 1 : Date Counter plus 1 Note: Write 1 Cleared	R/W	0
5	HRF	Hour Interrupt Flag 0 : Hour Counter not plus 1 1 : Hour Counter plus 1 Note: Write 1 Cleared	R/W	0
4	MNF	Minute Interrupt Flag 0 : Minute Counter not plus 1 1 : Minute Counter plus 1 Note: Write 1 Cleared	R/W	0
3	SCF	Second Interrupt Flag 0 : Second Counter not plus 1 1 : Second Counter plus 1 Note: Write 1 Cleared	R/W	0
2	RTCCNT2F	RTC Timer2 Interrupt Flag 0 : Timer1 Interrupt Unhappen 1 : Timer1 Interrupt Happen Note: Write 1 Cleared	R/W	0
1	RTCCNT1F	RTC Timer1 Interrupt Flag 0 : Timer1 Interrupt Unhappen 1 : Timer1 Interrupt Happen Note: Write 1 Cleared	R/W	0
0	ALMF	Alarm Event Flag, alarm event that matches with real-time clock occurs 0 : Alarm Event Unhappened 1 : Alarm Event Happened Note: Write 1 Cleared	R/W	0

- Current temperature register RTC_TEMP(0x3C)

Bit	Name	Descriptions	R/W	Reset Value
31:10	---	Reserved	R	0
09:00	TEMP	The Present Temperature Value. Bit 9 is Sign Bit; Bit 8~2 are Integer Bits; Bit 1~0 are Decimal Place. // Temp[9] Temp[8:2] Temp[1] Temp[0]	R/W	-

		// Symbol -128℃~127℃ 0.5℃ 0.25℃ Range:-128℃~+127.75℃ TSE=00: Disable temperature compensation automatic .This register is invalid, read the value is meaningless . TSE=01:Set cycles temperature compensated automatically according to TCP. This register shows the temperature of the measurement cycle. TSE=10:Open users temperature compensation mode 0,temperature register can change, fill in the temperature value by users, every time the users write a temperature register to start a temperature compensation operation; TSE=11:Open users temperature compensation mode 1,temperature register can not change, every time the users write a temperature register to start a temperature compensation operation, The values of temperature register were measured by the SOC.		

- RTC DMA Enable Registers RTC_DMAEN(0xC0)

Bit	Name	Descriptions	R/W	Reset Value
31:08	---	Reserved	R	0
7	MO_DMAEN	Month Interrupt Start DMA Transfer Enable 0 : Disable 1 : Enable	R/W	0
6	DT_DMAEN	Date Interrupt Start DMA Transfer Enable 0 : Disable 1 : Enable	R/W	0
5	HR_DMAEN	Hour Interrupt Start DMA Transfer Enable 0 : Disable 1 : Enable	R/W	0
4	MN_DMAEN	Minute Interrupt Start DMA Transfer Enable 0 : Disable 1 : Enable	R/W	0
3	SC_DMAEN	Second Interrupt Start DMA Transfer Enable 0 : Disable 1 : Enable	R/W	0
2	RTCCNT2_DMAEN	RTC Timer2 Interrupt Start DMA Transfer Enable 0 :Disable 1 : Enable	R/W	0
1	RTCCNT1_DMAEN	RTC Timer1 Interrupt Start DMA Transfer Enable 0 : Disable 1 : Enable	R/W	0
0	ALM_DMAEN	Alarm Event Interrupt Start DMA Transfer Enable 0 : Disable	R/W	0

		1 : Enable		

RTC automatic temperature compensation need to define the following registers, These registers values will obtain in the production aspects of the users.

1. The initial frequency offest registers RTC_DOTA0:correct the initial frequency offest of crystal;(Each ammeter need to get the library functions which is the Renerge provided that can complete operation to this register)
2. Conic vertex temperature register RTC_XT0(Obtain the batch parameters of crystal, configure option bytes, write through the programming interface)
3. Crystal oscillator temperature coefficient register RTC_ALPHA(Obtain the batch parameters of crystal, configure option bytes, write through the programming interface)

7 WDT

SoC built-in hardware watchdog, for abnormal detection program.

7.1 Overview

The watchdog has the following characteristics:

◎ Overflow time can be set:16ms,32ms,128ms,512ms,1s,2s,4s,8s;

◎ Dog window period can be set;

Generated watchdog reset when any of the following conditions:

◎ The watchdog timer counter overflow;

◎ The outside of the 0xBB data write into WDT_EN;

◎ Writing the data in WDT_EN during the dog windows closed;

◎ Writing the data in WDT_EN by bitband space;

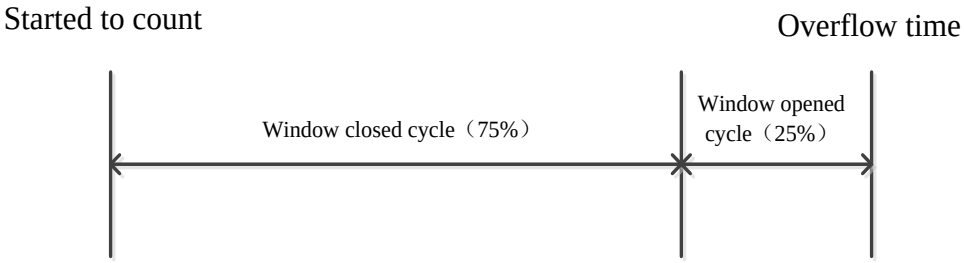
7.2 Configuration of Watchdog Timer

RN821X's WDT is hardware watchdog, cannot be configured directly by registers, need by setting the option byte way to configure it. Configuration of watch dog have interval interrupt, window opened cycle, Overflow Time, CPU sleep setting, CPU debug setting.etc.

Name	Descriptions	Factory default values
Interval interrupt	0:Disable(Disable interval interruption) 1:Enable(When reach the 75% of overflow events, generate interval interruption)	0
Window opened cycle	0:25% 1:50% 2:75% 3:100% Write 0xBB in WDTE register during the window opened, the watchdog cleared and re-count; Write 0xBB in WDTE register during the window closed, would generate internal reset signal .	3
Overflow Time	0:16ms	4

	1:32ms 2:128ms 3:512ms 4:1s 5:2s 6:4s 7:8s	
CPU Sleep Settings	0:Disable(When the CPU is in sleep or deepsleep not open WDT) 1:Enable(When the CPU is in sleep or deepsleep open WDT)	0
CPU Debug Settings	0:Disable(When the CPU is in debug status is not open WDT) 1:Enable(When the CPU is in debug status is open WDT) Note: CPU is in the debug state refers to users would stop Cortex M0 through debugging interface(PC pointer stops counting).If the chip is in the development process ,enabling this setting is not recommended. For if this setting is enabled, WDT still accounting number when the chip is in debug state, it will generate an interrupt overflow occurs, will cause the debugging can not be.	0

The definition of window open cycle as shown in the figure below, For example, with 25% of the window open cycle:



7.3 Registers Descriptions

WDT Register base address

Modules Name	Physical Address	Mapping Address
WDT	0x40030000	0x40030000

WDT Register Offset Address

Registers Name	Address Offset	Descriptions
WDT_EN	0x0	Enable Register

- WDT_EN(0x0)

Bit	Name	Descriptions	R/W	Reset Value
31:9	---	Reserved	R	0
8	WR_BUSY	WDT Busy When WR_BUSY =1,WDT_EN can not be written; Only when WR_BUSY =0,can do write operations to the WDT EN register.	R	0

7:0	WDTE	0XBB is written to reset the watchdog timer and start counting operation again. The generation of reset signal sets this register to 0x55	R/W	55

Special attention: When the WDTE is written to 0xBB by user program, WR_BUSY changes to 1, only when WR_BUSY changes to 0 again represents that write the data to watchdog succeed, Before this, please don't close the APB clock of WDT module .Users write the data to watchdog need to pay attention to this matter before execute WFI directive .

8 LCD

SoC built-Segment type LCD controller.

RN8211 only supports part paragraph, See RN8211 packaging figure.

8.1 Overview

LCD controller has the following characteristics:

- ◎ Supports up to 4x34, 6x32, 8x30 LCD driving mode;
- ◎ Support for type A an B two driving waveforms;
- ◎ Support 1/3 and 1/4 bias ratio;
- ◎ Support static,1/2,1/3,1/4,1/6,1/8 duty ratio;
- ◎ Support 16 level of contrast driving mode;
- ◎ The built-in charge pump bias voltage generation;

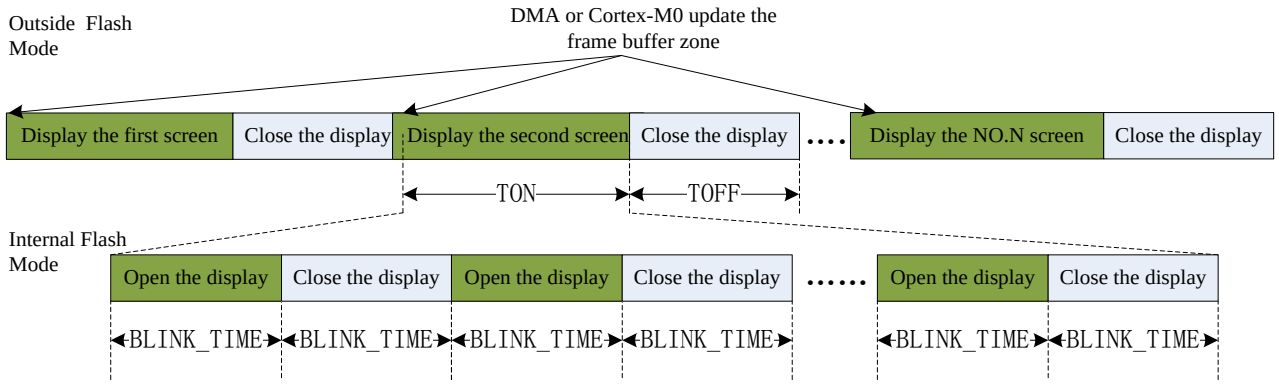
8.1.1 Scan Clock Frequency

LCD waveform scanning frequency is come from the LOSC(Frequency is 32768Hz) divider. Frequency division coefficient is configurated through LCD CLKDIV register. It is generally require that the frame's refresh rate of the LCD screen is slightly greater than 60Hz.The frame frequency of green label for normal use is in table 8-1.

Table 8-1 Scan frequency and frame frequency of LCD

LCD_CLKDIV	Scan frequency	Static Duty ratio	1/2 Duty ratio	1/3 Duty ratio	1/4 Duty ratio	1/6 Duty ratio	1/8 Duty ratio
0xff	64Hz	64Hz	32Hz	21.3Hz	16Hz	10.7Hz	8Hz
0x7f	128Hz	128Hz	64Hz	42.7Hz	32Hz	21.3Hz	16Hz
0x54	192.8Hz	192.8Hz	96.4Hz	64.3Hz	48.2Hz	32.1Hz	24.0Hz
0x3f	256Hz	256Hz	128Hz	85.3Hz	64Hz	42.7Hz	32Hz
0x2a	381.3Hz	381.3Hz	190.5Hz	127.0Hz	95.3Hz	63.5Hz	47.6Hz
0x1f	512Hz	512Hz	256Hz	170.7Hz	128Hz	85.3Hz	64Hz

8.1.2 Flash Mode



LCD supports two kinds of flash mode:Internal flash and Outside flash.These two modes can be enabled simultaneously.

Figure 8-1 LCD flash mode

As shown in figure 8-1,After LCD enabled, it would according to the defined length of time LCD BLINK register TON bit field to open the display ,and then it would according to the defined length of time LCD BLINK register TON bit field to close the display.

When the display is open or closed, LCD can send interrupt request or DMA request. Users can use these events to update the frame buffer.

Fit with wrapping characteristics of DMA, It can realize automatic wheel of a plurality of frame buffer.

8.1.2.1 Internal Flash Mode

LCD supports that insert flash mode in display time which is specified length by the LCD_BLINK register TON bit field. The interval of flashing is given by bit field of BLINK_TIME of LCD_BLINK register. When BLINK_TIME is equal to 0,internal flash mode is prohibited; and when BLINK_TIME is not equal to 0 ,TON must be an even multiple of BLINK_TIME.

8.1.2.2 Outside Flash Mode

When TOFF of the LCD_BLINK register is not equal to 0,Blink mode is enabled. According to the TON and TOFF values of LCD BLINK registers determine the flicker frequency after Blink mode enabled.

8.1.3 LCD Driving Waveform

LCD driving waveform and display waveform type, duty ratio related to bias voltage ratio.

Display waveforms of type A is line inversion drive mode, That is to complete a turn positive and negative drive in each frame; Display waveforms of type B is frame inversion drive mode, That is to complete a turn positive and negative drive in every two frame. The display waveform of type B drive mode shows the effect will be better when the duty ratio is larger

The user needs to select the duty ratio of LCD output waveform according to application of the number of COM:

- One COM: When select static duty ratio, only use COM0;
- Two COMs: When select 1/2 duty ratio, use COM0,COM1;
- Three COMs: When select 1/3 duty ratio, use COM0 ～COM2;
- Four COMs: When select 1/4 duty ratio,useCOM0 ～COM3;
- Six COMs: When select 1/6 duty ratio, use COM0 ～COM5;
- Eight COMs: When select 1/8 duty ratio, use COM0 ～COM7;

8.1.3.1 Driving waveform of type A

Figure 8-2 LCD driving waveform(1/4 Duty,1/3 Bias, Type A)

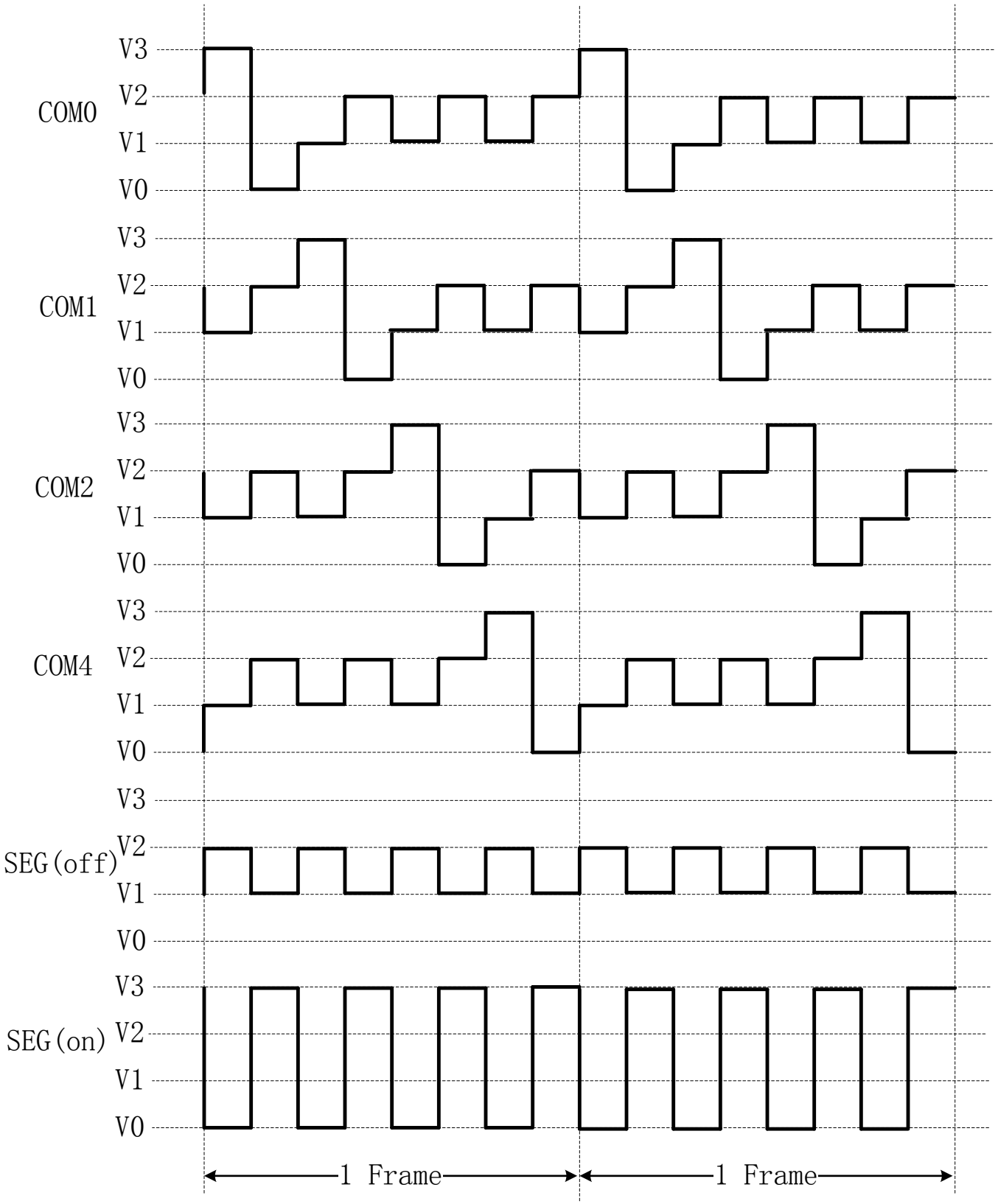
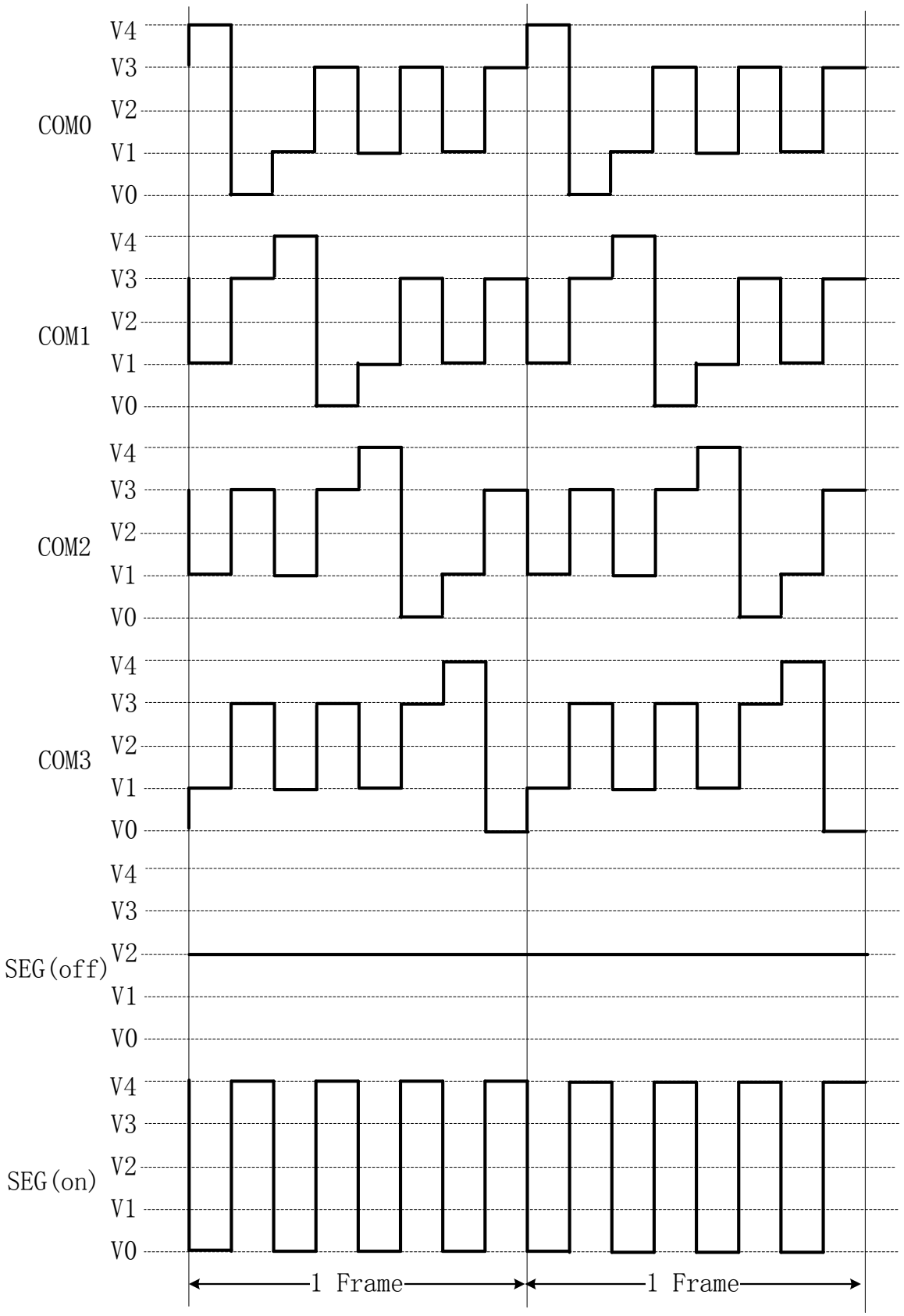


Figure8-3 LCD driving waveform(1/4 Duty,1/4 Bias, Type A)



8.1.3.1 **Driving Waveform of type B**

Figure8-4 LCD driving waveform(1/4 Duty,1/3 Bias, Type B)

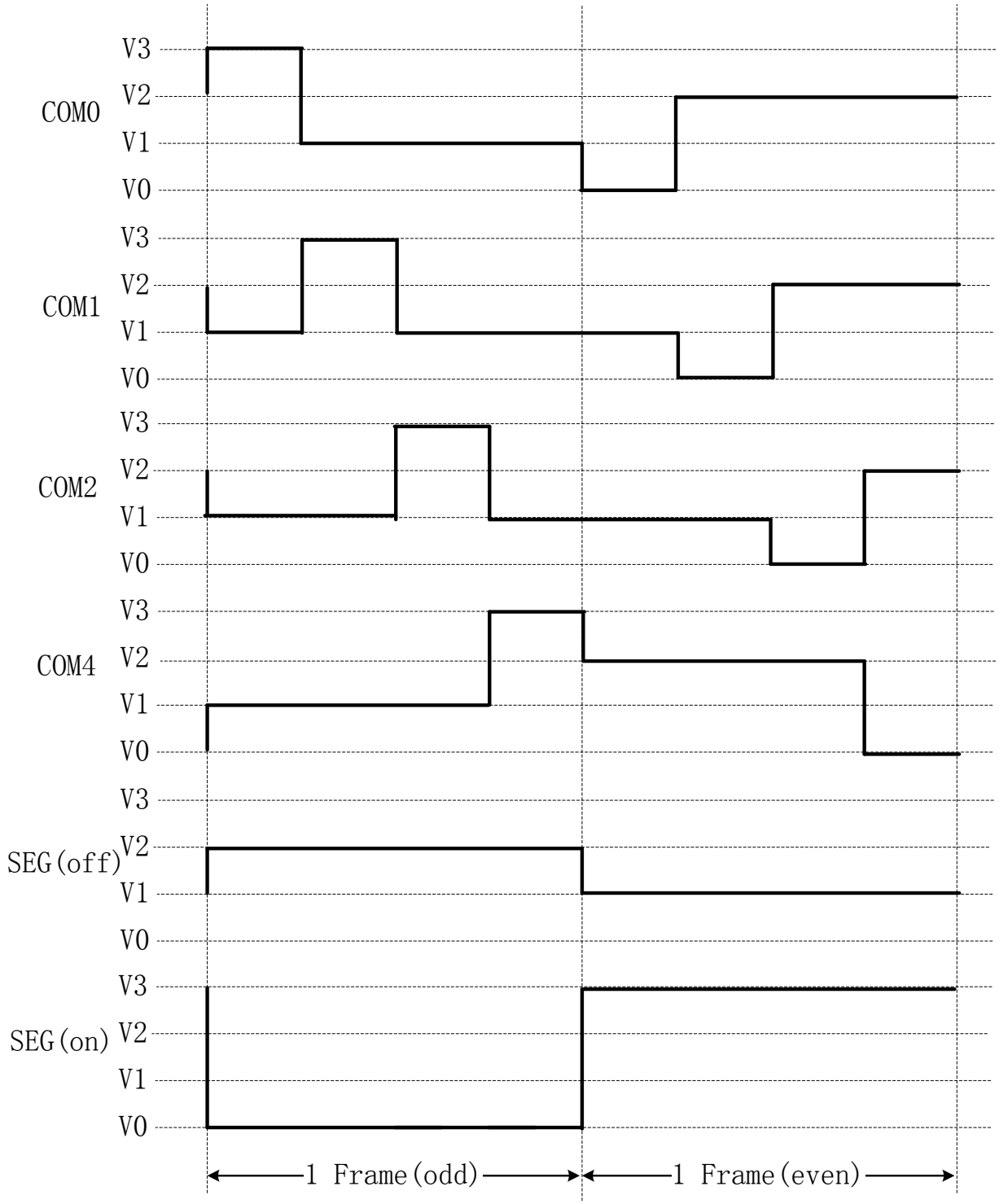
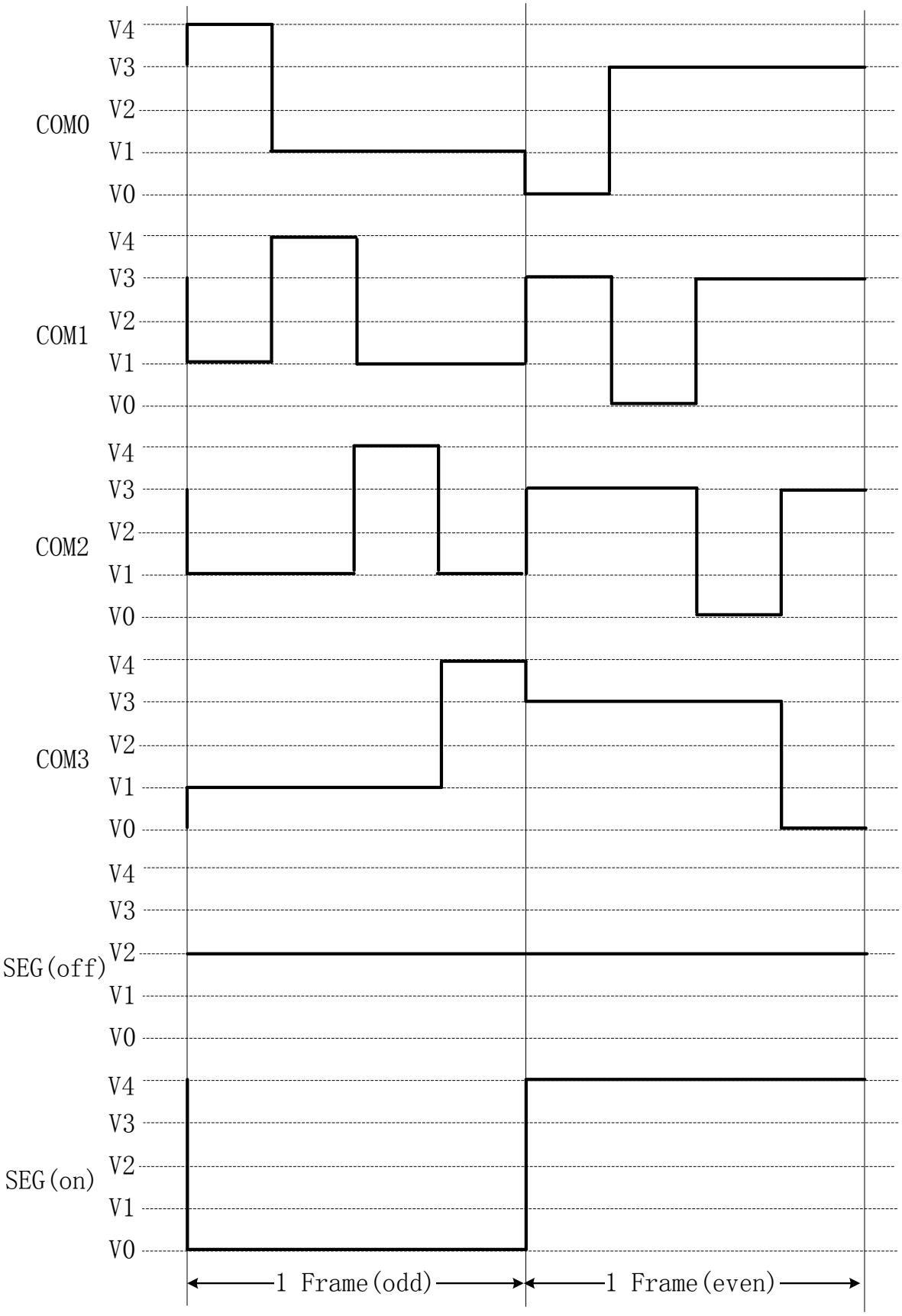


Figure8-5 LCD driving waveform(1/4 Duty,1/4 Bias, Type B)



8.1.4 Bias Voltage of LCD

The bias voltage of LCD can use Charge Pump to provide. Charge Pump is required to produce 4 voltage (Va,Vb,Vc,Vd)in order to meet the 1/4 bias Application. For different settings of bias ratio, the Charge Pump output voltage mode is different, as shown in table 8-2.

Table 8-2 The relationships between drive voltage of LCD and bias ratio

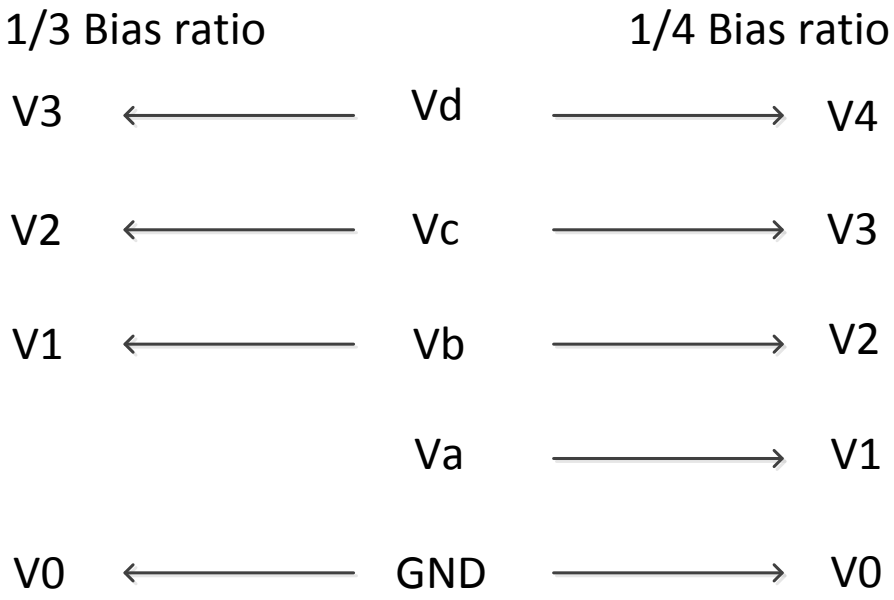
Bias ratio	Grayscale Select	Va	Vb	Vc	Vd	Vd(MAX)
1/3Bias ratio	BIASLVL[5] = 0	Va = Vref*(32+BIASLVL[4:0])/63	Vb = Va	Vc = 2*Va	Vd = 3*Va	3.75 V
	BIASLVL[5] = 1	Va = Vref*(1 + BIASLVL[4:0]/63)	Vb = Va	Vc = 2*Va	Vd = 3*Va	5.59 V
1/4Bias ratio	BIASLVL[5] = 0	Va = Vref*(32+BIASLVL[4:0])/63	Vb = 2*Va	Vc = 3*Va	Vd = 4*Va	5.0 V
	BIASLVL[5] = 1	Va = Vref*(1 + BIASLVL[4:0]/63)	Vb = 2*Va	Vc = 3*Va	Vd = 4*Va	6.032V

The maximum of LCD for Vd is 5.2 V. When the selection is 1/4 bias ratio and the set of BIASLVL[5:0] is larger than 6’h2d,LCD controller BIASLVL [5:0] clamped to 6'h2d automatically.

LCD selecte LBGR as the reference default, the typical output value of LBGR is 1.27V.

Applied voltage selection of 1/3 and 1/4 bias ratio, as shown in figure 8-6:

Figure8-6 Bias voltage selection



8.1.5 LCD Frame Buffer Mapping

The mapping relationship between LCD_BUFx register and different specifications segment code of the LCD screen as shown below.

i.When using the 8COM,it is need 30 LCD_BUFs,LCD screen can support up to 8 * 30

LCD_BUF[i] i=0~29 SEG maximum 30	SEG[i+4] COM7	SEG[i+4] COM6	SEG[i+4] COM5	SEG[i+4] COM4	SEG[i+4] COM3	SEG[i+4] COM2	SEG[i+4] COM1	SEG[i+4] COM0

ii.When using the 6COM,it is need 32 LCD_BUFs,LCD screen can support up to 6 * 32

LCD_BUF[i] i=0~31 SEG maximum 32	-	-	SEG[i+2] COM5	SEG[i+2] COM4	SEG[i+2] COM3	SEG[i+2] COM2	SEG[i+2] COM1	SEG[i+2] COM0

iii.When using the 4COM,3COM,2COM,1COM,it is need 17 LCD_BUFs,LCD screen can support up to 4*34

LCD_BUF[i] i=0~16 SEG maximum 34	SEG[2* i+1] COM3	SEG[2*i+ 1] COM2	SEG[2*i+ 1] COM1	SEG[2*i+ 1] COM0	SEG[2* i] COM3	SEG[2* i] COM2	SEG[2* i] COM1	SEG[2* i] COM0

8.2 Register Descriptions

LCD Register Base Address

Modules Name	Physical Address	Mapping Address
LCD	0x40048000	0x40048000

LCD Register Offset Address

Regiesters Name	Address Offset	Descriptions
LCD_CTL	0x0	LCD Control Register
LCD_STATUS	0x4	LCD Status Register
LCD_CLKDIV	0x8	LCD Clock Control Register
LCD_BLINK	0xc	LCD Flash Control Register
LCD_PS	0x10	LCD PUMP setting time Register
LCD_BUF[i]	0x20+i*1(i=0-31)	LCD Data Register(A total of 32 8-bit Registers)

- LCD Control Register LCD_CTL(0x0)

Bit	Name	Descriptions	R/W	Reset Value
31:13	---	Reserved	R	0
12	PWD_PUMP	LCD PUMP Switch: 0: Open PUMP, LCD voltage generate from internal PUMP. 1:Close PUMP, can select an external resistor strings voltage divider mode;	R/W	0
11	TYPE	LCD Drive Type Select 0:Type A 1:Type B	R/W	0
10:5	BIASLVL	LCD Bias voltage regulation Control charge pump output voltages of different magnitudes in order to control LCD contrast	R/W	0
4	BIAS	LCD Bias Control 0:1/3 Bias 1:1/4 Bias	R/W	0
3:1	DUTY	LCD Duty ratio Control 000:Static Output(COM0)	R/W	0

		001:1/2 Duty ratio(COM0~1) 010:1/3 Duty ratio(COM0~2) 011:1/4 Duty ratio(COM0~3) 100:1/6 Duty ratio(COM0~5) 101:1/8 Duty ratio(COM0~7) Other: Reserverd		
0	EN	LCD Module Enable 0:LCD Module Close 1:LCD Module Enable	R/W	0

- LCD Status Register LCD_STATUS(0x4)

Bit	Name	Descriptions	R/W	Reset Value
31:6	---	Reserved	R	0
6	LCD_BUSY	LCD Busy Bit 0:Not Busy 1:Busy Note: When LCD_BUSY=1,LCD_CTRL(In addition to EN Bit),LCD_CLKDIV,LCD_BLINK,LCD_PS registers cannot be modified	R	0
5	DMAOFFEN	Display Off DRQ Enable Bit 0:Disable 1:Enable Note:RN8211 not Support	R/W	0
4	DMAONEN	Display On DRQ Enable Bit 0:Disable 1:Enable Note:RN8211 not Support	R/W	0
3	IRQOFFEN	Display Off IRQ Enable Bit 0:Disable 1:Enable	R/W	0
2	IRQONEN	Display On IRQ Enable Bit 0:Disable 1:Enable	R/W	0
1	DOFF	Display Off Pending Bit 0:No interruption event 1:Set when display off by the light changed Note: Write 1 Cleared	R/W	0
0	DON	Display On Pending Bit 0:No interruption event 1:Set when display off by the brighter Note: Write 1 Cleared	R/W	0

- LCD Clock Control Register LCD_CLKDIV(0x8)

Bit	Name	Descriptions	R/W	Reset Value
31:8	---	Reserved	R	0
7:0	CLKDIV	LCD Clock divider modulus LCD_CLK=fosc/(2*(CLKDIV+1)) (fosc is 32768Hz)	R/W	0

- LCD Flash Control Register LCD_BLINK(0xC)

Bit	Name	Descriptions	R/W	Reset Value
31:24	---	Reserved	R	0
25:18	BLINK_TIME	Step is 0.25s,Support 0~63.75s Set TON display a cycle, the time of ON and OFF is equal to 0.25*BLINK_TIME. Note: When set to 0, it is represented TON long bright in the display cycle, do not flash. When the value of setting greater than 0, TON must be 2n times BLINK_TIME(N is an integer greater than 0).	R/W	0
17:9	TOFF	Step is 0.25s,Support 0~127.5s,When using this function, set to be > 3s;The actual time is:0.25s*TOFF	R/W	0
8:0	TON	Step is 0.25s,Support 0~127.5s,When using this function, set to be > 3s;The actual time is::0.25*TON	R/W	0

- LCD setting time of charge pump Register LCD_PUMP(0x10)

Bit	Name	Descriptions	R/W	Reset Value
31:12	---	Reserved	R	0
11:0	PS	LCD PUMP Setup time Time = Tosc * (PS+4) (Tosc is30.5uS) Note: Users do not need to configure this register.	R/W	0xccc

- LCD Data Register LCD_BUFx(x=0~31)(Address 0x20– 0x3F)

Bit	Name	Descriptions	R/W	Reset Value
31:8	---	Reserved	R	0
7:0	LCD_BUFx	SEG display data LCD screen, Each bits of the physical meaning is as follows: 0:Corresponding to the display unit does not display 1:Corresponding to the display unit do display **Note:RN8211 only support Part of the field, The users should not operate other fields buffers**	R/W	0

9 Timer

SoC built-in two 32-bit timers. Each timer can be completely independent work; Not shared any resources between timer, but can operate synchronous .

The timer is suitable for a variety of uses, with the following features:

- ◎ Interval timing;
- ◎ Square wave output;
- ◎ External, internal event count
- ◎ The single pulse output;
- ◎ PWM Output
- ◎ Pulse width measurement

RN8211 only support TC0,not support TC1.

9.1 Overview

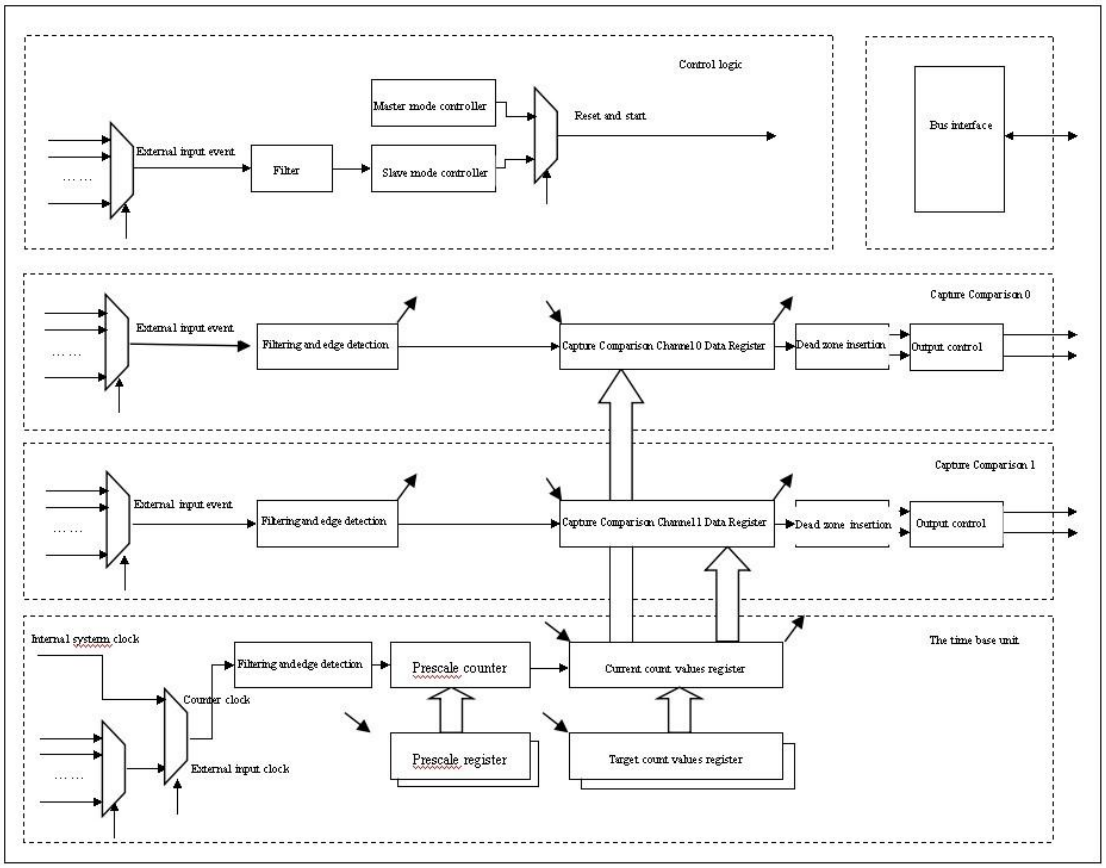
Timer has the following characteristics:

- ◎ Two 32-bit timers, each timer:
  - ■ Has a 32-bit incremental auto-reload counter;
  - ■ Has a 16-bit programmable prescaler, Frequency coefficients are optional from 1~65535;
  - ■ Support count value dynamic access to;
  - ■ Support free-running mode;
  - ■ Support single run;
- ◎ Each has 2capture,compare channels, and each channel can be independently configured to :
  - ■ Input capture;
  - ■ Output camparison;
  - ■ Single pulse output;
  - ■ The complementary PWM:
    - ◆ Dead zone length is programmable：
      - ● The dead zone length of two edge can be set up independently;
      - ● The polarity of the output is configurable;
    - ◆ Configurable invalid processing：
      - ● Output disabled;
      - ● Output cleared;
      - ● Output three states;
- ◎ Slave mode support for:
  - ■ External reset and restart;
  - ■ External gating;
- ◎ Input capture support for:
  - ■ Positive edge capture;
  - ■ Negative edge capture;
  - ■ Double edge capture;
  - ■ Cycle measurement;
  - ■ Pulse width measurement;
  - ■ Optional filtering;
- ◎ Comparison of output support for:
  - ■ Three state output;
  - ■ Inverted output;
  - ■ Fixed level output;
  - ■ The pulse width can configure pulse output;
  - ■ Compare register update at anytime;
- ◎ Support interrupt:

- Counter overflow;
- Input capture;
- Output comparison;

9.2 Function Block Diagram

The function block diagram of Counting timer shown below, please refer to. Each counter timer contains a 32-bit counter and 4 32-bit capture, compare channels.



9.3 Register Descriptions

RN8211 only support TC0,not support TC1,users must not operate TC1 register.

Module registers base Address

Module Name	Physical Address	Mapping Address
TC0	0x40010000	0x40010000
TC1	0x40014000	0x40014000

TC module registers Offset Address

Registers Name	Address Offset	Descriptions
TC_CNT	0x0	Instructions of the current count values
TC_PS	0x4	Prescale Register
TC_DN	0xC	Target Count Value Register
TC_CCD0	0x14	Capture Comparison Channel 0 Data Register
TC_CCD1	0x18	Capture Comparison Channel 1

		Data Register
TC_CCFG	0x1C	Clock Configuration Register
TC_CR	0x20	Control Register
TC_CM0	0x24	Capture Comparison Channel 0 mode Register
TC_CM1	0x28	Capture Comparison Channel 1 mode Register
TC_IE	0x2C	IER
TC_STA	0x30	Status Register

- The current count values Register TC_CNT(0x00)

Bit	Name	Descriptions	R/W	Reset Value
31:0	CNT	The current count values	R	0

- Prescale Register TC_PS(0x04)

Bit	Name	Descriptions	R/W	Reset Value
31:16	-	Reserved	R	0
15:0	PS	Frequency coefficient, divide values(PS+1),0 for not division	R/W	0

- Target count value Register TC_DN(0x0C)

Bit	Name	Descriptions	R/W	Reset Value
31:0	DN	Target count value, The actual count clock cycle is DN+1	R/W	0

- Capture comparison channel 0 data Register TC_CCD0(0x014)

Bit	Name	Descriptions	R/W	Reset Value
31:0	CCD	Comparative Capture Data	R/W	0

Note: When configuration of channel 0 is capture function(That is CCM bit field of TC_CM0 register is 0),TC_CCD0 register can not be written

- Capture comparison channel 1 data Register TC_CCD1(0x018)

Bit	Name	Descriptions	R/W	Reset Value
31:0	CCD	Comparative Capture Data	R/W	0

Note: When configuration of channel 1 is capture function(That is CCM bit field of TC_CM1 register is 0),TC_CCD1 register can not be written

- Clock Configuration Register TC_CCFG(0x01C)

Bit	Name	Descriptions	R/W	Reset Value
31:24	-	Reserved	R	0
23:16	FLTOPT	The settings of external clock input filter parameter, setting number of clock cycles of filter.	R/W	0
15	-		R	0
14:13	ECLKMODE	External input clock mode: 00:Positive Edge	R/W	0

		01:Negative Edge 10:Double Edge 11:Reserved(is equal to double edge)		
12:8	CS	Selection of external input: 0:UART0 RXD 1: UART1 RXD 2: UART2 RXD 3: UART3 RXD 4: The output outn[0] of another timer (TC0 or TC1) 5: The output outp[0] of another timer (TC0 or TC1) 6: The output outn[1] of another timer (TC0 or TC1) 7: The output outp[1] of another timer (TC0 or TC1) 8: UART4 RXD 9: UART5 RXD 10:7816_0 Input P41 11:7816_1 Input P42 12:7816_1 Input P43 13～15: Reserved 16:sf_out 17: qf_out 18: pf_out 19: rtc_out 20: p1[0] Outer IO 21: p1[1] Outer IO 27～22: Reserved 28: p3[0] Outer IO 29~31: Reserved	R/W	0
7:2	-	Reserved	R	0
1	FLTEN	Filtering enables of external clock input 0:Disable 1:Enable	R/W	0
0	CM	Selection of count clock source: 0:Internal system clock 1:External system clock(Select clock source by the CS)	R/W	0

- Control Register TC_CR(0x020)

Bit	Name	Descriptions	R/w	Reset Value
31:29	-	Reserved	R	0
28	DBGSTBDIS	The counter is enabled when in debug: 0:Disable(When the CPU is in debug state ,the counter stops counting) 1:Enable(When the CPU is in debug state, the counter continues to count) Note: CPU is in debug state refers to users would stop Cortex	R/W	0

		M0 through debugging interface(PC pointer stops counting).		
27	SLVDE	Slave Mode DMA Request Enable: 0:Disable 1:Enable	R/W	0
26	CC1DE	Capture comparison channel 1 DMA Request Enable: 0:Disable 1:Enable	R/W	0
25	CC0DE	Capture comparison channel 0 DMA Request Enable: 0:Disable 1:Enable	R/W	0
24	OVDE	Overflow DMA Request Enable: 0:Disable 1:Enable	R/W	0
23:21	-	Reserved	R	0
20	SLVGATELVL	Effective level of slave mode gated mode: 0:Effective level is Low level 1:Effective level is High level	R/W	0
19:12	SLVFLTOPT	Slave Mode input filter parameters	R/W	0
11:10	SLVTRGMODE	Selection of slave Mode control mode : 00:Positive edge cleared the internal counter 01:Negative edge cleared the internal counter 10:Double edge cleared the internal counter 11:Gated mode(The internal counter counts when the external input signal is effective level)	R/W	0
9:5	SLVCHANSEL	Election of slave mode external input events: Consistent with definitions of external input clock which clock configuration register (0x01C) bit field in CS difinited.	R/W	0
4	OPS	Election of single count mode: 0:Disable single count mode(Not stop after counter overflow ,the loop count); 1: Enable single count mode(Stop after counter overflow)	R/W	0
3	SLVFLTEN	Filtering enables of slave mode external input events: 0:Disable 1:Enable	R/W	0
2	SLVEN	Slave mode enable: 0:Disable 1:Enable	R/W	0
1	-	Reserved	R	0
0	START	Timer start: 0:Stop 1:Start	R/W	0

- Capture comparison channel 0,1 mode Register TC_CM0/1(0x024 and 0x028)

Bit	**Name**	**Descriptions**	**R/W**	**Reset Value**

31:30	-	Reserved	R	0
29	DFTLVL	The default level of comparison output: 0:Low level 1:High level	R/W	0
28	EFELVL	Effective level of comparison output: 0:Low level 1:High level	R/W	0
27:25	OM	Mode of comparison output : 000:No output(Three states) 001:Set to effective level 010:Set to invalid level 011:Flip flop 100:Forced to effective level 101:Forced to invalid level 110:PWM mode1 111:PWM mode2	R/W	0
24:20	CS	Selection of capture external input events: Consistent with definitions of external input clock which clock configuration register (0x01C) bit field in CS difinited.	R/W	0
19	FLTEN	Filtering enables of capture external input events: 0:Disable 1:Enable	R/W	0
18:11	FLTOPT	Filtering parameter of capture external input events	R/W	0
10:9	CPOL	Polarity selection of capture external input events: 00:Positive Edge 01:Negative Edge 10:Double Edge 11:Reserved	R/W	0
8:3	DL	Length of output dead zone of comparison (Only support PWM mode 1 and PWM mode 2,this bit is invalid in other modes)	R/W	0
2	DIEN	Insert enable of output dead zone of comparison:(Only support PWM mode 1 and PWM mode 2,this bit is invalid in other modes) 0:Disable 1:Enable	R/W	0
1	CCM	Selection of capture or comparison mode: 0:Capture 1:Comparison	R/W	0
0	ENABLE	Channel enables: 0:Disable 1:Enable	R/W	0

- IERTC_IE(0x2C)

Bit	Name	Descriptions	R/W	Reset Value
31:4	-	Reserved	R	0
3	SLVIE	Slave Mode Interrupt Enable: 0:Disable 1:Enable	R/W	0
2	CC1IE	Capture Comparison Channel 1 Interrupt Enable: 0:Disable 1:Enable	R/W	0
1	CC0IE	Capture Comparison Channel 0 Interrupt Enable: 0:Disable 1:Enable	R/W	0
0	OVIE	Overflow Interrupt Enable: 0:Disable 1:Enable	R/W	0

- State Register TC_STA(0x30)

Bits	Name	Descriptions	R/W	Reset Value
31:4	-	Reserved	R	0
3	SLVF	Slave Mode Event Flag:(Write 1 cleared) 0:No Slave Mode Event 1:Slave Mode Event	R/W	0
2	CC1F	Event Flag of Capture Comparison Channel 1:(Write 1 cleared) 0:No capture or compare event 1:Has capture or compare event	R/W	0
1	CC0F	Event Flag of Capture Comparison Channel 0:(Write 1 cleared) 0:No capture or compare event 1:Has capture or compare event	R/W	0
0	OVF	Event Flag of Overflow:(Write 1 cleared) 0:No Overflow Event 1:Overflow Event	R/W	0

9.4 Typical Applications

9.4.1 Automatic Operation Mode, Timing Function

The automatic operation mode is the interval timer function.

The basic timing functions**,** Only need to set the following register**:**

1、 Target count value register is the timing length, which counted by the clock of counting.

2、 Enable overflow of interrupt enable register which interrupts enable.

3、 Control register which starts timer.

The timer will take target count values as cycle generates interrupt.

Configuration instructions of commonly used selectable function：

1、 Can modify the prescaler register values and change the frequency of timer counter clock .

2、 Configurable clock configure register, CM modify the configuration is external input clock, modify the external input clock options of CS bit configuration at the same time. External input clock frequency can not be higher than two frequency divider of internal system clock frequency.

3、 Single count mode, when the timer overflow and then stop; OPS bit of configuration control register is 1,that is single count mode.

4、 External input clock source as the output of another timer, and it can be connected in cascade mode for the two timers, also can increase the register bits width of the timer.

9.4.2 Input Capture Mode, Function of Pulse Width Measurement

The main function of input capture mode is measure the width of the pulse.

The basic function of pulse width measurement, only need to set the following register:

1、 Target count value register, counted by counting clock and it can be set to the maximum value.

2、 Settings of capture comparison channel 0,1 mode register, ENABLE channel 0,1 enable it, CCM is configured to capture mode, CPOL select the polarity of the capture, CS select external input event.

3、 Enable capture comparison channel 0,1 of interrupt enable register which interrupts enable.

4、 Control register which starts timer.

When the timer capture to capture polarity of the external input event, then generate an interrupt, the current count is saved in the capture comparison channel data register at the same time. If using two channels, a channel to capture positive edge and another channel to capture negative edge, the pulse width can be calculated through data register of two channels.

Configuration instructions of commonly used selectable function:

1、 Can modify the prescaler register values and change the frequency of timer counter clock .

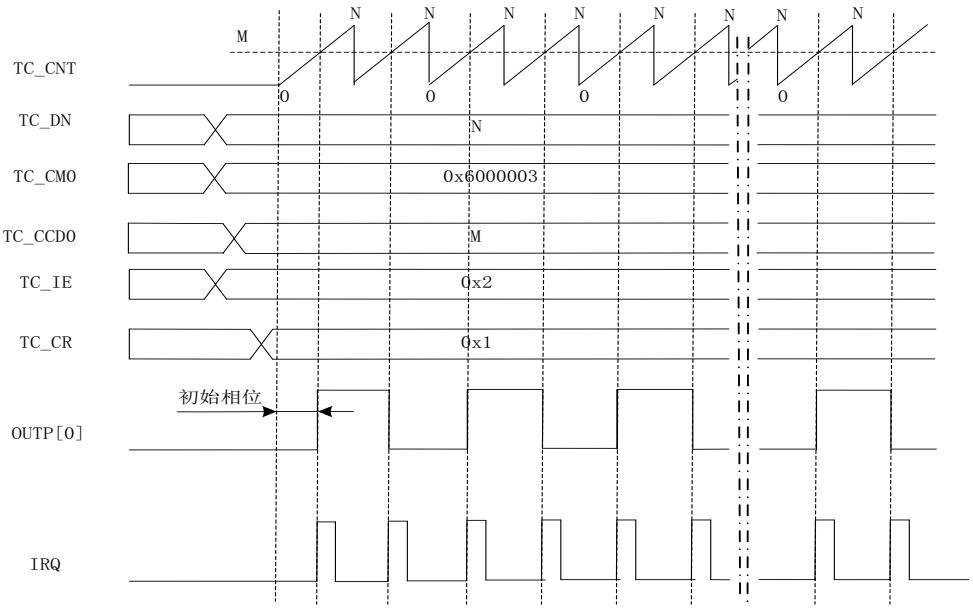
2、 Configurable clock configure register, CM modify the configuration is external input clock, modify the external input clock source of CS bit configuration at the same time. External input clock frequency can not be higher than two frequency divider of internal system clock frequency.

3、 Filtering function of external input event, enabled the FLTEN filtering function of capture comparison channel mode register and set filter cycle number by configuring the FLTOPT.

4、 External input clock source as the output of another timer, and it can be connected in cascade mode for the two timers, also can increase the register bits width of the timer.

9.4.3 Comparison Output Mode, Function of Square Wave Output

Function of square wave output that is dividing the frequency output to the count clock of TC .Each timer has two output channels, each channel has two output terminals P and N, where P is the positive output port, N is the reverse of the output port P.



Function of square wave output, only need to set the following register:

1、 Target count value register, counted by counting clock and it can be set to the maximum value.

2、 Settings of capture comparison channel 0,1 data register, ENABLE channel 0,1 enable it, CCM is configured to comparison mode, DFTLVL is configured to default level, EFELVL is configured to effective level, the output of OM is configured to flip function.

3、 Set the capture comparison channel 0,1 data register.(The setting values less than target count value register)

4、 Enable capture comparison channel 0,1 of interrupt enable register which interrupts enable.

5、 Control register which starts timer.

The values of the target count value register decided to cycle of square wave output, the value of capture comparison channel 0,1 data register is the flip flop point of output.

Configuration instructions of commonly used selectable function:

1、 Can modify the prescaler register values and change the frequency of timer counter clock.

2、 Configurable clock configure register, CM modify the configuration is external input clock, modify the external input clock source of CS bit configuration at the same time. External input clock frequency can not be higher than two frequency divider of internal system clock frequency.

3、 Filtering function of external input clock, enabled the FLTEN filtering function of clock configuration register and set filter cycle number by configuring the FLTOPT.

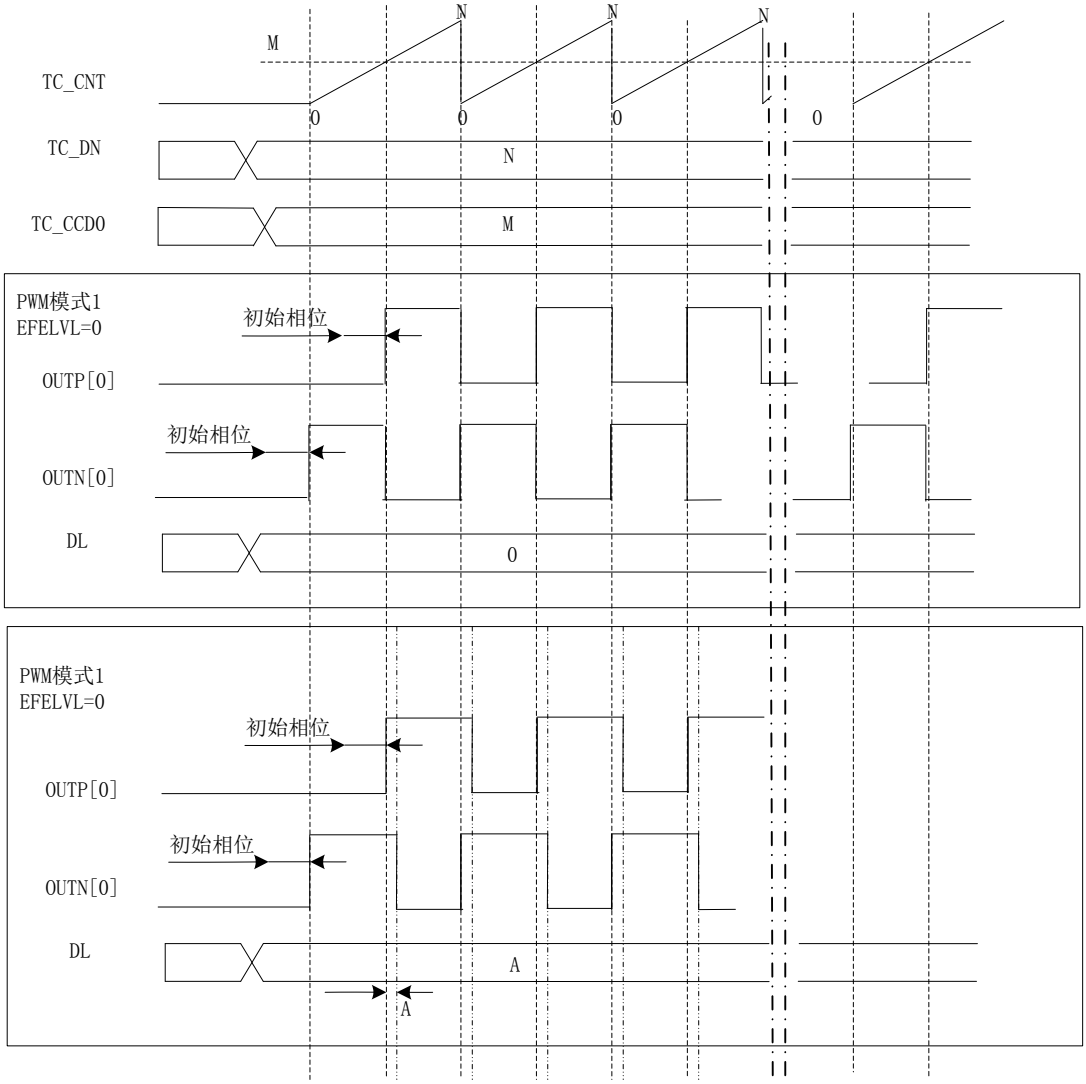
9.4.4 Mode of Compare Output, Function of PWM Output

The mode of pulse width measurement(PWM)can generates a signal which is determined the frequency by a TC_DN register and is determined the duty ratio by a TC_CCDx register .It support two PWM modes: PWM mode 1 and PWM mode 2:

PWM mode 1:If TC_CNT<TC_CCDx,the output is effective level, otherwise it is invalid level.

PWM mode 2:If TC_CNT>=TC_CCDx,the output is effective level, otherwise it is invalid level.

Below is the typical application diagram of PWM mode 1.



Function of PWM output, only need to set the following register:

1、 Target count value register, counted by counting clock.

2、 Settings of capture comparison channel 0, 1 mode register, ENABLE channel 0,1 enable it, CCM is configured to comparison mode, DFTLVL is configured to default level, EFELVL is configured to effective level, the output of OM is configured to PWM mode 1 or PWM mode 2.

3、 Set the capture comparison channel 0,1 data register, must be smaller than target count value register.

4、 Control register which starts timer.

Output positive waveform of PWM mode 1/PWM mode 2 in the channel of the P-ternimal, and in the channel of the N-terminal which output the reverse waveform to the P-side in the channel.

PWM mode 1:Cycle is values of target count value register plus1,effective level cycle is the number of cycles of channel data register values plus 1.

PWM mode 2:Cycle is values of target count value register plus1,invalid level cycle is the number of cycles of channel data register values plus 1.

Configuration instructions of commonly used selectable function:

1、 Can modify the prescaler register values and change the frequency of timer counter clock.

2、 Configurable clock configure register, CM modify the configuration is external input clock, modify the external input clock source of CS bit configuration at the same time. External input clock frequency can not

be higher than two frequency divider of internal system clock frequency.

3、 Complementary output of dead zone insertion, DIEN dead zone insertion enables, DL is to configure length of dead zone insertion. Add the delay in switch between P and N, that is do not let the two edges flip flop at the same time .

When effective level EFELVL is Low level: Output negative edge of P and N delayed DL cycles.

When effective level EFELVL is High level: Output positive edge of P and N delayed DL cycles.

9.4.5 Slave Mode, External Clear and Gating Functions

The salve mode adds an external input evens to control the internal counter clear and gating functions in the original feature.

External clear function, you need to set the following registers:

1、 Target count value register, counted by the count clock.

2、 Enable overflow in the interrupt enable register interrupt enable.

3、 Control register, SLVEN slave mode enable, SLVTRGMODE slave mode control mode selection,SLVCHANSEL the external input events of slave mode selection.

4、 Control, start the timer.

Such increasing a function of external clear and internal CNT in free-running mode.

Common optional functions configuration instructions:

1、 The prescaler register value can be modified, the timer count clock frequency can be changed.

2、 Configurable clock configuration register, CM modify the configuration to the external input clock, while modifying the external input clock source of the CS bit configuration. The frequency of external input clock source can not higher than the two frequency of internal system clock.

3、 Single count mode, the timer stop after overflowing; configuration control register OPS bit is 1 is the single count mode.

4、 It can be connected two timer to cascade mode when external input clock source is another timer output, which increases the timer register bits wide.

5、 In the slave mode control mode selection, if you choose to gated mode, SLVGATELVL slave mode gated active level configuration, the internal counter of slave mode input will count when gating level is effective.

6、 Configurate input capture mode in slave mode, capture mode select one edge ane slave mode polarity select another edge when the external input events of slave mode and capture is in same configuration, it can access to the pulse width from capture/compare channel data register.

10 Analog Peripherals

10.1 Features

10bit SAR ADC;

- You can measure the input voltage of battery VBAT;
- Multiplexing;

The main features of one LVD circuit are as follows:

- The input of LVD can choose the power for the chip or an external input PIN;
- LVD threshold is adjustable, multiple stalls can be set from 2.7V to 4.9V;
- When selecting an external PIN as input (LVDIN0), the threshold value is fixed at about 1.2V.

The main features of two comparator circuit CMP1 and CMP2 are as follows:

- External PIN input, the threshold is fixed at about 1.2V;
- CMP2 is low-power comparator, CMP2 is recommended to use the main power down power monitoring;
- RN8211 does not supported CMP1;

10.2 Register

Base address of analog peripheral module

Module Name	Physical Address	Address Mapping
ANA	0x4002C000	0x4002C000

Register offset address of analog peripheral module

Register Name	Address Offset	Description
SAR_CTL	Offset+0x0	SAR-ADC Control Register
SAR_START	Offset+0x4	SAR-ADC Start Register
SAR_STAT	Offset+0x8	SAR-ADC Status Register
SAR_DAT	Offset+0xC	SAR-ADC Data Register
LVD_CTL	Offset+0x10	Comparator Control Register
LVD_STAT	Offset+0x14	Comparator Status Register

- SAR_CTL

ADC Control Register Address 0x4002C000+ 0x700

Bit	Name	Description	R/W Sign	Reset Value
31:17	---	Reserved	R	0
16:12	REF_WAIT	The wait time from REF started to ADC started: 5'd0: 976uS 5'd31: (31+1)*976=31.232ms Wait Time=(REF_WAIT+1)* 976uS	R/W	0
11:7	SAR_WAIT	The wait time from SAR ADC started to sampling convert started: 5'd0: 30.5uS 5'd31: (31+1)*30.5=976us Wait Time=(SAR_WAIT+1)*30.5us Note: Step of start ADC measurement: Start REF, wait time of REF_WAIT; Start ADC and Temperature Sensor, wait time of SAR_WAIT; Input clock and reset single, the sampling results obtained after 16 clock cycles. The above steps are achieved from hardware automatic control.	R/W	0xE
6	SARDMA_IE	SAR-DMA Control: 1:Enable DMA request; 0:Unable DMA request;	R/W	0

5	SAR_IE	SAR-ADC Interrupt Control: 1:Enable ADC interrupt output; 0:Unable ADC interrupt output.	R/W	0
4:3	SAR_PGA	SAR-ADC Gain Control: 00: 0.5 01: 1 10: 1.5 11: 2	R/W	0
2:0	SAR_CH	SAR-ADC Channel Choose 000:Temperature measurement 001:VBAT(obtain 1.8V after 1/2 patrial pressure, PGA use 0.5 times, measure input 0.9V) 010:External pin input VIN0 011:External pin input VIN1 100:External pin input VIN2 101:External pin input VIN3 110:External pin input VIN4 111:External pin input VIN5 Regardless of which channel is selected, automatic temperature measurement is the highest priority.	R/W	0
Remark: the above registers could write only when ST=0 in SAR_START.				

- SAR_START

SAR-ADC Start Register Address 0x4002C000+ 0x4

Bit	Name	Description	R/W Sign	Reset Value
31:01	---	Reserved	R	0
0	ST	SAR-ADC Start Bit 0:SAR-ADC No Operation; 1:Start SAR-ADC sampling one time, automatically clear after the completion of the sampling. Note: Automatic temperature measurement controlled by the RTC is not controlled by the bit, and a higher priority than the configuration bits.	R/W	0

- SAR_STATUS

SAR-ADC Status Register Address 0x4002C000+ 0x8

Bit	Name	Description	R/W Sign	Reset Value
31:02	---	Reserved	R	0
1	TPS_BUSY	Automatical temperature measurement bit, =1:Automatical temperature measurement in process; =0:No automatical temperature measurement.	R	0

		When TPS_BUSY is 1,software write ADC_START register, hardware operations will work after TPS_BUSY is 0.		
0	DREADY	ADC Date Ready Pending Bit 0:ADC The conversion result is not completed 1:ADC The conversion result is completed Note: Write 1 clear; Automatical temperature measurement controlled by the RTC is not indicated in this state;	R/W	0

- SAR_DAT

ADC DAT Register Address 0x4002C000+ 0xC

Bit	Name	Description	R/W Sign	Reset Value
15:10	---	Reserved	R	0
9:0	SAR-DAT	The conversion result of ADC	R	0

- LVD_CTL

LVD Control Register Address 0x4002C000+ 0x10

Bit	Name	Description	R/W Sign	Reset Value
31:10	---	Reserved	R	0
9	SWHBIE	Switch to battery enable interrupt: =0:Enable uninterrupted; =1:Enable interrupt;	R/W	0
8	SWHMIE	Switch to the main power enable interrupt: =0:Enable uninterrupted; =1:Enable interrupt;	R/W	0
7	CMP2IE	Comparator 2 enable interrupt: =0:Enable uninterrupted; =1:Enable interrupt;	R/W	0
6	CMP1IE	Comparator 1 enable interrupt: =0:Enable uninterrupted; =1:Enable interrupt; RN8211 does not support this register bit;	R/W	0
5	LVDIE	LVD enable interrupt: =0:Enable uninterrupted; =1:Enable interrupt;	R/W	0
4	LVDC	Reserved	R	0
3:0	LVDS	Set LVD threshold voltage: 0000 2.7 0001 2.7 0010 2.7 0011 2.9 0100 3.1 0101 3.3 0110 3.5 0111 3.7 1000 3.9 1001 4.1 1010 4.3 1011 4.5 1100 4.7 1101 4.9	R/W	0

		1110 Detect voltage of external pin LVDIN0 to compare with LBGR(1.25V); 1111 Reserved;		

Note:LVD,Comparator 1 and Comparator 2 merge an interrupt vector; Power switches to single interrupt vector; SAR-ADC with a single interrupt vector.

- LVD_STAT

LVD Status Register Address 0x4002C000+ 0x14

Bit	Name	Description	R/W Sign	Reset Value
31:10	---	Reserved	R	0
9	SWHF	Power switch state flag: =0: Main power mode; =1: Battery Mode. Read-only	R	0
8	SWHBIF	Switch to battery interrupt flag: =0:No interrupt is generated;=1:Generate an interrupt; Interrupt is generated when the power is switched from the main power to the battery, cleared by writing 1;	R/W	0
7	SWHMIF	Switch to main power interrupt flag: =0:No interrupt is generated;=1:Generate an interrupt; Interrupt is generated when the power is switched from the battery to the main power, cleared by writing 1;	R/W	0
6	CMP2IIF	Comparator 2 interrupt flag =0:No interrupt is generated;=1:Generate an interrupt; Interrupt is generated when the input voltage is low relative to the threshold or becomes high, cleared by writing 1;	R/W	0
5	CMP1IIF	Comparator 1 interrupt flag =0:No interrupt is generated;=1:Generate an interrupt; Interrupt is generated when the input voltage is low relative to the threshold or becomes high, cleared by writing 1;	R/W	0
4	LVDIIF	LVD interrupt flag =0:No interrupt is generated;=1:Generate an interrupt; Interrupt is generated when the input voltage is low relative to the threshold or becomes high, cleared by writing 1;	R/W	0
3	---	Reserved	R	0
2	CMP2IIF	Comparator 2 status flag =0:Below threshold; =1:Above threshold;	R	0
1	CMP1IF	Comparator 1 status flag =0:Below threshold; =1:Above threshold; RN8211 does not support this register bit;	R	0
0	LVDIF	LVD status flag =0:Below threshold;	R	0

		=1:Above threshold;		

11 GPIO

11.1 Overview

- Contain PA,PB,PC three GPIO
- PA ports include four P0 ports, two P1 ports, eight P2 ports, four P3 ports
- PB ports include eight P4 ports, eight P5 ports, eight P6 ports, eight P7 ports
- PC ports include eight P8 ports, eight P9 ports ,four P11 ports
- GPIO is peripheral of AHB
- Support bitband operation;
- **RN8211/RN8211B support only part of IO ports, the user should not change the IO port which does not support the relevant register.**

11.2 Register Description

GPIO Register Base Address:

Module Name	Physical Address	Address Mapping
GPIO	0x50000000	0x50000000

GPIO Register Offset Address:

Register Name	Address Offset	Description
PMA	0x00H	PA port mode register(input or output)
PA	0x04H	PA port data register
PCA0	0x08H	PA port reuse register 0
PCA1	0x0CH	PA port reuse register 1
PUA	0x10H	PA port pull-up selection register
PIMA	0x14H	PA port input mode configuration
PIEA	0x18H	PA port input enable selection
PMB	0x1CH	PB port mode register(input or output)
PB	0x20H	PB port data register
PCB	0x24H	PB port reuse register

PUB	0x28H	PUB port pull-up selection register
PIMB	0x2CH	PB port input mode configuration
PIEB	0x30H	PB port input enable selection
PMC	0x34H	PC port mode register(input or output)
PC	0x38H	PC port date register
PCC	0x3CH	PC port reuse register
PUC	0x40H	PUC port pull-up selection register PCC PC port reuse register
PIEC	0x44H	PC port input enable selection
PIMB	0x48H	PC port input mode configuration
PCE	0x60H	SEGCOM port reuse register
PASET	0X64H	PA port data reset register, write 1 to this register, a correspond bit in PA port will be write 1;
PACLR	0X68H	PA port data clear register, write 1 to this register, a correspond bit in PA port will be cleared;
PBSET	0X6CH	PB port data reset register, write 1 to this register, a correspond bit in PB port will be write 1;
PBCLR	0X70H	PB port data clear register, write 1 to this register, a correspond bit in PB port will be cleared;
PCSET	0X74H	PC port data reset register, write 1 to this register, a correspond bit in PC port will be write 1;
PCCLR	0X78H	PC port data clear register, write 1 to this register, a correspond bit in PC port will be cleared;

Note: IO port types, see Chapter 1.4 Pin Arrangement.

Recommends using bitband function (see chapter 4.3.2) to access GPIO registers, facilitate the IO port register bit operations related.

Also can be SET / CLR register (0x64H ~ 0x78H) write GPIO data register;

If the IO port configuration options for the multiplexing function outside the IO port, mode register, the data register, input enable register is invalid, the pull-up selection, input mode selection is valid in all multiplex configuration.

RN8211 /RN8211B support only part of IO ports, the user should not change the IO port does not support the relevant registers.

PA port mode register PMA(input or output)(0x00)

Where PM12~PM17,PM31,PM33,PM34,PM35 no practical significance, users do not configure it.

Bit	Name	Description	R/W Sign	Reset Value
31:24	PM37~PM30	=0 Output Mode =1 Input Mode PM37 and PM36 are read only, read 1, only can be input model;	R/W	FF
23:16	PM27~PM20	=0 Output Mode =1 Input Mode	R/W	FF
15:8	PM17~PM10	=0 Output Mode =1 Input Mode	R/W	FF
7:5	---	Reserved	R	0
4:0	PM04~PM00	=0 Output Mode =1 Input Mode	R/W	1F

PA port data register PA(0x04)

Where P12~P17,P31,P33,P34,P35 no practical significance, users do not configure it.

Bit	Name	Description	R/W Sign	Reset Value
31:30	**P37~P36**	**P36 and P37 data input register, read-only;**	**R**	**0**
29:24	P35~P30	Define data needed in the chip output port. If you read in the input mode, the pin level is read. If you read in the output mode, then read the output latch value	R/W	00
23:16	P27~P20	Define data needed in the chip output port. If you read in the input mode, the pin level is read. If you read in the output mode, then read the output latch value	R/W	00
15:8	P17~P10	Define data needed in the chip output port. If you read in the input mode, the pin level is read. If you read in the output mode, then read the output latch value	R/W	00
7:5	---	Reserved	R	0
4:0	P04~P00	Define data needed in the chip output port. If you read in the input mode, the pin level is read. If you read in the output mode, then read the output latch value If defined as an analog input, the input mode to read a value of 0.	R/W	00

PA port reuse 0 register PCA0(0x08)

When selected as an analog input, the input mode is automatically selected, PMA register is invalid.
Where PM12~PM17,PM31,PM33,PM34,PM35 no practical significance, users do not configure it.

Bit	Name	Description	R/W Sign	Reset Value
31:30	---	Reserved	R	0
29	SWD_SEL	=0:P24 and P25 don’t select SWD,define by PC245(bit27);	R/W	1

		=1:P24 and P25 select SWD;		
28	PC267	Define the port P26 and P27 multiplex configuration: =0:select IO port; =1:select UART3 port.	R/W	00
27	PC245	Define the port P24 and P25 multiplex configuration: =0:select IO port; =1:select UART2 port.	R/W	00
26	PC223	Define the port P22 and P23 multiplex configuration: =0:select IO port; =1:select UART1 port.	R/W	00
25	PC201	Define the port P20 and P21 multiplex configuration: =0:select IO port; =1:select UART0 port.	R/W	00
24:13	---	Reserved	R	0
12:11	PC11[1:0]	Define the port P11 multiplex configuration: =00:select IO port; =01:select KEY input port; =10: select TC output port; =11: select TC input port. P11 correspond TC output tc0_p[0]		
10:9	PC10[1:0]	Define the port P10 multiplex configuration: =00:select IO port; =01:select KEY input port; =10: select TC output port; =11: select TC input port. P10 correspond TC output tc0_n[0]	R/W	00
8:7	---	Reserved	R	0
6:4	PC04~PC02	Define the port P04~P02 multiplex configuration: =0:select IO port; =1:select analog input port	R/W	0
3	---	Reserved	R	0
2	PC01	Define the port P01 multiplex configuration: =0:select IO port; =1:select analog input port	R/W	0
1	---	Reserved	R	0
0	PC00	Define the port P00 multiplex configuration: =0:select IO port; =1:select analog input port	R/W	0

PA port reuse 1 register PCA1(0x0C)

Bit	Name	Description	R/W Sign	Reset Value

31:16	---	Reserved	R	0
15:14	PC37[1:0]	Define the port P37 multiplex configuration: =00:select IO port; =01:select an external interrupt input port INT7; =1x:select pin crystal POSCI Note:Just PC36 [1] and PC37 [1] in any one of the high, then choose to POSC	R/W	0
13:12	PC36[1:0]	Define the port P36 multiplex configuration: =00:select IO port; =01:select an external interrupt input port INT6; =1x:select pin crystal POSCO Note:Just PC36 [1] and PC37 [1] in any one of the high, then choose to POSC	R/W	0
11:10	---	Reserved	R	0
9:8	---	Reserved	R	0
7:6	---	Reserved	R	0
5:4	PC32[1:0]	Define the port P32 multiplex configuration: =00:select IO port; =01:select an external interrupt input port INT2; =10:select as RTC output RTC_OUT (the default choice for the RTC output) =11: select IO port.	R/W	10
3:2	---	Reserved	R	0
1:0	PC30[1:0]	Define the port P30 multiplex configuration: =00:select IO port; =01:select an external interrupt input port INT0; =10:select TC input =11: Reserved	R/W	0

PA port pull-up select register PUA(0x10)

Note:When the IO port in output mode or analog PAD mode, regardless of how the configuration register PU, PIN not enable pull-up.

Where PU12~PU17,PU31,PU33,PU34,PU35 no practical significance, users do not configure it.

Bit	Name	Description	R/W Sign	Reset Value
31:24	PU37~PU30	Define port pull-up configuration: =0:Don't select pull-up; =1:Select pull-up;	R/W	00
23:16	PU27~PU20	Define port pull-up configuration: =0:Don't select pull-up; =1:Select pull-up; Note:P24 and P25 as SWD default pull-up enable.	R/W	30

15:8	PU17~PU10	Define port pull-up configuration: =0:Don't select pull-up; =1:Select pull-up;	R/W	00
7:5	--	Reserved	R	0
4:0	PU04~PU00	Define port pull-up configuration: =0:Don't select pull-up; =1:Select pull-up;	R/W	00H

PA port input mode configuration register PIMA(0x14)

Where PIL12~PIL17,PID12~PID17 no practical significance, users do not configure it.

Bit	Name	Description	R/W Sign	Reset Value
31:24	PIL27~PIL20	Define port P20~P27 input buffer type: =0:CMOS buffer,Vil=0.3VCC Vih=0.7VCC; =1:TTL buffer,Vil=0.16VCC Vih=0.4VCC;	R/W	00
23:16	PIL17~PIL10	Define port P10~P17 input buffer type: =0:CMOS buffer,Vil=0.3VCC Vih=0.7VCC; =1:TTL buffer,Vil=0.16VCC Vih=0.4VCC;	R/W	00
15:8	PID27~PID20	Define port P20~P27 whether is N-ch open-drain output: =0:Normal mode; =1:N-ch open-drain output mode;	R/W	00
7:0	PID17~PID10	Define port P10~P17 whether is N-ch open-drain output: =0:Normal mode; =1:N-ch open-drain output mode;	R/W	00

PA port input enable register PIEA(0x18)

Where PIE12~PIE17,PIE31,PIE33,PIE34,PIE35 no practical significance, users do not configure it.

Bit	Name	Description	R/W Sign	Reset Value
31:24	PIE37~PIE30	Input Enable: =1:No input enable; =0:Input enable; Note:The P30 is set to enter the electricity needs BOOTROM enabled, ISP is easy to detect.	R/W	FF
23:16	PIE27~PIE20	Input Enable: =1:No input enable; =0:Input enable;	R/W	FF
15:8	PIE17~PIE10	Input Enable:	R/W	FF

		=1:No input enable; =0:Input enable;		
7:5	Reserved	Reserved	R	0
4:0	PIE04~PIE00	Input enable: =1:No input enable; =0:Input enable;	R/W	3F

PB port mode register PMB(input or output)(0x1C)

Bit	Name	Description	R/W Sign	Reset Value
31:24	PM77~PM70	=0 Output mode =1 Input mode	R/W	FF
23:16	PM67~PM60	=0 Output mode =1 Input mode	R/W	FF
15:8	PM57~PM50	=0 Output mode =1 Input mode	R/W	FF
7:0	PM47~PM40	=0 Output mode =1 Input mode	R/W	FF

When the IO port is set to 7816 port or SPI port, direction register does not work, it controls by the communication module itself.

PB port data register PB(0x20)

Bit	Name	Description	R/W Sign	Reset Value
31:24	P77~P70	Define data needed in the chip output port. If you read in the input mode, the pin level is read. If you read in the output mode, then read the output latch value	R/W	00
23:16	P67~P60	Define data needed in the chip output port. If you read in the input mode, the pin level is read. If you read in the output mode, then read the output latch value	R/W	00
15:8	P57~P50	Define data needed in the chip output port. If you read in the input mode, the pin level is read. If you read in the output mode, then read the output latch value	R/W	00
7:0	P47~P40	Define data needed in the chip output port. If you read in the input mode, the pin level is read. If you read in the output mode, then read the output latch value	R/W	00

PB port reuse register PCB(0x24)

Bit	Name	Description	R/W	Reset

			Sign	Value
31:24	PC77~PC70	PC77~PC70 define port multiplex configuration: =0:select IO port; =1:select LCD.	R/W	00
23:16	PC67~PC60	PC67~PC60 define port multiplex configuration: =0:select IO port; =1:select LCD.	R/W	00
15:8	PC57~PC50	PC57~PC50 define port multiplex configuration: =0:select IO port; =1:select others. P50-PF,P51-QF,P52-SCL,P53-SDA P54- UART5-RX,P55- UART5-TX,P56-ZX-OUT,P57-SF P50 default is PF,P51 default is QF, other default select GPIO.	R/W	03
7:0	PC47~PC40	P47~P40 define port multiplex configuration: =0:select IO port; =1:P40~P43 select 7816 P44~47 select SPI. Default select GPIO. PC44 is only valid in SPI slave mode, in SPI master mode not configured for 1.	R/W	00

PB port pull-up/pull-down selection register PUB(0x28)

Bit	Name	Description	R/W Sign	Reset Value
31:24	PU77~PU70	PU77~PU70 define P7 port whether is internal pull-down: =0:No pull-down; =1:Internal pull-down.	R/W	00
23:16	PU67~PU60	PU67~PU60 define P6 port whether is internal pull-down: =0:No pull-down; =1:Internal pull-down.	R/W	00
15:8	PU57~PU50	PU57~PU50 define P5 port whether is internal pull-down: =0:No pull-up; =1:Internal pull-up.	R/W	00
7:0	PU47~PU40	PU47~PU40 define P4 port whether is internal pull-down: =0:No pull-up; =1:Internal pull-up.	R/W	00

PB port input mode register PIMB(0x2C)

Bit	Name	Description	R/W Sign	Reset Value
31:24	PIL57~PIL50	Define port P50~P57 input buffer type:	R/W	00

		=0:CMOS buffer, Vil=0.3VCC Vih=0.7VCC; =1:TTL buffer, Vil=0.16VCC Vih=0.4VCC; Which PIL51 and PIL50 read-only bit 0;		
23:16	PIL47~PIL40	Define port P40~P47 input buffer type: =0:CMOS buffer, Vil=0.3VCC Vih=0.7VCC; =1:TTL buffer, Vil=0.16VCC Vih=0.4VCC;	R/W	00
15:8	PID57~PID50	Define port P50~P57 whether is N-ch open-drain output: =0:Normal mode; =1:N-ch open-drain mode; Which PID51 and PID50 read-only bit 0;	R/W	00
7:0	PID47~PID40	Define port P40~P47 whether is N-ch open-drain output: =0:Normal mode; =1:N-ch open-drain mode;	R/W	00

PB port input enable register PIEB(0x30)

Bit	Name	Description	R/W Sign	Reset Value
31:24	PIE77~PIE70	Input Enable: =1:No input enable; =0:Input enable;	R/W	FF
23:16	PIE67~PIE60	Input Enable: =1:No input enable; =0:Input enable;	R/W	FF
15:8	PIE57~PIE50	Input Enable: =1:No input enable; =0:Input enable;	R/W	FF
7:0	PIE47~PIE40	Input Enable: =1:No input enable; =0:Input enable;	R/W	FF

PC port mode register PMC(input or output)(0x34)

Bit	Name	Description	R/W Sign	Reset Value
31:28	Reserved	----------	R	x
27:24	PM113~PM110	=0 Output mode =1 Input mode	R/W	F
23:16	Reserved	----------	R	x
15:8	PM97~PM90	=0 Output mode =1 Input mode	R/W	FF
7:0	PM87~PM80	=0 Output mode	R/W	FF

		=1 Input mode		

PC port data register PC(0x38)

Bit	Name	Description	R/W Sign	Reset Value
31:28	Reserved	----------	R	0
27:24	P113~P110	Define data needed in the chip output port. If you read in the input mode, the pin level is read. If you read in the output mode, then read the output latch value	R/W	0
23:14	Reserved	----------	R	0
15:8	P97~P90	Define data needed in the chip output port. If you read in the input mode, the pin level is read. If you read in the output mode, then read the output latch value	R/W	00
7:0	P87~P80	Define data needed in the chip output port. If you read in the input mode, the pin level is read. If you read in the output mode, then read the output latch value	R/W	00

PC port reuse register PCC(0x3C)

Bit	Name	Description	R/W Sign	Reset Value
31:29	Reserved	----------	R	0
28	SPI_MUX	SPI_MUX defines whether P4 is used as SPI or P11. =0:select P4 as SPI; =1: select P11 as SPI;		
27:24	PC113~PC110	PC113~PC110 define port multiplex configuration: =0:select IO port; =1:select SPI .		
31:14	Reserved	----------	R	0
15:8	PC97~PC90	PC97~PC90 define port multiplex configuration: =0:select IO port; =1:select LCD.	R/W	00
7:0	PC87~PC80	PC87~PC80 define port multiplex configuration: =0:select IO port; =1:select LCD.	R/W	00

PC port pull-down selection register PUC(0x40)

Bit	Name	Description	R/W Sign	Reset Value

31:28	Reserved	----------	R	0
27:24	PU113~PU110	PU113~PU110 define port whether is internal pull-down: =0:No pull-down; =1: Internal pull-down.		
23	Reserved	----------	R	0
15:8	PU97~PU90	PU97~PU90 define port whether is internal pull-down: =0:No pull-down; =1: Internal pull-down.	R/W	00
7:0	PU87~PU80	PU87~PU80 define port whether is internal pull-down: =0:No pull-down; =1: Internal pull-down.	R/W	00

PC port input enable register PIEC(0x44)

Bit	Name	Description	R/W Sign	Reset Value
31:28	Reserved	----------	R	x
27:24	PIE113~PIE110	Input Enable: =1:No input enable; =0:Input enable;	R/W	F
23:16	Reserved	----------	R	x
15:8	PIE97~PIE90	Input Enable: =1:No input enable; =0:Input enable;	R/W	FF
7:0	PIE87~PIE80	Input Enable: =1:No input enable; =0:Input enable;	R/W	FF

PC port input mode register PIMB(0x48)

Bit	Name	Description	R/W Sign	Reset Value
31:8	---	Reserved	R/W	00
7:4	PIL113~PIL110	Define port P113~P110 input buffer type: =0:CMOS buffer, Vil=0.3VCC Vih=0.7VCC; =1:TTL buffer, Vil=0.16VCC Vih=0.4VCC;	R/W	00
3:0	PID113~PID110	Define port P113~P110 whether is N-ch open-drain output: =0:Normal mode; =1:N-ch open-drain mode;	R/W	00

SEGCOM port reuse register PCE(0x60)

Bit	Name	Description	R/W Sign	Reset Value
31:4	---	Reserved	R	0
3:0	SEG3/COM7~SEG0/COM4	SEG3/COM7~SEG0/COM4 define port multiplex configuration: =0:select SEG; =1:select COM.	R/W	00

PA port data set register PASET(0x64)

Bit	Name	Description	R/W Sign	Reset Value
31:30	Reserved	----------	R	0
29:24	P35~P30	Set chip port status 0:No effect 1:The port is set, output high level	R/W	00
23:16	P27~P20	Set chip port status 0:No effect 1:The port is set, output high level	R/W	00
15:8	P17~P10	Set chip port status 0:No effect 1:The port is set, output high level	R/W	00
7:5	---	Reserved	R	0
4:0	P04~P00	Set chip port status 0:No effect 1:The port is set, output high level	R/W	00

Note: Read value is meaningless

PA port clear set register PACLR(0x68)

Bit	Name	Description	R/W Sign	Reset Value
31:30	Reserved	----------	R	00
29:24	P35~P30	Clear chip port status 0:No effect 1:The port is cleared, output low level	R/W	0
23:16	P27~P20	Clear chip port status 0:No effect 1:The port is cleared, output low level	R/W	00
15:8	P17~P10	Clear chip port status	R/W	00

		0:No effect 1:The port is cleared, output low level		
7:5	---	Reserved	R	0
4:0	P04~P00	Clear chip port status 0:No effect 1:The port is cleared, output low level	R/W	00

Note: Read value is meaningless

PB port data set register PBSET(0x6C)

Bit	Name	Description	R/W Sign	Reset Value
31:24	P77~P70	Set chip port status 0:No effect 1:The port is set, output high level	R/W	00
23:16	P67~P60	Set chip port status 0:No effect 1:The port is set, output high level	R/W	00
15:8	P57~P50	Set chip port status 0:No effect 1:The port is set, output high level	R/W	00
7:0	P47~P00	Set chip port status 0:No effect 1:The port is set, output high level	R/W	00

Note: Read value is meaningless

PB port clear set register PBCLR(0x70)

Bit	Name	Description	R/W Sign	Reset Value
31:24	P77~P70	Clear chip port status 0:No effect 1:The port is cleared, output low level	R/W	0
23:16	P67~P60	Clear chip port status 0:No effect 1:The port is cleared, output low level	R/W	00
15:8	P57~P50	Clear chip port status 0:No effect 1:The port is cleared, output low level	R/W	00
7:0	P47~P40	Clear chip port status 0:No effect 1:The port is cleared, output low level	R/W	00

Note: Read value is meaningless

PC port data set register PCSET(0x74)

Bit	Name	Description	R/W Sign	Reset Value
31:28	Reserved	----------	R	0
27:24	P113~P110	Set chip port status 0:No effect 1:The port is set, output high level	R/W	00
23:16	Reserved	----------	R	0
15:8	P97~P90	Set chip port status 0:No effect 1:The port is set, output high level	R/W	00
7:0	P87~P80	Set chip port status 0:No effect 1:The port is set, output high level	R/W	00

Note: Read value is meaningless

PC port clear set register PCCLR(0x78)

Bit	Name	Description	R/W Sign	Reset Value
31:28	Reserved	----------	R	00
27:24	P113~P110	Clear chip port status 0:No effect 1:The port is cleared, output low level	R/W	00
23:16	Reserved	----------	R	00
15:8	P97~P90	Clear chip port status 0:No effect 1:The port is cleared, output low level	R/W	00
7:0	P87~P80	Clear chip port status 0:No effect 1:The port is cleared, output low level	R/W	00

Note: Read value is meaningless

12 External Interrupt Controller

SoC internally installed external interrupt controller (INTC), handle the interrupt request from input pins on the chip.

12.1 Introduce

External interrupt controller has the following features:

◎ Supports four external interrupt mode setting: up and down along the edge and can be set up

bilateral;

◎ Support for external interrupt status indication;

◎ Support for external interrupt trigger by software;

◎ Support for external interrupt status;

◎ Support for external interrupt mask;

◎ Support for external interrupt filtering;

12.2 Register Description

Module register base address

Module Name	Physical Address	Address Mapping
INTC	0x40044000	0x40044000

INTC Module register address offset

Register Name	Address Offset	Description
INTC_CTL	0x0	INTC Control Register
INTC_MODE	0x4	INTC Mode Register
INTC_MASK	0x8	INTC Mask Register
INTC_STA	0xc	INTC Status Register

- INTC_CTL

INTC Control Register Address 0x40044000+0x0

Bit	Name	Description	R/W Sign	Reset Value
31:08	---	Reserved	R	0
7:6	Enable	Enable signal, Enable[7:6] correspond to the external interrupt request 7 and 6, correspond to the external pins:P37/INT7 and P36/INT6. 0:Close correspond external interrupt 1:Enable correspond external interrupt	R/W	0
5:3	---	Reserved	R	0
2	Enable	Enable signal, Enable[2] correspond to the external interrupt request 2, Correspond to the external pins: P32/INT2. 0:Close correspond external interrupt 1:Enable correspond external interrupt	R/W	0
1	---	Reserved	R	0
0	Enable	Enable signal, Enable[0] correspond the external interrupt request 0, Correspond to the external pins: P30/INT0. 0:Close correspond external interrupt 1:Enable correspond external interrupt	R/W	0

- INTC_MODE

INTC Mode Register Address 0x40044000+0x4

Bit	Name	Description	R/W Sign	Reset Value

31:06	---	Reserved	R	0
15:14	MODE7	External interrupt request 7 (P37/INT7)mode select 00:Rising edge 01:Falling edge 10:Double edge 11:Reserved	R/W	0
13:12	MODE6	External interrupt request 6 (P36/INT6)mode select 00:Rising edge 01:Falling edge 10:Double edge 11:Reserved	R/W	0
11:6	---	Reserved	R	0
5:4	MODE2	External interrupt request 2 (P32/INT2)mode select 00:Rising edge 01:Falling edge 10:Double edge 11:Reserved	R/W	0
3:2	---	Reserved	R	0
1:0	MODE0	External interrupt request 0(P30/INT0)mode select 00:Rising edge 01:Falling edge 10:Double edge 11:Reserved	R/W	0

- INTC_MASK

INTC Mask Register Address 0x40044000+0x8

Bit	Name	Description	R/W Sign	Reset Value
31:08	---	Reserved	R	0
7:6	MASK	MASK[7:6] correspond to the external interrupt request 7 and 6 0:Interrupt disabled 1:Interrupt enabled	R/W	0
5:3	---	Reserved	R	0
2	MASK	MASK[2] correspond to the external interrupt request 2 0:Interrupt disabled 1:Interrupt enabled	R/W	0
1	---	Reserved	R	0
0	MASK	MASK[0] correspond to the external interrupt request 0 0:Interrupt disabled 1:Interrupt enabled	R/W	0

- INTC_STA

INTC Status Register Address 0x40044000+0xc

Bit	Name	Description	R/W Sign	Reset Value

31:08	---	Reserved	R	0
7:6	STA	STA[7:6] correspond to the external interrupt request 7 and 6 0:Interrupt event has not occurred 1:Interrupt event has occurred Note: Write 1 cleared	R/W	0
5:3	---	Reserved	R	0
2	STA	STA[2] correspond to the external interrupt request 2 0:Interrupt event has not occurred 1:Interrupt event has occurred Note: Write 1 cleared	R/W	0
1	---	Reserved	R	0
0	STA	STA[0] correspond to the external interrupt request 0 0:Interrupt event has not occurred 1:Interrupt event has occurred Note: Write 1 cleared	R/W	0

13 KBI

SoC chip key interface controller.

13.1 Feature

Key interface controller has the following feature:

- ◎ Support for 2 keys,correspond pins are P10/KEY0 and P11/KEY1;
- ◎ Support for each key state check;
- ◎ Support each key input filter, filter time is 24ms;
- ◎ Support each key individually masked interrupts.

13.2 Register Description

Table 13-1 KBI Register Base Address

Module Name	Physical Address	Address Mapping
KBI	0x40028000	0x40028000

Table 13-2 KBI Register Address Offset

Register Name	Address Offset	Description
KBI_CTL	0x0	Control Register
KBI_SEL	0x4	SEL Register
KBI_DATA	0x8	Data Register
KBI_MASK	0xc	Mask Register

- Control Register(0x0)

Table 13-3 KBI Control Register KBI _CTL

Bit	Name	Description	R/W Sign	Reset Value
31:2	---	Reserved	R	0
1:0	EN	Enable signal,EN[1:0] correspond to the KEY[1:0], Correspond to the external pins:P10/KEY0 and P11/KEY1. 0:Close correspond KEY 1:Enable correspond KEY	R/W	0

- SEL Register(0x4)

Table 13-4 KBI SEL Register KBI _SEL

Bit	Name	Description	R/W Sign	Reset Value
31:2	---	Reserved	R	0
1:0	SEL	SEL[1:0] correspond to the KEY[1:0] 0:Rising edge active 1:Falling edge active	R/W	0

- Date Register(0x8)

Table 13-5 KBI Data Register KBI _DATA

Bit	Name	Description	R/W Sign	Reset Value
31:2	---	Reserved	R	0
1:0	DAT	DAT[1:0] correspond to the KEY[1:0]. Write 1 cleared 0:Key is not pressed 1:Key is pressed	R/W	0

- Mask Register(0xC)

Table 13-6 KBI Mask Register KBI _MASK

Bit	Name	Description	R/W Sign	Reset Value
31:2	---	Reserved	R	0
1:0	MASK	MASK[1:0] correspond to the KEY[1:0] 0:Interrupt disabled 1:Interrupt enabled	R/W	0

14 UART

SoC internally installed 5 UART interface for external asynchronous serial communication. RN8211 only support UART0,UART1,UART2,UART5.

14.1 Introduce

UART interface controller has the following feature:

◎ Five full-duplex UART interface;
◎ Internally installed baud rate generator, the baud rate is configured to support different;
◎ Data bits wide support 5/6/7/8bit;
◎ Stop bits can set 1 or 2bit;
◎ Optional 38kHz modulated IR;
◎ Supports automatic baud rate detection;
◎ Support IR wake;

14.2 Register Description

Table 14-1 UART Register Base Address

Module Name	Physical Address	Address Mapping
UART0	0x40000000	0x40000000
UART1	0x40004000	0x40004000

UART2	0x40008000	0x40008000
UART3	0x4000C000	0x4000C000
UART5	0x4001C000	0x4001C000

Table 14-2 UART Register Address Offset

Register Name	Address Offset	Description
UART_CTL	0x0	UART Control Register
UART_BAUD	0x4	UART Baud Rate Configuration Register
UART_STAT	0x8	UART Status Indication Register
UART_TXD	0xC	UART Transmit data register
UART_RXD	0x10	UART Receive data register

- Control Register(0x0)

Table 14-3 Control Register UART_CTL

Bit	Name	Description	R/W Sign	Reset Value
31:12	---	Reserved	R	0
12	IRSEL	Infrared modulation polarity selection: 0:Positive polarity, the default drive level is high 1:Negative polarity, the default drive level is low	R/W	0
11	ILBE	Enable internal loop back 0:Internal loop back unable 1:Internal loop back enable, TXD and RXD shorted inside the module	R/W	0
10	IRE	Infrared modulation enable bit 0:Close infrared modulation output 1:Open infrared modulation output, low-carrier modulation with 38k output data	R/W	0
9:7	PARS	Select the parity bit 0:No parity 1:Odd parity 2:Even parity 3:Fixed zero parity 4: Fixed one parity Other: User-defined parity	R/W	0
6:5	DATLEN	Transmission bit data width 0:5-bit 1:6-bit 2:7-bit 3:8-bit	R/W	0
4	STOPS	Stop bit wide select 0:1-bit stop bit 1:2-bit stop bit	R/W	0
3	ERRIE	Error interrupt enable bit, the corresponding flag bit is the status	R/W	0

		indicator register bit5~bit2. 0:Close interrupt 1:Open interrupt		
2	RXIE	Receive data interrupt enable bit, the corresponding flag bit is the status indicator register bit1. 0:Close interrupt 1:Open interrupt	R/W	0
1	TXIE	Transmit data interrupt enable bit, the corresponding flag bit is status indicator registers bit0. 0:Close interrupt 1:Open interrupt	R/W	0
0	EN	Module enable 0:Close 1:Open	R/W	0

- Baud Rate Configuration Register(0x4)

Table 14-4 Baud Rate Configuration Register UART_ BAUD

Bit	Name	Description	R/W Sign	Reset Value
31:12	---	Reserved	R	0
11:0	CLKDIV	UARTx clock divide The formula of baud rate is: System Clock/[16*(CLKDIV+1)]	R/W	0

- Status Indication Register(0x8)

Table 14-5 Status Indication Register UART_STA

Bit	Name	Description	R/W Sign	Reset Value
31:8	---	Reserved	R	0
9	tx_fifo_full	Transmit FIFO is full: 0:Not full 1:Full	R	0
8	tx_fifo_empty	Transmit FIFO is empty: 0:Not empty 1:Empty	R	1
7	TB	Send state flag 0:Did not send 1:Sending data	R	0
6	RB	Receive status flag 0:Did not receive 1:Receiving data	R	0
5	DE	Data errors, write one cleared 0:No error 1:Error	R/W	0
4	FE	Frame error, write one cleared 0:No error	R/W	0

		1:Error		
3	OE	Overflow error, write one cleared 0:No error 1:Error	R/W	0
2	PE	Parity error, write one cleared 0:No error 1:Error	R/W	0
1	TX	Send flag, write one cleared 0:Data not yet been sent or no data to be transmitted 1:Date has sent	R/W	0
0	RX	Receive flag, write one cleared 0:No receive data 1:Data has received	R/W	0

- Transmit data register(0xC)

Table 14-6 Baud Rate Configuration Register UART_ TXD

Bit	Name	Description	R/W Sign	Reset Value
31:9	---	Reserved	R	0
8	UP	User defined parity bit	R/W	0
7:0	TXDATA	Transmit data register	R/W	0

- Receive data register(0x10)

Table 14-7 Receive data register UART_ RXD

Bit	Name	Description	R/W Sign	Reset Value
31:9	---	Reserved	R	0
8	UP	Parity bit	R	0
7:0	RXDATA	Receive data register	R	0

15 ISO7816

SoC internal installed two ISO7816 channels, support for external 2 7816 protocol interface device. RN8211 does not support ISO7816.

15.1 Introduce

ISO7816 interface controller has the following features:

◎ Support standard ISO7816 protocol, working in master mode;
◎ Support card clock output, frequency can be set between 1 ~ 5MHz;
◎ Support 7816 various frequency division ratio setting;
◎ Support MSB first output logic low and logic high output LSB first data encoding;
◎ Support 1, 2 ETU width set the width of the error signal;
◎ Support 0~254 ETU width EGT configuration;
◎ Supports sending data transmission error retransmission mechanism, the number of retransmissions can be set between 0 to 7;
◎ 7816 card stack supports two interfaces (Esam and card): esam modules receive and transmit ports with a pin;

◎ Support card interface for receiving and sending separation;

15.2 Register Description

Table 15-1 ISO7816 Register Base Address

Module Name	Physical Address	Address Mapping
ISO7816	0x40038000	0x40038000

Table 15-2 ISO7816 Register Address Offset

Register Name	Address Offset	Description
ISO7816_CTL0	0x0	Control Register 0
ISO7816_CTL1	0x4	Control Register 1
ISO7816_CLK	0x8	Clock Configuration Register
ISO7816_BDDIV0	0xc	Baud Rate Configuration Register 0
ISO7816_BDDIV1	0x10	Baud Rate Configuration Register 1
ISO7816_STAT0	0x14	Status Indication Register 0
ISO7816_STAT1	0x18	Status Indication Register 1
ISO7816_DAT0	0x1c	Data Transmit Register 0
ISO7816_DAT1	0x20	Data Transmit Register 1

- Control Register(0x0)

Table 15-3 ISO7816 Control Register 0 ISO7816_CTL0

Bit	Name	Description	R/W Sign	Reset Value
31:28	---	Reserved	R	0
27	RX_GT0	Receive data GT select bit, when sending fixed 2etu 1:Receive data GT is 1etu 0:Receive data GT is 2etu	R/W	0
26	TX0_DMA_EN	Send DMA request 1:Enable DMA request 0:Unable DMA request	R/W	0
25	RX0_DMA_EN	Receive DMA request 1:Enable DMA request 0:Unable DMA request	R/W	0
24:17	EGT0	EGT width selection value (0 to 255), that the extra guard time N, the default value N = 0. In the range of 0 to 254, N is used to calculate the delay between two consecutive data of a start edge: 12 etu + (Q ×(N / f)). Formula, Q should take one of two values below: ——When T=15 does not exist in answer to reset, take F/D; ——When T=15 exit in answer to reset, take Fi/Di; N = 255 means that during transport protocol, a minimum of two consecutive characters start edge delay between the two directions of transmission are the same. The minimum delay value is: ——T=0,12etu	R/W	0

		——T=1,11etu		
16: 14	REP_CNT0	Odd Even parity data automatically control the number retransmissions when error 000:0 time 001:1 time 010:2 times 011:3 times 100:4 times 101:5 times 110:6 times 111:7 times	R/W	011
13	RXPAR_ESEL0	Receive data parity error handling mode selection 1: Parity error, according to the T = 0 protocol post back error signal. Set RX_PAR_ERR flag, interrupt. 0: Parity error, do not send error signal, set RX_PAR_ERR flag, direct interrupt.	R/W	1
12:11	ERRWTH0	Error signal width select bit applies only to receive, and RXPAR_ESEL0 = 1 00:2 etu 01:1 etu 10:1.5 etu 11:2 etu	R/W	01
10:8	PARSEL0	Parity bits select 000:No parity 001:Odd parity 010:Even parity 011:Fixed zero parity 100: Fixed one parity Other: Reserved	R/W	010
7	BGT_EN0	Data received BGT control bits transmitted 0:Close BGT function, data between transmission and reception don't insert BGT 1:Open BGT function, data between transmission and reception insert BGT(22etu)	R/W	0
6	ERR_IRQ_EN0	Transmission error interrupt enable bit, data collision when transmitting data, the data is received and the received data frame format overrun error 0:Prohibit transmission error interrupt is generated 1:Enable transmission error interrupt is generated	R/W	0
5	RX_IRQ_EN0	Data receive interrupt enable bit, enables data is shifted from the shift register to the receive buffer register to generate an interrupt 0:Prohibit data reception interrupt is generated 1:Enable data reception interrupt is generated	R/W	0
4	TX_IRQ_EN0	Data transmit interrupt enable bit to enable the completion of the data from the transmit shift register to generate an interrupt 0:Prohibit sending data to generate an interrupt 1:Enable data transmission interrupt is generated	R/W	0

3	RX_EN0	Receive data enable 0:Prohibit data reception 1:Enable data reception	R/W	0
2	TX_EN0	Enable sending data 0:Prohibit data transmission 1:Enable data transmission	R/W	0
1	DIRSEL0	Data coding mode selection bit 0:LSB first pass being logical data encoding 1:MSB first pass negative logic data encoding (data negated)	R/W	0
0	EN0	ISO7816 The controller enable bit 0:Controller close 1:Controller open	R/W	0

- ISO7816 control register1(0x04)

Table 15-4 ISO7816 control register1 ISO7816_CTL1

Bit	Name	Descriptions	R/W	Reset Value
31	CARD1_CHECK_EN	Card out Detect Flag, it is only active after the detection function of OLD is enable 1:Enable card out detection interrupt function 0:Disable card out detection interrupt function	R/W	0
30	OLD1_IRQ_EN	OLD detection interrupt function flag, it is only active after detection function of OLD is enable 1:Enable OLD detection interrupt function 0:Disable OLD detection interrupt function	R/W	0
29	OLD1_EN	OLD detection function flag 1:Enable OLD detection function 0:Disable OLD detection function	R/W	0
28	RX1_GT0	GT of received data choice bit, it is always 2etu When data is transmitted 1:GT of received data is 1etu 0:GT of received data is 2etu	R/W	0
27	TX1_DMA_EN	Send DMA requests enable 1:Enable DMA requests 0:Disable DMA requests	R/W	0
26	RX1_DMA_EN	Receive DMA requests 1:Enable DMA requests 0:Disable DMA requests	R/W	0
25	IO1_EN	bidirectional data enable signal 1:78161_IO port is a bidirectional signal 0:78161_IO port is a one-way signal ,output only, The data are input at 78161_I port	R/W	1
24:17	EGT1	EGT width selection(0~255), extra protection time N Default N=0. In the range of 0 to 254,N:before it was ready to	R/W	0

		receive the next character, the card need the delay(it sent by card or interface device) which start with onset of the first character: 12 etu +(Q×(N/f)) In the formula, Q should be one of two values: F/D, it is used to compute the value of etu. When T = 15 don't exist in the reset reply, Fi/Di, When T = 15 exist in the reset reply. N=255when the transmission protocol is effective, Minimize Delay between onset of two continuation character in either direction remains the same. Minimize Delay: When T=0,12etu When T=1,11etu		
16: 14	REP_CNT1	When Parity selection is wrong, the times of automatic repeat request 000:0time 001:1time 010:2times 011:3times 100:4times 101:5times 110:6times 111:7times	R/W	011
13	RXPAR_ESEL1	Receive data parity error handling mode selection 1: Parity check is wrong, According to T = 0 protocol, error signal will be post back, RX_PAR_ERR flag bit will be set and generate the interrupt. 0: Parity check is wrong, do not send error signal, RX_PAR_ERR flag bit will be set, generate the interrupt.	R/W	1
12:11	ERRWTH1	Width selection bit of the error signal 00:2 etu 01:1 etu 10:1.5 etu 11:2 etu	R/W	01
10:8	PARSEL1	Parity select bit 000:No parity 001:Odd 010:Even 011:Fixed to zero check 100: Fixed to one check Other: Reserved	R/W	010
7	BGT_EN1	BGT control bit between data transmission and reception 0:Disable BGT function, do not insert the BGT between data reception and transmission 1:Enable BGT function, insert the BGT between data reception to transmission	R/W	0
6	ERR_IRQ_EN1	Transmit error interrupt flag, Data conflicts when data is	R/W	0

		transmitting, Data overflow when data is receiving and the received data frame is error 0:Disable the interrupt when data transmission is error 1:Enable the interrupt when data transmission is error		
5	RX_IRQ_EN1	Receive interrupt flag, data transfer from shift registers to receive buffer registers 0:Disable data reception interrupt to generate 1:Enable data reception interrupt to generate	R/W	0
4	TX_IRQ_EN1	Transmit interrupt flag, set by hardware after completion of a serial transfer from shift registers 0:Disable the interrupt between data transmission 1:Enable the interrupt between data transmission	R/W	0
3	RX_EN1	Receive data enable 0:Disable receive data 1:Enable receive data	R/W	0
2	TX_EN1	Transmit data enable 0:Disable transmit data 1:Enable transmit data	R/W	0
1	DIRSEL1	Data coding mode selection bit 0:LSB first pass that is positive logic data coding method 1:MSB first pass negative logic data coding method(negate values)	R/W	0
0	EN1	ISO7816 Controller flag 0:Disable the controller 1:Enable the controller	R/W	0

- ISO7816_CLK(0x08)

Table 15-5 ISO7816 Clock Control Register1 ISO7816_CLK

Bit	Name	Descriptions	R/W	Reset Value
31:4	---	Reserved	R	0
3	CLKO_EN	Card clock output flag 0:Disable card clock output 1:Enable card clock output	R/W	0
2:0	CLKDIV	ISO7816 Divider factor of clock output(CLK_O) ISO7816 source clock of module gain from fsyspll of system clock 000:No frequency division;001:2 frequency division; 010:4 frequency division; 011:8 frequency division; 100:16 frequency division 101:32 frequency division; 110:64 frequency division; 111:128 frequency division;	R/W	0

- ISO7816 Baud rate coefficient 0 Register(0x0c)

Table 15-6 ISO7816 Baud rate coefficient 0 Register ISO7816_BDDIV0

Bit	Name	Descriptions	R/W	Reset Value
31:22	---	Reserved	R	0

21	FDS0_EN	Enable soft configuration coefficient of F/D 1:Baud rate coefficient will be determined by FDS0 which is written by software 0:Baud rate coefficient will be determined by FD0	R/W	0
20:8	FDS0	Baud rate coefficient which are configured by software, this bit can be written only when FDS0_EN is 1,In other cases,it is13'd372.	R/W	13'd372
7:0	FD0	8bit FI and DI is transmitted from answer to reset	R/W	8'h01

- ISO7816 Baud rate coefficient1 Registers(0x10)

Table 15-7 ISO7816 Baud rate coefficient1 Registers ISO7816_BDDIV1

Bit	Name	Descriptions	R/W	Reset Value
31:22	---	Reserved	R	0
21	FDS0_EN	Enable soft configuration coefficient of F/D 1:Baud rate coefficient will be determined by FDS0 which is written by software 0:Baud rate coefficient will be determined by FD0	R/W	0
20:8	FDS0	Baud rate coefficient which are configured by software, this bit can be written only when FDS0_EN is 1, In other cases, it is13'd372.	R/W	13'd372
7:0	FD0	8bit FI and DI is transmitted from answer to reset	R/W	8'h01

- ISO7816 State 0 Registers(0x14)

Table 15-8 ISO7816 State 0 Registers ISO7816_ STAT0

Bit	Name	Descriptions	R/W	Reset Value
31:12	---	Reserved	R	0
11	FRAME_ERR0	Receive data frame format error interrupt flag this bit will be reset by writing '1' 1: Send the error frame format error of receiving data , it will generate the interrupt when transmission error interrupt is enable 0:Unsent the error frame format error of receiving data	R/W	0
10	BDDIV_R0	Baud rate matching instruction, the matching instructions between FI and DI,FD default is 8'h01,clock matching, it will be set as 1 when FD unmatched. 1:matched 0:unmatched	R	1
9	TX_FLAG0	Transmit data buffer empty flag. It automatic set after power-on reset, And it shows Buffer is empty and can be written.. The flag will be automatically cleared after MCU is written. After shift data from transmit buffer registers to shift registers, this bit will be set as 1 1:Data transmit buffer is empty 0:The data transmit buffer has data to be transmitted	R	1
8	RX_FLAG0	Data buffer full flag,7816 Interface controller receives every bit data, hardware automatic clear settings, it shows Interface controller receives 1 bit data, Reading data receive buffer register will be reset. 1:1 byte data is received, data buffer is full	R	0

		0:There is no data received, data buffer is empty		
7	RXBUSY0	Reception data busy flag. Set by hardware, reset by software Hardware automatic clear settings 0:Receive data idle 1:RSR are receiving data, it will be set as 1 after start bit is received, it will automatic clear zero after stop bit is received	R	0
6	TXBUSY0	Transmit data busy flag. Set by hardware, reset by software Hardware automatic clear settings 0:Transmit data idle 1:TXSHF are sending data, it will be set as 1 after start bit is send, it will automatic clear zero after stop bit is send	R	0
5	TXPAR_ERRIF0	Send data parity error flag, there is still parity error after retry, then this bit is turned on. this bit will be reset by writing '1' 1:Parity error occurred when data is transmitted. 0:Parity error didn’t occur when data is transmitted.	R/W	0
4	RXPAR_ERRIF0	Receive data parity error flag bit, there is still parity error after retry, then this bit is turned on. this bit will be reset by writing '1' 1:Parity error occurred when receiving data is received 0:Parity error didn’t occur when data is received	R/W	0
3	COL_IF0	Send data conflict error interrupt flag. Set by hardware, reset by software, this bit will be reset by writing '1' 0:No interrupt 1:Interrupt occurs	R/W	0
2	OVL_IF0	Receive data overflow flags. Set by hardware, reset by software this bit will be reset by writing '1' 0:No overflow 1:Interrupt occurs, The receive buffer register didn’t be read, and received the new data. Overflow flag bit is enable	R/W	0
1	RXIF0	Transmit data interrupt flag bit. After shift data from shift registers to transmit buffer registers, it will be set as 1. Set by hardware, reset by software this bit will be reset by writing '1' 0:No interrupt 1:Interrupt occurs	R/W	0
0	TXIF0	Transmit data interrupt flag. After move data from send buffer registers to shift registers, it will be set as 1,Set by hardware, reset by software, this bit will be reset by writing '1' 0:No interrupts 1:Interrupt occurs	R/W	0

- ISO7816 Status 1 Registers(0x18)

Table 15-9 ISO7816 Status 1 Registers ISO7816_ STAT1

Bit	Name	Descriptions	R/W	Reset

				Value
31:14	---	Reserved	R	0
13	CARD_OUT_FLAG	This bit is Effective, after CARD_CHECK_EN enabled. this bit will be reset by writing '1'. 1:Detected card was uprooted(the width of high level pulse of input port is more than 40mS) 0:Pulling out the card is not detected(the width of high level pulse of input port is not more than 40mS)	R	0
12	OLD_FLAG	After OLD_EN enabled, this bit is Effective, To match the received RA9105 signal of OLD interrupt flag bit, this bit will be reset by writing '1'. 1:OLD signal has been received. 0:OLD signal hasn't been received.	R/W	0
11	FRAME_ERR0	Receive data overflow flag, this bit will be reset by writing '1' 1:Send received data frame format error, Interrupt occurs when the transmit error interrupt is enabled 0:Unsent received data frame format error	R/W	0
10	BDDIV_R1	Baud rate matching direction, FI and DI matching direction; FD defaults to 8'h01,clock matching, it will be set as 1 when FD unmatched. 1:matched 0:unmatched	R	1
9	TX_FLAG1	Send Buffer empty flag. It automatic setting after power-on reset, And it shows Buffer is empty, and it can be written. The flag will be automatically clean after MCU is written, After move data from send buffer registers to shift registers, this bit will be set as 1 1:Buffer is empty 0:There is data which are ready to send in the buffer	R	1
8	RX_FLAG1	The data reception complete flag,7816 Interface receives every bit data, receiver channel generate the interrupt. Set by hardware, reading data receiving buffer register clean. Interface controller receives every bit data, Hardware automatic Clear Settings, it shows Interface controller receives 1 bit data, Read data receiving buffer register will be reset. 1:1 byte data is received, receive data buffer is full 0:There is no data received, receive data buffer is empty	R	0
7	RXBUSY1	Receive data busy flag. Hardware set, reset by software Hardware automatic clear settings 0:Data reception go idle 1:RSR are receiving data, it will be set as 1 after start bit is received, it will automatic clear zero after stop bit is received	R	0
6	TXBUSY1	Transmit data busy flag. Hardware set, reset by software Hardware automatic Clear Settings 0:Data transmission go idle	R	0

		1:TXSHF are sending data, it will be set as 1 after start bit is transmitted, it will automatic clear zero after stop bit is transmitted		
5	TXPAR_ERRIF1	Transmit data parity error flag bit. Hardware set, reset by software this bit will be reset by writing '1' 1:Parity error occurred data is transmitted 0:Parity error didn't occur data is transmitted	R	0
4	RXPAR_ERRIF1	Receive data parity error flag bit. Hardware set, reset by software this bit will be reset by writing '1'. 1:Parity error occurred data is received 0:Parity error didn't occur data received	R/W	0
3	COL_IF1	Send data conflict error interrupt flag bit. set by hardware, reset by software this bit will be reset by writing '1' 0:No interrupts 1:Interrupt occurs	R/W	0
2	OVL_IF1	Receive data overflow flag bit .Set by hardware, reset by software this bit will be reset by writing '1' 0:There is no overflow 1:Interrupt occurs, The receive buffer register don't be read, and received the new data. Overflow flag bit is enable	R/W	0
1	RXIF1	Receive data interrupts flags bit. After move data from shift registers to send buffer registers ,it will be set as 1,Set by hardware, reset by software this bit will be reset by writing '1' 0:No interrupts 1:Interrupt occurs	R/W	0
0	TXIF1	Sending data interrupts flag bit. After move data from send buffer registers to shift registers, it will be set as 1.Set by hardware, reset by software this bit will be reset by writing '1' 0:No interrupts 1:Interrupt occurs	R/W	0

- ISO7816 Data Register0(0x1C)

Table 15-10 ISO7816 Data Register0 ISO7816_ DAT0

Bit	Name	Descriptions	R/W	Reset Value
Reserved	--	--	R	0
8	DATA0[8]	It is PARITY bit of data frames,when parsel is in User-defined mode	R/W	0
7:0	DAT0	Data Register0	R/W	0

- ISO7816 Data Register1(0x20)

Table 15-11 ISO7816 Data Register1 ISO7816_ DAT1

Bit	Name	Descriptions	R/W	Reset

				Value
Reserved	--	--	R	0
8	DATA1[8]	It is PARITY bit of data frames,when parsel is in User-defined mode	R/W	0
7:0	DAT1	Data Register1	R/W	0

16 IIC Interface

A n I2C Interface embedded in Soc.

16.1 Overview

The controller of I2C Interface have the following features:

Master and slave mode were supported;

7-bit address were supported

Many types of the divider setting were supported;

100kbps and fast mode(400kbps) were supported;

16.2 Register Descriptions

Table 16-1 I^2C register address

Module Name	Physical Address	Mapping Address
I^2C	0x40024000	0x40024000

Table 16-2 I^2C register offset address

Register	Address Offset	Descriptions
I^2C_CTL	0x0	Control Register
I^2C_CLK	0x4	Clock configuration registers
I^2C_STAT	0x8	Status Register
I^2C_ADDR	0xC	Slave device address Register
I^2C_DATA	0x10	Transmits and receives data Register

- Control Register(0x0)

Table 16-3 Control Register I^2C_CTL

Bit	Name	Descriptions	R/W	Reset Value
31:6	---	Reserved	R	0
5	MODE	MASTER/SLAVE 1:MASTER 0:SLAVE	R/W	0
4	ACK	ACK sending enable 1: After received the signal of the ninth SCL, generate ACK 0:After received the signal of the ninth SCL, don't generate ACK	R/W	0
3	IRQE	I^2C interrupt enable 0:Disable interrupt	R/W	0

		1:Enable interrupt		
2:1	BUSCON	A bus control bit, start command is effective when bus is idle or host is posted. Start command is effective when host is posted When timing of the stop or start is detected, command bit will be clear 00:no action 01:Producing the time for START 10:Producing the time for STOP 11:Reserved	R/W	0
0	EN	Module enable 1:Enable I2C 0:Disable I2C	R/W	0

- Clock configuration register(0x4)

Table 16-4 Clock configuration register I²C_ CLK

<table>
<tr><th>Bit</th><th>Name</th><th>Descriptions</th><th>R/W</th><th>Reset Value</th></tr>
<tr><td>31:3</td><td>---</td><td>Reserved</td><td>R</td><td>0</td></tr>
<tr><td>2:0</td><td>CLKDIV</td><td>I2C clock separate frequency parameters selection bit:
I2C calculating formula for communication clock rate:
SCL=APBCLK/m, there into m produced by CLKDIV, shown in the table below. It generated High-speed mode or Normal-mode communication clock according to different System frequency and Separate frequency parameters.
If configuration option is not in the table below, it defaults to divide-by-ten.
<table>
<tr><td>System frequency</td><td colspan="2">Separate frequency parameters /CLKDIV(m)</td></tr>
<tr><td></td><td>High-speed mode</td><td>Normal-mode</td></tr>
<tr><td>1.8432Mhz</td><td>000(6)</td><td>010(20)</td></tr>
<tr><td>3.6864Mhz</td><td>001(10)</td><td>011(38)</td></tr>
<tr><td>7.3728Mhz</td><td>010(20)</td><td>100(76)</td></tr>
<tr><td>14.7456Mhz</td><td>011(38)</td><td>101(152)</td></tr>
<tr><td>29.4912Mhz</td><td>100(76)</td><td>110(304)</td></tr>
</table></td><td>R/W</td><td>001</td></tr>
</table>

- Status describing register(0x8)

Table 16-5 Status describing register I2C_ STAT

Bit	Name	Descriptions	R/W	Reset Value
31:9	---	Reserved	R	0
8	DIR	Direction of Reading or writing flag 1:Write. 0:Read.	R	0

7	MATCH	Address matching, When timing of the stop or start is detected, command bit will be clear 0:Address mismatch 1:Address matching	R	0
6	BUSY	Traffic Status flag 0:IIC is idle 1:IIC is busy	R	0
5	COL	Sending conflict interrupt. this bit will be reset by writing '1' Sending data register is not empty or When receiving data, user write new data to data register. Trigger sending interrupt flag 0:No trigger send conflict interrupt 1:Trigger send conflict interrupt	R/W	0
4	OVERF	Receive overflow interrupt flag. this bit will be reset by writing '1' When receiving data, a new data is received before previous data don't be took away, Trigger overflow interrupt flag 0:No trigger overflow interrupt 1:Trigger overflow interrupt	R/W	0
3	TXEMPT	Sending data register is empty error flag. this bit will be reset by writing '1' In slave mode, the host asked slave to send data ,when send buffer is empty, trigger send data is empty error interrupt flag 0:No trigger send data is empty error interrupt 1:Trigger send data is empty error interrupt	R/W	0
2	TRANC	Transfer complete interrupt flag. this bit will be reset by writing '1' When sending data, send buffer is empty , or when receiving data , receive buffer is full. Trigger transfer complete interrupt flag 0:Transfer has not been completed 1:Transfer has been completed	R/W	0
1	RX_NACK	Received NACK interrupt flag. this bit will be reset by writing '1' 1:Received NACK 0:No NACK was received	R/W	0
0	STPD	STOP time sequence inspection interrupt flag. this bit will be reset by writing '1' When timing of the start is detected or module is power off, this bit will be clear 0:No STOP timing detected	R/W	0

		1:Detect STOP timing		

- Slave device address register(0xC)

Table 16-6 Slave device address register I^2C_ ADDR

Bit	Name	Descriptions	R/W	Reset Value
31:8	---	Reserved	R	0
7:1	SADR	Device address, it can not be written during the transport address. In host mode, it is slave device address; In slave mode, this address is used to compare with address which host send.	R/W	0
0	RW	Direction of Reading or writing of host flag 0:write 1:read	R/W	0

- Send/receive data register(0x10)

Table 16-7 Send/receive data register I2C_ DATA

Bit	Name	Descriptions	R/W	Reset Value
31:8	---	Reserved	R	0
7:0	TRDAT	Send/receive data	R/W	0

17 SPI Interface

Soc has **an in-built SPI Interface.**

RN8211 **nonsupport SPI Interface.**

17.1 Overview

The controller of SPI Interface have the following features:

Full-duplex mode of SPI were supported;

master / slave mode were supported

Setting the clock polarity and phase were supported;

Send and receive independent double buffer were supported;

Transfer mode of LSB and MSB can be 8bit or 16 bit or 32bit

256 kinds of baud rate can be set, up to 3.6864MHz;

Complete interrupt of data transmission were supported;

Conflict interruption of data transmission were supported;

Error interruption of SCSN mode were supported;

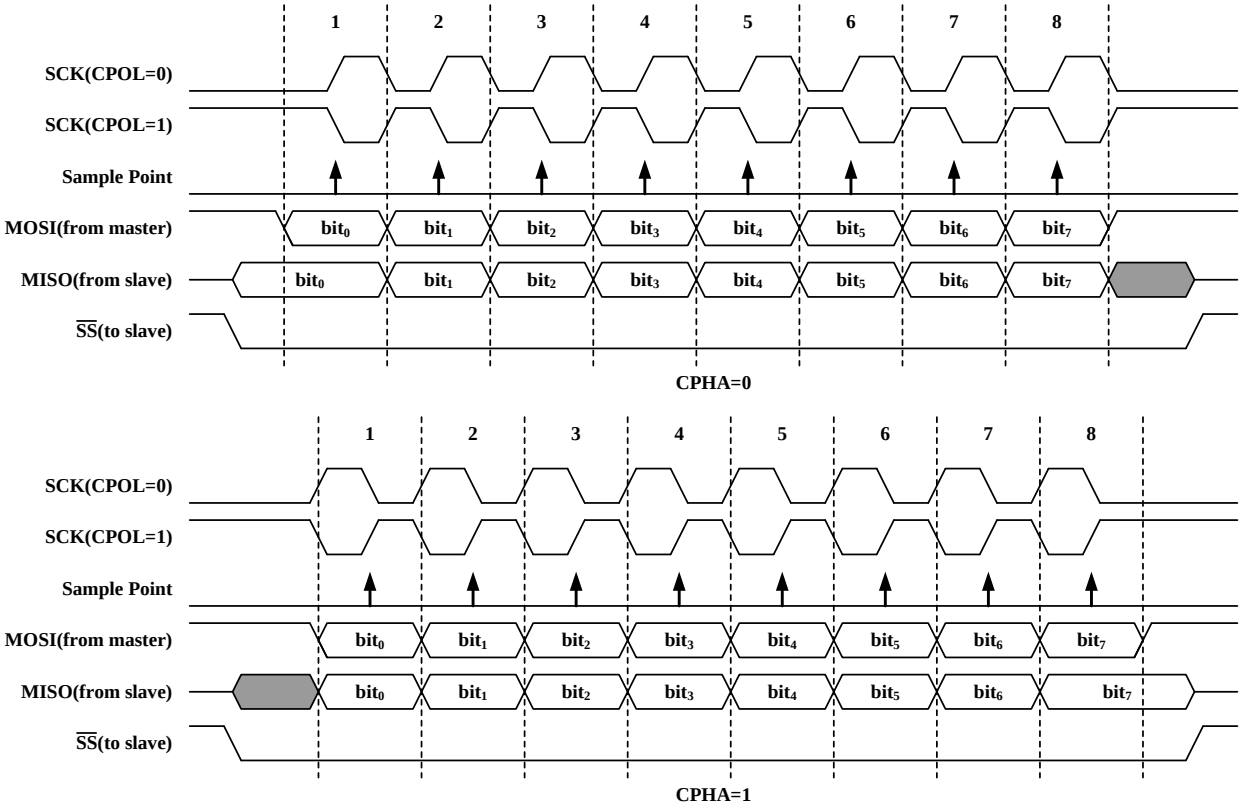
17.2 Descriptions of Functions

SPI Interface meets the SPI HOST protocol standard, SPI clock mode is depending on the setting of CPOL(Clock Polarity) and CPHA(Clock Phase) parameter:CPOL shows front edge seat of clock is positive edge or negative edge, CPHA shows front edge seat of clock is data sampling or data setup.

Detailed working mode is as follows Table:

Table 17-1 SPI clock mode

Table14-2 SPI clock mode



SPI MODE	CPOL/CPHA	Front edge seat	Rear edge
0	**0/0**	positive edge**,** data sampling	negative edge**,** data setup
1	**0/1**	positive edge**,** data setup	negative edge**,** data sampling
2	**1/0**	negative edge**,** data sampling	positive edge**,** data setup
3	**1/1**	negative edge**,** data setup	positive edge**,** data sampling

The width of the data transmission can be 8bit or 16 bit or 32bit,SPI clock source from the system clock, generate the communication clock After a divider coefficient.

Support data transmission interrupt conflicts, data reception overflow interrupt , transmission end interrupt and SS mode error interrupt other four interrupts.

Send data conflicts, when data is transmitting (txbusy 1), then there is a write command , then TXCOLIF set as 1.

If COL_IRQ_EN=1, interrupt occurs, meanwhile this send command wouldn't be response, the data which is sending will transferred over.

Receive data overflow: Before the data over which to receive don't enter into shifting register,RXDATA register is not read, data overflow will generate ,RXCOLIF will be set as 1,if COL_IRQ_EN=1,interrupt occurs, meanwhile new receiving data will be save into receive data register,the old data will be overwritten.

End Of transmission interrupt:End Of transmission(sck_end),if TR_IRQ_EN=1,interrupt occurs, meanwhile, TRIF will be set as 1.

SCSN mode error interrupt: In the slave mode, SCSN must be input, When data is transmitted, SCSN become high, SCSN mode error flag will be set as 1;In the host mode, only enable the host model SCSN error detection(SCSN_EN=1),meanwhile SCSN is low, SCSN mode error flag will be set as 1. When SCSN mode error flag is 1, transmission is terminated, SOI module is reset, if ERR_IRQ_EN=1, interrupt occurs.

17.3 Register Descriptions

Table 17-2 SPI register address

modules	physical address	mapping address
UART0	0x40020000	0x40020000

Table 17-3 SPI register offset address

Register	Address Offset	Descriptions
SPI_CTL	0x0	Control Register
SPI_STAT	0x4	Status Register
SPI_TXDATA	0x8	Transmit Data Register
SPI_RXDATA	0xC	Data Receive Register

- Control Register(0x0)

Table 17-4 SPI Control Register SPI_CTL

Bit	Name	Descriptions	R/W	Reset Value
31:22	---	Reserved	R	0
21	TX_DMA_EN	Sends request of DMA 1:Enable request of DMA 0:Disable request of DMA	R/W	0
20	RX_DMA_EN	Receive request of DMA 1:Enable request of DMA 0:Disable request of DMA	R/W	0
19:12	CLKDIV	SCK clock division factor SCK frequency=system clock frequency/(2*(CLKDIV + 1))	R/W	0
11:10	WIDTH	Data width selection 0:8bit 1:16bit 2:32bit 3:Reserved,8bit	R/W	0
9	SCSN_EN	SCSN model error detection enable, Works only in the master mode 0:Disable SCSN model error detection in the master mode, SCSN is GPIO 1:Enable SCSN model error detection in the master mode ,SCSN as the input of SPI	R/W	0
8	CPHA	Clock phase selection 0:Former edge sampling data 1:Former edge data is established	R/W	0
7	CPOL	Clock polarity selection 0:“SCK” will be set as low, when idle 1:“SCK” will be set as high, when idle	R/W	0
6	LMSB	LSB/MSB selection 0:MSB is transferred first 1:LSB is transferred first	R/W	0
5	TXCOL_IRQ_EN	Data conflict interrupt enable 0:Disable write conflict interrupt 1:Enable write conflict interrupt	R/W	0

4	RXCOL_IRQ_EN	Data conflict interrupt enable 0:Disable read conflict interrupt 1:Enable read conflict interrupt	R/W	0
3	ERR_IRQ_EN	SCSN mode error interrupt enable 0:Disable mode error interrupt 1:Enable mode error interrupt	R/W	0
2	TR_IRQ_EN	Data transmission interrupt enable 0:Disable transmit data interrupt 1:Enable transmit data interrupt	R/W	0
1	MAST/SLAV	MASTER/SLAVE 1:MASTER 0:SLAVE	R/W	1
0	EN	Enable 0:Disable SPI Interface 1:Enable SPI Interface	R/W	0

- Status Register(0x4)

Table 17-5 SPI Status Register SPI_ STAT

Bit	Name	Descriptions	R/W	Reset Value
31:5	---	Reserved	R	0
4	TXBUSY	Sending data busy state flag. 0:Sending data is idle, bus can write command of SPITX register 1:Data is sending, bus can not write command of SPITX register	R	0
3	TXCOLIF	Write conflict flag. this bit will be reset by writing '1' When data is sending (TXBUSY is 1), user write new sending data to SPI, then new sending data will be lost. Write conflict flag will be set as 1. 0:No write data conflict interrupt 1:Generate the interrupt of write data conflict	R/W	0
2	RXCOLIF	Receiving data overflow flag. this bit will be reset by writing '1' When receiving data in a row, if user don't read RXDATA register, generate the receiving data overflow 0:No receiving data overflow interrupt 1:Generatethe receiving data overflow interrupt	R/W	0
1	ERRIF	SCSN mode conflict interrupt flag bit: when SPI is in host mode, only when SCSN_EN is 1,meanwhile"SCSN"is low, this bit will be set as 1;when SPI is in slave mode, "SCSN" as slave input, When the data was transmitted, if "SCSN" is high, this bit will be set as 1;if ERR_IRQ_EN=1,interrupt occurs, if generate the mode conflict, SPI module will be reset. this bit will be reset by writing '1' 0:No mode conflict interrupt	R/W	0

		1:Generatethe mode conflict interrupt		
0	TRIF	Sending data interrupt flag bit, When the data transfer is finished, this bit will be set as 1,if TR_IRQ_EN=1,interrupt occurs, this bit will be reset by writing '1' 0:No sending data interrupt 1:Generatethe sending data interrupt, send data register is empty.	R/W	0

- Transmit Data Register(0x8)

Table 17-6 SPI Transmit Data Register SPI_ TXDATA

Bit	Name	Descriptions	R/W	Reset Value
31:0	TXDATA	Transmit Data Register	R/W	0

- Data Receive Register(0xC)

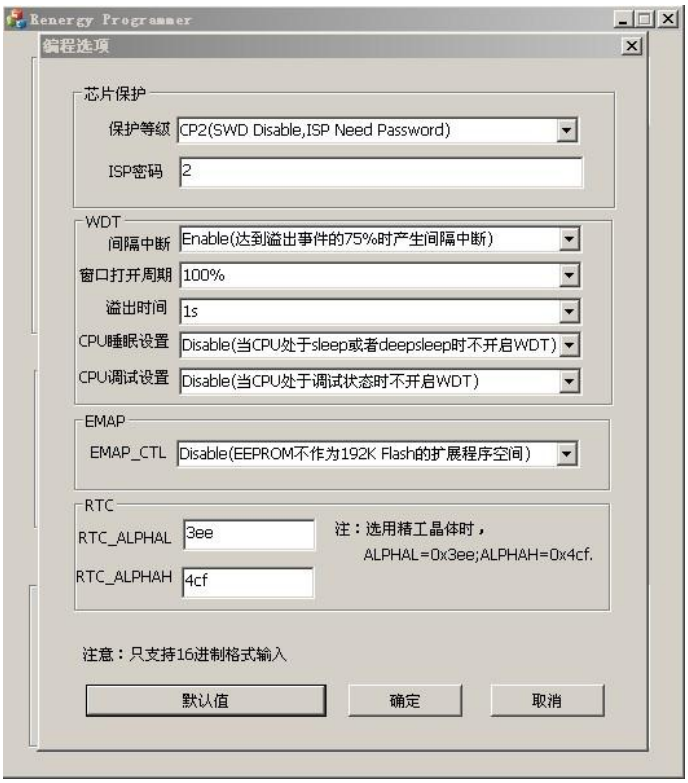
Table 17-7 SPI Data Receive Register SPI_ RXDATA

Bit	Name	Descriptions	R/W	Reset Value
31:0	RXDATA	Data Receive Register	R	0

18 Option Byte

RN821x built in an area of option byte, when the chip is reset, it will automatically configuration option byte and perform specific function. It include protection of the chip, WDT, EMAP and RTC setting.

Programming of option byte can be setting by the programming tool from Renergy (MINIPRO programming unit or ISP programming tools),What an example to MINIPRO programming unit,open the dialog, you can set option byte, As shown in the figure(Please see the detailed operation method from “MINIPRO instruction manual of programming unit”).



18.1 Chip Protection Settings

Protect function of option byte can protect built-in Flash/EEPROM of RN821x,user can protect the chip by protection lever setting and ISP password setting. The following protection levels are provided:

Protection level	Name	description
0	CP0	Without any protection(no password is required for ISP access)
1	CP1	SWD Interface can access chip, password is required for ISP access
2	CP2	Disable access chip by SWD Interface, password is required for ISP access
3	CP3	Disable access chip by SWD and ISP Interface(ISP only have the function of the whole erase FLASH(Erase operation will reduce the protection level to CP0 in CP3)

18.2 WDT Setting

Option byte provide interval interrupt of WDT, window open cycle, overflow time, CPU sleep setting, CPU debug setting, See detailed meaning on the section of WDT. As shown in the table below:

Name	Description	default
Interval interrupt	0:Disable(Disable interrupt of intervals) 1:Enable(When reaches 75% of the spills, interval interrupt occurs)	0
Window open cycle	0:25% 1:50% 2:75% 3:100% During the window open, write 0xBB to WDTE register, watchdog reset and count again; During the window close, write 0xBB to WDTE register, The internal reset signal generate.	3
Overflow time	0:16ms 1:32ms 2:128ms 3:512ms 4:1s 5:2s 6:4s 7:8s	4
CPU sleep setting	0:Disable(When CPU is sleep or deepsleep, WDT is off) 1:Enable(When CPU is sleep or deepsleep, WDT is on)	0
CPU debug setting	0:Disable(When CPU in a state of commissioning , WDT is off) 1:Enable(When CPU in a state of commissioning, WDT is on) Notes: When CPU in a state of commissioning, it show user stop Cortex M0	0

	by debug interface (PC pointer stop counting).	

18.3 EMAP Setting

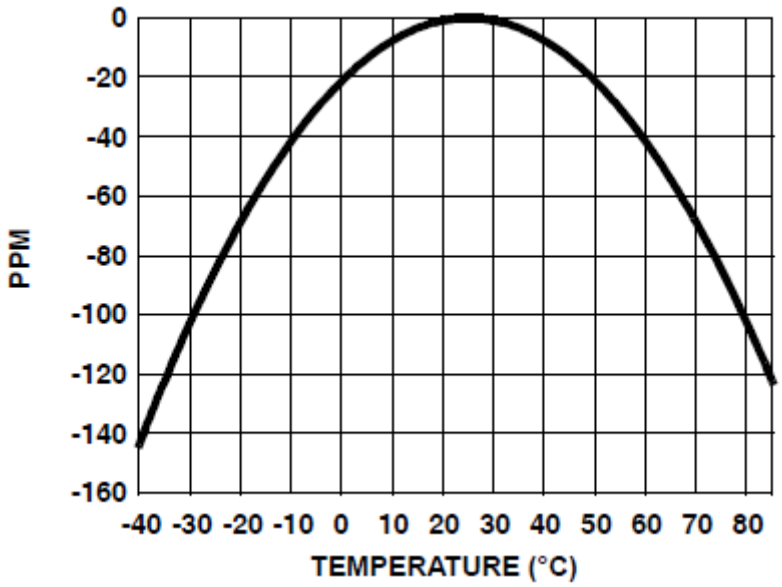
In order to support a program space more than 192 KB,RN821X(RN8215 can support setting of EMAP. but RN8211/RN8213 can not)set 32K EEPROM as program space of 192K Flash by option byte. If select EEPROM as program space of 192K Flash. The program space of RN821X may be extended to 224KB.Read address of EEPROM was right behind FLASH,Begin with 0x30000(REMAP=0x0).

18.4 RTC Setting

With temperature compensation ,the RTC of RN821X can make a automatic compensation to the 32K crystal , so it can provide the exact second pulse in the range of -25℃～70℃.

Among them, the temperature frequency curve of the crystal as shown below, is the vertex of a quadratic curve 25 degrees (f=f0-alpha*(T-T0)), T0 is 25 degrees). However, The alpha of quadratic curve is different between the high temperature section (25 ℃ ~ 85 ℃) and low-temperature (-25 ℃ ~ 70 ℃), so the option bytes provide separately the parameter RTC_ALPHAL and RTC_ALPHAH ,Each of them is filled with round (alpha * 32768) ,which means rounding operation.

If the choice is high consistency crystals (VT-200-F) provided by Seiko, then ALPHAL = 0x3ee, ALPHAH = 0x4cf.



19 Programming Support

SoC support the built-in programming of the internal EEPROM and FLASH .

We recommend that customers can call our library functions to achieve IAP function and use our programmer to complete the ISP function.

19.1 Overview

SoC programming system has the following features:

◎ Built in the FLASH / EEPROM content protection mechanisms

◎ Supports ISP programming mode;
◎ Support IAP programming mode;
◎ Support downloads recording mode by SWD;
◎ support volume production recording mode;

19.2 Flash/EEPROM Protection Mechanisms

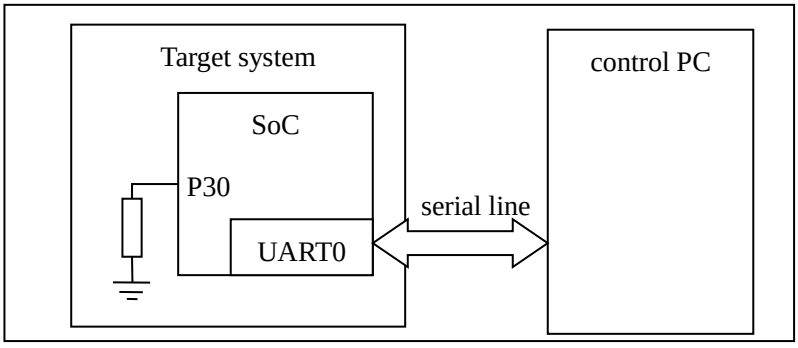
EEPROM protection is to allow users to enable different levels of security to restrict the access to the on-chip Flash and EEPROM. Protection mechanisms protect the different level of protection in the following table. Users can set chip protection class by set the “option byte”.

Table 19-1 The protection level of SoC

Protection level	Name	description
0	CP0	Without any protection(no password is required for ISP access)
1	CP1	SWD Interface can access chip,password is required for ISP access
2	CP2	Disable access chip by SWD Interface,password is required for ISP access
3	CP3	Disable access chip by SWD and ISP Interface(ISP only have the function of the whole erase FLASH(Erase operation will reduce the protection level to CP0 in CP3)

19.3 In System Programming(ISP)

The user can pull P30 signal to low, and reset the SoC, let SoC into the ISP mode. ISP mode of connection diagram as shown in figure 18-1 Table 18-1 ISP hardware configuration diagram



ISP major process:

According to the connection diagram configuration and connect the target system and control host;
Reset the target system;
Control host configuration of serial port for a start bit, 8 data bits, 1 stop bit;
Control the host to send “?”;
The target system response “Synchnonized /r/n”;
Control the host to send “Synchnonized /r/n”;
The target system response “7373(1843)/r/n”;(If the current system frequency is 7.3728M,send 7373;If the current system frequency is1.8432M,send 1843)

Control host can perform the corresponding ISP commands according to need;

19.3.1 ISP Communications Protocol

All command of ISP send in the form of a ASCII text. Text use (/r) or (/n)as end mark.

All ISP response is < CR > < LF > the end of the ASCII string sent.

The data were sent and received in the original format (not converted to ASCII) .

- Command format

command parameter0 parameter1 ... parametern/r/n

{DATA}

- command format

return code/r/n

response 0/r/n

response 1/r/n

...

Response /r/n

{DATA}

- data format

After starting the orders of WM and RM, the data transmission of ISP will start up. The data transmits in a unit of line, and the maximum of 32 bit data in a line is 16(If the number of the data less than 16, the actual number will be sent); When each a block data is transmitted (the maximum line of one block is 32, and if the line number less than 32, the actual number will be sent), a check line will be sent, which is the .

When RN821X received a complete block of data, the data will be verified. If the check is passed, send a "OK / r / n" command; If the validation is error or the data packets is illegal , then sent a "RS / r / n" command. If the programmer receives “RS/r/n” command, you need to re-send the Block data.

Data transmission format:

When the row data is 0x7e, it means 0x7d, 0x5e sent; When the row data is 0x7d, it means 0x7d, 0x5d sent

Data line format: (B behalf transmit data Byte, hexadecimal)

Table 19-2 ISP data transmission format

The first row	**1**	**2**	**3**	**4**	**5**	**6**	**……**	**64**	**65**	**The last row**
0x7e	Num	B0	B1	B2	B3	B4	……	B62	B63	0x7e

Correction line format:(ASCII code. S represent the cumulative checksum SUM)

Table 19-3 ISP data validation format

The first row	**1**	**2**	**3**	**4**	**5**	**The last row**
0x7e	0xff	S0	S1	S2	S3	0x7e

19.3.2 The Used Resources

ISP uses the RAM within the range 0x10001000 to 0x10002800 on chip, Stack is located at the top of RAM. Flash, EEPROM can use the RAM within the scope 0x10000000-0x10001000 (4KB) for programming.

19.3.3 ISP Command

Each ISP commands support specific status code. When receive the undefined command, command processor to send the return code

INVALID_COMMAND.

Command and return code is ASCII format. Only when receives the ISP command execution is completed, the ISP command processor will send CMD SUCCESS, the host can send a new ISP commands.

ISP command can be divided into three types:

1. Normal command:Only under the CP0,or CP1,CP2 and password is right,it can be access
2. UN command Under the CP0,CP1,CP2 level of protection(password does not provide),it can be access
3. In any case, FC,AL command can access

Table 19-4 ISP command

Command	**Instruction**	**Nature**
Baud rate setting	BS <Baud rate> <stop bit>	Normal command
Echo	RD <switch settings>	Normal command
Write memory	WM <Address> <Byte size> <Mode>	Normal command
Read memory	RM <Address> <Byte size> <Mode>	Normal command
Flash page erase	FP <Page address>	Normal command
Flash block erase	FS <Block address>	Normal command
Flash chip erase	FC	Special commands
Flash block blank check	FQ <Block address>	Normal command
EEPROM page erase	EP <Page address>	Normal command
EEPROM block erase	ES <Block address>	Normal command
EEPROM chip erase	EC	Normal command
EEPROM block blank check	EQ <Block address>	Normal command
FLASH Programming	FW <FLASH address> <RAM address> <Byte size>	Normal command
EEPROM Programming	EW <EEPROM address> <RAM address> <Byte size>	Normal command
Chip ID	ID	Normal command
Read ISP version	VE	Normal command
Memory compare	MC <Address1> <Address2> <Byte size>	Normal command
Running	GO <Address>	Normal command
Unlock	UN <password>	Special commands
Access to confidential level	AL	Special commands
Enable PFPM	PM <switch settings>	Normal command
Reset by software	RS	Normal command
Enable NVM(FLASH/EEPROM)	NV <NVM option>	Normal command

- Baud rate setting

Table 19-5 ISP Baud rate setting command

Command	**BS** <Baud rate> **<stop bit>**

Input	Baud rate:9600 or 19200 or 38400 or 57600 or 115200 Stop bit:1 or 2
Return code	CMD_SUCCESS or INVALID_BAUD_RATE or INVALID_STOP_BIT or INVALID_PARAM
Annotation	Change ISP communication serial frame format, Including baud rate and stop bit. Serial port start bit is 1,data bit is 8.New frame format is effective After return CMD SUCCESSS.
Example	"BS 9600 2"Serial port baud rate will be set as 9600bps,two stop bit.

- Echo

Table 19-6 ISP Echo command

Command	**RD <switch settings>**
Return code	CMD_SUCCESS or INVALID_PARAM
Annotation	Command and data echo. Default is on. When echo on,SoC send command and data which to receive back to host.
Example	"RD 0"echo off.

- Write memory

Table 19-7 ISP Write memory command

Command	**WM** <Address> <Byte size> <mode>
Input	Address: address to start, it should be 32 bits; Byte size: the number of bytes, must be in multiples of four; mode:0 as a serial port,1 as parallel
Return code	CMD_SUCCESS or FM_MODE_ERROR or ADDR_NOT_ALIGN or COUNT_ERROR or COUNT_ERROR or ADDR_NOT_MAPPED or INVALID_PARAM
Annotation	Write data to SRAM
Example	"WM 268436224 4 0" "78" "56" "34" "12" Write 0x12345678 to address 0x10000300 via a serial port

- Read memory

Table 19-8 ISP Read memory command

Command	**RM <Address> <Byte size> <Mode>**
Input	Address: address to read, it should be 32 bits; Byte size: To compare the number of bytes, must be in multiples of four; mode:0 as a serial port,1 as parallel
Return code	CMD_SUCCESS or FM_MODE_ERROR or ADDR_NOT_ALIGN or COUNT_ERROR or COUNT_ERROR or ADDR_NOT_MAPPED or INVALID_PARAM
Annotation	Read the content of SARM of SoC
Example	"RM 268436224 4 0"Read the content which SRAM address is 0x10000300 via a serial port

- Flash page erase

Table 19-9 ISP Flash page erase command

Command	**FP <Page address>(FPGA version is 0 to 3071)**
Input	Page address: Optional between 0 to 1535;
Return code	CMD_SUCCESS or INVALID_PAGE or INVALID_PARAM
Annotation	Erase the content of the specify page of Flash of SoC
Example	“ES 1”Erase the content of the page 1

- Flash block erase

Table 19-10 ISP Flash block erase command

Command	**FS <Block address>**
Input	**Block address**: Optional between 0 to 47;
Return code	CMD_SUCCESS or INVALID_SECTOR or INVALID_PARAM
Annotation	Erase the content of the specify block of EEPROM of SoC
Example	“FS 0”Erase the content of the block 0

- Flash chip erase

Table 19-11 ISP Flash chip erase command

Command	**FC**
Input	NC
Return code	CMD_SUCCESS or INVALID_PARAM
Annotation	Erase all the content of Flash of SOC.
Example	“FC” erase all the content of Flash.

- Flash block blank check

Table 19-12 ISP Flash block blank check command

Command	**FQ <Block address>**
Input	**Block address**: Optional between 0 to 47;
Return code	CMD_SUCCESS or INVALID_SECTOR or INVALID_PARAM
Annotation	Check if the content of the specify block of EEPROM is empty(Unprogrammed after erase it)
Example	“FQ 1”Check if the content of the 1 block is empty

- EEPROM page erase command

Table 19-13 ISP EEPROM page erase command

Command	**EP <Page address>**
Input	**Page address**: Optional between 0 to 511; (FPGA version is 0 to 1023)
Return code	CMD_SUCCESS or INVALID_PAGE or INVALID_PARAM
Annotation	Erase the content of the specify page of EEPROM of SoC
Example	“ES 1”Erase the content of the page 1

- EEPROM block erase

Table 19-14 ISP EEPROM block erase command

Command	**ES <Block address>**
Input	**Block address**: Optional between 0 to 7;(FPGA version is 0 to 15)
Return code	CMD_SUCCESS or INVALID_SECTOR or INVALID_PARAM
Annotation	Erase the content of the specify block of EEPROM of SoC

Example	“ES 1”Erase the content of the block 1

- EEPROM page erase

Table 19-15 ISP EEPROM page erase command

Command	**EC**
Input	NC
Return code	CMD_SUCCESS or INVALID_PARAM
Annotation	Erase all the content of the block of FLASH of SoC. This command will remove key and the protection level settings, The chip will be set back to factory state.
Example	“EC” Erase all the content of the block of EEPROM.

- EEPROM block blank check

Table 19-16 ISP EEPROM block blank check command

Command	**EQ** <block **address**>
Input	Page address: Optional between 0 to 7;(FPGA version is 0 to 15)
Return code	CMD_SUCCESS or INVALID_SECTOR or INVALID_PARAM
Annotation	Check if the content of the specify block of EEPROM is empty(Unprogrammed after erase it)
Example	“EQ 1”Check if the content of the 1 block is empty

- Flash Programming

Table 19-17 ISP Flash program command

Command	**FW <FLASH address> <RAM address> <Byte size>**
Input	FLASH address: target address of FLASH to write RAM address: the SRAM address of source buffer Byte size: the number of bytes written(If Byte size is different from number of bytes of Flash page, the rest of this Flash will be set as 0
Return code	CMD_SUCCESS or COUNT_ERROR or SRC_ADDR_NOT_ALIGN or SRC_ADDR_NOT_MAPPED or DST_ADDR_NOT_ALIGN or DST_ADDR_NOT_MAPPED or INVALID_PARAM
Annotation	It is used to program FLASH.
Example	“FW 0 268436224 128”copy 128 bytes data which SRAM address is 0x10000300 to FLASH address 0.

- EEPROM Programming

Table 19-18 ISP EEPROM programming command

Command	**EP <EEPROM address> <RAM address> <Byte size>**
Input	EEPROM address: target address of FLASH/EEPROM to write SRAM address: the SRAM address of source buffer Byte size: the number of bytes written
Return code	CMD_SUCCESS or COUNT_ERROR or SRC_ADDR_NOT_MAPPED or DST_ADDR_NOT_MAPPED or INVALID_PARAM
Annotation	It is used to program EEPROM.

- Chip ID

Table 19-19 ISP ID of chip command

Command	**ID**

Input	NC
Return code	CMD_SUCCESS or INVALID_PARAM
Annotation	Return ID of chip
Example	“ID” will return“9103”

- Read ISP version

Table 19-20 ISP Read ISP version command

Command	**VE**
Input	NC
Return code	CMD_SUCCESS or INVALID_PARAM
Annotation	Return ISP version
Example	“VE” will return“1.0”

- Memory compare

Table 19-21 ISP memory compare command

Command	**MC <Address1> <Address2> <byte size>**
Input	Address1(DST):Starting address of to compare the memory region 1 ,it should be with the word alignment; Address2(SRC):Starting address of to compare the memory region 2 ,it should be with the word alignment; Byte size: To compare the number of bytes, must be in multiples of four;
Return code	CMD_SUCCESS or COUNT_ERROR or SRC_ADDR_NOT_ALIGN or SRC_ADDR_NOT_MAPPED or DST_ADDR_NOT_ALIGN or DST_ADDR_NOT_MAPPED or COMPARE_ERROR or INVALID_PARAM
Annotation	This command is used to compare the content of the two regions of memory.
Example	“MC 268436224 268436224 4”Compare 4 bytes data which SRAM address is 0x10000300 with 4 bytes data which SRAM address is 0x10000300

- Running

Table 19-22 ISP Running command

Command	**GO** <Address>
Input	Address: Address of Code execution start Flash or RAM . This address must be Thumb address
Return code	CMD_SUCCESS or ADDR_NOT_THUMB or ADDR_NOT_MAPPED or INVALID_PARAM
Annotation	This command is used to execute the program in RAM or Flash .Once successfully execute the command, it could no longer return to the ISP command handler.
Example	“GO 5”Jump to address 0 x00000004 to execute

- Unlocked

Table 19-23 ISP unlocked command

Command	**UN**
Input	Password:32bit Hexadecimal number
Return code	CMD_SUCCESS or INVALID_PASS or INVALID_PARAM

Annotation	This command is used to unlock ISP.
Example	“UN 567”Enter the password 567 to unlock the ISP

- Access to confidential level

Table 19-24 ISP access to confidential level command

Command	**AL**
Input	NC
Return code	CMD_SUCCESS or INVALID_PARAM
Annotation	This command is used to access to confidential level of ISP
Example	“AL”will return confidential level of SoC

- Enable PFPM

Table 19-25 ISP Enable PFPM command

Command	**PM <switch settings>**
Input	switch settings:0(OFF)or 1(ON)
Return code	CMD_SUCCESS or INVALID_PARAM
Annotation	This command enable/disable PFPM(parallel programming pattern)
Example	“PM 1”enable PFPM

- Reset by software

Table 19-26 ISP System reset command

Command	**RS**
Input	NC
Return code	CMD_SUCCESS or INVALID_PARAM
Annotation	This command enable reset by software
Example	“RS” will enable reset by software

- Enable NVM

Table 19-27 ISP Enable NVM command

Command	**NV <NVM option>**
Input	NVM option:0(Flash)or 1(EEPROM)
Return code	CMD_SUCCESS or INVALID_PARAM
Annotation	This command enable Flash or EEPROM
Example	“NV 0”Enable Flash write, programming.

19.3.4 ISP Return Code

Table 19-25 ISP return code

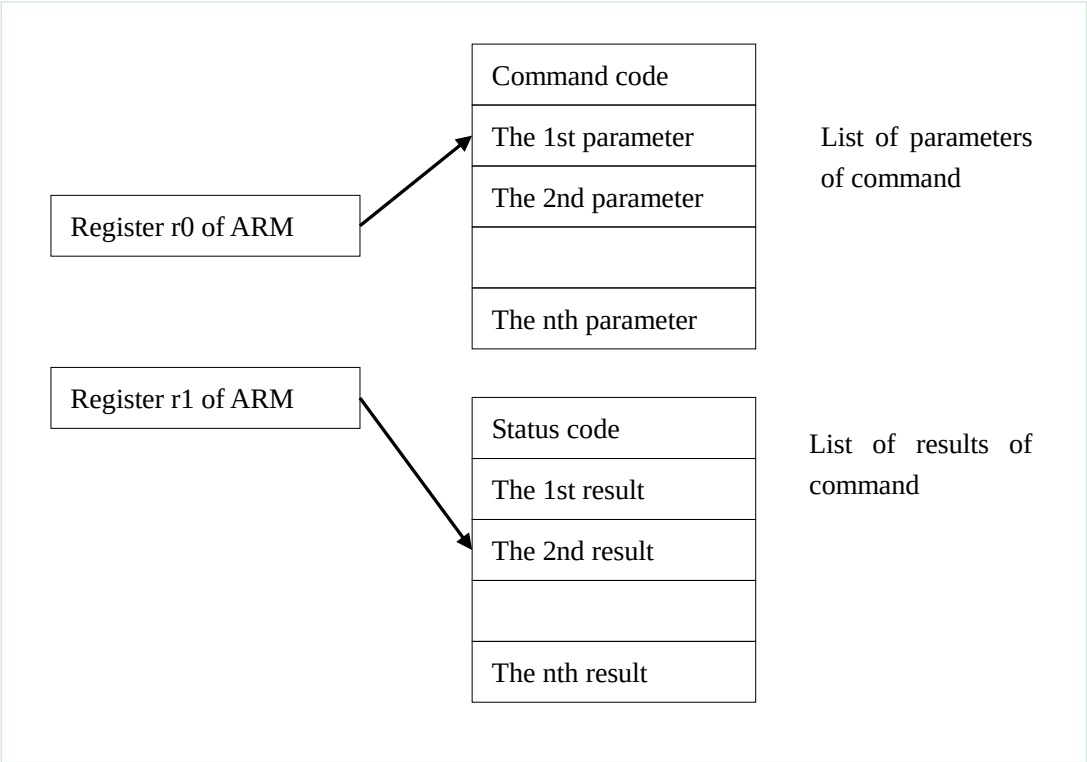
Return code(ASCII code)	**Mark**	**Description**
0	CMD_SUCCESS	Successfully executed command. Only after successfully executed command, ISP will send this code

1	INVALID_COMMAND	Invalid command
2	INVALID_PARAM	Invalid parameter(ASCII of parameter is not 0-9)
3	INVALID_BAUD_RATE	Invalid baud rate
4	INVALID_STOP_BIT	Invalid stop bit
5	ADDR_NOT_ALIGN	Address is not for boundary with byte
6	COUNT_ERROR	Byte count is not in multiples of four
7	ADDR_NOT_MAPPED	Address have space of crossing the line
8	INVALID_SECTOR/INVALID_PAGE	Invalid SECTOR_NUM or PAGE_NUM
9	SECTOR _NOT_BLANK	SECTOR is not empty
10	SRC_ADDR_NOT_ALIGN	Source address is not for boundary with byte
11	SRC_ADDR_NOT_MAPPED	Source address have space of crossing the line
12	DST_ADDR_NOT_ALIGN	Destination address is not for boundary with byte
13	DST_ADDR_NOT_MAPPED	Destination address have space of crossing the line
14	COMPARE_ERROR	Contrast Error
15	FM_MODE_ERROR	Memory model error
16	ADDR_NOT_THUMB	The address is not Thumb command
17	INVALID_PASS	Wrong password

19.4 In-Application Programming (IAP)

About In-Application Programming, we should call programs of IAP by word pointer in the register r0,The word pointer point to RAM that contains the command code and parameters. Result of IAP command return to results table which register r1 is pointing to. User can give the same value to pointer in the register r0 and r1, so we can reuse the command table to hold the result. Parameter table should be big enough to save all the result. About parameter passing , please see table 18-2.The number of parameters and the results depend on IAP command.“Flash programming”, “EEPROM programming” The maximum number of for command parameters, the number of result is 1.Command processor send status code(INVALID_COMMAND) after receive an undefined command. Program of IAP is Thumb code, address is 0x1800_1c01.

Figure 19-2 IAP parameter passing



19.4.1 IAP Command

Table 19-26 IAP command

IAP command	Command code	Instructions
Flash page erase	0x50	See the section of ISP
Flash block erase	0x51	See the section of ISP
Flash chip erase	0x52	See the section of ISP
Flash block blank check	0x53	See the section of ISP
EEPROM page erase	0x54	See the section of ISP
EEPROM block erase	0x55	See the section of ISP
EEPROM chip erase	0x56	See the section of ISP
EEPROM block blank check	0x57	See the section of ISP
Flash programme	0x58	See the section of ISP
EEPROM programme	0x59	See the section of ISP
Enable NVM	0x5a	See the section of ISP
Analog reset by software	0x5b	See the section of ISP

19.4.2 IAP Instructions

IAP is use as follows:

Online Updater (update FLASH);

Customer information (power)update(update EEPROM);

When online upgrade, it need to erase or write Flash. It will last about 4 ms to erase Flash, Increase processing delays about the interrupt.

An implementation method of the IAP:

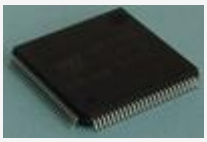
When the user needs to online upgrade, he needs to add a procedures section of IAP upgrade with software. This

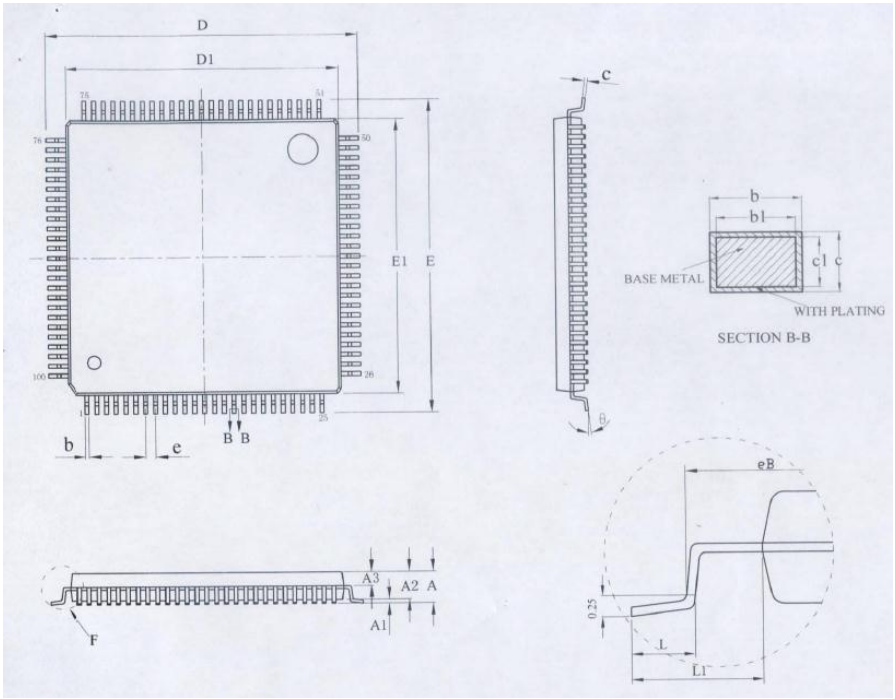
program is used to receive programs or data from remote host by the communication port (example UART). By IAP Interface SOC supplied. These programs or data is written to EEPROM or FLASH in the SOC.

19.5 Production Platform

Renergy provides a variety of programming methods, Specific elaborate can refer to “RN821x_RN831x Application Notes and Instructions of 008-programming platform”.

20 Package Size

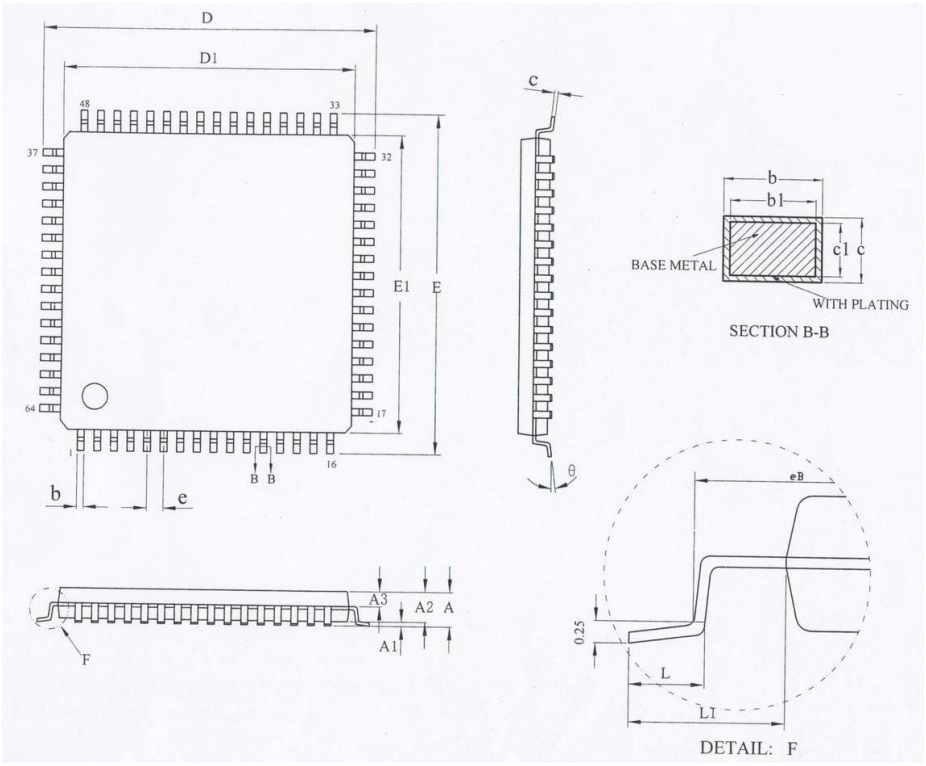
LQFP100L (1414×1.4)		14.00×14.00×1.40	e=0.50



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	---	1.6
A1	0.05	---	0.20
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.19	---	0.27
b1	0.18	0.20	0.23
c	0.13	---	0.18
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20

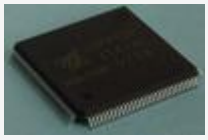
E1	13.90	14.00	14.10
eB	15.05	---	15.35
e	0.50BSC		
L	0.45	---	0.75
L1	1.00BSC		
θ	0	-----	7°

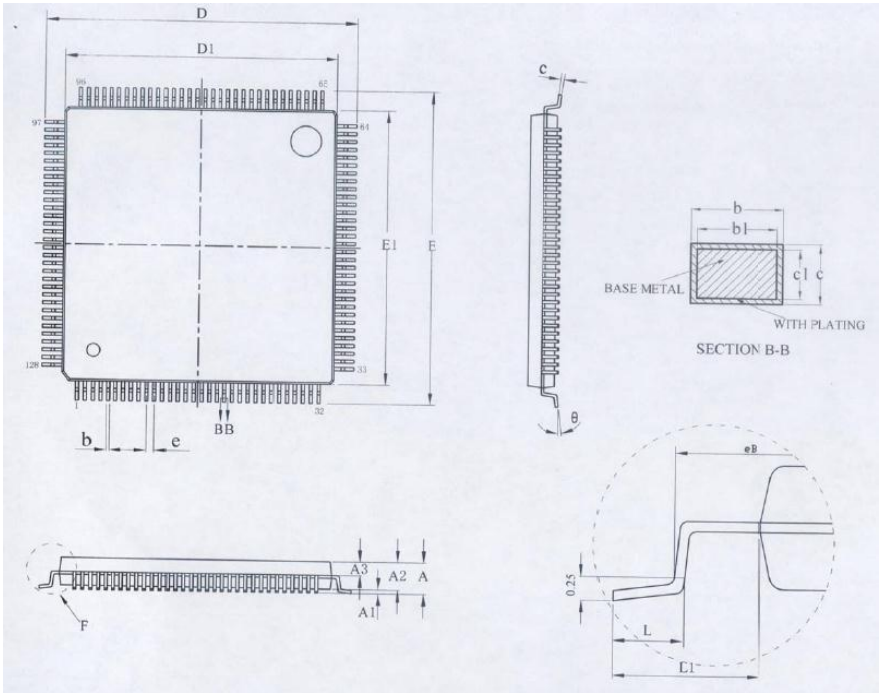
LQFP64L (0707×1.4)		7.00×7.00×1.40	e=0. 40



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	---	1.6
A1	0.05	---	0.20
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	---	0.25
b1	0.16	0.18	0.20
c	0.13	---	0.18
c1	0.12	0.127	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10

E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	---	8.25
e	0.40BSC		
L	0.40	---	0.65
L1	1.00BSC		
θ	0	-----	7°

LQFP128L (1414×1.4)		14.00×14.00×1.40	e=0.40



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	---	1.6
A1	0.05	---	0.20
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.15	---	0.23
b1	0.14	0.16	0.19
c	0.13	---	0.18
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20

E1	13.90	14.00	14.10
eB	15.05	---	15.35
e	0.40BSC		
L	0.45	---	0.75
L1	1.00BSC		
θ	0	-----	7°

21 Package Information

Line1: Company Trademark
Line2: Corporate name
Line3: Product Name
Line4: Product Lot number
The Product Lot number consists of 10 characters including number and letter.

The 1st character shows the wafer out year, showed by numbers 1 to 9 and letters which A indicates 2010 and the like, pls see details in follower “Year Code Table”.

The 2nd character shows the wafer out month, showed by numbers 1 to 9 and letters which A indicates 10 and the like, pls see details in follower “Month Code Table”.

The 3rd to 5th characters show the serial number of wafer lot (begin with 001 and increase by one).

The 6th character is reserved.

The 7th and 8th characters shows the chip packaging company and production line.

The 9th character shows the month for chip packaging, showed by numbers 1 to 9 and letters which A indicates 10 and the like, pls see details in follower “Month Code Table”.

The 10th character shows the date for chip packaging, showed by numbers 1 to 9 and letters which A indicates 10 and the like, pls see details in follower “Date Code Table”.

Lower left quarter: PIN1 flag

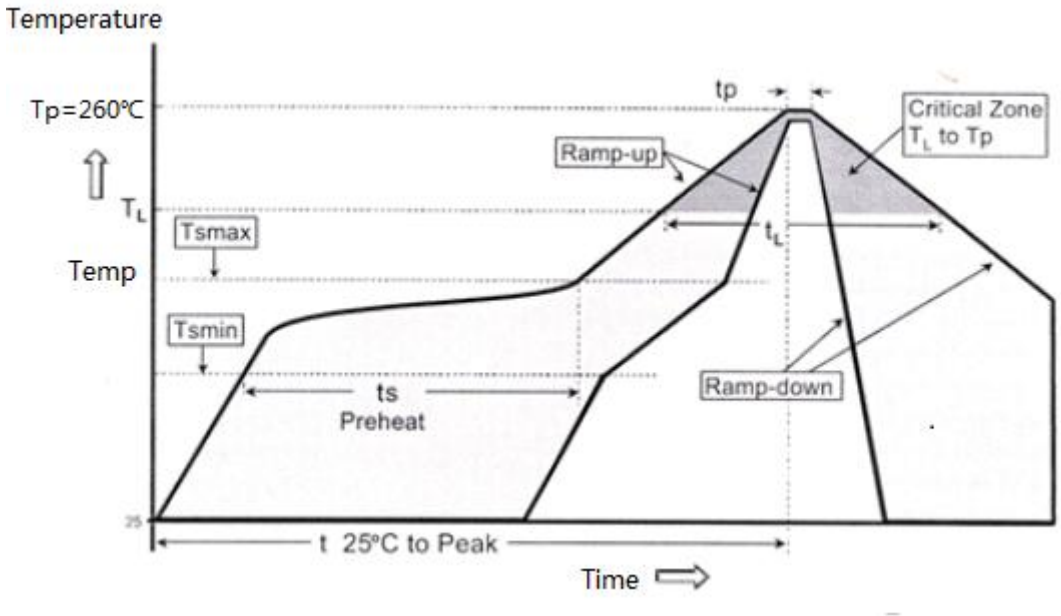
Year Code Table										
Year	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
Code	1	2	3	4	5	6	7	8	9	A
Year	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020

Code	B	C	D	E	F	G	H	J	K	L
Year	2021	2022	2023	2024	2025	2026	2027	2028	2029	
Code	M	N	P	R	S	T	U	V	W	

Month Code Table											
Month	1	2	3	4	5	6	7	8	9	10	11	12
Code	1	2	3	4	5	6	7	8	9	A	B	C

Date Code Table										
Date	1	2	3	4	5	6	7	8	9	10
Code	1	2	3	4	5	6	7	8	9	A
Date	11	12	13	14	15	16	17	18	19	20
Code	B	C	D	E	F	G	H	J	K	L
Date	21	22	23	24	25	26	27	28	29	30
Code	M	N	P	R	S	T	U	V	W	X
Date	31									
Code	Y									

22 Temperature Setting Conditions of SMT



parameter	value
TL Tp (TL to Tp)	217℃ 260℃ Max 3℃/second
 Ts min Ts max Time（max-min）（ts）	 150℃ 200℃ 60-180 second
Ts max - (Ts max to TL)	Max 3℃/ second