Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

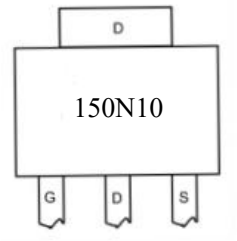
Bvdss	Rdson	ID
100V	3.3mΩ	150A

Application

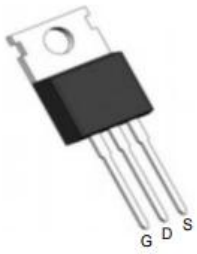
RoHS

- DC-DC Converters
- Power management function
- Synchronous-rectification applications

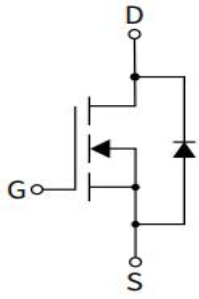
Package



Marking and pin assignment



TO220 top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
150N10	S150N10T	TO220	50

Absolute Maximum Ratings (T_C=25℃unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{Gs}	±20	V
Continuous Drain Current	I_D@T_C = 25℃	I_D	150	A
V_{GS}@10V[1,6]	I_D@T_C = 100℃	I_D	96	A
Pulsed Drain Current[2]		I_{DM}	619	A
Single Pulsed Avalanche Energy[3]		E_{As}	726	mJ
Avalanche Current		I_{AS}	150	A
Power Dissipation[4]	T_C = 25℃	P_D	312	W
Junction Temperature		T_J	-55~+150	℃
Storage Temperature		T_{STG}	-55~+150	℃

Thermal Resistance Ratings

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-ambient[1]	$R_{\theta JA}$	55	℃/W
Thermal Resistance Junction-Case[1]	$R_{\theta JC}$	0.6	℃/W

Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HLS150N10T	TO220	1	2	3	Tube

Electrical Characteristics (T_j=25℃unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V	100	-	-	V
Static Drain-Source On-Resistance[2]	$R_{DS(on)}$	V_{GS} = 10V, I_D = 20A	-	3.3	3.8	mΩ
		V_{GS} = 4.5V, I_D = 10A	-	-	-	
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS} , I_D =250uA	2	3	4	V
Drain-Source Leakage Current	I_{DSS}	V_{DS} = 80V, V_{GS} = 0V T_J = 25°C	-	-	1.0	μA
		V_{DS} = 80V, V_{GS} = 0V T_J = 55°C	-	-	5.0	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V , V_{DS}=0V	-	-	±100	nA
Forward Transconductance	gfs	V_{DS} = 5V, I_D = 20A	-	50	-	S
Gate Resistance	Rg	V_{GS} = 0V, V_{DS}= 0V, f = 1MHz	-	1.9	-	Ω
Total Gate Charge	Qg	V_{DS} = 50V, V_{GS} = 10V, I_D = 20A	-	84	-	nC
Gate Source Charge	Qgs		-	24	-	
Gate Drain Charge	Qgd		-	27	-	
Turn-ON Delay Time	$T_{d(on)}$	V_{GS} = 10V, V_{DD}= 50V I_D = 10A, R_{GEN} = 2.5Ω	-	21	-	ns
Rise Time	T_r		-	35	-	
Turn-OFF Delay Time	$T_{d(off)}$		-	49	-	
Fall Time	T_f		-	30	-	
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 50V, f = 1MHz	-	4797	-	pF
Output Capacitance	C_{oss}		-	900	-	
Reverse Transfer Capacitance	C_{rss}		-	19.1	-	
Diode Continuous Current[1,5]	I_S	V_G=V_D=0V,Force Current	-	-	150	A
Diode Forward Voltage[2]	V_{SD}	I_S = 1A, V_{GS} = 0V,T_J = 25°C	-	-	1.2	V

Notes:

1.The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3.The EAS data shows Max. rating . The test condition is TJ = 25°C, L = 3mH, IAS = 22A, VGS = 10V, VDD =

50V; 100% test at L = 0.3mH, IAS = 45A.

4.The power dissipation is limited by 150℃ junction temperature

5.The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

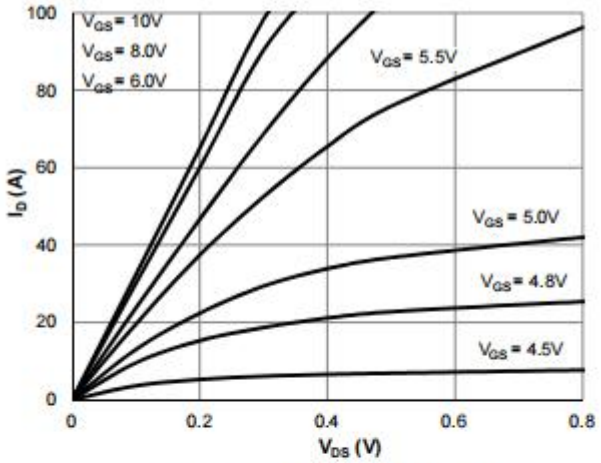


Figure 1: Saturation Characteristics

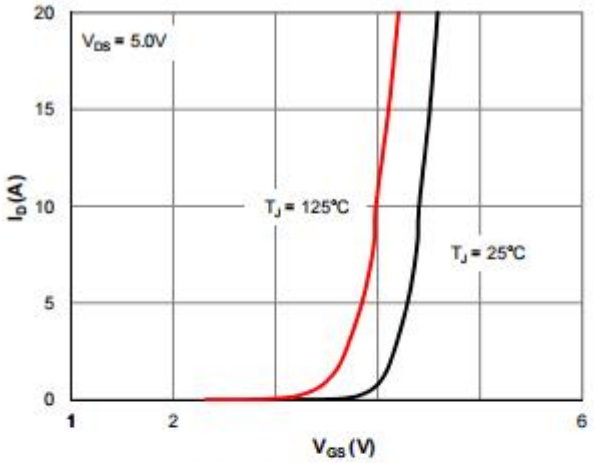


Figure 2: Transfer Characteristics

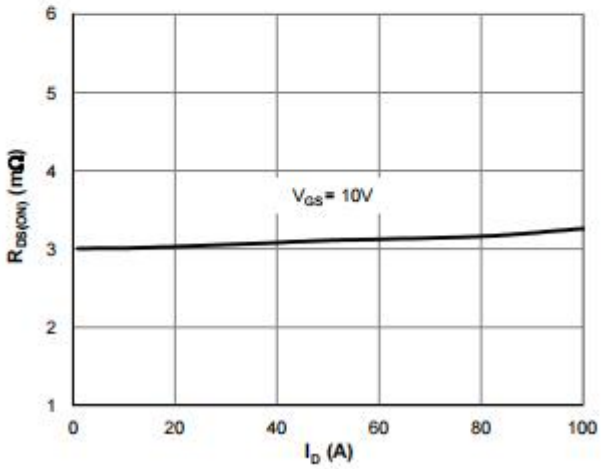


Figure 3: $R_{DS(ON)}$ vs. Drain Current

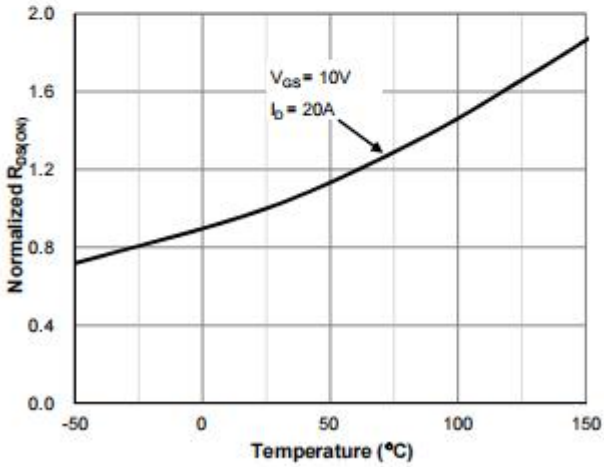


Figure 4: $R_{DS(ON)}$ vs. Junction Temperature

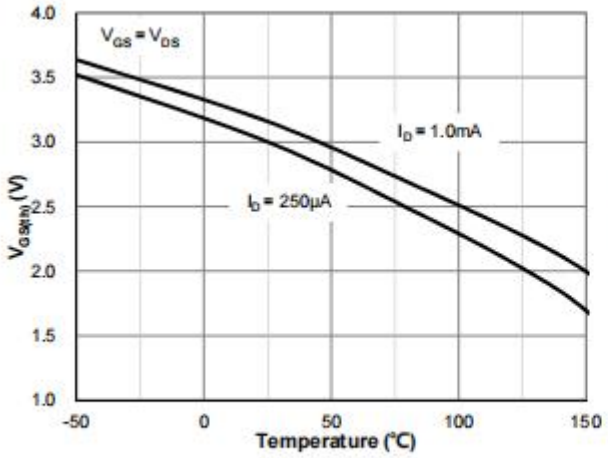


Figure 5: VGS(th) vs. Junction Temperature

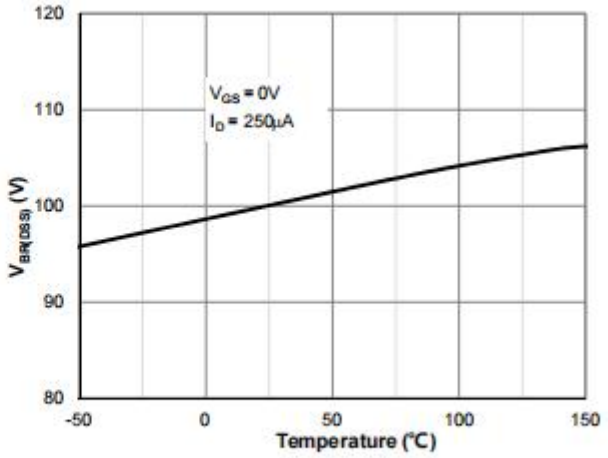


Figure 6: $V_{BR(DSS)}$ vs. Junction Temperature

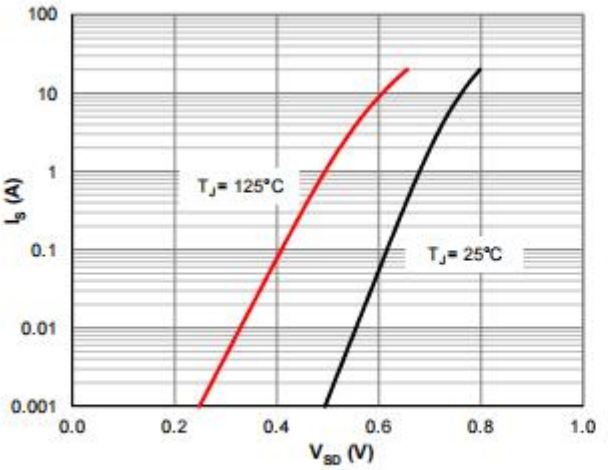


Figure 7: Body-Diode Characteristics

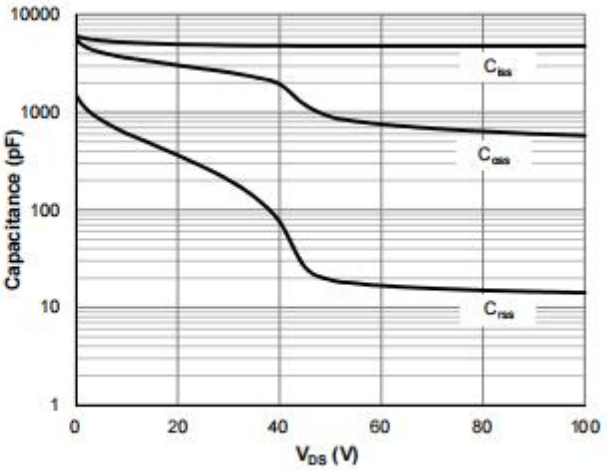


Figure 8: Capacitance Characteristics

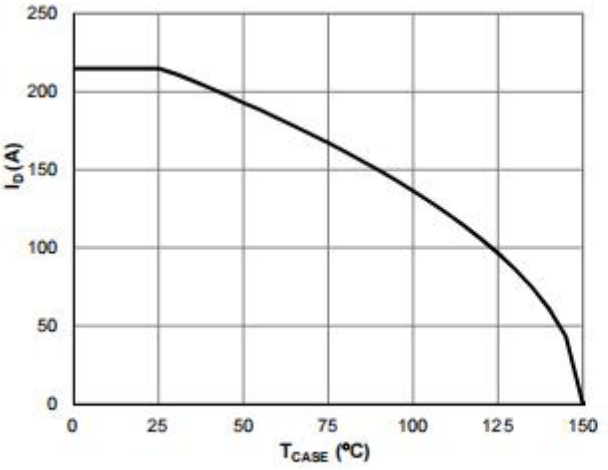


Figure 9: Current De-rating

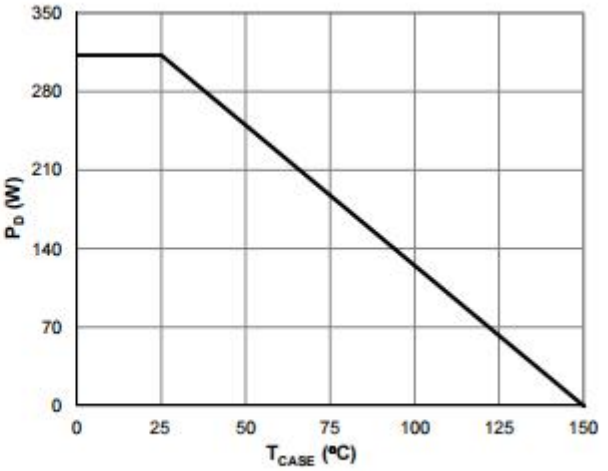


Figure 10: Power De-rating

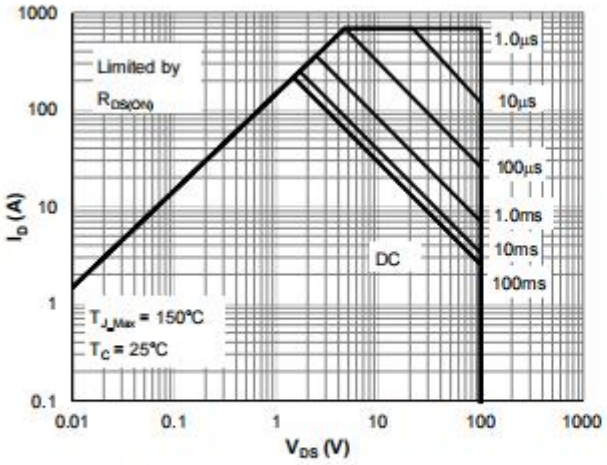


Figure 11: Maximum Safe Operating Area

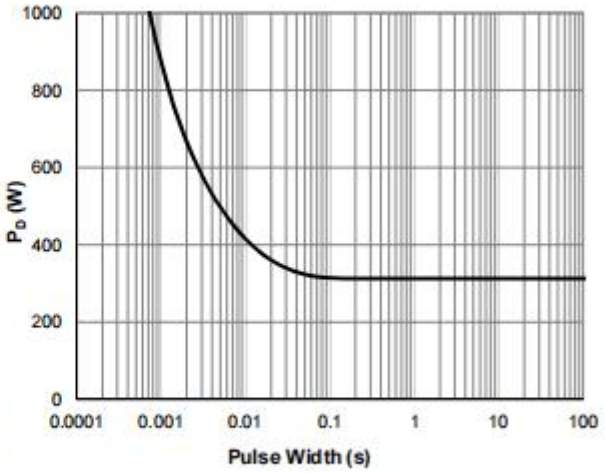


Figure 12: Single Pulse Power Rating, Junction-to-Case

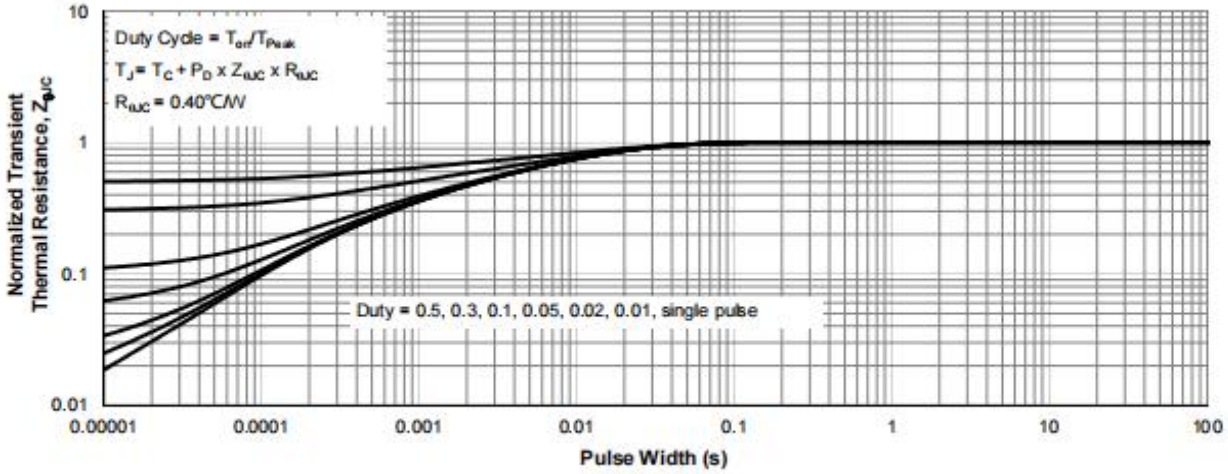
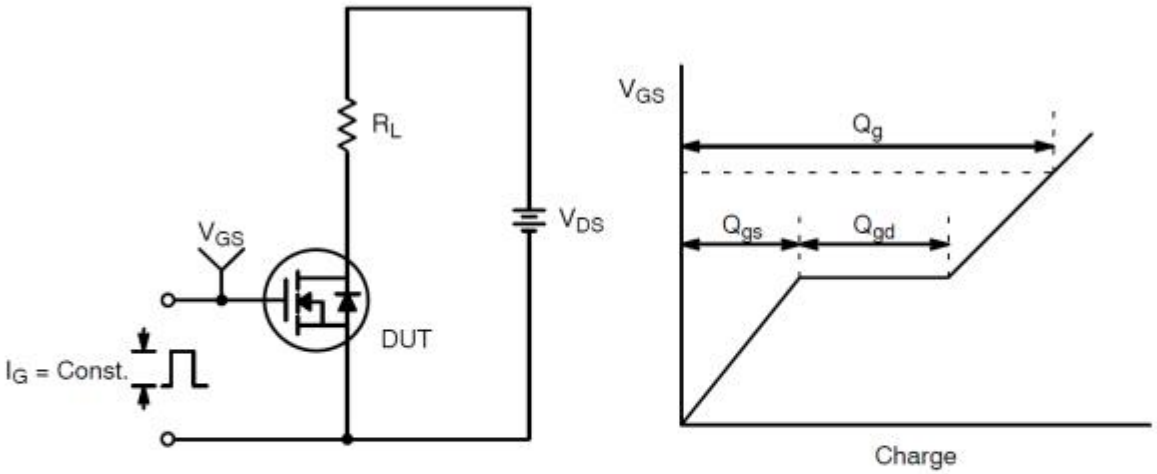
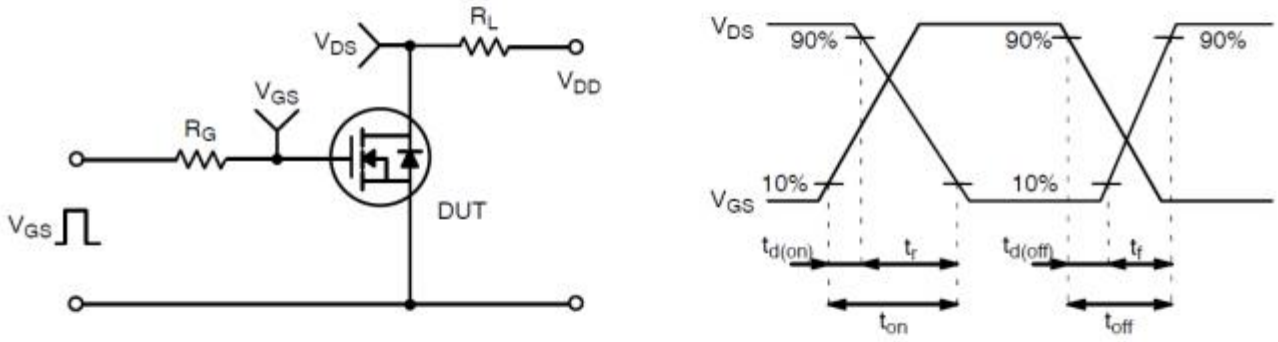


Figure 13: Normalized Maximum Transient Thermal Impedance

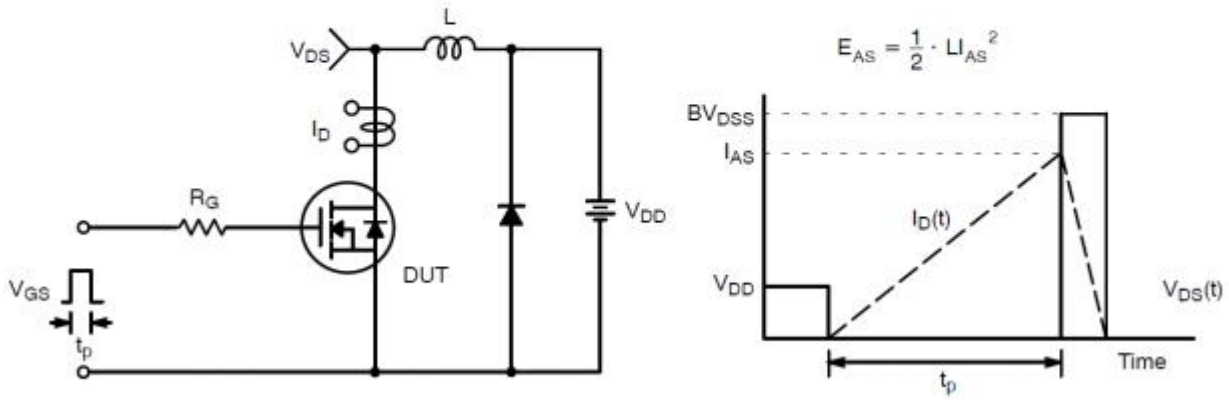
Test Circuit and Waveform



Gate Charge Test Circuit & Waveform

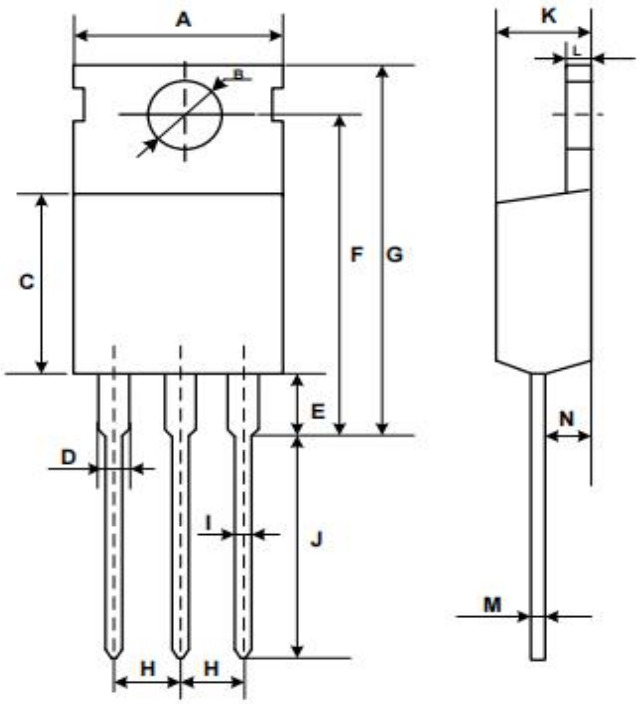


Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

Package Dimensions TO220



SYMBOL	MM	
	MIN	MAX
A	9.70	10.30
B	3.40	3.80
C	8.80	9.40
D	1.17	1.47
E	2.60	3.50
F	15.10	16.70
G	19.55MAX	
H	2.54REF	
I	0.70	0.95
J	9.35	11.00
K	4.30	4.77
L	1.20	1.45
M	0.40	0.65
N	2.20	2.60

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