Linko Semiconductor Co., Ltd.

LKS32AT089XL Datasheet

1 Overview

1.1 Function

LKS32AT089XLN8Q9 is a 32-bit MCU targeting automobile applications With the three-phase full-bridge bootstrap gate driver, it can directly drive six N-channel MOSFETs.

Features

- 96MHz 32-bit Cortex-M0 core
- Customized instruction set DSP for motor control
- Ultra low power sleep mode, 10uA sleep current with MCU low low power consumption
- Three-phase full-bridge bootstrap gate driver
- Automotive temperature range
- High ESD and group pulse reliability
- Pass AEC-Q100 Grade 1 testing certification

- **Memory**
  - 64kB Flash with optional encryption to prevent hex theft
  - 8kB RAM
- **Operating Conditions**
  - Dual power supply. The MCU is powered by 2.2V ~ 5.5V voltage(B-version chip is powered by 3.0V~5.5V),with an integrated internal LDO for the digital circuit. Drive module power supply please refer to Chapter 22.
  - When the chip uses 7-20V VCC power supply, the internal LDO can generate 5V power supply to the MCU, or power supply to the outside of the chip
  - Operating Conditions: -40~125℃
- **Clock**
  - 4MHz built-in high-precision RC oscillator, with an accuracy of ± 1% at -40 ~ 105 ℃ and ± 1.5% at -40 ~ 125 ℃
  - 32KHz built-in low-speed clock for low-power mode
  - Operating on an external 4MHz crystal is available
  - Internal PLL up to 96 MHz
- **Peripheral Modules**
  - Two UARTs
  - One SPI, support master-slave mode
  - One IIC, support master-slave mode
  - One CAN-bus, recommended to use external crystal as reference clock
  - One LIN
  - Two 16-bit standard timers (TIM), support capture and edge-aligned PWM function

- Two 32-bit standard timers (TIM), support capture and edge-aligned PWM function; support orthogonal code input, CW/CCW input, and pulse&symbol input
- Motor control PWM module, supports 8 channels/4 pairs of PWM waveform output, independent dead-band control
- Hall signal interface with speed measurement and debouncing function
- Hardware watchdog
- 4 Groups of 16bit GPIO at the most. P0.0/P0.1/P1.0/P1.1 could be used as wake-up source。
  P0.15 ~ P0.0 could be used as external IRQ source

- **Analog Modules**
  - 12bit SAR ADC, simultaneous double sampling, 3Msps sampling and conversion rate, up to 13 analog signal channels
  - Four operational amplifiers. Differential PGA mode is available.
  - Two comparators. Hysteresis mode is available.
  - 12bit digital-to-analog converter (DAC)
  - ± 2 ℃ built-in temperature sensor
  - 1.2V 0.8% built-in linear regulator
  - Low-power LDO and power monitoring circuit
  - RC oscillator with high precision and low temperature drift
  - Crystal oscillator circuits

1.2 Performance Advantages

- High reliability, high integration level, small package size, saving BOM cost;
- Integrated 4 channels high-speed OPAs and 2 channels comparators, meeting the needs of different system topology like single resistance/double resistance/three resistance current sampling;
- High-speed OPA is integrated with over-voltage protection circuit, which allows high-voltage common-mode signals to be input, which could support direct current sampling of MOSFET resistance with the simplest circuit topology.
- Via a proprietary technique, ADC and high-speed OPA could cooperate well, making them able to handle a wider current dynamic range, while ensuring the sampling precision of high-speed small current and low-speed hight current;
- The control circuit is simple and efficient, with strong anti-interference ability, stable and reliable;
- Three-phase full-bridge bootstrap gate driver is integrated;
- Supports IEC/UL60730 functional safety certification;

Applicable to control systems such as inductive BLDC/non-inductive BLDC/inductive FOC/non-inductive FOC and stepper motors, permanent magnet synchronous and asynchronous motors.

1.3 Naming Conventions

LKS32 MC 080 R 8 T 8 XX （X）

Device series

LKS32	= 32bit MCU

Product type

MC	= Motor Control Applications
AT	= Automobile Applications

Device sub family

080/081/082/ 083/085/088	= 2.2~5.5V,1 ADC,4 PGA,DSP
084D/086	= 2.2~5.5V,1 ADC,4 PGA,DSP,6N Driver
087(A)	= 2.2~5.5V,1 ADC,2 PGA
087C	= 2.2~5.5V,1 ADC,2 PGA, CAN
087D/087E	= 7.5~28V, 1 ADC,2 PGA,3P3N Driver
089	= 2.2~5.5V,1 ADC,2 PGA
089XL	= 2.2~5.5V,1 ADC,4 PGA,DSP,6N Driver,LIN

Pin count

L	= 16 pins
H	= 20 pins
M	= 24 pins
K	= 32 pins
F	= 40 pins
C	= 48 pins
N	= 52 pins
R	= 64 pins
V	=100 pins
Z	=144 pins

Code size

4	= 16Kbyte Flash Memory
6	= 32Kbyte Flash Memory
8	= 64Kbyte Flash Memory
B	=128Kbyte Flash Memory
C	=256Kbyte Flash Memory

Package

P	= TSSOP
T	= TQFP/LQFP
Q	= QFN
S	= SSOP
H	= BGA

Temperature range

6	= -40~85°
8	= -40~105°
9	= -40~125°

Options

TR	= Tape and reel packing
P	= Engineering Samples

Version

X	= Version, B~Z

Fig. 1-1 Naming Conventions of Linko Components

1.4 Resource Diagram

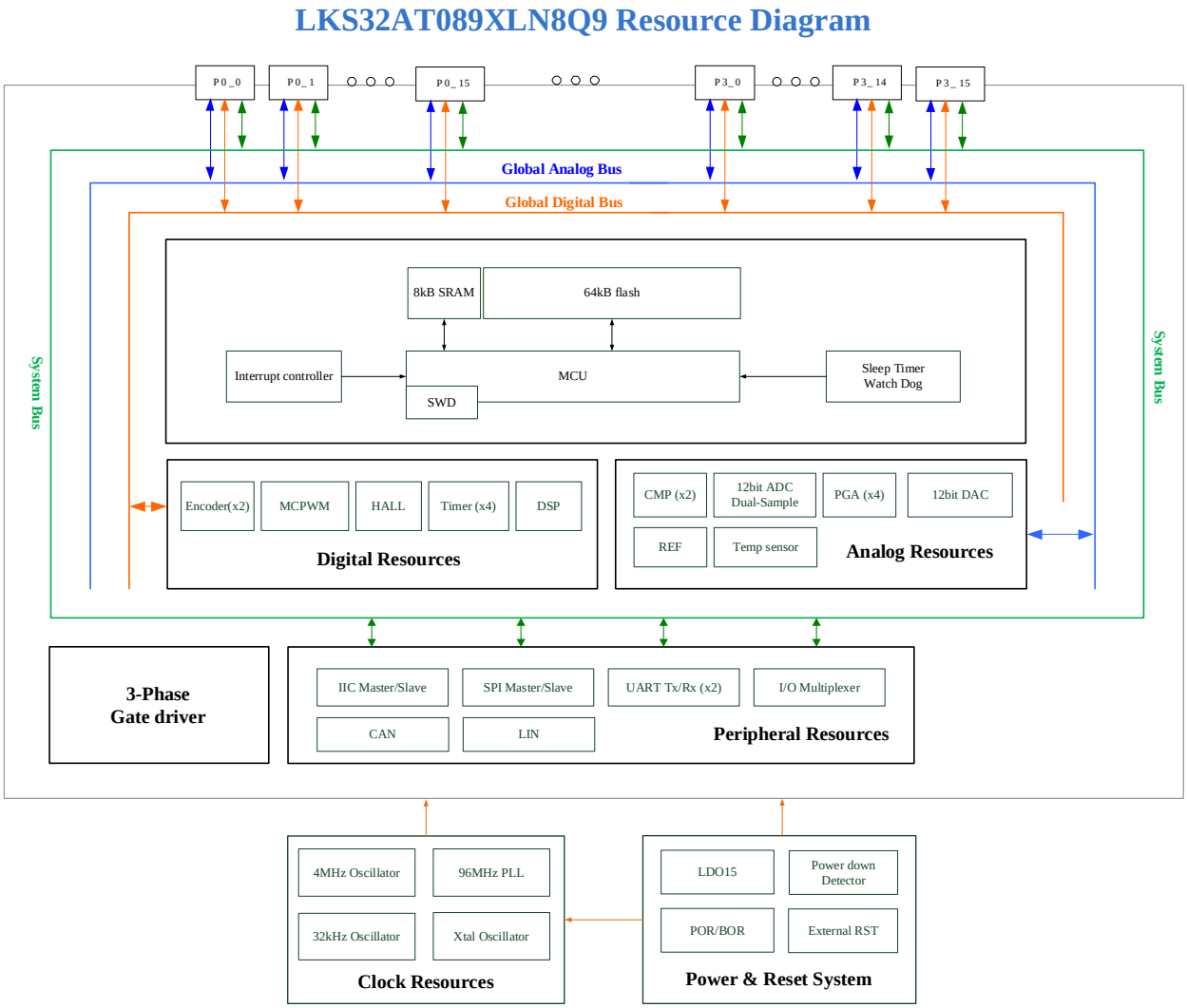

Fig. 1-2 LKS32AT089XLN8Q9 Resource Diagram

1.5 FOC System Example

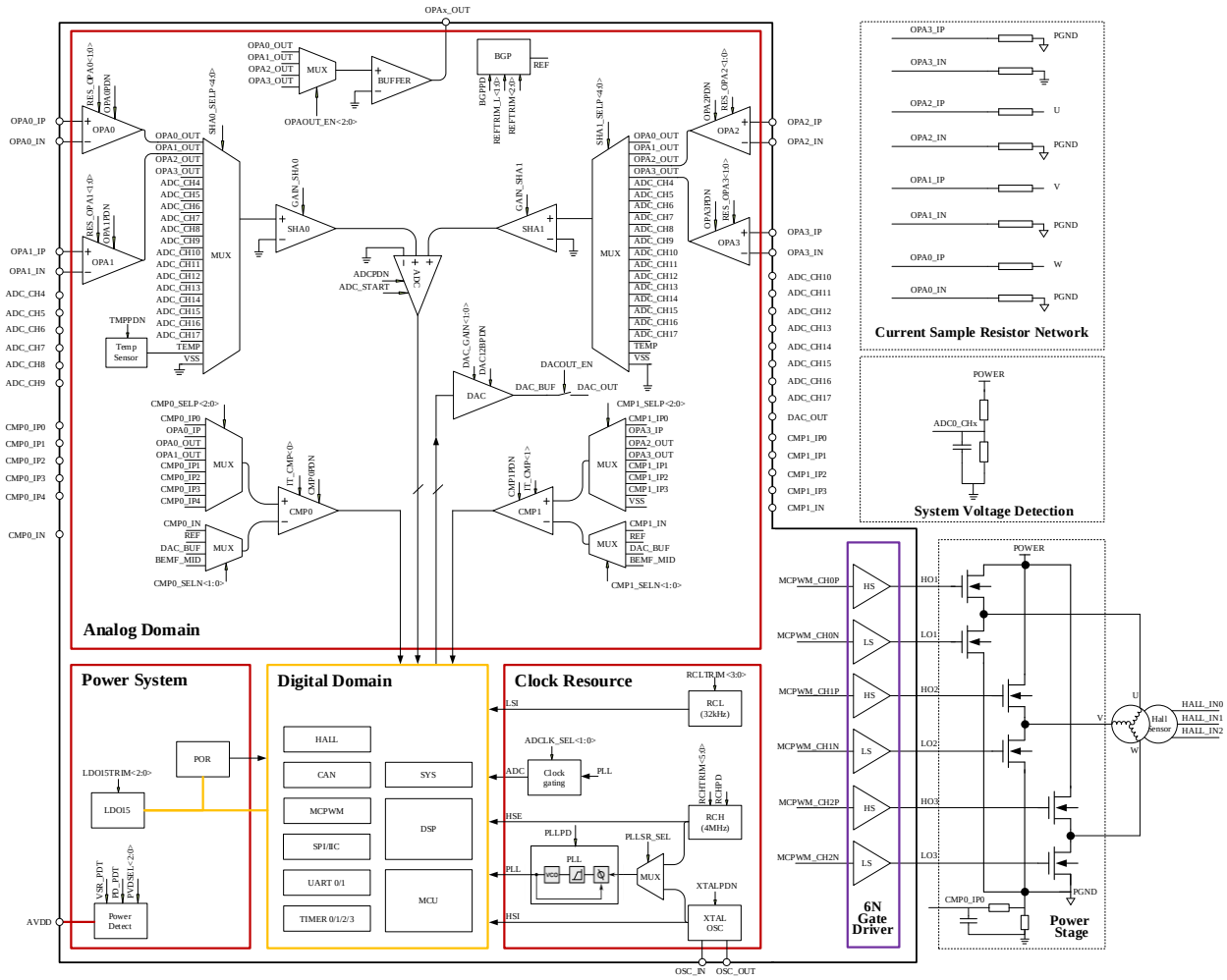

Fig. 1-3 LKS32AT089XLN8Q9 Simplified Schematic of FOC System

2 Device Selection Guide

Table 2-1 LKS08x family device selection guide

	Frequency (MHz)	Flash (kB)	RAM (kB)	ADC ch.	DAC	Comparator	Comparator ch.	OPA	HALL	SPI	IIC	UART	CAN	Temp. Sensor	PLL	QEP	Gate driver	Gate Driver current (A)	Pre-drive supply (V)	Gate floating voltage (V)	Others	Package
LKS32MC080R8T8(B)	96	64	8	13	12BITx1	2	9	4	3	1	1	2	Yes	Yes	Yes	Yes						LQFP64
LKS32MC081C8T8(B)	96	64	8	12	12BITx1	2	9	4	3	1	1	2		Yes	Yes							TQFP48
LKS32MC082K8Q8(B)	96	64	8	8	12BITx1	2	6	3	3	1	1	2		Yes	Yes							QFN5*5 32L-0.75
LKS32MC083C8T8(B)	96	64	8	12	12BITx1	2	9	4	3	1	1	2	Yes	Yes	Yes	Yes						TQFP48
LKS32MC084DF6Q8	96	32	8	11	12BITx1	2	7	4	3	1	1	2		Yes	Yes		6N	+1.2/-1.5	4.5~20*1	200		QFN5*5 40L-0.75
LKS32AT085C8Q9	96	64	8	12	12BITx1	2	9	4	3	1	1	2	Yes	Yes	Yes	Yes						QFN6*6 48L-0.55
LKS32AT086N8Q9	96	64	8	11	12BITx1	2	9	4	3	1	1	2	Yes	Yes	Yes	Yes	6N	+1.2/-1.5	4.5~20	200		QFN6*6 52L-0.55
LKS32MC086N8Q8	96	64	8	11	12BITx1	2	9	4	3	1	1	2	Yes	Yes	Yes	Yes	6N	+1.2/-1.5	4.5~20	200		QFN6*6 52L-0.55
LKS32MC087M6S8(B)	96	32	8	5	12BITx1	2	6	2	3			1		Yes	Yes							SSOP24L
LKS32MC087AM6S8(B)	96	32	8	5	12BITx1	2	6	2	3			1		Yes	Yes							SSOP24L
LKS32MC087CM8S8(B)	96	64	8	5	12BITx1	2	6	2	3			1	Yes	Yes	Yes							SSOP24L
LKS32MC087DM6S8	96	32	8	5	12BITx1	2	6	2	3			1		Yes	Yes		3P3N	+0.05/-0.3	7~28		5V LDO*2	SSOP24L
LKS32MC087EM6S8	96	32	8	5	12BITx1	2	7	2	3			1		Yes	Yes		3P3N	+0.05/-0.3	7~28		5V LDO	SSOP24L
LKS32MC088C6T8(B)	96	32	8	12	12BITx1	2	9	4	3	1	1	2		Yes	Yes							TQFP48
LKS32MC088KU8Q8	96	64	8	8	12BITx1	2	7	3	3	1	1	2	Yes	Yes	Yes	Yes	6N	+0.45/-1	4.5~20	600	5V LDO	QFN43L
LKS32AT089XLN8Q9	96	64	8	11	12BITx1	2	9	4	3	1	1	2	Yes	Yes	Yes	Yes	6N	+1.2/-1.5	4.5~20	200	5V LDO	QFN6*6 52L-0.55

*1 : Some devices are divided into different versions due to the integration of multiple pre drives. The power supply voltage range of the pre drive is different. Please refer to the electrical performance parameters for details.

*2 : Some devices are equipped with a 5V LDO, which is powered by 7.5~28V VCC and could supply 5V to MCU or peripheral devices. Please refer to Pin assignment table for more information.

3 Pin Assignment

3.1 Pin Assignment and Pin Function Description

3.1.1 Special Notes

The red pin in the pin assignment figures below has built-in pull-up resistors:
RSTN has a 100kΩbuilt-in pull-up resistor, which is enabled automatically after power-up.
SWDIO/SWCLK has a 10kΩ built-in pull-up resistor, which is enabled automatically after power-up.
The remaining red pins have 10kΩ built-in pull-up resistors, which could be software-enabled.

UARTx_TX(RX): UART TX and RX support interchange. When the second function of GPIO is selected as UART, and GPIO_PIE is input enabled, it can be used as UART_RX; when GPIO_POE is enabled, it can be used as UART_TX. Generally, the same GPIO does not enable input and output at the same time, otherwise the input PDI will receive the data sent by the PDO.
SPI_DI(DO): The DI and DO of SPI can also be interchanged. When the second function of GPIO is SPI, and GPIO_PIE is input enable, it can be used as SPI_DI; when GPIO_POE is output enable, it can be used as SPI_DO. Generally, the same GPIO does not enable input and output at the same time, otherwise the input PDI will receive the data sent by the PDO.

3.1.2 LKS32AT089XLN8Q9

Fig. 3-1 LKS32AT089XLN8Q9 Pin Assignment

Table 3-1 LKS32AT089XLN8Q9 Pin Function Description

No.	Pin Name	Type	Pin Function Description
0	GND	Ground	Ground Pin. It's strongly recommended to connect all the GND Pin together on PCB
1	HALL_IN1/MCPWM_CH2N/UART1_TX(RX)/TIM1_CH1/ADC_TRIG0/CMP1_IP2/P2.5	Input/Output	Hall sensor B-phase input/motor PWM channel 2 low side/UART1 TX(RX)/Timer1 channel 1/ADC trigger signal 0/positive input

No.	Pin Name	Type	Pin Function Description
			2 for comparator 1/P2.5
2	HALL_IN0/MCPWM_CH2P/UART1_TX(RX)/TIM1_CH0/ADC_TRIG3/CMP1_IP1/CAN_RX/ P2.4	Input/Output	Hall sensor A-phase input/motor PWM channel 2 high-side output/UART1 TX(RX)/Timer1 channel 0/ADC trigger signal 3/positive input 1 for comparator 1/P2.4, with a 10k software-enabled built-in pull-up resistor
3	CMP1_OUT/MCPWM_BKIN0/SPI_CS/REF/P2.3	Input/Output	Comparator 1 output/motor PWM breaking signal 0/SPI chip select signal/voltage reference signal/P2.3
4	CMP1_IN/P2.2	Input/Output	Comparator 1 negative input/P2.2
5	SPI_CLK/ADC_CH14/CMP1_IP0/P2.1	Input/Output	SPI clock/ADC channel 14/positive input for comparator 1/P2.1, with a 10k software-enabled built-in pull-up resistor
6	OPA3_IP/P3.15	Input/Output	OPA3 positive input/P3.15
7	OPA3_IN/P3.14	Input/Output	OPA3 negative input/P3.14
8	SPI_DI(DO)/SDA/P2.10	Input/Output	SPI data output/IIC data/P2.10, with 10k software-enabled built-in pull-up resistor
9	SPI_DI(DO)/SCL/ADC_CH12/CMP0_IP0/P2.9	Input/Output	SPI data input/IIC clock/ADC channel 12/positive input 0 for comparator 0/P2.9/OPA2 negative input/P3.11
10	VBAT	Power	LIN supply voltage
11	OPA2_IP/P3.10	Input/Output	OPA2 positive input/P3.10
12	MCPWM_CH3N/UART0_TX(RX)/SDA/TIM0_CH1/ADC_TRIG3/SIF/P1.11	Input/Output	Motor PWM channel 3 low-side output/UART 0 TX(RX)/IIC data/Timer0 channel 1/ADC trigger signal 3/P1.11, with a 10k software-enabled built-in pull-up resistor
13	ADC_CH13/MCPWM_CH3P/UART0_TX(RX)/SCL/TIM0_CH0/ADC_TRIG2/P1.10	Input/Output	Motor PWM channel 3 high-side output/UART 0 (TX)RX/IIC clock/Timer0 channel 0/ADC trigger signal 2/P1.10, with a 10k software-enabled built-in pull-up resistor
14	VB3	Input/Output	High-side floating input supply voltage 3
15	HO3	Output	The high-side gate drive signal output 3 is controlled by the PWM output function of the MCU P1.8 port, and HO3 output will be in the same phase with P1.8 signal, that is, when input is '1', and HO3 output is '1'.
16	VS3	Input/Output	High-side floating bias voltage 3
17	VB2	Input/Output	High-side floating input supply voltage 2
18	VCC	Power	Full-bridge drive module power supply, 7 ~ 20V
19	HO2	Output	The high-side gate drive signal output 2 is controlled by the PWM output function of the

No.	Pin Name	Type	Pin Function Description
			MCU P1.6 port, and HO2 output will be in the same phase with P1.6 signal, that is, when input is '1', and HO2 output is '1'.
20	VS2	Input/Output	High-side floating bias voltage 2
21	VB1	Input/Output	High-side floating input supply voltage 1
22	HO1	Output	The high-side gate drive signal output 1 is controlled by the PWM output function of the MCU P1.4 port, and HO1 output will be in the same phase with P1.4 signal, that is, when input is '1', and HO1 output is '1'.
23	VS1	Input/Output	High-side floating bias voltage 1
24	LO1	Output	The low-side gate drive signal output 1 is controlled by the PWM output function of the MCU P1.5 port, that is, GPIO1_F7654[7:4] needs to be configured, and P3.13 shall be set to the output state, i.e. GPIO3_POE[13]. LO1 output will be in the same phase with P1.5 signal, that is, when P1.5 output is '1', and LO1 output is '1'.
25	LO2	Output	The low-side gate drive signal output 2 is controlled by the PWM output function of the MCU P1.7 port, that is, GPIO1_F7654[15:12] needs to be configured, and P1.12 shall be set to the output state, i.e. GPIO1_POE[12]. LO2 output will be in the same phase with P1.7 signal, that is, when P1.7 output is '1', and LO2 output is '1'.
26	LO3	Output	The low-side gate drive signal output 3 is controlled by the PWM output function of the MCU P1.9 port, that is, GPIO_FBA98[3:0] needs to be configured, and P1.15 shall be set to the output state, i.e. GPIO1_POE [15]. LO3 output will be in the same phase with P1.9 signal, that is, when P1.9 output is '1', and LO3 output is '1'.
27	OPA0_IN/P3.7	Input/Output	Negative input for OPA 0/P3.7
28	ADC_CH11/OPAx_OUT/LDO15/P2.7	Input/Output	ADC channel 11/OPAx output/LDO15 output/P2.7, with 10k software-enabled built-in pull-up resistor
29	OPA1_IN/P3.1	Input/Output	OPA 1 negative input/P3.1
30	OPA1_IP/P3.0	Input/Output	OPA1 positive input/P3.0
31	OPA0_IP/P3.5	Input/Output	OPA0 positive input/P3.5
32	NC	NC	No connection

No.	Pin Name	Type	Pin Function Description
33	MCPWM_CH0N/UART0_TX(RX)/SPI_DI(DO)/P1.0/OSC_IN/P2.8	Input/Output	Motor PWM channel 0 low-side output/UART0 TX(RX)/SPI data input/P1.0, with 10k software-enabled built-in pull-up resistor/Crystal oscillator input/P2.5
34	MCPWM_CH0P/UART0_TX(RX)/SPI_DI(DO)/TIM0_CH0/ADC_TRIG1/CMP0_IN/P0.15/OSC_OUT/P3.9	Input/Output	Motor PWM channel 0 high-side output/UART0 TX(RX)/SPI data output/Timer0 channel 0/ADC trigger signal 1/negative input for comparator 0/P0.15/Crystal oscillator output/P3.9
35	CMP0_OUT/MCPWM_BKIN1/SPI_CLK/TIM0_CH1/ADC_TRIG0/SIF/ADC_CH10/CMP0_IP4/P0.14	Input/Output	Comparator 0 output/motor PWM breaking signal 1/SPI clock/Timer0 channel 1/ADC trigger signal 0/SIF/ADC channel 10/ positive input 4 for comparator 0/P0.14
36	HALL_IN2/ADC_CH17/CMP0_IP3/CAN_TX/P0.13	Input/Output	Hall sensor C-phase input/ADC channel 17/ positive input 3 for comparator 0/P0.13
37	HALL_IN1/TIM3_CH1/ADC_CH16/CMP0_IP2/CAN_RX/P0.12	Input/Output	Hall sensor B-phase input/Timer3 channel 1/ADC channel 16/positive input 2 for comparator 0/CAN_RECEIVE/P0.12
38	HALL_IN0/TIM3_CH0/ADC_CH15/CMP0_IP1/P0.11	Input/Output	Hall sensor A-phase input/Timer3 channel 0/ADC channel 15/positive input 1 for comparator 0/P0.11
39	MCPWM_CH1N/TIM2_CH1/ADC_TRIG2/P2.12	Input/Output	Motor PWM channel 1 low-side output/Timer2 channel 1/ADC trigger signal 2/P2.12
40	MCPWM_CH1P/TIM2_CH0/P2.11	Input/Output	Motor PWM channel 1 high-side output/Timer 2 channel 0/P2.11
41	UART1_TX(RX)/TIM1_CH1/CAN_TX/P0.7	Input/Output	UART1 TX(RX)/Timer1 channel 1/CAN_SEND/P0.7, with a 10k software-enabled built-in pull-up resistor
42	UART1_TX(RX)/TIM1_CH0/CAN_RX/P0.6	Input/Output	UART1 TX(RX)/Timer1 channel 0/CAN_RECEIVE/P0.6, with a 10k software-enabled built-in pull-up resistor
43	ADC_CH9/P0.5	Input/Output	ADC channel 9/P0.5
44	SDA/TIM2_CH1/ADC_CH8/P0.4	Input/Output	IIC data/Timer2 channel 1/ADC channel 8/P0.4
45	SCL/TIM2_CH0/ADC_CH7/P0.3	Input/Output	IIC clock/Timer2 channel 0/ADC channel 7/P0.3
46	AVDD	Power	Chip power input, voltage range 3.0 ~ 5.5V. Off-chip decoupling capacitor ≥1uF is recommended, and should be placed as close as possible to the AVDD pin.
47	RSTN/P0.2	Input/Output	RSTN/P0.2 is usually used as RSTN. Add a 100nF capacitor between RSTN and ground, RSTN has a 100k built-in pull-up resistor.

No.	Pin Name	Type	Pin Function Description
48	ADC_CH4/DAC_OUT/P0.0	Input/Output	ADC channel 4/DAC output/P0.0, with a 10k software-enabled built-in pull-up resistor
49	INH/EN	Input/Output	Used to control the working state of the external power supply, rear wake events for high level /LDO Enables pins
50	SWDIO/SCL/P2.14	Input/Output	SWD data/IIC clock/P2.14 with 10k built-in pull-up resistor
51	SWCLK	Output	SWD clock with 10k built-in pull-up resistor
52	HALL_IN2/MCPWM_CH3P/TIM3_CH0/ ADC_TRIG1/CMP1_IP3/P2.6	Input/Output	Hall sensor C-phase input/motor PWM channel 3 high-side output/Timer3 channel 0/ADC trigger signal 1/positive input 3 for comparator 1/P2.6, with a 10k software-enabled built-in pull-up resistor

3.2 Description of Pin Multiplex Function

Table 3-2 LKS32AT089XLN8Q9 Pin Function Selection

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AFE
P0.0												ADC_CH4, DAC_OUT
P0.1												ADC_CH6
P0.2												
P0.3						SCL		TIM2_CH0				ADC_CH7
P0.4						SDA		TIM2_CH1				ADC_CH8
P0.5												ADC_CH9
P0.6				UART1_TX(RX)			TIM1_CH0					
P0.7				UART1_TX(RX)			TIM1_CH1					
P0.8												
P0.9						SCL		TIM2_CH0				
P0.10						SDA		TIM2_CH1				
P0.11		HALL_IN0						TIM3_CH0				ADC_CH15/CMP0_IP1
P0.12		HALL_IN1						TIM3_CH1				ADC_CH16/CMP0_IP2
P0.13		HALL_IN2										ADC_CH17/CMP0_IP3
P0.14	CMP0_OUT		MCPWM_BKIN1		SPI_CLK		TIM0_CH1		ADC_TRIG0		SIF	ADC_CH10/CMP0_IP4
P0.15			MCPWM_CH0P	UART0_TX(RX)	SPI_DI(DO)		TIM0_CH0		ADC_TRIG1			CMP0_IN

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AFE
P1.0			MCPWM_CH0N	UART0_TX(RX)	SPI_DI(DO)							
P1.1					SPI_CS							
P1.2								TIM3_CH0				
P1.3								TIM3_CH1				ADC_CH5
P1.4	LRC		MCPWM_CH0P									
P1.5	HRC		MCPWM_CH0N									
P1.6			MCPWM_CH1P									
P1.7			MCPWM_CH1N									
P1.8			MCPWM_CH2P									
P1.9			MCPWM_CH2N									
P1.10			MCPWM_CH3P	UART0_TX(RX)		SCL	TIM0_CH0		ADC_TRIG2			ADC_CH13
P1.11			MCPWM_CH3N	UART0_TX(RX)		SDA	TIM0_CH1		ADC_TRIG3		SIF	
P1.12			MCPWM_CH1N									
P1.13					SPI_CLK		TIM0_CH0					
P1.14					SPI_DI(DO)		TIM0_CH1					
P1.15			MCPWM_CH2N									

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AFE
P2.0					SPI_CS			TIM2_CH1				
P2.1					SPI_CLK							ADC_CH14/ CMP1_IP0
P2.2												CMP1_IN
P2.3	CMP1_OUT		MCPWM_BKIN0		SPI_CS							REF
P2.4		HALL_IN0	MCPWM_CH2P	UART1_TX(RX)			TIM1_CH0		ADC_TRIG3			CMP1_IP1
P2.5		HALL_IN1	MCPWM_CH2N	UART1_TX(RX)			TIM1_CH1		ADC_TRIG0			CMP1_IP2
P2.6		HALL_IN2	MCPWM_CH3P					TIM3_CH0	ADC_TRIG1		SIF	CMP1_IP3
P2.7												ADC_CH11/ OPAx_OUT/ LDO15
P2.8				UART1_TX(RX)				TIM3_CH0				OSC_IN
P2.9					SPI_DI(DO)	SCL						ADC_CH12/ CMP0_IP0
P2.10					SPI_DI(DO)	SDA						
P2.11			MCPWM_CH1P					TIM2_CH0				
P2.12			MCPWM_CH1N					TIM2_CH1	ADC_TRIG2			
P2.13			MCPWM_CH3N					TIM3_CH1				
P2.14						SCL						
P2.15						SDA						

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AFE
P3.0												OPA1_IP
P3.1												OPA1_IN
P3.2												
P3.3												
P3.4												
P3.5												OPA0_IP
P3.6												
P3.7												OPA0_IN
P3.8												
P3.9				UART1_TX(RX)				TIM3_CH1				OSC_OUT
P3.10												OPA2_IP
P3.11												OPA2_IN
P3.12												
P3.13	HRC		MCPWM_CH0N									
P3.14												OPA3_IN
P3.15												OPA3_IP

4 Package Size

4.1 LKS32AT089XLN8Q9

QFN6*6 52L-0.55 Profile Quad Flat Package:

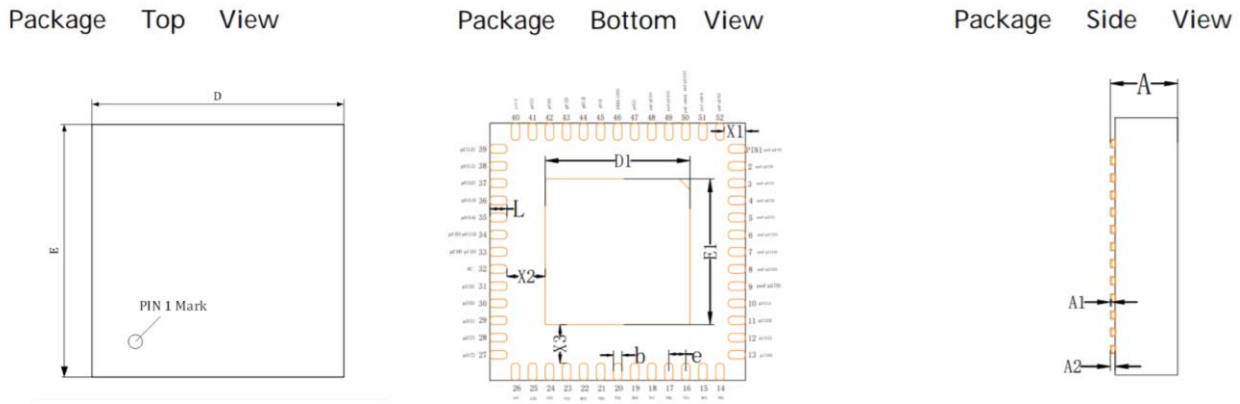

Fig. 4-1 LKS32AT089XLN8Q9 Package Diagram

Table 4-1 LKS32AT089XLN8Q9 Package Dimension

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.500	0.550	0.600
A1	0.007	0.012	0.017
A2		0.040	
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D1	3.350	3.400	3.450
E1	3.350	3.400	3.450
L	0.350	0.400	0.450
b	0.150	0.200	0.250
e	0.350	0.400	0.450
X1	0.450	0.500	0.550
X2	0.850	0.900	0.950
X3	0.850	0.900	0.950

5 Electrical Characteristics

Table 5-1LKS32AT089XLN8Q9 electrical absolute characteristics

Parameter	Min.	Max.	Unit	Description
MCU Power Supply Voltage (AVDD)	-0.3	+6.0	V	
Gate Driver Power Supply Voltage (VCC)	-0.3	+25.0	V	
5v LDO input voltage (VIN)	-0.3	+45	V	
LIN supply voltage (VBAT)	-0.3	+58	V	
LIN pin voltage	-58	+58	V	
5v LDO output current		100	mA	
Operating Temperature	-40	+125	˚C	
Storage Temperature	-40	+150	˚C	
Junction Temperature	-	150	°C	
Pin Temperature (solder for10 seconds)	-	260	°C	

Table 5-2LKS32AT089XLN8Q9 Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit	Description
MCU Power Supply Voltage (AVDD)	3.0	5	5.5	V	The AVDD reset level is 2.7V ± 0.2V
Analog Power Supply Voltage ($AVDD_A$)	3.3	5	5.5	V	ADC use 2.4V internal reference
	2.8	5	5.5	V	ADC use 1.2V internal reference
Gate Driver Power supply voltage (VCC)	7		20	V	
5v LDO input voltage (VIN)	2.7		40	V	
LIN supply voltage (VBAT)	5.5	12	27	V	

OPA could work under 3.0V, but the output range will be limited.

Table 5-3LKS32AT089XLN8Q9 ESD parameters

Item	Pin	Min.	Max.	Unit
ESD test (HBM)	Gate Driver Pins(PIN14~26)	-2000	2000	V
	LIN pin: VBAT(PIN10), WAKE_N(PIN32), LIN(PIN42)	-4000	4000	V
	Other Pins	-6000	6000	V

According to "MIL-STD-883J Method 3015.9", under the environment of 25°C and 55% relative humidity, electrostatic discharge is applied to all IO pins of the tested chip for 3 times, with an interval of 1s each time. If there is a higher requirement for ESD, it is recommended to place TVS diodes on the relevant external pins for protection.

表 5-4 LKS32AT089XLN8Q9 Latch-up parameters

Parameter	Min.	Max.	Uint
Latch-up current (85°C)	-200	200	mA

According to "JEDEC STANDARD NO.78E NOVEMBER 2016", Apply an overvoltage to all power IO and inject 200mA current into each signal IO. The test results show that the chip's latch resistance grade is 200mA.

Table 5-5LKS32AT089XLN8Q9 IO absolute characteristics

Parameter	Description	Min.	Max.	Unit
$V_{IN-GPIO}$	GPIO Signal Input Voltage Range	-0.3	6.0	V
I_{INJ_PAD}	Maximum Injection Current of A Single GPIO	-11.2	11.2	mA
I_{INJ_SUM}	Maximum Injection Current of All GPIOs	-50	50	mA

Table 5-6LKS32AT089XLN8Q9 IO DC Parameters

Parameter	Description		AVDD	Conditions	Min.		Max.	Unit
V_{IH}	High input level of digital IO		5V	-	0.7*AVDD			V
			3.3V		2.0			
V_{IL}	Low input level of digital IO		5V	-			0.3*AVDD	V
			3.3V				0.8	
V_{HYS}	Schmidt hysteresis range		5V	-	0.1*AVDD			V
			3.3V					
I_{IH}	Digital IO current consumption when input is high		5V	-			1	uA
			3.3V					
I_{IL}	Digital IO current consumption when input is low		5V	-	-1			uA
			3.3V					
V_{OH}	High output level of digital IO			Current = 11.2mA	AVDD-0.8			V
V_{OL}	Low output level of digital IO			Current = 11.2mA			0.5	V
R_{pup}	Pull-up resistor*	Reset pin			100	200	400	kΩ
		Normal pin			8	10	12	
R_{io-ana}	Connection resistance between IO and internal analog circuit				100		200	Ω
C_{IN}	Digital IO Input-capacitance		5V	-			10	pF
			3.3V					

* Only some IOs have built-in pull-up resistors, see section “Pin Function Description” for details.

Table 5-7LKS32AT089XLN8Q9 Circuit module current consumption IDD

Module	Min	Typ	Max	Unit
CMP		0.005		mA

OPA		0.450		mA
ADC		3.710		mA
DAC		0.710		mA
Temp Sensor		0.150		mA
BGP		0.154		mA
4MHz RC		0.105		mA
PLL		0.080		mA
CPU+flash+SRAM (96MHz)		8.667		mA
CPU+flash+SRAM (12MHz)		1.600		mA
CRC		0.070		mA
DSP		3.421		mA
UART		0.107		mA
DMA		1.340		mA
MCPWM		0.053		mA
TIMER		0.269		mA
SPI		0.500		mA
IIC		0.500		mA
CAN		2.200		mA
Sleep	10	30	50	uA

Unless otherwise specified, the above tests are conducted at room temperature of 25 ° AVDD=5V, using a 96MHz clock. Due to device model deviations in the manufacturing process, there may be individual differences in current consumption among different chips.

Table 5-8LKS32AT089XLN8Q9 Sleep current consumption Iq

Module	Min	Typ	Max	Unit
VIN (12V, INH=1)	40	70	100	uA
VIN (12V, INH=0)	0.1	0.2	0.25	uA
VCC (12V)	40	43	95	uA
VBAT (12V)	10	20	40	uA

6 Analog Characteristics

Table 6-1LKS32AT089XLN8Q9 analog characteristics

Parameter	Min.	Normal	Max.	Unit	Description
Analog-to-Digital Converter (ADC)					
Power Supply	2.8	5	5.5	V	ADC use 2.4V internal reference
	3.3	5	5.5	V	ADC use 1.2V internal reference
Sampling rate		3		MHz	$f_{adc}/16$
Differential Input Signal Range	-REF		+REF	V	When Gain=1; REF=2.4V
	-3.6		+3.6	V	When Gain=2/3; REF=2.4V
Single-ended Input Signal Range	-0.3		AVDD+0.3	V	Limited by the input voltage of the IO port
DC offset		5	10	mV	Correctable
Effective number of bits (ENOB)	10.5	11		bit	
INL		2	3	LSB	
DNL		1	2	LSB	
SNR	63	66		dB	
Input Resistance	100k			Ohm	
Input Capacitance		10pF		F	
Reference Voltage (REF)					
Power Supply	3.0	5	5.5	V	
Output Deviation	-9		9	mV	
Rejection Ratio of Power Supply		70		dB	
Temperature Coefficient		20		ppm /°C	
Output Voltage		1.2		V	
Digital-to-Analog Converter (DAC)					
Power Supply	3.0	5	5.5	V	
Load Resistance	5k			Ohm	Output BUFFER is on
Load capacitance			50p	F	
Output voltage range	0.05		AVDD-0.1	V	
Conversion speed			1M	Hz	
DNL		1	2	LSB	
INL		2	4	LSB	
OFFSET		5	10	mV	
SNR	57	60	66	dB	
Operational Amplifier (OPA)					
Power Supply	2.8	5	5.5	V	
Bandwidth		10M	20M	Hz	
Load Resistance	20k			Ohm	

Parameter	Min.	Normal	Max.	Unit	Description
Load Capacitance			5p	F	
Input Common Mode Voltage Range (VICM)	0		AVDD	V	
Output Signal Range	0.1		AVDD-0.1	V	Under minimum load resistance
OFFSET		10	15	mV	This OFFSET is the equivalent differential input deviation obtained when the OPA differential input is short-circuited and OPA OUT is measured from 0 level. The output deviation of OPA is the OPA magnification xOFFSET
Common Mode Voltage (Vcm)	1.65	1.9	2.2	V	Measurement condition: normal temperature. Operational amplifier swing=2 × min(AVDD-Vcm, Vcm). It is recommended that the application using OPA single output should be powered on to measure Vcm and make software subtraction correction. For more analysis, please refer to the official website application note "ANN009 - Differences between Operational Amplifier Differential and Single Operating Mode".
Common Mode Rejection Ratio (CMRR)		80		dB	
Power Supply Rejection Ratio (PSRR)		80		dB	
Load Current			500	uA	
Slew Rate		5		V/us	
Phase Margin (PM)		60		Degree	
Comparator (CMP)					
Power Supply	3.0	5	5.5	V	
Input Signal Range	0		AVDD	V	
OFFSET		5	10	mV	
Delay		0.15u		S	Default power consumption
		0.6u		S	Low power consumption
Hysteresis		20		mV	HYS='0'
		0		mV	HYS='1'

Description of Analog Register Table:

Address space of 0x40000040 to 0x40000050 are the calibration registers of each analog module. These registers will be set to a unique calibration value in factory. Generally, users are advised not to configure or change these values. If fine-tuning is required, please read the original settings first, and then adjust based on those values.

Addresses space of 0x40000020 to 0x4000003c are registers open to users. The blank registers must be configured to 0 (these registers will be reset to 0 after power on). Other registers could be configured in situations.

7 Power Management System

AVDD Power System

The power management system is composed of LDO15 module, power detection module (PVD), power-on/power-off reset module (POR).

VDD is powered by 3.0V~5.5V, and all internal digital circuits and PLL modules are powered by an internal LDO15.

The LDO15 is automatically turned on after power-on. No software configuration is necessary. And the LDO15 output voltage can be adjusted by software.

LDO15 has been calibrated before it leaves the factory. Generally.

LKS32AT089XLN8Q9 integrates a 5V LDO. When the chip is powered by 7-20V VCC, the internal LDO can generate 5V to power the MCU, or power to the off-chip.

The POR module monitors the voltage of the LDO15. When the voltage of the LDO15 is lower than 1.1V, for example, at the beginning of power-on or at the time of power-off, it will provide a reset signal for the digital circuit to avoid any abnormal operation.

The PVD module monitors the 5V input power. If it is below a certain threshold, it will remind the MCU by sending an alarm (interrupt) signal. The interrupt reminder threshold can be set to different voltages through the PVDSEL<1:0> registers. The PVD module can be turned off by setting PD_PDT = '1'. For the corresponding value of specific register, please refer to the analog register table.

VCC Power System

The operating power supply voltage range of VCC is 7 ~ 20V, which provides power for the on-chip gate driver module. If this voltage is below 5V it will be considered as undervoltage.

8 Clock System

The clock system consists of a 32KHz RC oscillator, a 4MHz RC oscillator, an external 4MHz crystal oscillator, and a PLL.

The 32K RC clock is used in the MCU system as a slow clock for modules such as reset/wakeup source filters or used in the low power mode; The 4MHz RC clock can be used as the main clock of the MCU, and can provide a reference clock to PLL. PLL clock is up to 96MHz; The external 4MHz crystal oscillator is used as a backup clock.

Both 32k and 4M RC clocks will been through factory calibration. In the range of -40 ~ 105 ℃, the accuracy of the 32K RC clock is ± 50%, and the accuracy of the 4M RC clock is ± 1%.

The 4M RC clock is turned on by setting RCHPD = ’0’ (ON by default, turn off when set to “1’). The RC clock needs a reference voltage and current provided by the Bandgap voltage reference module; thus, do remember to turn on the BGP module before turning on the RC clock. When the chip is powered on, the 4M RC clock and BGP module are both turned on automatically. The 32K RC clock is always on and cannot be turned off.

The PLL multiplies the 4M RC clock to provide a higher frequency clock for modules like MCU and ADC. The highest frequency of MCU and PWM module is 96MHz, and the typical working frequency of ADC module is 48MHz. It can be set to different frequency by the register ADCLKSEL <1:0>.

PLL is turned on by setting PLLPDN = ’1’ (OFF by default, turn on when set to '1'). Before turning on the PLL module, the BGP (Bandgap) module should be turned on first. After the PLL is turned on, it needs a settling time of 6us to achieve a stable frequency output. When the chip is powered on, the RCH clock and BGP module are both turned on. PLL is OFF by default and could be enabled by software.

The crystal oscillator circuit has a built-in amplifier and an oscillator capacitor. Connect a crystal between IO OSC_IN/OSC_OUT and set XTALPDN = ’1’ to start the oscillation.

9 Reference Voltage

Reference voltage and current are provided for ADC, DAC, RC clock, PLL, temperature sensor, operational amplifier, comparator and FLASH. Before using any of the above modules, the BGP voltage reference should be turned on first.

When the chip is powered on, the BGP module is turned on automatically. The voltage reference is turned on by setting BGPPD = ’0’. From OFF to ON, BGP needs about 2us to stabilize. BGP output voltage is about 1.2V, and accuracy is ± 0.8%

The voltage reference can be measured by setting REF_AD_EN = ’1’ and via IO P2.3.

10 Analog Digital Converter

The chip integrated a synchronous double-sampling SAR ADC which is shut down by default when the chip is powered up. Before turning on ADC, the BGP module, 4M RC clock and PLL should be turned on first. In the default configuration, ADC clock is 48MHz, which corresponds to a conversion rate of 3Msps.

The synchronous double sampling circuit can sample the two input analog signals at the same time. After the sampling is completed, the ADC converts the two signals one by one and writes them into the corresponding data registers.

ADC takes 16 ADC clock cycles to complete one conversion, of which 13 are conversion cycles and 3 are sampling cycles. I.E. $f_{conv}=f_{adc}/16$. When the ADC clock is set to 48MHz, the conversion rate is 3Msps.

When the ADC is working at a lower frequency, the power consumption can be reduced by setting register CURRIT<1:0>.

ADC could work in different modes: One-time single channel trigger mode, continuous single channel sampling mode, One-time 1 to 20 channels scanning mode, continuous 1 to 20 channels scanning mode. It has a set of 20 independent registers for each analog channel.

The ADC trigger can be MCPWM/Timer trigger signals T0, T1, T2 and T3 happened for the preset number of times, or software trigger event.

Among the 20 analog channels, the 19th channel is analog ground and is used to measure the offset of the ADC. The ADC values of other channels will be automatically subtracted by this offset. The offset is calibrated in factory and store in flash. Each time the chip is powered up, this offset will be loaded into ADC_DC register automatically. If the user needs to improve the offset over the whole temperature, it can be recalculated time by time (for example, each hour) when the ADC is idle.

When GAIN_REF = 0, the ADC voltage reference is 2.4V. The ADC has two gain modes, which are set by GAIN_SHAx, corresponding to 1x and 2/3 x gain setting; 1x gain corresponds to an input signal range of ± 2.4V, and 2/3 gain corresponds to an input signal range of ± 3.6V. When measuring the output signal of the OPA, select the specific ADC gain according to the maximum signal that the OPA may output.

11 Operational Amplifier

4-channel of rail-to-rail OPAs (3 channels for 084D) are integrated, with a built-in feedback resistor R2/R1. A resistor R0 is required to be connected in series to the external pin. The resistance of feedback resistors R2:R1 can be adjusted by register RES_OPA0<1:0> to achieve different gain. For the corresponding value of specific register, please refer to the analog register table.

The close-loop gain of OPA is R2/(R1+R0), where R0 is the resistance of the external resistor.

For the application of MOS resistance direct sampling, it is recommended to connect an external resistance of >20kΩ to reduce the current flowing into the chip pin when the MOS is turned off;

For the application of small resistance sampling, it is recommended to connect an external resistor of 100Ω.

The OPA can select one of the output signals of the 4-channels amplifiers by setting OPAOUT_EN <2:0>, and send it to the P2.7 IO port through a buffer for measurement (see the corresponding relationship in the datasheet 'Pin Function Description"). Because of this buffer, the OPA is able to be output to an IO while operating normally.

When the chip is powered on, the OPA module is OFF by default. It can be turned on by setting OPAxPDN = ’1’, and turn on the BGP module before turning on the amplifier.

For built-in clamp diodes are integrated between the positive and negative OPA inputs, the motor phase line could be directly connected to the OPA input through a matching resistor, thereby simplifying the external circuit for MOSFET current sampling.

12 Comparator

Built-in 2-channel rail-to-rail comparators with programmable comparator speed, hysteresis voltage, and signal source.

The comparison delay can be set to 0.15uS/0.6uS by register IT_CMP. and the hysteresis voltage can be set to 20mV/0mV by CMP_HYS.

The signal sources of the positive and negative inputs can be programmed by register CMP_SELP<2:0> and CMP_SELN<1:0>. For details, please refer to the analog register description.

When the chip is powered on, the comparator module is OFF by default. The comparator is turned on by setting CMPxPDN = ’1’, and turn on the BGP module before turning on the comparator.

13 Temperature Sensor

The typical accuracy is 2℃ in the range of -40~85℃,The chip has a temperature sensor with a typical accuracy of 2 ℃ in the range of -40~85 ℃ and 3℃ in the range of 85~105℃. The temperature sensor will be calibrated in factory, and the calibration value is saved in the flash info area.

When the chip is powered on, the temperature sensor module is OFF by default. Turn on the BGP module before turning on the temperature sensor.

The temperature sensor is turned on by setting TMPPDN = '1', and it takes about 2us to be stable after turning on. Thus, it should be turned on at least 2us ahead before the ADC measures the sensor output.

14 Digital Analog Converter

The chip has a 1-channel 12bit DAC, the maximum range of the output signal can be set to 1.2V/3V/4.85V through the register DAC_GAIN <1:0>.

The 12bit DAC can be output via IO port P0.0 by setting register DACOUT_EN = 1, which can drive a load resistance of over 5kΩ and a load capacitance of 50pF.

The maximum output data rate of the DAC is 1Msps.

When the chip is powered on, the DAC module is OFF by default. DAC can be turned on by setting DAC12BPDN = 1. Turn on the BGP module before turning on the DAC module.

15 Processor

- 32-bit Cortex-M0 + DSP dual-core processor
- Two-wire SWD debug pin
- System frequency is up to 96MHz

16 Storage

16.1 Flash

- built-in flash including 64kB main area and 1kB NVR
- Endurance: 20,000 Cycles(min)
- Data retention: more than 100 years
- Single byte program: 7.5us(max), Sector erase: 5ms(max)
- Sector size 512bytes, supporting Sector erase/program and in-application program, erase/program one sector while accessing another
- Flash data anti-theft by programming the last word of flash to any words other than 0xFFFFFFFF

16.2 SRAM

- built-in 8kB SRAM

17 Motor Control PWM

- MCPWM operating frequency is up to 96MHz
- Supports up to 4 channels of complementary PWM output with adjustable phase
- The width of dead-zone in each channel can be configured independently
- Support edge-aligned PWM
- Support software control IO mode
- Support IO polarity control
- Internal short circuit protection to avoid short circuit due to configuration error
- External short circuit protection, enabling fast shutdown by monitoring the external signals
- Internal ADC sampling interrupt
- Preload MCPWM register configuration and update simutaneously
- Programmable load time and period

18 Timer

- 4-channel standard timer, 2-channel 16-bit timer, 2-channel 32-bit timer.
- Support capture mode for measuring external signal/pulse width
- Support comparison mode for timed interruption of edge-aligned PWM

19 Hall Sensor Interface

- Built-in 1024 cycles filtering
- 3-channel Hall signal input
- 24-bit counter, with overflow and capture interrupt

20 DSP

- Customized DSP instruction set for motor control algorithm, , three-stage pipeline achitecture
- Operating frequency is up to 96MHz
- 32/16-bit divider, could finish one division calculation in 10 cycles
- 32-bit hardware SQRT, could finish one SQRT calculation in 8 cycles
- Q15 format Cordic trigonometric function module, could finish sin/cos/artanc calculation in 8 cycles
- DSP has independent program memory and data memory, DSP could execute its program independently, and can also be called by MCU to perform a certain calculation as a AHB slave like a coprocessor
- Support DSP IRQ and pause state for data exchange purpose with MCU

21 LIN

- Data transfer rate up to 20kbps via LIN
- Integrated 30kΩ LIN pull-up resistor
- Use INH pins to control system-level power consumption
- Non-interference operation during power on/off on LIN bus and RXD output
- Protection functions: ±58V LIN bus fault tolerance, 42V load drop support, IEC ESD protection, undervoltage protection on VBAT input, TXD dominant state timeout, thermal shutdown, system-level unpowered node or ground disconnection failure protection.

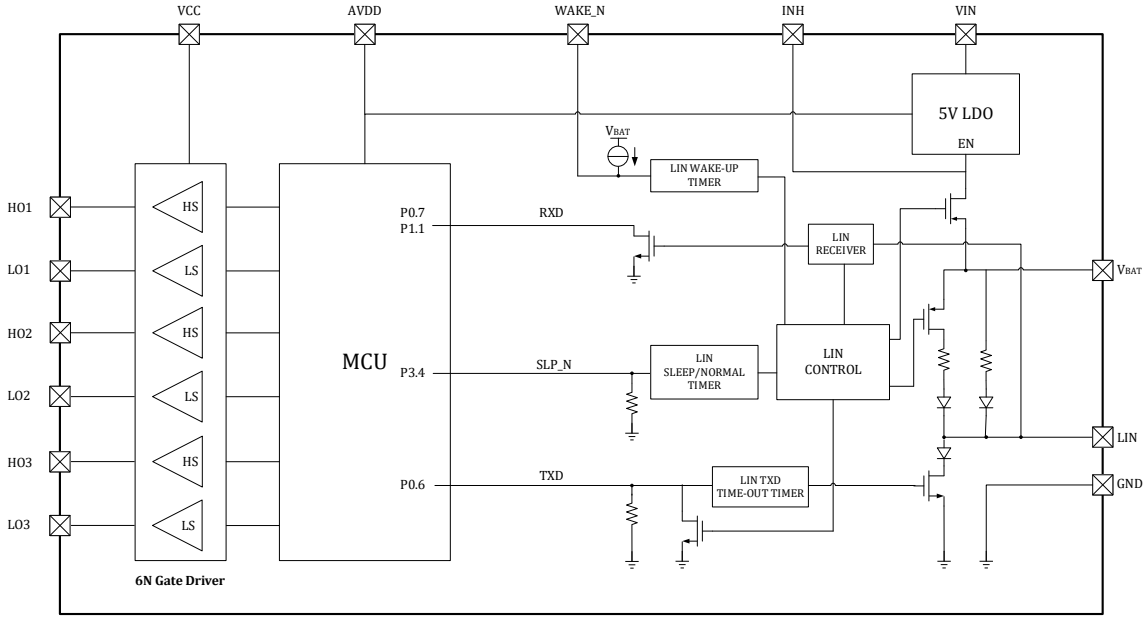

Fig. 21-1 Power supply and sleep related pin description

The RXD pins of the LIN transceiver are connected to P0.7(UART_RXD) and P1.1(GPIO WAKE), the TXD pins are connected to P0.6 (UART_TXD), and the P3.4 controls the SLP_N pins of the transceiver.

In normal mode, when SLP_N signal appears a falling edge, and the level retention time of SLP_N is longer than 10us, and the pin of WAKE_N is high, LIN-PHY enters the sleep mode. In sleep mode, the INH signal will always be in the suspended state, while in other modes, the INH pin is at high level.

According to the application of INH/EN pin can be an external pull or pulldown resistor. When the external pull-down resistance is connected, after LIN-PHY sleep, the INH signal is lowered by the external pull-down resistance, 5V LDO is turned off, and no longer supplies power to MCU through AVDD. In this case, smaller dormant power consumption can be achieved (VIN current of 5V LDO power supply < 1uA).When the external pull-up resistor is attached, after the LIN-PHY sleeps, the 5V LDO still supplies power to the MCU, and the MCU can go to sleep.

VCC is the integrated predrive power supply inside the chip. It is not affected during sleeping and can be powered off during sleeping.

The VBAT powers the chip LIN-PHY independently and the VIN powers the 5V LDO.It usually does not lose power when sleeping.

The LIN TXD pin is equipped with a 500kΩ pulldown resistor, the SLP_N pin is equipped with a 500kΩ pulldown resistor, and the WAKE_N pin is equipped with a 500kΩ pullup resistor.

The LIN transceiver has four main operating modes, which are sleep mode, standby mode, normal mode and power on mode.

Sleep mode: This mode is the mode with the lowest power consumption. It can be woken up remotely by LIN pin, locally by WAKE_N pin, or directly by SLP_N pin. The necessary conditions for wakening in sleep mode are as follows: the remote wakening time through LIN pin must be longer than twake(dom)LIN(LIN wake-up time 150μs); The local wake time of the WAKE_N pin must be greater than twake(dom)WAKE_N(WAKE_N wake-up time 60μs). The direct wake-up time through the SLP_N pin must be greater than tgotonorm(10μs). Once the LIN-PHY is awakened, the MCU core can be further awakened by P1.1 pins.

Standby mode: When the device is in sleep mode, if a local or remote wake up event is detected, the device will automatically enter standby mode immediately. The low level on the RXD pin will indicate the wake up process. The INH pin is set to high after the device moves from sleep mode to standby mode.

If the SLP_N pin is set to high level in standby mode, the following situations may occur:

(1) Immediately reset the wake source flag; Causes the strong pull-down state that may exist on the TXD to be released before the actual mode switch is performed (after $t_{gotonorm}$).

(2) When the high level maintenance time on the SLP_N pin exceeds the $t_{gotonorm}$, the device enters the normal mode.

(3) The wake up request signal on the RXD pin is reset immediately.

Normal mode: LIN bus level is 12V. When LIN receives, it is converted to 5V and sent to MCU via RXD. When transmitting, MCU TXD is converted to 12V and output to bus. In sleep, standby, or power-on mode, the device will enter normal mode as long as the high level of the SLP_N pin is maintained longer than the $t_{gotosleep}$. If the low level hold time on the SLP_N pin is greater than $t_{gotosleep}$(10μs), the device switches to sleep mode.

Power-on mode: When in power-on mode, the RXD pin is suspended and the TXD pin is weakly pulled down, but neither the transmitter nor the receiver is activated. If the high level holding time of the SLP_N pin is longer than that of $t_{gotosleep}$, the device enters normal mode.

In normal mode, when the SLP_N pin has a falling edge and the low level maintenance time of SLP_N is greater than $t_{gotosleep}$, the sleep mode is entered. In sleep mode, the INH pin will always be in

the suspended state. In other modes, the INH pin is at a high level. EN can be enabled by external pull-up or pull-down resistance control 5V LDO. If the external connection is pulled up, 5v LDO will always maintain power supply; if it is pulled down, it will stop power supply to MCU during sleep, and the overall sleep power consumption of the chip will be lower.

22 General Peripherals

- Two UART, full-duplex operation, support 7/8 data bit, 1/2 stop bit, odd/even/no parity mode, with 1 byte tx buffer, 1 byte rx buffer, support Multi-drop Slave/Master mode, support 300 to 115200 baud rate
- One SPI, support master-slave mode
- One IIC, support master-slave mode
- One CAN-bus
- Hardware watchdog, driven by 32kHz RC clock and which is independent of system high-speed clock, with write protection and 2/4/8/64 seconds reset interval.

23 Gate Driver Module

23.1 Module Parameter

23.1.1 LKS32AT089XLN8Q9(YYWWXC)

Table 23-1 KS32AT089XLN8Q9(YYWWXC) Module Parameter

Parameter	Min	Typ	Max	Unit	Description
Absolute Maximum Ratings					
Low side and logic fixed supply VCC	-0.3		+25.0	V	To ground
High side floating supply VB	-0.3		+250	V	
High side offset VS	VB-25		VB+0.3	V	
High side output $HO_{1,2,3}$	VS-0.3		VB+0.3	V	
Low side output $LO_{1,2,3}$	-0.3		VCC+0.3	V	
Logic input $HIN/LIN_{1,2,3}$	-0.3		VCC+0.3	V	Lower of +15V or VCC+0.3
Allowable offset voltage slew rate dVs/dt			50	V/ns	
Junction temperature TJ	-40		150	℃	
Storage temperature Ts	-55		150	℃	
Lead temperature			300	℃	Soldering for 10s
Recommended Operating Conditions					
Low side and logic fixed supply VCC	+7		+20	V	To ground
High side floating supply VB	VS+8		VS+20	V	
High side offset VS	-5		200	V	
High side output $HO_{1,2,3}$	VS		VB	V	
Low side output $LO_{1,2,3}$	0		VCC	V	
Logic input $HIN/LIN_{1,2,3}$	0		VCC	V	
Ambient temperature T_A	-40		125	℃	
Gate driver Electrical Characteristic					
Quiescent VCC supply current		50	100	uA	HIN=LIN=0V
Quiescent VBS supply current		20	40	uA	HIN=LIN=0V
Floating supply leakage I_{LK}			10	uA	VB=VS=220V
VCC supply under-voltage trigger voltage	3.6	4.9	6.4	V	
VBS supply under-voltage trigger voltage	3.5	4.8	6.2	V	
VCC supply under-voltage hysteresis voltage	0.25	0.5	0.8	V	

VBS supply under-voltage hysteresis voltage	0.25	0.5	0.8	V	
High level input threshold voltage V_{IH}	2.8			V	
Low level input threshold voltage V_{IL}			0.8	V	
Input bias current I_{source}		32	120	uA	HIN=LIN=5V
Input bias current I_{sink}			1	uA	HIN=LIN=0V
High level output, V_{BIAS}-V_O			1	V	I_O=20mA
Low level output, V_O			1	V	I_O=20mA
High level output short current I_{O+}	650	1000		mA	V_{CC}/V_{BS}=15V
Low level output short current I_{O-}	650	1000		mA	V_{CC}/V_{BS}=15V
Turn-on propagation delay T_{on}		270	500	ns	
Turn-off propagation delay T_{off}		80	150	ns	
Turn-on rise time T_r		15	30	ns	C_L=1nF
Turn-off fall time T_f		12	30	ns	
Dead time D_T	100	200	400	ns	
Delay matching M_T			80	ns	T_{on} & T_{off} for (HS-LS)

[1]YYWW is date code on chip package

23.2 Recommended Application Diagram

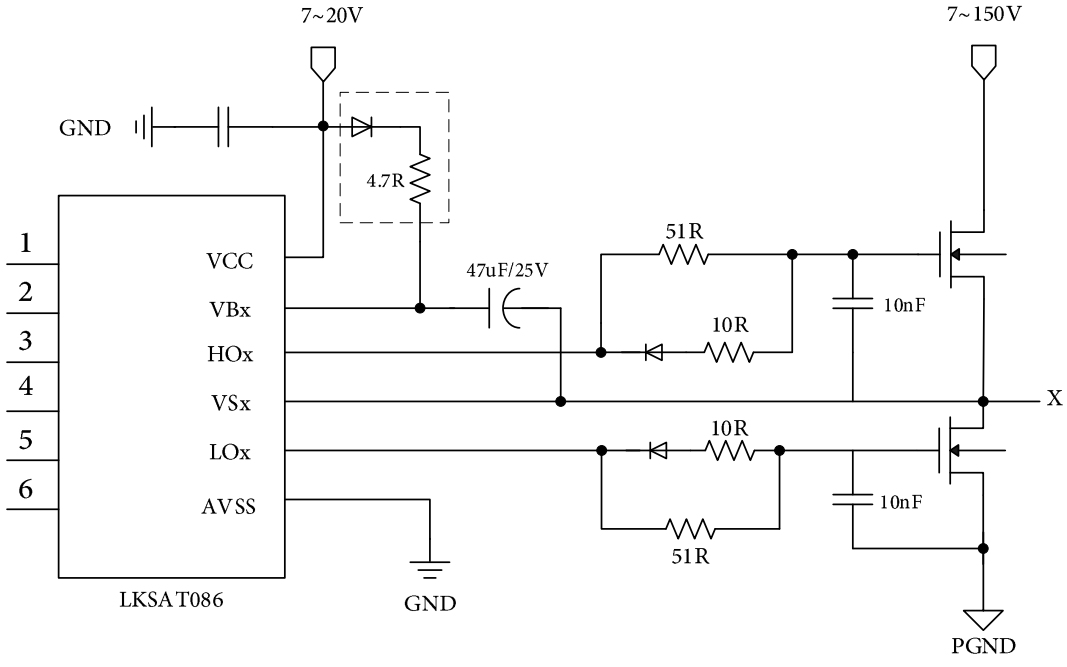

Fig. 23-1LKS32AT089XLN8Q9 Application Diagram

Only the gate drive module pins are shown in the figure, where x = 1,2,3 corresponding to the three sets of MOS gate drive outputs. The application diagram of each set is shown in Fig. 23-1.

Table 23-2 Gate Driver Module LIN/HIN V.S. MCU Pin

Gate Driver Input	LKS32AT089XLN8Q9	Note
LIN1	P1.5	P3.13 should be output enabled
HIN1	P1.4	
LIN2	P1.7	P1.12 should be output enabled
HIN2	P1.6	
LIN3	P1.9	P1.15 should be output enabled
HIN3	P1.8	

Gate driver input-output transfer function:

Table 23-3LKS32AT089XLN8Q9 truth table

{HIN,LIN}	HO	LO	
00	0	0	Low side and high side are all off
01	0	1	Low side on
10	1	0	High side on
11	0	0	Low side and high side are all on, which will trigger short protection

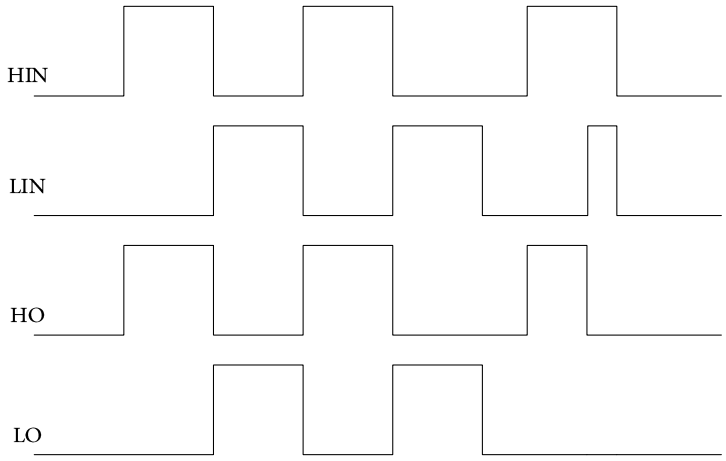

Fig. 23-2LKS32AT089XLN8Q9 polarity illustration

24 Special IO Multiplexing

Notes for Special IO Multiplexing of LKS08x

The SWD protocol includes two signals: SWCLK and SWDIO. SWCLK is a clock signal. To the chip, it is an input and will always be an input. SWDIO is a data signal. It switches between the input state and the output state during data transmission, and the default is the input state.

Users could use two IOs of SWD as GPIOs P0.0/P2.15. The precautions are as follows:

- The default state of GPIO multiplexing is disabled, IO are used as SWD. After the hard reset of the chip, the initial state of IOs are SWD. Both IOs of SWD are fixed pull-up inside the chip (the internal pull-up resistor of the chip is about 10K). Please pay attention to the initial IO voltage level if application has specific requirements.
- When GPIO multiplexing is enabled, tools such as KEIL cannot directly access the chip, i.e., the Debug and erase download functions cannot access the chip since SWD are now general GPIO. If the program needs to be downloaded again, there are two solutions.
- Firstly, it is recommended to use Linko's dedicated offline downloader to erase. It is recommended to leave a certain margin before switching SWD to GPIO, such as about 100ms, to ensure that the offline downloader can erase the chip and prevent the deadlock. This margin is to ensure a successful offline downloader erasing. A greater margin means a greater probability of the successful one-time erasion.
- Secondly, the application should have a GPIO multiplexing exit mechanism. For example, some other IO invert (usually input), indicates that the SWDIO is required externally, and the software needs to be reconfigured to disable the multiplexing. At this moment, the KEIL function can access the chip via SWD again.

When SWDCLK and SWDIO pins are used as GPIO, they should not act at the same time. That is, when SWDCLK multiplexing is enabled and changes, SWDIO can remain at level 0 (similar to time division multiplexing).

For RSTN signal, the default is for the external reset pin of LKS08x chip.

LKS08x allow users to multiplex RSTN as other IOs, and the multiplexed IO is P0.2. The precautions are as follows:

- The default state of reset IO multiplexing is disabled, and the software needs to write 1 to SYS_RST_CFG[5] to multiplex RSTN as GPIO. I.e., the initial state of P0[2] is RSTN. RSTN is provided with a pull-up resistor inside the chip (the internal pull-up resistor of the chip is about 100K). Attention shall be paid when the application has requirements for initial electric level.
- The default state of P0[2] is used as external reset, and the program can only be executed after the RSTN is released. The application needs to ensure that the RSTN has sufficient protection, such as the peripheral circuit with a pull-up resistor. It is better to add a capacitor.
- After RST IO multiplexing is enabled, the external reset is unavailable to the chip. If a hard reset is required, the reset source can only be power-down/watchdog reset.
- The multiplexing of RSTN does not affect the use of KEIL.

25 Ordering Information

Device	Package Size	Quantity per disc/tube	Quantity in box	Quantity in case
LKS32AT089XLN8Q9	QFN6*6 52L-0.55	490/disc	4900PCS	29400PCS

26 Version History

Table 26-1 Document's Version History

Date	Version No.	Description
2024.06.05	1.04	Update ESD level
2023.12.12	1.03	Added description of pull-up resistance values
2023.11.09	1.02	OPA OFFSET Adds the description, Renewal storage temperature
2023.07.09	1.01	Remove the statement‘SLP_N is not recommended to sleep if INH drops down’
2023.05.23	1.0	Initial Version

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