Rochester Electronics

Datasheet

PART NUMBER

54HC4060E-ROCV

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Delete vendor CAGE 27014. Change vendor CAGE 18714 to 34371. Technical changes in table I. Editorial changes throughout.	91-12-17	

REV																									
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REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A										
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14										

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
87-11-25

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, HIGH-SPEED CMOS, COUNTER, BINARY 14 STAGE, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-87680

SHEET 1 OF 14

DESC FORM 193
SEP 87

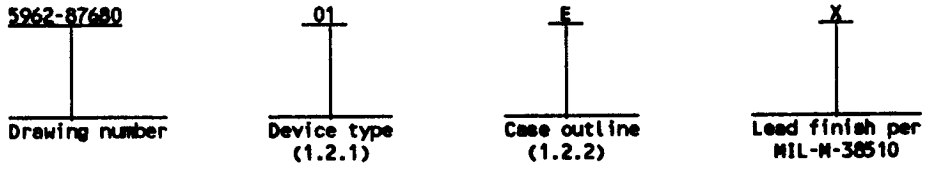
* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1763

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54HC4060	Counter, binary, 14 stage

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, andas follows:

Outline letter	Case outline
E	D-2 (16-lead, .840" x .310" x .200"), dual-in-line package
2	C-2 (20-terminal, .358" x .358" x .100"), square chip carrier package

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage	-0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage	-0.5 V dc to V_{CC} + 0.5 V dc
Clamp diode current	±20 mA
DC output current (per pin)	±25 mA
DC V_{CC} or GND current (per pin)	±50 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 2/	500 mW
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J)	+175°C

1/ Unless otherwise specified, all voltages are referenced to ground.

2/ For T_C = +100°C to +125°C, derate linearly at 8 mW/°C to 300 mW.

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+2.0 V dc to +6.0 V dc
Case operating temperature range (T_C)	-55°C to +125°C

Input rise and fall time:

V_{CC} = 2.0 V	0 to 1000 ns
V_{CC} = 4.5 V	0 to 500 ns
V_{CC} = 6.0 V	0 to 400 ns

Minimum removal time, reset inactive to clock (t_{rem}):

T_C = +25°C:

V_{CC} = 2.0 V	160 ns
V_{CC} = 4.5 V	32 ns
V_{CC} = 6.0 V	27 ns

T_C = -55°C to +125°C:

V_{CC} = 2.0 V	240 ns
V_{CC} = 4.5 V	48 ns
V_{CC} = 6.0 V	41 ns

Minimum clock pulse width (t_{w1}):

T_C = +25°C:

V_{CC} = 2.0 V	90 ns
V_{CC} = 4.5 V	18 ns
V_{CC} = 6.0 V	15 ns

T_C = -55°C to +125°C:

V_{CC} = 2.0 V	135 ns
V_{CC} = 4.5 V	27 ns
V_{CC} = 6.0 V	23 ns

Minimum reset pulse width (t_{w2}):

T_C = +25°C:

V_{CC} = 2.0 V	90 ns
V_{CC} = 4.5 V	18 ns
V_{CC} = 6.0 V	15 ns

T_C = -55°C to +125°C:

V_{CC} = 2.0 V	135 ns
V_{CC} = 4.5 V	27 ns
V_{CC} = 6.0 V	23 ns

Maximum frequency (f_{max}):

T_C = +25°C:

V_{CC} = 2.0 V	4 MHz minimum
V_{CC} = 4.5 V	20 MHz minimum
V_{CC} = 6.0 V	24 MHz minimum

T_C = -55°C to +125°C:

V_{CC} = 2.0 V	2.6 MHz minimum
V_{CC} = 4.5 V	13.0 MHz minimum
V_{CC} = 6.0 V	15.0 MHz minimum

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawing (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
High-level output voltage Q4-Q10, Q12-Q14 2/	V_{OH1}	$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $\lvert I_O \rvert \le 20\ \mu A$	$V_{CC} = 2.0$ V	1, 2, 3	1.9		V
			$V_{CC} = 4.5$ V		4.4		
			$V_{CC} = 6.0$ V		5.9		
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $\lvert I_O \rvert \le 4.0$ mA	$V_{CC} = 4.5$ V		3.7		
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $\lvert I_O \rvert \le 5.2$ mA	$V_{CC} = 6.0$ V		5.2		
Low-level output voltage Q4-Q10, Q12-Q14 2/	V_{OL1}	$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $\lvert I_O \rvert \le 20\ \mu A$	$V_{CC} = 2.0$ V	1, 2, 3		0.1	V
			$V_{CC} = 4.5$ V			0.1	
			$V_{CC} = 6.0$ V			0.1	
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $\lvert I_O \rvert \le 4.0$ mA	$V_{CC} = 4.5$ V			0.4	
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $\lvert I_O \rvert \le 5.2$ mA	$V_{CC} = 6.0$ V			0.4	
High-level output voltage Osc OUT 1 and Osc OUT 2 2/ 3/	V_{OH2}	$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $\lvert I_O \rvert = 20\ \mu A$	$V_{CC} = 2.0$ V	1, 2, 3	1.9		V
			$V_{CC} = 4.5$ V		4.4		
		$V_{IN} = 5.0$ V or 0.8 V, $\lvert I_O \rvert = 20\ \mu A$	$V_{CC} = 6.0$ V		5.9		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
High-level output voltage Osc OUT 1 and Osc OUT 2 2/ 3/	V_{OH2}	$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $\lvert I_O \rvert \le 2.6$ mA	$V_{CC} = 4.5$ V Osc OUT 1	1,2,3	3.7		V
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $\lvert I_O \rvert \le 2.6$ mA	$V_{CC} = 4.5$ V Osc OUT 2		3.7		
		$V_{IN} = 5.0$ V or 0.8 V $\lvert I_O \rvert = 3.3$ mA	$V_{CC} = 6.0$ V Osc OUT 1		5.2		
		$V_{IN} = 5.0$ V or 0.8 V $\lvert I_O \rvert = 3.3$ mA	$V_{CC} = 6.0$ V Osc OUT 2		5.2		
Low-level output voltage Osc OUT 1 and Osc OUT 2 2/ 3/	V_{OL2}	$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $\lvert I_O \rvert = 20$ µA	$V_{CC} = 2.0$ V	1, 2, 3		0.1	V
			$V_{CC} = 4.5$ V			0.1	
		$V_{IN} = 5.0$ V or 0.8 V, $\lvert I_O \rvert = 20$ µA	$V_{CC} = 6.0$ V			0.1	
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $\lvert I_O \rvert \le 2.6$ mA	$V_{CC} = 4.5$ V Osc OUT 1			0.4	
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $\lvert I_O \rvert \le 2.6$ mA	$V_{CC} = 4.5$ V Osc OUT 2			0.4	
		$V_{IN} = 5.0$ V or 0.8 V $\lvert I_O \rvert = 3.3$ mA	$V_{CC} = 6.0$ V Osc OUT 1			0.4	
		$V_{IN} = 5.0$ V or 0.8 V $\lvert I_O \rvert = 3.3$ mA	$V_{CC} = 6.0$ V Osc OUT 2			0.4	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
High-level input voltage	V_{IH}	4/	V_{CC} = 2.0 V	1, 2, 3	1.5		V
			V_{CC} = 4.5 V		3.15		
			V_{CC} = 6.0 V		4.2		
Low-level input voltage	V_{IL}	4/	V_{CC} = 2.0 V	1, 2, 3		0.3	V
			V_{CC} = 4.5 V			0.9	
			V_{CC} = 6.0 V			1.2	
Input capacitance	C_{IN}	V_{CC} = GND, see 4.3.1c		4		10	pF
Quiescent current	I_{CC}	V_{CC} = 6.0 V; V_{IN} = V_{CC} or GND		1, 2, 3		160	µA
Input leakage current	I_{IN}	V_{CC} = 6.0 V; V_{IN} = V_{CC} or GND		1, 2, 3		±1.0	µA
Functional tests		see 4.3.1d		7			
Propagation delay time CLOCK to Q4 5/	t_{PHL1}, t_{PLH1}	C_L = 50 pF minimum See figure 4	V_{CC} = 2.0 V	9		530	ns
			V_{CC} = 4.5 V			106	
			V_{CC} = 6.0 V			90	
			V_{CC} = 2.0 V	10, 11		795	
			V_{CC} = 4.5 V			159	
			V_{CC} = 6.0 V			135	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Propagation delay time Qn to Qn + 1 5/	t_{PHL2}, t_{PLH2}	C_L = 50 pF minimum See figure 4	V_{CC} = 2.0 V	9		125	ns
			V_{CC} = 4.5 V			25	
			V_{CC} = 6.0 V			21	
			V_{CC} = 2.0 V	10, 11		190	
			V_{CC} = 4.5 V			38	
			V_{CC} = 6.0 V			32	
Propagation delay time RESET to any Q 5/	t_{PHL3}, t_{PLH3}	C_L = 50 pF minimum See figure 4	V_{CC} = 2.0 V	9		240	ns
			V_{CC} = 4.5 V			48	
			V_{CC} = 6.0 V			41	
			V_{CC} = 2.0 V	10, 11		360	
			V_{CC} = 4.5 V			72	
			V_{CC} = 6.0 V			61	
Transition time 6/	t_{THL}, t_{TLH}	C_L = 50 pF minimum See figure 4	V_{CC} = 2.0 V	9		75	ns
			V_{CC} = 4.5 V			15	
			V_{CC} = 6.0 V			13	
			V_{CC} = 2.0 V	10, 11		110	
			V_{CC} = 4.5 V			22	
			V_{CC} = 6.0 V			19	

See footnotes on next page.

TABLE I. Electrical performance characteristics - Continued.

1/ For a power supply of 5.0 V ±10 percent the worst case output voltage (V_{OH} and V_{OL}) occur for HC at 4.5 V. Thus the 4.5 V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V respectively. (The V_{IH} value at 5.5 V is 3.85 V). The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0 V values should be used. Power dissipation capacitance (C_{PD}), typically 100 pF, determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

2/ V_{CC} = 2.0 V and V_{CC} = 6.0 V shall be guaranteed, if not tested, to the specified limits in table I.

3/ Outputs Osc OUT 1 and Osc OUT 2 are not designed to be used to drive an external device.

4/ V_{IH} and V_{IL} tests are not required to be tested and shall be applied as forcing functions for the V_{OH} or V_{OL} tests.

5/ AC testing at V_{CC} = 2.0 V and V_{CC} = 6.0 V shall be guaranteed, if not tested, to the specified limits in table I.

6/ Transition time (t_{TLH}, t_{THL}), if not tested, shall be guaranteed to the specified limits in table I.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot ofmicrocircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

Device type	01	
Case outlines	E	2
Terminal number	Terminal symbol	
1	Q12	NC
2	Q13	Q12
3	Q14	Q13
4	Q6	Q14
5	Q5	Q6
6	Q7	NC
7	Q4	Q5
8	GND	Q7
9	OUT 2	Q4
10	OUT 1	GND
11	CLOCK	NC
12	RESET	OUT 2
13	Q9	OUT 1
14	Q8	CLOCK
15	Q10	RESET
16	V_{CC}	NC
17	---	Q9
18	---	Q8
19	---	Q10
20	---	V_{CC}

FIGURE 1. Terminal connections.

Device type 01

CLOCK	RESET	Output state
⎍	L	No change
⎎	L	Advance to next state
X	H	All outputs are low

FIGURE 2. Truth table.

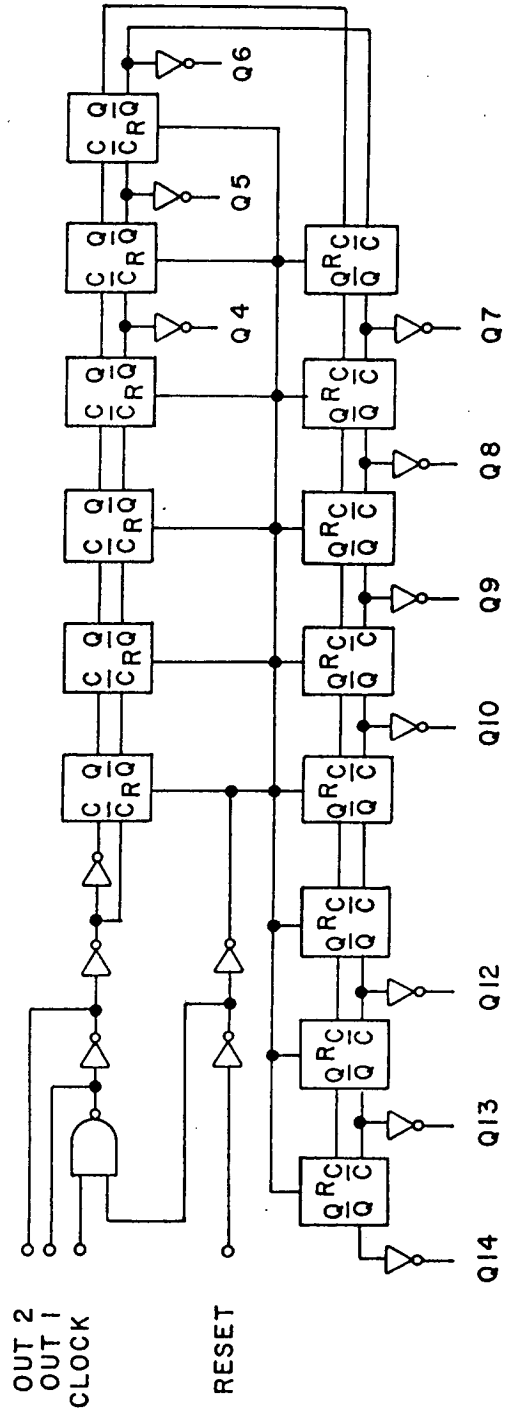


FIGURE 3. Logic diagram.

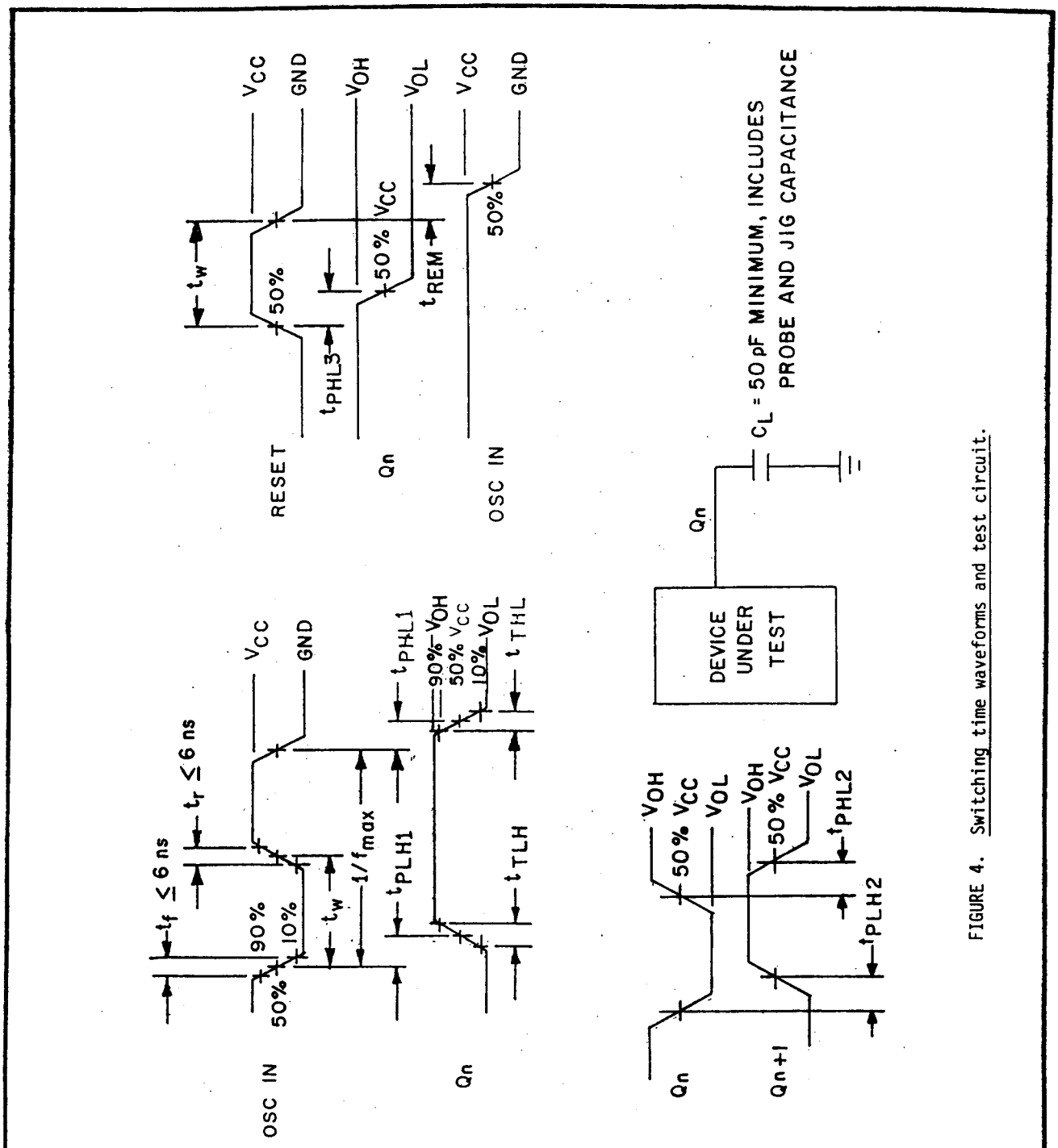


FIGURE 4. Switching time waveforms and test circuit.

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4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Test all applicable pins on 5 devices with zero failures.

d. Subgroups 7 and 8 tests shall verify the truth table as specified on figure 2 herein.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1,2,3,4,7,8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroup 10 and 11, if not tested shall be guaranteed to the specified limits in table 1

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8525.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.