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Nyfea product specification

PRODUCT SPECIFICATION

产品规格书

Customer 客户名称： _____

Product Name品名： Real Time Clock

PART NO. 型号规格： FRTC1339M

Issue Date发布日期： _____

Prepared 制作	Checked 审核	Customer Check客户核准
ChenTT	Zelig	

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Features

- Real-time clock (RTC) counts seconds,minutes, hours, day, date, month, and year
- with leap-year compensation valid up to 2100
- 2-wire serial interface
- Two time-of-day alarms
- Programmable square-wave output
- Oscillatorstop flag
- Automatic power-fail detect and switch circuitry
- Trickle charge capability
- Operating Temperature: -40 ~ 125℃

Applications

- Handhelds (GPS, POS Terminal)
- Consumer Electronics (Set-Top Box, Digital Recording, Network Appliance)
- Office Equipment (Fax/Printer, Copier)
- Medical (Glucometer, Medicine Dispenser)
- Telecommunications (Router, Switcher, Server)

Description

The FRTC1339M serial real-time clock is a low- power clock/date device with two programmable time-of-day alarms and a programmable square- wave output. Address and data are transferred serially by a 2-wire bidirectional bus . The clock/date provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days , including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. The FRTC1339M has a built-in power- sense circuit that detects power failures and automatically switches to the backup supply.

Ordering Information

Ordering Code	Package	Package Description
FRTC1339M	MSOP-8	Pitch 0.65mm

Pb-free and Green

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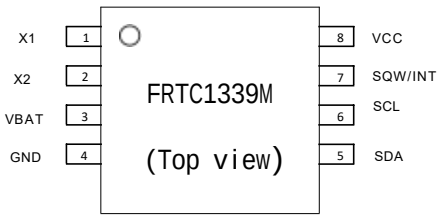
Pin Configurations



MSOP8(Top view)

Pin Name	Pin No.	Description
X1	1	32 . 768 kHz Crystal Connection
X2	2	
V_{BACKUP}	3	Secondary Power Supply
GND	4	Ground
SDA	5	Serial Data.
SCL	6	Serial Clock.
SQW	7	Square-Wave/ Interrupt Output ,Open drain
V_{CC}	8	Power Supply

Marking information

Marking	Information
FRTC	Part number: FRTC
1339M	1339M
YYWW	date code

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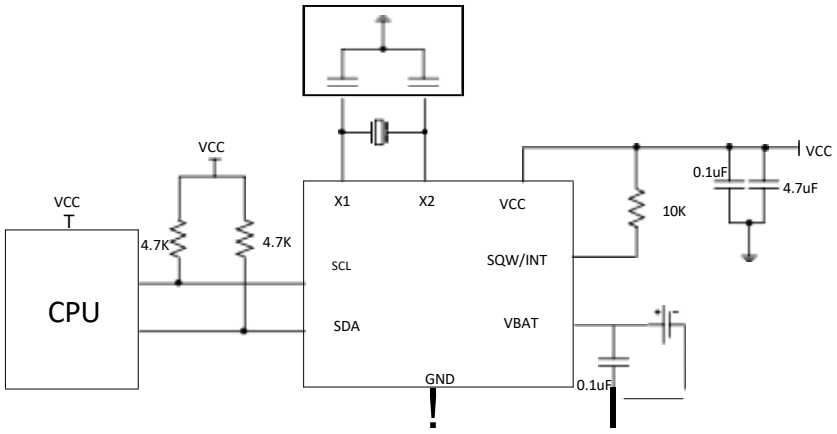
Typical Application Circuit



Notes:

1. It is recommended to add 0.1uf capacitor to VBAT pin.
2. If the time accuracy requirement is high, please reserve the crystal matching capacitor.

Maximum Ratings

Symbol	Parameter	Min	TYP	Max	Unit
T_{store}	Storage Temperature	-55	-	+125	°C
T_{op}	Operating Temperature Range	-40	-	+85	°C
V_{IN}	Voltage Range on Any Pin Relative to Ground	-0.3	-	6	V

Note:
Stresses greater than those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

(TA = -40°C to +85°C)

Symbol	Parameter	Conditions	Min	TYP	Max	Unit
V_{CC}	Supply Voltage	FRTC1339M	2.97	3.3	5.5	V
V_{IH}	SCL/SDA pins		0.7 x V_{CC}	-	V_{CC} + 0.5	V
V_{IL}	SCL/SDA pins		-0.5	-	+0.3 x VCC	V
V_{PF}	Power-Fail Voltage	FRTC1339M	2.70	2.85	2.97	V
V_{BACKUP}	Backup supply Voltage		1.4	3.0	3.7	V

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DC Electrical Characteristics

Unless otherwise specified, -40°C≤T_A≤ 85°C, ($V_{CC(MIN)}$ ≤V_{CC}≤ $V_{CC(MAX)}$)

Symbol	Parameter	Test Conditions*1	MIN	TYP	MAX	Unit
I_{LI}	Input Leakage	SCL only	-	-	1	μA
I_{LO}	I/O Leakage	SDA and SQW/INT		-	1	μA
I_{OL}	Logic 0 Out: SDA and SQW/INT	V_{OL} = 0.4V, V_{CC} > 2.0V	3	-		mA
	Logic 0 Out: SDA and SQW/INT	V_{OL} = 0.2 (V_{CC}),V_{CC} ⩽2.0V	3	-		mA
	Logic 0 Out: SDA and SQW/INT	V_{OL} = 0.2 (V_{CC}) 1.3V < V_{CC} < 1.8V	250	-		μA
I_{CCA}	V_{CC} Active Current*2		-	-	450	μA
I_{CCS}	V_{CC} Standby Current*3		-	80	150	μA
R1	Trickle Charge Resistor Register	10h = A5h, V_{CC} = Typ, V_{BACKUP} = 0V		250		Ω
R2	Trickle Charge Resistor Register	10h = A6h, V_{CC} = Typ, V_{BACKUP} = 0V		2000		Ω
R3	Trickle Charge Resistor Register	10h = A7h, V_{CC} = Typ, V_{BACKUP} = 0V		4000		Ω
I_{BKLKG}	V_{BACKUP} Leakage Current			25	100	nA
I_{BKOSC}	V_{BACKUP} Current*4	V_{CC} = 0V, EOSC = 0, SQW Off		400	700	nA
I_{BKSQW}	V_{BACKUP} Current*4	V_{CC} = 0V, EOSC = 0, SQW On		600	1000	nA
I_{BKDR}	V_{BACKUP} Current*4	V_{CC} = 0V, EOSC = 1		10	100	nA

Note:
1. Limits at -40°C are guaranteed by design and not production tested.
2. I_{CCA}: SCL at f_{SC} max, V_{IL} = 0.0V, V_{IH} = V_{CC}, trickle charge disabled.
3. Specified with 2-wire bus inactive, V_{IL} = 0.0V, V_{IH} = V_{CC}, trickle charge disabled.
4. Using recommended crystal on X1 and X2.

Crystal Specifications*1

Symbol	Parameter	MIN	TYP	MAX	Units
f_O	Nominal Frequency		32.768		kHZ
ESR	Series Resistance			70	kΩ
C_L	Load Capacitance		6		pF

Note:
1. The crystal, traces, and crystal input pins should be isolated from RF generating signals.

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AC Electrical characteristics

(T_A = -40°C to +85°C) *1 V_{CC} = MIN to MAX

Symbol	Parameter	Test Conditions*1	MIN	TYP	MAX	Unit
f_{SCL}	SCL Clock Frequency	Fast mode	100		400	kHz
		Standard mode			100	kHz
t_{BUF}	Bus Free Time Between STOP and START Condition	Fast mode	1.3			µs
		Standard mode	4.7			
$t_{HD:STA}$	Hold Time (Repeated) START Condition*2	Fast mode	0.6			µs
		Standard mode	4.0			
t_{LOW}	LOW Period of SCL Clock	Fast mode	1.3			µs
		Standard mode	4.7			
t_{HIGH}	HIGH Period of SCL Clock	Fast mode	0.6			µs
		Standard mode	4.0			
$t_{SU:STA}$	Setup Time for Repeated START Condition	Fast mode	0.6			µs
		Standard mode	4.7			
$t_{HD:DAT}$	Data Hold Time*3/4	Fast mode	0		0.9	µs
		Standard mode	0			
$t_{SU:DAT}$	Data Setup Time*5	Fast mode	100			ns
		Standard mode	250			
t_R	Rise Time of Both SDA and SCL Signals *6	Fast mode	20 + 0.1C_B		300	ns
		Standard mode	20 + 0.1C_B		1000	
t_F	Fall Time of Both SDA and SCL Signals *6	Fast mode	20 + 0.1C_B		300	ns
		Standard mode	20 + 0.1C_B		300	
$t_{SU:STO}$	Setup Time for STOP Condition	Fast mode	0.6			µs
		Standard mode	4.0			
C_B	Capacitive Load for Each Bus Line*6				400	pF
$C_{I/O}$	I/O Capacitance (SDA, SCL) *7			10		pF
t_{OSF}	Oscillator Stop Flag (OSF) Delay*8			100		ms

Note:

1. Limits at -40°C are guaranteed by design and not production tested.
2. After this period, the first clock pulse is generated
3. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL
4. The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
5. A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \geqslant$ to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R\ MAX} + t_{SU:DAT}$ = 1000 + 250 = 1250ns before the SCL line is released.
6. C_B—total capacitance of one bus line in pF
7. Guaranteed by design. Not production tested
8. The parameter t_{OSF} is the time period the oscillator must be stopped for the OSF flag to be set over the voltage range of $V_{CC\ MIN}$V $\leqslant V_{CC} \leqslant V_{CC\ MAX}$ and 1.4V $\leqslant V_{BAT} \leqslant$ 3.7V

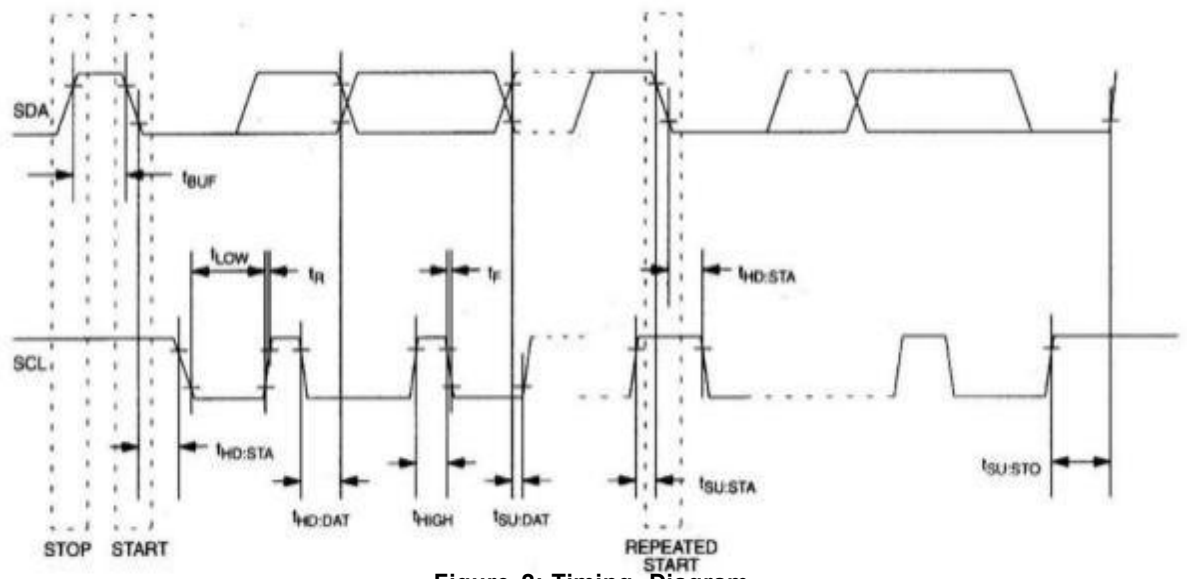

Figure 2: Timing Diagram

Power-Up/Power-Down Characteristics

(TA = -40°C to +85°C) *1

Symbol	Parameter	Test Conditions*1	MIN	TYP	MAX	Unit
t_{REC}	Recovery at Power-Up*2				2	ms
t_{VCCF}	V_{CC} Fall Time	$V_{PF(MAX)}$ to $V_{PF(MIN)}$	300			μs
t_{VCCR}	V_{CC} Rise Tim	$V_{PF(MIN)}$ to $V_{PF(MAX)}$	0			μs

Note:
1. Limits at -40°C are guaranteed by design and not production tested.
2. This delay applies only if the oscillator is enabled and running. If the oscillator is disabled or stopped, no power-up delay occurs.

Test Circuits

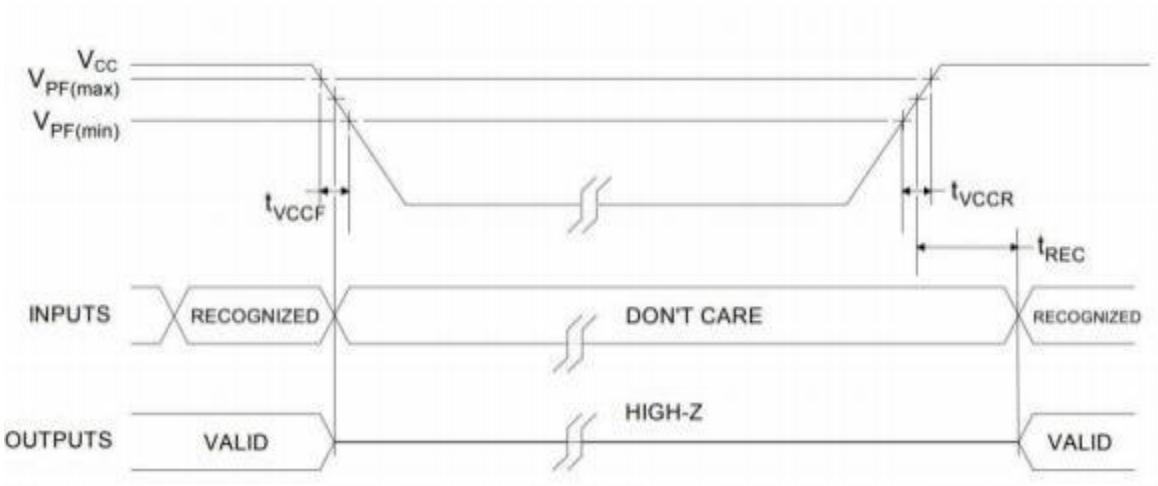

Figure 3: Power-Up/Power-Down Timing

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Functional Description

The FRTC1339M serial real-time clock is a low-power clock/date device with two programmable time-of-day alarms and a programmable square-wave output. Address and data are transferred serially by a 2-wire bidirectional bus. The clock/date provides seconds, minutes, hours , day, date, month , and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/ PM indicator. The FRTC1339M has a built-in power-sense circuit that detects power failures and automatically switches to the backup supply

Application Information

The FRTC1339M operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code followed by data. Subsequent registers can be accessed sequentially until a STOP condition is executed. The device is fully accessible and data can be written and read when V_{CC} is greater than V_{PF} . However, when V_{CC} falls below V_{PF} , the internal clock registers are blocked from any access. If V_{PF} is less than V_{BACKUP} , the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{PF} . IfV_{PF} is greater than V_{BACKUP} , the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{BACKUP} . The registers are maintained from the V_{BACKUP} source until V_{CC} is returned to nominal levels. The block diagram in Figure: Block Diagram shows the main elements of the serial real-time clock.

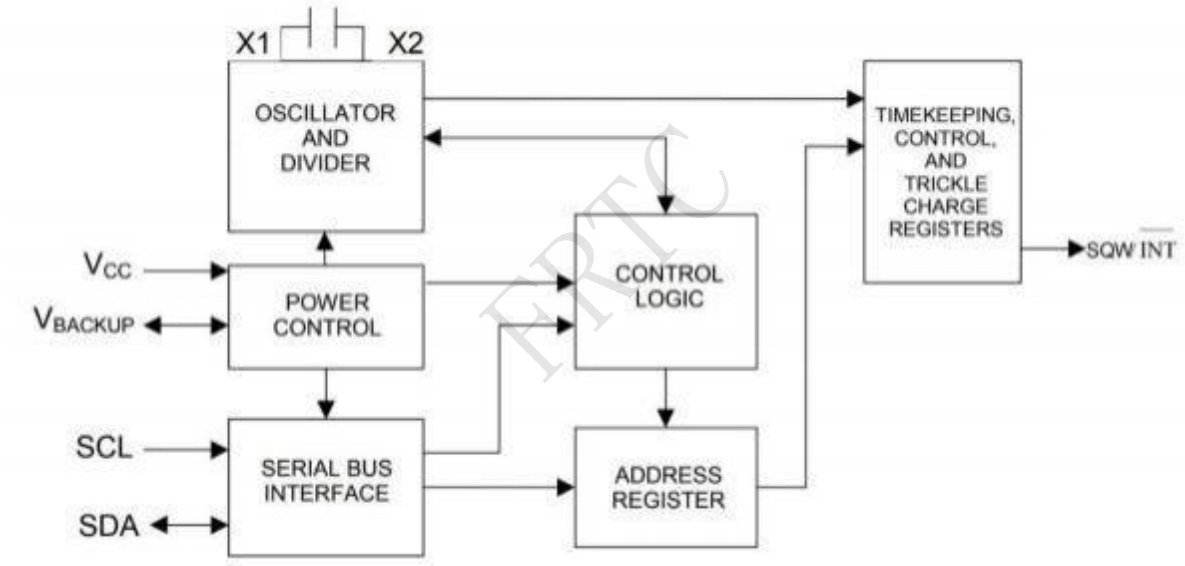

Figure 4: Block Diagram

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Signal Descriptions

V_{CC}, GND - DC power is provided to the device on these pins.

SCL (Serial Clock Input) - SCL is used to synchronize data movement on the serial interface.

SDA (Serial Data Input/Output) - SDA is the input/output pin for the 2-wire serial interface. The SDA pin is an open-drain output and requires an external pullup resistor.

V_{BACKUP} (Secondary Supply Input) - Connection for a secondary power supply. Supply voltage must be held between 1.4V and 3.7V for proper operation. This pin can be connected to a primary cell such as a lithium button cell. Additionally, this pin can be connected to a rechargeable cell or a super cap when used with the trickle charge feature.

SQW/ INT (Square-Wave/Interrupt Output) - Programmable square-wave or interrupt-output signal. The SQW/ INT pin is an open-drain output and requires an external pullup resistor.

X1, X2 - These signals are connections for a standard 32.768kHz quartz crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 6pF. The FRTC1339M can also be driven by an external 32.768kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.

The oscillator is controlled by an enable bit in the control register. Oscillator startup times are highly dependent upon crystal characteristics, PC board leakage, and layout. High ESR and excessive capacitive loads are the major contributors to long startup times. A circuit using a crystal with the recommended characteristics and proper layout usually starts within one second.

Clock Accuracy

The address map for the registers of the FRTC1339M is shown in below figure . The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error is added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit can result in the clock running fast.

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Address Map

During a multibyte access, when the address pointer reaches the end of the register space (10h), it wraps around to location 00h. On a 2- wire START, STOP, or address pointer incrementing to location 00h, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock can continue to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Function	Range
00H	0	10 Seconds			Seconds				Seconds	00-59
01H	0	10 Minutes			Minutes				Minutes	00-59
02H	0	12/24	AM/PM 10HR	10HR	Hour				Hours	1-12 +AM/PM 00-23
03H	0	0	0	0	0	Day			Day	1-7
04H	0	0	10 Date		Date				Date	00-31
05H	Century	0	0	10 Month	Month				Month/ Century	01-12 +Century
06H	10 Year				Year				Year	00-99
07H	A1M1	10 Seconds			Seconds				Alarm 1 Seconds	00-59
08H	A1M2	10 Minutes			Minutes				Alarm 1 Minutes	00-59
09H	A1M3	12/24	AM/PM 10 Hour	10 Hour	Hour				Alarm 1 Hours	1-12 +AM/PM 00-23
0AH	A1M4	DY/DT	10 Date		Day Date				Alarm 1 Day Alarm 1 Date	1-7 1-31
0BH	A2M2	10 Minutes			Minutes				Alarm 2 Minutes	00-59
0CH	A2M3	12/24	AM/PM 10 Hour	10 Hour	Hour				Alarm 2 Hours	1-12 +AM/PM 00-23
ODH	A2M4	DY/DT	10 Date		Day Date				Alarm 2 Day Alarm 2 Date	1-7 1-31
0EH	EOSC	0	BBSQI	RS2	RS1	INTCN	A2IE	A1IE	Control	-
0FH	OSF	0	0	0	0	0	A2F	A1F	Status	-
10H	TCS3	TCS2	TCS1	TCS0	DS1	DS0	ROUT1	ROUT0	Trickle Charge	-

Figure: FRTC1339M TIMEKEEPER REGISTERS

Note: Unless otherwise specified, the registers' state are not defined when power is first applied or V_{CC} and V_{BACKUP} falls below the V_{BACKUP} min.

All registers need to be initialized after power-on.

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Time And Date Operation

The time and date information is obtained by reading the appropriate register bytes. The real-time clock registers are illustrated in timekeeper registers. The time and date are set or initialized by writing the appropriate register bytes. The contents of the time and date registers are in the binary coded decimal (BCD) format. The FRTC1339M can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12-hour or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/ PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours). All hours values, including the alarms, must be re-entered whenever the 12/24-hour mode bit is changed. The century bit (bit 7 of the month register) is toggled when the years register overflows from 99 to 00. The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined, but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any START or STOP, and when the address pointer rolls over to 0. The countdown chain is reset whenever the seconds register is written. Write transfers occur on the acknowledge pulse from the device. To avoid rollover issues, once the countdown chain is reset, the remaining time and date registers must be written within one second. The 1Hz square-wave output, if enabled, transitions high 500 ms after the seconds data transfer, provided the oscillator is already running.

Alarms

The FRTC1339M contains two time-of-day/date alarms. Alarm 1 can be set by writing to registers 07h to 0Ah.Alarm 2 can
be set by writing to registers 0Bh to 0Dh. The alarms can be programmed (by the alarm enable and INTCN bits of the control register) to activate the SQW/ INT output on an alarm match condition. Bit 7 of each of the time-of-day/date alarm registers are mask bits. When all of the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers 00h-06h match the values stored in the time-of-day/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Below table shows the possible settings.

Configurations not listed in the table result in illogical operation. The DY/DT bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0 to 5 of that register reflects the day of the week or the date of the month. If DY/ DT is written to a logic 0, the alarm is the result of a match with date of the month. If DY/ DT is written to a logic 1, the alarm is the result of a match with day of the week. When the RTC register values match alarm register settings, the corresponding alarm flag (A1 F or A2F) bit is set to logic 1. If the corresponding alarm interrupt enable (A1 IE or A2IE) is also set to logic 1 and the INTCN bit is set to logic 1, the alarm condition activates the SQW/ INT signal.

DY/DT	Alarm 1 Register Mask Bits (BIT 7)				Alarm Rate
	A1M4	A1M3	A1M2	A1M1	
X	1	1	1	1	Alarm once per second
X	1	1	1	0	Alarm when seconds match
X	1	1	0	0	Alarm when minutes and seconds match
X	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match

DY/DT	Alarm 2 Register Mask Bits (BIT 7)			Alarm Rate
	A2M4	A2M3	A2M2	
X	1	1	1	Alarm once per minute (00 second of every minute)
X	1	1	0	Alarm when minutes match
X	1	0	0	Alarm when hours and minutes match
0	0	0	0	Alarm when date, hours, and minutes match
1	0	0	0	Alarm when day, hours, and minutes match

Special Purpose Registers

The FRTC1339M has two additional registers (control and status) that control the RTC, alarms, and square-wave output.

Control Register (0Eh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EOSC	0	BBSQI	RS2	RS1	INTCN	A2IE	A1IE

EOSC (Enable Oscillator) - This bit when set to logic 0 starts the oscillator. When this bit is set to a logic 1, the oscillator is stopped. This bit is enabled (logic 0) when power is first applied.

BBSQI (Battery-Backed Square-Wave and Interrupt Enable) - This bit when set to a logic 1 enables the square-wave or interrupt output when V_{CC} is absent and the FRTC1339M is being powered by the V_{BACKUP} pin. When BBSQI is a logic 0, the SQW/ INT pin goes high impedance when V_{CC} falls below the power fail trip point. This bit is disabled (logic 0) when power is first applied.

RS2 and RS1 (Rate Select) - These bits control the frequency of the square-wave output when the square wave has been enabled. Table below shows the square-wave frequencies that can be selected with the RS bits. These bits are both set to logic 1 (32kHz) when power is first applied.

Square-Wave Output Frequency

RS2	RS1	SQW Output Frequency
0	0	1HZ
0	1	4.096kHz
1	0	8.192kHz
1	1	32.768kHz

INTCN (Interrupt Control) - This bit controls the relationship between the two alarms and the interrupt output pins. When the INTCN bit is set to logic 1, a match between the timekeeping registers and the Alarm 1 or Alarm 2 registers activate the SQW/INT pin (provided that the alarms are enabled). When the INTCN bit is set to logic 0, a square wave is output on the SQW/ INT pin. This bit is set to logic 0 when power is first applied.

A1IE (Alarm 1 Interrupt Enable) - When set to logic 1, this bit permits the A1F bit in the status register to assert SQW/ INT (when INTCN = 1). When the A1 IE bit is set to logic 0 or INTCN is set to logic 0, the A1F bit does not initiate the an interrupt signal. The A1 IE bit is disabled (logic 0) when power is first applied.

A2IE (Alarm 2 Interrupt Enable) - When set to a logic 1, this bit permits the A2F bit in the status register to assert SQW/ INT (when INTCN = 1). When the A2IE bit is set to logic 0 or INTCN is set to logic 0, the A2F bit does not initiate an interrupt signal. The A2IE bit is disabled (logic 0) when power is first applied.

Status Register (0Fh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OSF	0	0	0	0	0	A2F	A1F

OSF (Oscillator Stop Flag) - A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period of time and can be used to judge the validity of the clock and date data. This bit is edge-triggered and set to logic 1 anytime the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.
2) The voltage present on both V_{CC} and V_{BACKUP} are insufficient to support oscillation.
3) The EOSC bit is turned off.
4) External influences on the crystal (e.g., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0. This bit can only be written to a logic 0. Attempting to write to logic 1

leaves the value unchanged.

A1F (Alarm 1 Flag) – A logic 1 in the A1F bit indicates that the time matched the Alarm 1 registers. If the A1IE bit is a logic 1 and the INTCN bit is set to a logic 1, the SQW/ INT pin is also be asserted. A1F FRTC1339M is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

A2F (Alarm 2 Flag) – A logic 1 in the A2F bit indicates that the time matched the Alarm 2 registers. If the A2IE bit is a logic 1 and the INTCN bit is set to a logic 1, the SQW/ INT pin is also asserted. A2F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

Trickle Charge Register (10h)

The simplified schematic of Figure: Programmable Trickle Charge shows the basic components of the trickle charger. The trickle-charge select (TCS) bits (bits 4–7) control the selection of the trickle charger. In order to prevent accidental enabling, only a pattern on 1010 enables the trickle charger. All other patterns disable the trickle charger. The trickle charger is disabled when power is first applied. The diode select (DS) bits (bits 2 and 3) select whether or not a diode is connected between V_{CC} and V_{BACKUP}. The ROUT bits (bits 0, 1) select the value of the resistor connected between V_{CC} and V_{BACKUP}. Bit values are shown in below table

Table: Trickle Charge Register (10h) Bit Values

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Function
TCS3	TCS2	TCS1	TCS0	DS1	DS0	ROUT1	ROUT0	
X	X	X	X	0	0	X	X	Disabled
X	X	X	X	1	1	X	X	Disabled
X	X	X	X	X	X	0	0	Disabled
1	0	1	0	0	1	0	1	No diode, 250Ω resistor
1	0	1	0	1	0	0	1	One diode, 250Ω resistor
1	0	1	0	0	1	1	0	No diode, 2kΩ resistor
1	0	1	0	1	0	1	0	One diode, 2kΩ resistor
1	0	1	0	0	1	1	1	No diode, 4kΩ resistor
1	0	1	0	1	0	1	1	One diode, 4kΩ resistor

The user determines diode and resistor selection according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example:

Assume that a system power supply of 3.3V is applied to V_{CC} and a super cap is connected to V_{BACKUP}. Also assume that the trickle charger has been enabled with a diode and resistor R2 between V_{CC} and V_{BACKUP}. The maximum current I_{MAX} would, therefore, be calculated as follows:

$$I_{MAX} = (3.3V - \text{diode drop}) / R2 \approx (3.3V - 0.7V) / 2k\Omega \approx 1.3mA$$

As the super cap or battery charges, the voltage drop between V_{CC} and V_{BACKUP} decreases and, therefore, the charge current decreases.

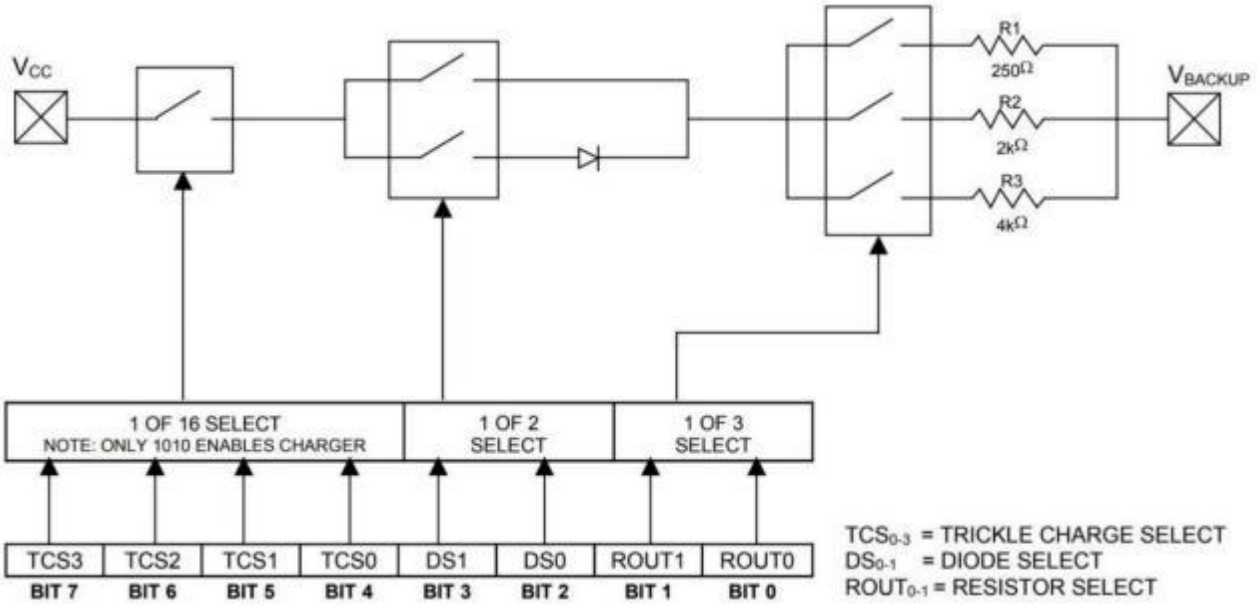

Figure 5: Programmable Trickle Charge

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I²C Bus

The FRTC1339M supports a bidirectional 2-wire bus and data transmission protocol. A device that sends data onto the
bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The FRTC1339M operates as a slave on the 2-wire bus. Connections to the bus are made by the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (Figure: Data Transfer on I2C Serial Bus).

1) Data transfer can be initiated only when the bus is not busy.
2) During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

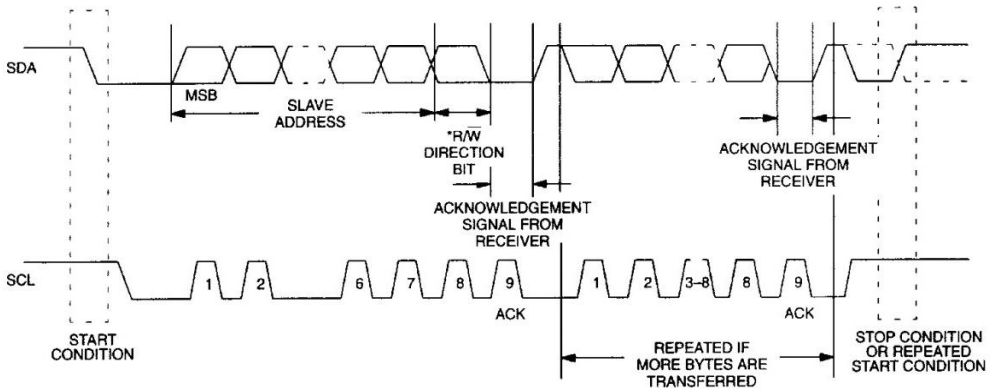

Figure 6 : Data Transfer on I2C Serial Bus

Depending upon the state of the R/W bit, two types of data transfer are possible:

1) **Data transfer from a master transmitter to a slave receiver.** The master transmits the first byte (the slave address). Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

2) **Data transfer from a slave transmitter to a master receiver.** The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, which is followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a "not acknowledge" is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The FRTC1339M can operate in the following two modes:

1) **Slave receiver mode (write mode):** Serial data and clock are received through SDA and SCL. An acknowledge bit is transmitted after each byte is received. START and STOP conditions are recognized as the beginning and end of a serial transfer. Hardware performs address recognition after reception of the slave address and direction bit (Figure: Data Write). The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7-bit FRTC1339M address—1 101000—followed by the direction bit (R/W), which, for a write, is 0. After receiving and decoding the slave address byte, the slave outputs an acknowledge on the SDA line. After the FRTC1339M acknowledges the slave address and write bit, the master transmits a register address to the FRTC1339M. This sets the register pointer on the FRTC1339M, with FRTC1339M
acknowledging the transfer. The master may then transmit zero or more bytes of data, with the FRTC1339M acknowledging each byte received. The register pointer increments after each data byte is transferred. The master generates a STOP condition to terminate the data write.

2) **Slave transmitter mode (read mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. The FRTC1339M transmits serial data on SDA while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (Figure Data Read). The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7-bit FRTC1339M address— 1101000—followed by the direction bit (R/W), which, for a read, is 1. After receiving and decoding the slave address byte, the slave outputs an acknowledge on the SDA line. The FRTC1339M then starts transmitting data using the register address pointed to by the register pointer. If the register pointer is not set before the initiation of a read mode, the first address that is read is the last one stored in the register pointer. The register pointer is incremented
after each byte is transferred. The FRTC1339M must receive a "not acknowledge" to end a read.

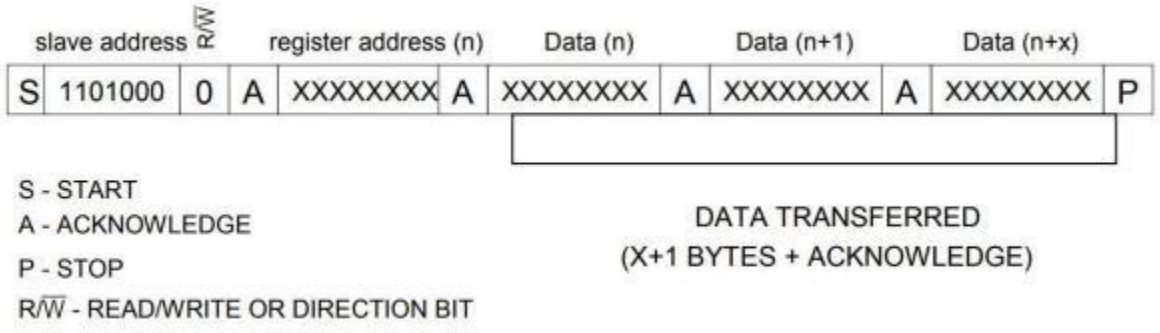

Figure 7 : Data Write— Slave Receiver Mode

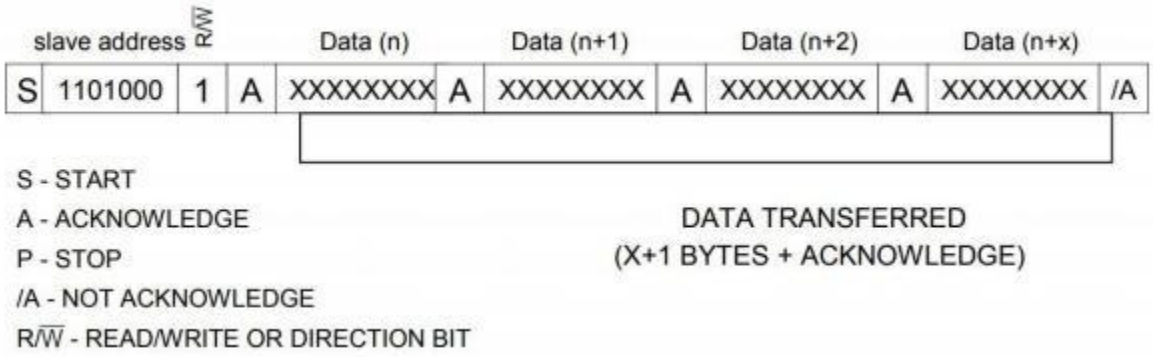

Figure 8: Data Read—Slave Transmitter Mode

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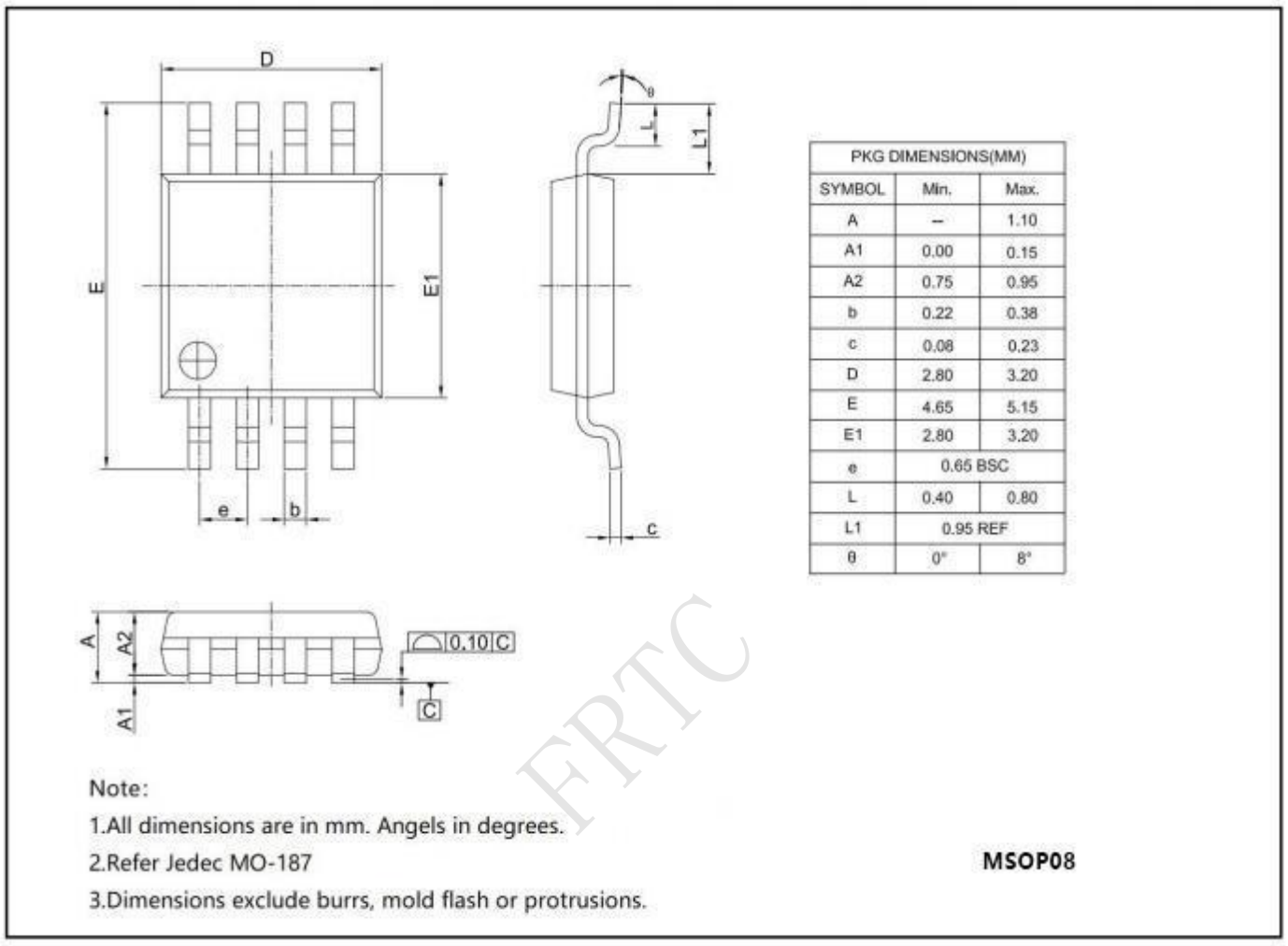
Package Information

FRTC1339M MSOP-8 Package



PKG DIMENSIONS(MM)		
SYMBOL	Min.	Max.
A	--	1.10
A1	0.00	0.15
A2	0.75	0.95
b	0.22	0.38
c	0.08	0.23
D	2.80	3.20
E	4.65	5.15
E1	2.80	3.20
e	0.65 BSC	
L	0.40	0.80
L1	0.95 REF	
θ	0°	8°

Reel Information

Package	Reel size (inch)	1 pin location	Reel width (mm)	Winding step (mm)	Tail blank tape length (mm)	Head blank tape length(mm)	SPQ	Reel/inner box	Maximum circuits per box (K)	Inner box/outer box	Maximum circuit number of outer box (K)	Humidity level	Moisture-proof packing
MSOP08	13	Top left corner	12	8	240	1120	4000	1	4	8	32	3	Yes

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Revision History

Revision	Description	Date
1.3		2025/01/03