

TPD2S703-Q1 汽车类 USB 双通道数据线路电池短路、V_{BUS} 短路保护和 IEC ESD 保护

1 特性

- 符合 AEC-Q100 标准
 - 工作温度范围: -40°C 至 +125°C
- VD+、VD- 上的电池短路 (高达 18V) 和 VBUS 短路保护
- ESD 性能 VD+, VD-
 - ±8kV 接触放电 (IEC 61000-4-2 和 ISO 10605 330pF, 330Ω)
 - ±15kV 气隙放电 (IEC 61000-4-2 和 ISO 10605 330pF, 330Ω)
- 高速数据开关 (1GHz 带宽)
- 只需要 5V 电源电压
- 可调节 OVP 阈值
- 快速过压响应时间 (典型值 200ns)
- 热关断特性
- 集成输入使能和故障输出信号
- 直通路由可保证数据完整性
 - 10 引脚 VSSOP 封装 (3mm × 3mm)
 - 10 引脚 WSON 封装 (2.5mm × 2.5mm)

2 应用

- 终端设备
 - 音响主机
 - 后座娱乐系统
 - 远程信息处理
 - USB 集线器
 - 导航模块
 - 媒体接口
- 接口
 - USB 2.0
 - USB 3.0

3 说明

TPD2S703-Q1 是一款用于汽车高速接口 (如 USB 2.0) 的双通道线路电池短路、V_{BUS} 短路保护和 IEC61000-4-2 ESD 保护器件。TPD2S703-Q1 包含两个数据线路 nFET 开关。这些开关通过提供业界一流的带宽, 实现最小的信号衰减, 同时可保护内部系统电路的 VD+ 和 VD- 引脚免受受过压情况的损坏, 从而确保安全的数据通信。在这些引脚上, 此器件可实现高达 18V 的直流电过压保护。这为汽车电池及 USB V_{BUS} 电压轨的数据线路短路提供了充分保护。过压保护电路可提供业内一流的电池短路保护, 能在 200ns 内关断数据开关, 以保护上游电路免受有害电压和电流尖峰的影响。

此外, 为优化电源树的大小和成本, TPD2S703-Q1 只需要一个 5V 单电源供电。该器件允许通过电阻分压器网络调整 OVP 阈值和钳位电路, 从而为任何收发器的系统保护优化提供一种简单且具有成本效益的方法。TPD2S703-Q1 还包括一个 FLT 引脚, 该引脚会在器件出现过压状况时发出指示, 并在过压状况消除后自动复位。

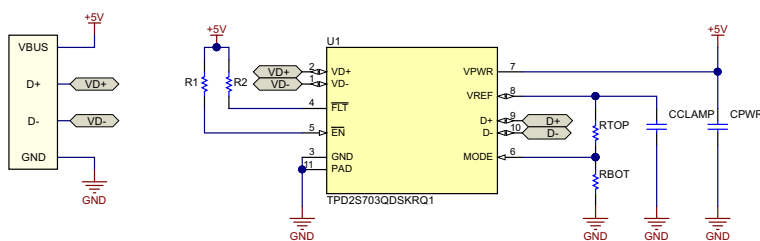
TPD2S703-Q1 还在 VD+ 和 VD- 引脚上集成了系统级别的 IEC 61000-4-2 和 ISO 10605 ESD 钳位, 因此无需再在应用中配置高压、低电容的外部 TVS 钳位电路。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
TPD2S703-Q1	VSSOP (10)	3.00mm × 3.00mm
	WSON (10)	2.50mm × 2.50mm

(1) 要了解所有可用封装, 请参见产品说明书末尾的可订购产品附录。

USB 2.0 端口提供电池短路和 IEC ESD 保护



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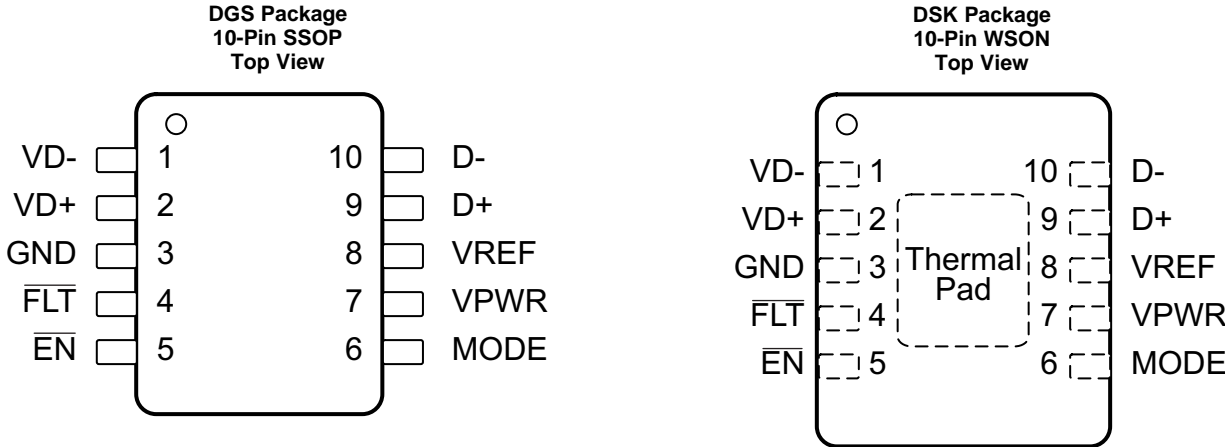
4 修订历史记录

Changes from Original (March 2017) to Revision A

Page

- Updated description from enable to $\overline{\text{FLT}}$ in *Recommended Operating Conditions* table **5**

5 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VD-	I/O	High voltage D- USB data line, connect to USB connector D+, D- IEC61000-4-2 ESD protection
2	VD+	I/O	High voltage D+ USB data line, connect to USB connector D+, D- IEC61000-4-2 ESD protection
3	GND	Ground	Ground pin for internal circuits and IEC ESD clamps
4	$\overline{\text{FLT}}$	O	Open-drain fault pin. See 表 1
5	$\overline{\text{EN}}$	I	Enable active-low input. Drive $\overline{\text{EN}}$ low to enable the switches. Drive $\overline{\text{EN}}$ high to disable the switches. See 表 1 for mode selection
6	MODE	I	Selects between device modes. See the Detailed Description section. Acts as LDO reference voltage for mode 1
7	VPWR	I	5-V DC supply input for internal circuits. Connect to internal power rail on PCB
8	VREF	I/O	Pin to set OVP threshold. See the Detailed Description section for instructions on how to set OVP threshold
9	D+	I/O	I/O protected low voltage D+ USB data line, connects to transceiver
10	D-	I/O	Protected low voltage D- USB data line, connects to transceiver

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted) ⁽¹⁾ ⁽²⁾

		MIN	MAX	UNIT
V _{PWR}	5-V DC supply voltage for internal circuitry	-0.3	7.7	V
V _{REF}	Pin to set OVP threshold	-0.3	6	V
VD+, VD-	Voltage range from connector-side USB data lines	-0.3	18	V
D+, D-	Voltage range for internal USB data lines	-0.3	V _{REF} + 0.3	V
V _{MODE}	Voltage on MODE pin	-0.3	7.7	V
V _{FLT}	Voltage on FLT pin	-0.3	7.7	V
V _{EN}	Voltage on enable pin	-0.3	7.7	V
T _A	Operating free air temperature ⁽³⁾	-40	125	°C
T _{STG}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) Thermal limits and power dissipation limits must be observed.

6.2 ESD Ratings—AEC Specification

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	All pins	±2000
		Charged-device model (CDM), per AEC Q100-011	All pins besides corners	±500
			Corner pins	±750

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	IEC 61000-4-2 contact discharge	VD+, VD- pins ⁽¹⁾	±8000
		IEC 61000-4-2 air-gap discharge	VD+, VD- pins ⁽¹⁾	±15000

- (1) See [Figure 23](#) for details on system level ESD testing setup.

6.4 ESD Ratings—ISO Specification

			VALUE	UNIT
V _{ESD} ⁽¹⁾	Electrostatic discharge	ISO 10605 (330 pF, 330 Ω) contact discharge (10 strikes)	VD+, VD- pins	±8000
		ISO 10605 (330 pF, 330 Ω) air-gap discharge (10 strikes)	VD+, VD- pins	±15000
		ISO 10605 (150 pF, 330 Ω) contact discharge (10 strikes)	VD+, VD- pins	±8000
		ISO 10605 (150 pF, 330 Ω) air-gap discharge (10 strikes)	VD+, VD- pins	±15000
		ISO 10605 (330 pF, 2 kΩ) contact discharge (10 strikes) ⁽²⁾	VD+, VD- pins	±8000
		ISO 10605 (330 pF, 2 kΩ) air-gap discharge (10 strikes)	VD+, VD- pins	±15000
		ISO 10605 (150 pF, 2 kΩ) air-gap discharge (10 discharges)	VD+, VD- pins	±25000

- (1) See [Figure 23](#) for details on system level ESD testing setup.
- (2) V_{REF} > 3 V.

6.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT	
V _{PWR}	5-V DC supply voltage for internal circuitry	4.5		7	V	
V _{REF}	Mode 0. Voltage range for V _{REF} pin (for setting OVP threshold)	3		3.6	V	
V _{REF}	Mode 1. Voltage range for V _{REF} pin (for setting OVP threshold)	0.63		3.8	V	
VD+, VD–	Voltage range from connector-side USB data lines	0		3.6	V	
D+, D–	Voltage range for internal USB data lines	0		3.6	V	
V _{EN}	Voltage range for enable	0		7	V	
V _{FLT}	Voltage range for $\overline{\text{FLT}}$	0		7	V	
I _{FLT}	Current into open drain $\overline{\text{FLT}}$ pin FET	0		3	mA	
C _{VPWR}	V _{PWR} capacitance ⁽¹⁾	V _{PWR} pin	1	10	μF	
C _{VREF}	V _{REF} capacitance	V _{REF} pin	0.3	1	3	μF
C _{MODE}	Allowed parasitic capacitance on mode pin from PCB and mode 1 external resistors			20	pF	
R _{MODE_0}	Resistance to GND to set to mode 0		2	2.6	kΩ	
R _{MODE_1}	Resistance to GND to set to mode 1 (calculate parallel combination of R _{TOP} and R _{BOT})	14	20		kΩ	

- (1) For recommended values for capacitors and resistors, the typical values assume a component placed on the board near the pin. Minimum and maximum values listed are inclusive of manufacturing tolerances, voltage derating, board capacitance, and temperature variation. The effective value presented should be within the minimum and maximums listed in the table.

6.6 Thermal Information

THERMAL METRIC ⁽¹⁾		TPD2S703-Q1		UNIT
		DGS (VSSOP)	DSK (WSON)	
		10 PINS	10 PINS	
θ _{JA}	Junction-to-ambient thermal resistance	167.3	61.5	°C/W
θ _{JCtop}	Junction-to-case (top) thermal resistance	56.9	51.3	°C/W
θ _{JB}	Junction-to-board thermal resistance	87.6	34	°C/W
ψ _{JT}	Junction-to-top characterization parameter	7.7	1.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	86.2	34.3	°C/W
θ _{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	7.7	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
MODE 1 ADJUSTABLE V_{REF}							
V _{MODE_CMP}	Mode 1 V _{REF} feedback regulator voltage	V _{MODE}	Standard mode 1 set-up. $\overline{EN} = 0$ V. Once V _{REF} = 3.3 V, measure voltage on mode pin	0.47	0.5	0.53	V
I _{MODE_LEAK}	Mode pin mode 1 leakage current	I _{MODE}	Standard mode 1. Remove R _{TOP} and R _{BOT} . Power up device and wait until start-up time has passed. Then force 0.53 V on the MODE pin and measure current into pin		50	200	nA
V _{REF_ACCURACY}	V _{REF} accuracy	V _{REF}	Informative, test parameters below; accuracy with R _{TOP} and R _{BOT} as ±1% resistors	–8%		8%	
V _{REF_3.3V}	Mode 1 V _{REF} set to 3.3 V	V _{REF}	Standard mode 1 set-up. R _{TOP} = 140 kΩ ± 1%, R _{BOT} = 24.9 kΩ ± 1%. $\overline{EN} = 0$. Measure value of V _{REF} once it settles	3.04	3.31	3.58	V
V _{REF_0.66V}	Mode 1 V _{REF} set to 0.66 V	V _{REF}	Standard mode 1 set-up. R _{TOP} = 47.5 kΩ ± 1%, R _{BOT} = 150 kΩ ± 1%. $\overline{EN} = 0$. Measure value of V _{REF} once it settles	0.6	0.66	0.72	V
V _{REF_3.8V}	Mode 1 V _{REF} set to 3.8 V	V _{REF}	Standard mode 1 set-up. R _{TOP} = 165 kΩ ± 1%, R _{BOT} = 24.9 kΩ ± 1%. $\overline{EN} = 0$. Measure value of V _{REF} once it settles	3.5	3.81	4.12	V
EN, FLT PINS							
V _{IH}	High-level input voltage	\overline{EN}	Mode 0. Connect VPWR = 5 V; V _{REF} = 3.3 V; VD+ = 3.3 V; Set VIH(\overline{EN}) = 0 V; Sweep VIH from 0 V to 1.4 V; Measure when D+ drops low (less than or equal to 5% of 3.3 V) from 3.3 V	1.2			V
	Low-level input voltage		Mode 0. Connect VPWR = 5 V; V _{REF} = 3.3 V; VD+ = 3.3 V. Set VIH(\overline{EN}) = 3.3 V; Sweep VIH from 3.3 V to 0.5 V; Measure when D+ rise to 95% of 3.3 V from 0 V	0.8			
I _{IL}	Input leakage current	\overline{EN}	Mode 0. VPWR = 5 V; V _{REF} = 3.3 V; VI (EN) = 3.3 V; Measure current into EN pin			1	μA
V _{OL}	Low-level output voltage	\overline{FLT}	Mode 0. Drive the TPS2S703-Q1 in OVP to assert FLT pin. Source I _{OL} = 1 mA into FLT pin and measure voltage on FLT pin when asserted			0.4	V
T _{SD_RISING}	The rising over-temperature protection shutdown threshold		VPWR = 5 V, ENZ = 0 V, T _A stepped up until FLTZ is asserted	140	150	165	°C
T _{SD_FALLING}	The falling over-temperature protection shutdown threshold		VPWR = 5 V, ENZ = 0 V, T _A stepped down from T _{SD_RISING} until FLTZ is cleared	125	138	150	°C
T _{SD_HYST}	The over-temperature protection shutdown threshold hysteresis		T _{SD_RISING} – T _{SD_FALLING}	10	12	15	°C
OVP CIRCUIT—VD±							
V _{OVP_RISING}	Input overvoltage protection threshold, V _{REF} > 3.6 V	VD±	Mode 1. Set V _{PWR} = 5 V; $\overline{EN} = 0$ V; R _{TOP} = 165 kΩ, R _{BOT} = 24.9 kΩ. Connect D± to 40-Ω load. Increase VD+ or VD– from 4.1 V to 4.9 V. Measure the value at which FLTZ is asserted	4.3	4.5	4.7	V
V _{OVP_RISING}	Input overvoltage protection threshold	VD±	Mode 1. Set V _{PWR} = 5 V; $\overline{EN} = 0$ V; R _{TOP} = 140 kΩ, R _{BOT} = 24.9 kΩ. Increase VD+ or VD– from 3.6 V to 4.6 V. Measure the value at which FLTZ is asserted. Repeat for R _{TOP} = 39 kΩ, R _{BOT} = 150 kΩ. Increase VD+ or VD– from 0.6 V to 0.9 V. Measure the value at which FLTZ is asserted. See the resultant values meet the equation, and make sure to observe data switches turnoff. Also check for mode 0 when V _{REF} = 3.3 V	1.19 × V _{REF}	1.25 × V _{REF}	1.31 × V _{REF}	V
V _{HYS_OVP}	Hysteresis on OVP	VD±	Difference between rising and falling OVP thresholds on VD±		25		mV
V _{OVP_FALLING}	Input overvoltage protection threshold	VD±	After collecting each rising OVP threshold, lower the VD± voltage until you see \overline{FLT} deassert. This gives the falling OVP threshold. Use this value to calculate V _{HYS_OVP}		VOV P_RI SING – VHYS _OVP		V
I _{VD_LEAK_0 V}	Leakage current on VD± during normal operation	VD±	Standard mode 0 or mode 1. Set VD± = 0 V. D± = floating. Measure current flowing into VD±	–0.1		0.1	μA

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{VD_LEAK_3.6V}$	Leakage current on VD_{\pm} during normal operation	VD_{\pm}	Standard mode 0 or mode 1. Set $VD_{\pm} = 3.6$ V. $D_{\pm} =$ floating. Measure current flowing into VD_{\pm}		2.5	4	μ A
$V_{OVP_3.3V}$	Input overvoltage threshold for $V_{REF} = 3.3$ V	VD_{\pm}	Standard mode 1. $R_{TOP} = 140$ k $\Omega \pm 1\%$, $R_{BOT} = 24.9$ k $\Omega \pm 1\%$. Connect D_{\pm} to 40- Ω load. Measure the value at which FLTZ is asserted	3.61	4.14	4.67	V
$V_{OVP_0.66V}$	Input overvoltage threshold for $V_{REF} = 0.66$ V	VD_{\pm}	Standard mode 1. $R_{TOP} = 47.5$ k $\Omega \pm 1\%$, $R_{BOT} = 150$ k $\Omega \pm 1\%$. Connect D_{\pm} to 40- Ω load. Measure the value at which FLTZ is asserted	0.72	0.83	0.94	V
SHORT-TO-BATTERY							
V_{DATA_STB}	Data line hotplug short-to-battery tolerance	V_{\pm}	Charge battery-equivalent capacitor to test voltage then discharge to pin under test through a 1 meter, 18-ga wire. (See Fig 23 application information for more details)			18	V
$V_{CLAMP_STB_DP/M_3V3}$	Data line system side clamping voltage during STB	D_{\pm}	Test both $D+$ and $D-$ FETs. Test $D+$ and $D-$ independently. Short $VD+$ and $VD-$ to 18 V via hotplug to a battery-equivalent capacitor with a 1 meter, 18-ga wire. $V_{REF} = 3.3$ V, $V_{PWR} = 5$ V. Test in standard mode 0 and mode 1		5.5	6	V
$V_{CLAMP_STB_DP/M_0V6}$	Data line system side clamping voltage during STB	D_{\pm}	Test both $D+$ and $D-$ FETs. Short $VD+$ and $VD-$ to 18 V via hotplug to a battery-equivalent capacitor with a 1 meter, 18-ga wire. $V_{REF} = 0.63$ V, $V_{PWR} = 5$ V. Test in standard mode 0 and mode 1		3.2	3.5	V
DATA LINE SWITCHES – $VD+$ to $D+$ or $VD-$ to $D-$							
R_{ON}	On resistance		Mode 0 or 1. Set $V_{PWR} = 5$ V; $V_{REF} = 3.3$ V; $\overline{EN} = 0$ V; Measure resistance between $D+$ and $VD+$ or $D-$ and $VD-$, voltage between 0 and 0.4 V		4	6.5	Ω
$R_{ON(Flat)}$	On resistance flatness		Mode 0 or 1. Set $V_{PWR} = 5$ V; $V_{REF} = 3.3$ V; $\overline{EN} = 0$ V; Measure resistance between $D+$ and $VD+$ or $D-$ and $VD-$, sweep voltage between 0 and 0.4 V. Take difference of resistance at 0.4-V and 0-V VD_{\pm} bias			1	Ω
BW_{ON}	On bandwidth (–3-dB)		Mode 0 or 1. Set $V_{PWR} = 5$ V; $V_{REF} = 3.3$ V; $\overline{EN} = 0$ V; Measure S21 bandwidth from $D+$ to $VD+$ or $D-$ to $VD-$ with voltage swing = 400 mVpp, $V_{cm} = 0.2$ V		960		MHz

6.8 Power Supply and Supply Current Consumption Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{UVLO_RISING_VPWR}$	V_{PWR} rising UVLO threshold	Use standard mode 0 set-up. Set $\overline{EN} = 0$ V, load D+ to 45 Ω , $VD+ = 3.3$ V. Set $V_{PWR} = 3.5$ V, and step up V_{PWR} until 90% of $VD+$ appears on D+	3.7	3.95	4.2	V
$V_{UVLO_HYST_VPWR}$	V_{PWR} UVLO hysteresis	Use standard mode 0 set up. Set $\overline{EN} = 0$ V, load D+ to 45 Ω , $VD+ = 3.3$ V. Set $V_{PWR} = 4.3$ V, and step down V_{PWR} until D+ falls to 10% of $VD+$. This gives $V_{UVLO_FALLING_VPWR} - V_{UVLO_RISING_VPWR} - V_{UVLO_FALLING_VPWR} = V_{UVLO_HYST_VPWR}$ for this unit	250	300	400	mV
$V_{UVLO_RISING_VREF}$	V_{REF} rising UVLO threshold in mode 0	Use standard mode 0 set up. Set $\overline{EN} = 0$ V, load D+ to 45 Ω , $VD+ = 3.3$ V. Set $V_{REF} = 2.5$ V, and step up V_{REF} until 90% of $VD+$ appears on D+	2.6	2.7	2.9	V
$V_{UVLO_HYST_VREF}$	V_{REF} UVLO hysteresis	Use standard mode 0 set up. Set $\overline{EN} = 0$ V, load D+ to 45 Ω , $VD+ = 3.3$ V. Set $V_{REF} = 3$ V, and step down V_{REF} until D+ falls to 10% of $VD+$. This gives $V_{UVLO_FALLING_VREF} - V_{UVLO_RISING_VREF} - V_{UVLO_FALLING_VREF} = V_{UVLO_HYST_VREF}$ for this unit	75	125	200	mV
$I_{VPWR_DISABLE_D_MODE0}$	V_{PWR} disabled current consumption	Use standard mode 0. $\overline{EN} = 5$ V. Measure current into V_{PWR}			110	μ A
$I_{VPWR_DISABLE_D_MODE1}$	V_{PWR} disabled current consumption	Use standard mode 1. $\overline{EN} = 5$ V. Measure current into V_{PWR}			110	μ A
$I_{VREF_DISABLE_D}$	V_{REF} disabled current consumption mode 0	Use standard mode 0. $\overline{EN} = 5$ V. Measure current into V_{REF}			10	μ A
I_{VPWR_MODE0}	V_{PWR} operating current consumption	Use standard mode 0. $\overline{EN} = 0$ V. Measure current into V_{PWR}			250	μ A
I_{VPWR_MODE1}	V_{PWR} operating current consumption	Use standard mode 1. $\overline{EN} = 0$ V. Measure current into V_{PWR}			350	μ A
I_{VREF}	V_{REF} operating current consumption mode 0	Use standard mode 0. $\overline{EN} = 0$ V. Measure current into V_{REF}		12	20	μ A
I_{CHG_VREF}	V_{REF} fast charge current	Standard mode 1. $0.1 \mu F < C_{VREF} < 3 \mu F$. Set-up for charging to 3.3 V. Use a high voltage capacitor that does not derate capacitance up the 3.3 V. Measure slope to calculate the current when C_{VREF} cap is being charged. Test to check this OPEN LOOP method		22		mA
$I_{D_OFF_LEAK_STB}$		Mode 0. Measured flowing into D+ or D- supply, $V_{PWR} = 0$ V, $VD+$ or $VD- = 18$ V, $\overline{EN} = 0$ V, $V_{REF} = 0$ V, $D_{\pm} = 0$ V	-1		1	μ A
$I_{D_ON_LEAK_STB}$		Mode 0. Measured flowing into D+ or D- supply, $V_{PWR} = 5$ V, $VD+$ or $VD- = 18$ V, $\overline{EN} = 0$ V, $V_{REF} = 3.3$ V, $D_{\pm} = 0$ V	-1		1	μ A
$I_{VD_OFF_LEAK_STB}$		Mode 0. Measured flowing out of $VD+$ or $VD-$ supply, $V_{PWR} = 0$ V, $VD+$ or $VD- = 18$ V, $\overline{EN} = 0$ V, $V_{REF} = 0$ V, $D_{\pm} = 0$ V			120	μ A
$I_{VD_ON_LEAK_STB}$		Mode 0. Measured flowing out of $VD+$ or $VD-$ supply, $V_{PWR} = 5$ V, $VD+$ or $VD- = 18$ V, $\overline{EN} = 0$ V, $V_{REF} = 3.3$ V, $D_{\pm} = 0$ V			120	μ A
$I_{VPWR_TO_VREF_LEAK}$	Leakage from V_{PWR} to V_{REF}	Use standard mode 0. Set $V_{REF} = 0$ V. Measured current flowing out of V_{REF} pin			1	μ A
$I_{VREF_TO_VPWR_LEAK}$	Leakage from V_{REF} to V_{PWR}	Use standard mode 0. Set $V_{PWR} = 0$ V. Measured as current flowing out of V_{PWR} pin			1	μ A

6.9 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
ENABLE PIN AND VREF FAST CHARGE					
T_{VREF_CHG}	V_{REF} fast charge time		0.5	1	ms
		Time between when 5 V is applied to V_{PWR} , and V_{REF} reaches $V_{VREF_FAST_CHG}$. Needs to happen before or at same time $t_{ON_STARTUP}$ completes			

Timing Requirements (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$T_{ON_STARTUP_MODE0}$	Device turnon time from UVLO mode 0	Mode 0. $\overline{EN} = 0$ V, measured from V_{PWR} and $V_{REF} = UVLO^+$ to data FET ON, V_{PWR} comes to $UVLO^+$ second. Place 3.3 V on VD_{\pm} . Ramp V_{REF} to 3.3 V, then V_{PWR} to 5 V and measure the time it takes for D_{\pm} to reach 90% of VD_{\pm}		0.5	1	ms
$T_{ON_STARTUP_MODE1}$	Device turnon time from UVLO mode 1	Informative. mode 1. $\overline{EN} = 0$ V, measured from $V_{PWR} = UVLO^+$ to data FET ON		$0.5 + T_{CHG_C_VREF}$		ms
$T_{ON_STARTUP_MODE1_3.3V}$	Device turnon time from UVLO mode 1	Mode 1. $\overline{EN} = 0$ V, measured from $V_{PWR} = UVLO^+$ to data FET ON, $C_{VREF} = 1 \mu F$, $V_{REF_FINAL} = 3.3$ V. Measure the time it takes for D_{\pm} to reach 90% of VD_{\pm}		0.6	1	ms
$T_{ON_EN_MODE0}$	Device turnon time mode 0	Mode 0. $V_{PWR} = 5$ V, $V_{REF} = 3.3$ V, time from \overline{EN} is asserted until data FET is ON. Place 3.3 V on VD_{\pm} , measure the time it takes for D_{\pm} to reach 90% of VD_{\pm}		150		μs
$T_{ON_EN_MODE1}$	Device turnon time mode 1	Mode 1. $V_{PWR} = 5$ V, $V_{REF_INITIAL} = 0$ V, time from \overline{EN} is asserted until data FET is ON. Place 3.3 V on VD_{\pm} , measure the time it takes for D_{\pm} to reach 90% of VD_{\pm}		$150 + T_{CHG_VREF}$		μs
$T_{ON_EN_MODE1_3.3V}$	Device turnon time mode 1 for $V_{REF} = 3.3$ V	Mode 1. $V_{PWR} = 5$ V, $V_{REF_INITIAL} = 0$ V, time from \overline{EN} is asserted until data FET is ON. Place 3.3 V on VD_{\pm} , measure the time it takes for D_{\pm} to reach 90% of VD_{\pm} . $C_{VREF} = 1 \mu F$, $V_{REF_FINAL} = 3.3$ V		300		μs
T_{OFF_EN}	Device turnoff time	Mode 0 or 1. $V_{PWR} = 5$ V, $V_{REF} = 3.3$ V, time from \overline{EN} is deasserted until data FET is off. Place 3.3 V on VD_{\pm} , measure the time it takes for D_{\pm} to fall to 10% of VD_{\pm} , $R_{D_{\pm}} = 45 \Omega$		5		μs
T_{CHG_CVREF}	Time to charge C_{VREF}	Informative. Mode 1. Time from $V_{REF} = 0$ V to $80\% \times V_{REF_FINAL}$ after \overline{EN} transitions from high to low		$(C_{VREF} \times 0.8 (V_{REF_FINAL} - I_{C_HG_VREF}))$		s
$T_{CHG_CVREF_3.3V}$	Time to charge C_{VREF} to 3.3 V	Mode 1. Time from $V_{REF} = 0$ V to $90\% \times 3.3$ V after \overline{EN} transitions from high to low, $C_{VREF} = 1 \mu F$		132		μs
$T_{CHG_CVREF_0.66V}$	Time to charge C_{VREF} to 0.66 V	Mode 1. Time from $V_{REF} = 0$ V to $90\% \times 0.63$ V after \overline{EN} transitions from high to low, $C_{VREF} = 1 \mu F$. $R_{TOP} = 47.5 k\Omega \pm 1\%$, $R_{BOT} = 150 k\Omega \pm 1\%$		26		μs
OVER VOLTAGE PROTECTION						
$t_{OVP_response_VBUS}$	OVP response time to $VBUS$	Mode 0 or 1. Measured from OVP condition to FET turn off. Short VD_{\pm} to 5 V and measure the time it takes D_{\pm} voltage to reach $0.1 \times V_{D_{\pm_CLAMP_MAX}}$ from the time the 5-V hot-plug is applied. $R_{LOAD_D_{\pm}} = 45 \Omega$. ^{(1) (2)}		2		μs
$t_{OVP_response}$	OVP response time	Mode 0 or 1. Measured from OVP condition to FET turn off. Short VD_{\pm} to 18 V and measure the time it takes D_{\pm} voltage to reach $0.1 \times V_{D_{\pm_CLAMP_MAX}}$ from the time the 18-V hot-plug is applied. $R_{LOAD_D_{\pm}} = 45 \Omega$. ^{(1) (2)}		0.1	1	μs
$t_{OVP_Recov_FLT}$	Recovery time \overline{FLT} pin	Measured from OVP clear to \overline{FLT} deassertion ⁽¹⁾		32		ms
$t_{OVP_Recov_FET}$	Recovery time for data FET to turn back on	Measured from OVP clear until FET turns back on. Drop $VD+$ from 16 V to 3.3 V with $V_{REF} = 3.3$ V, measure time it takes for $D+$ to reach 90% of 3.3 V		32		ms
t_{OVP_ASSERT}	\overline{FLT} assertion time	Measured from OVP on $VD+$ or $VD-$ to \overline{FLT} assertion	12.6	18	23.4	ms

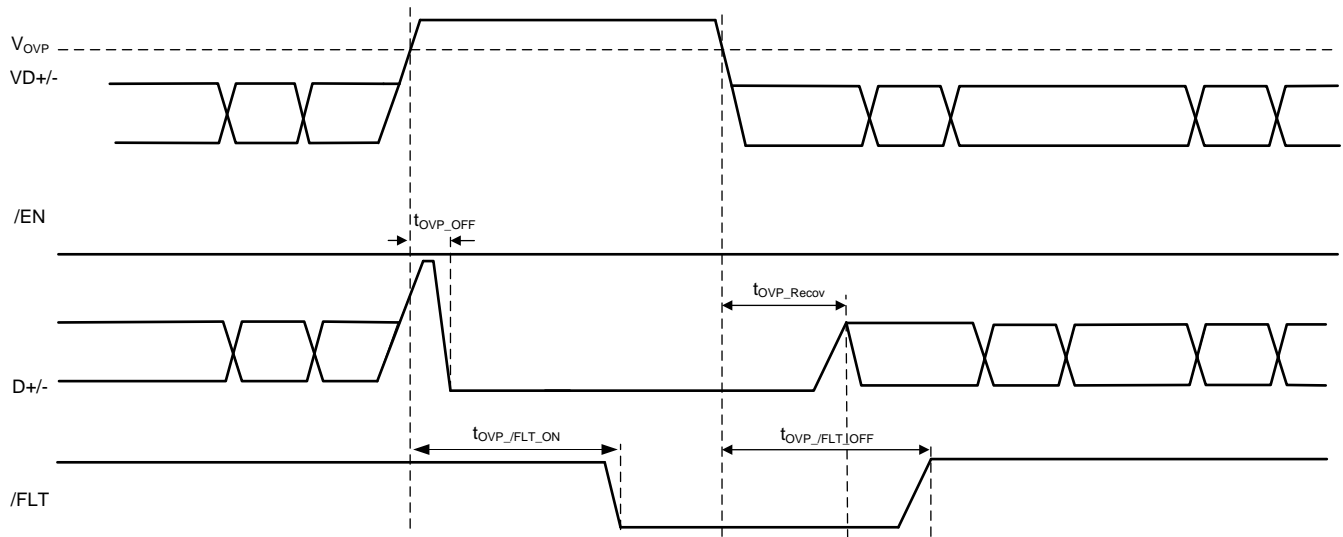
(1) Shown in [Figure 1](#).

(2) Specified by design, not production tested.

TPD2S703-Q1

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(1) OVP Operation – $VD+$, $VD-$

图 1. TPD2S703-Q1 Timing Diagram

6.10 Typical Characteristics

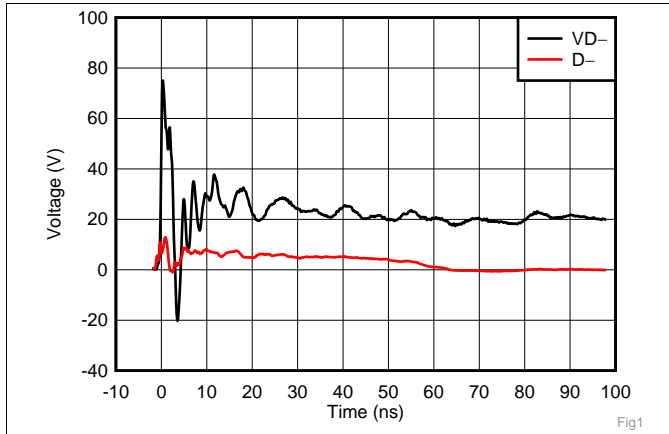


Fig1

图 2. 8-kV IEC 61400-4-2 Contact Waveform

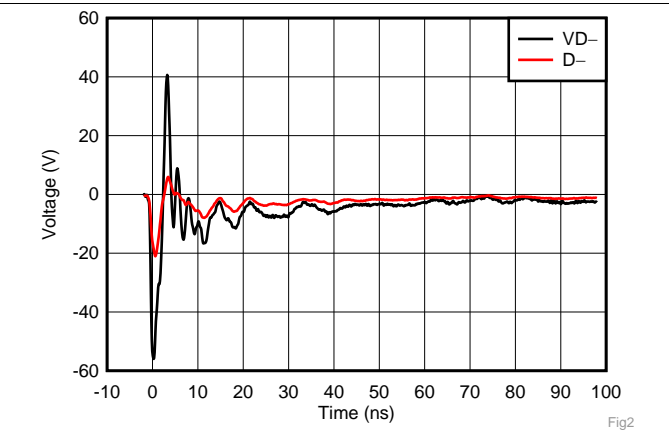


Fig2

图 3. -8-kV IEC 61400-4-2 Contact Waveform

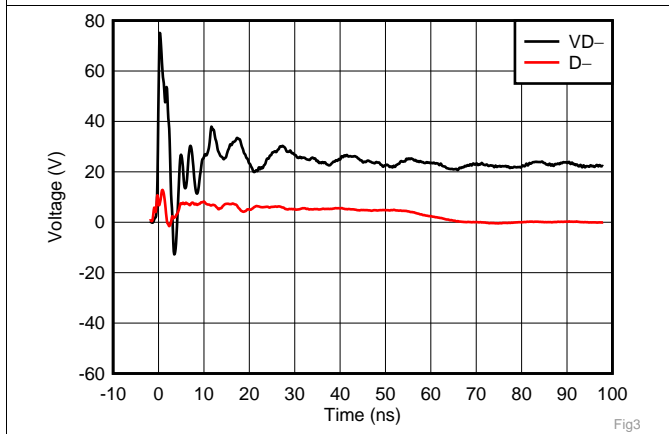


Fig3

图 4. 8-kV ISO 10605 (330-pF, 330-Ω) Contact Waveform

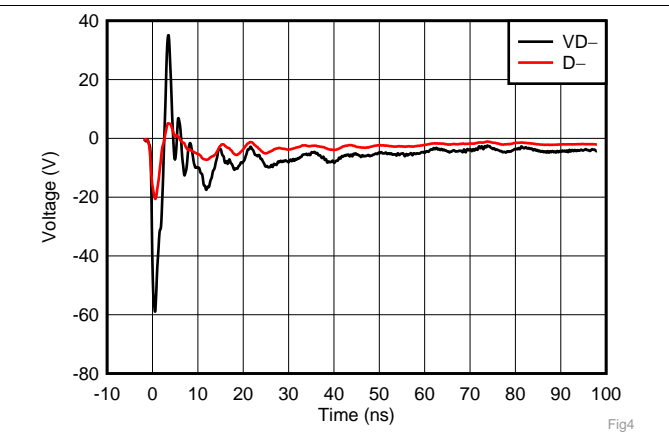


Fig4

图 5. -8-kV ISO 10605 (330-pF, 330-Ω) Contact Waveform

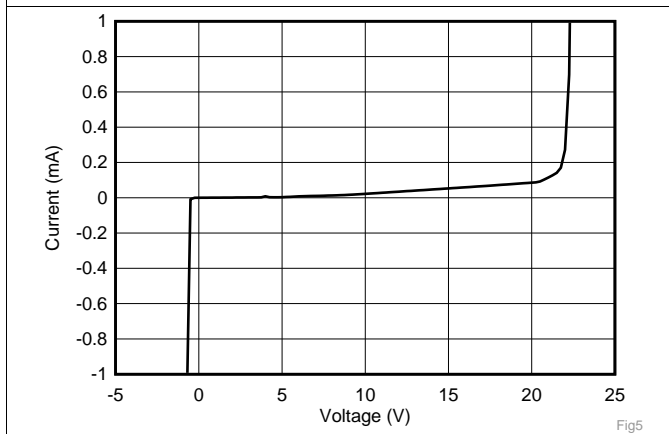


Fig5

图 6. Data Line I-V Curve

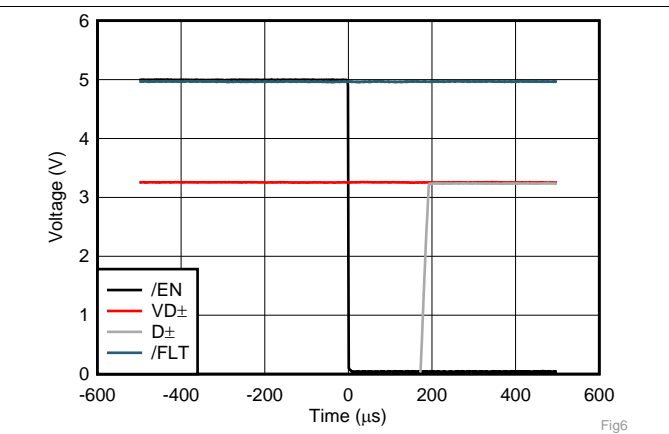


Fig6

图 7. Data Switch Turnon Time

Typical Characteristics (接下页)

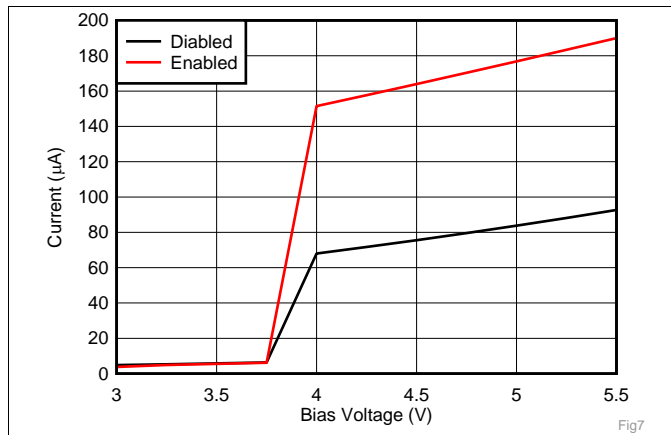


图 8. V_{PWR} Operating Current vs Bias Voltage

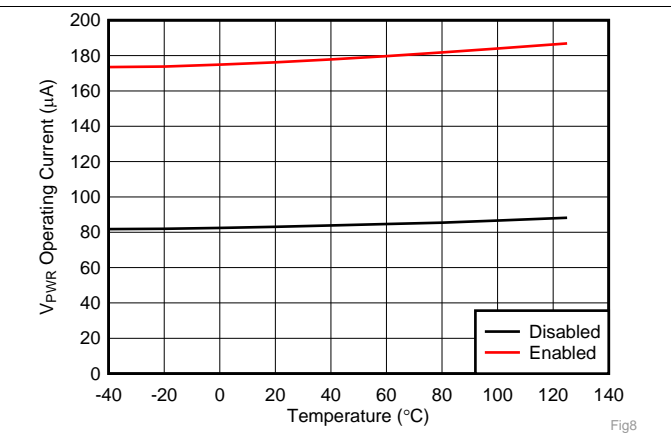


图 9. V_{PWR} Operating Current vs Temperature ($V_{PWR} = 5\text{ V}$)

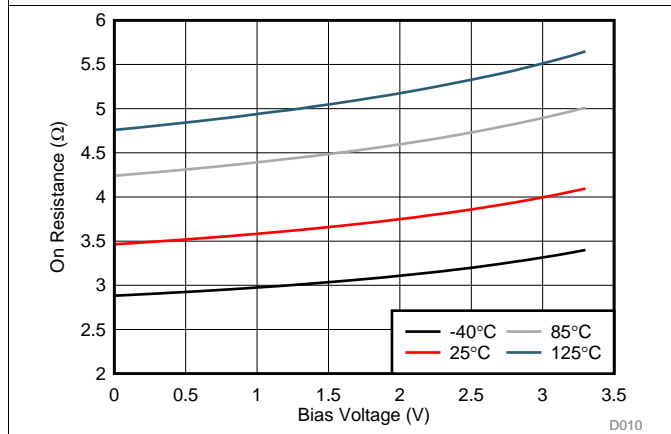


图 10. VD_{\pm} Leakage Current at 18 V Across Temperature (Enabled)

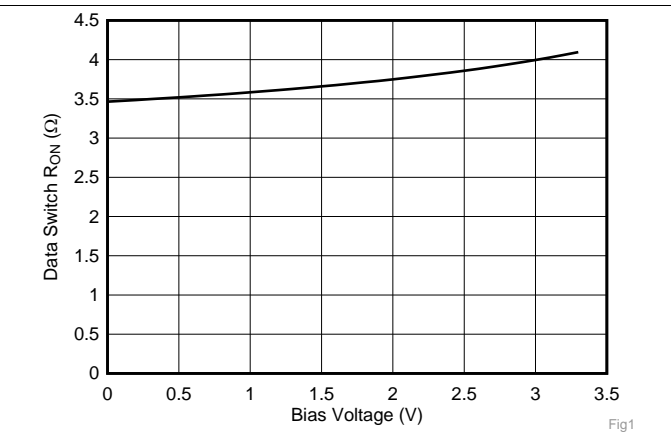


图 11. Data Switch R_{ON} vs Bias Voltage

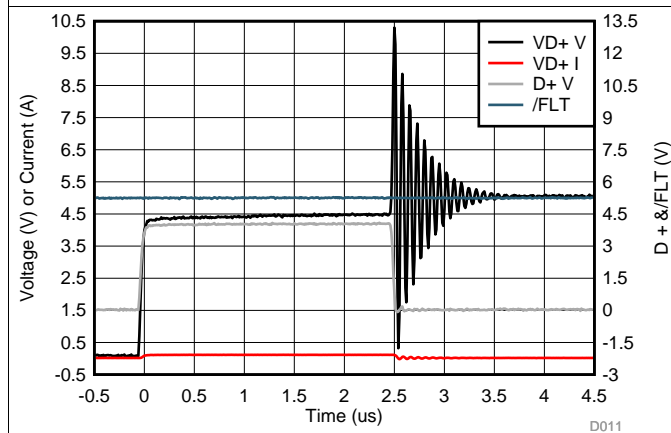


图 12. Data Switch Short-to-5 V Response Waveform

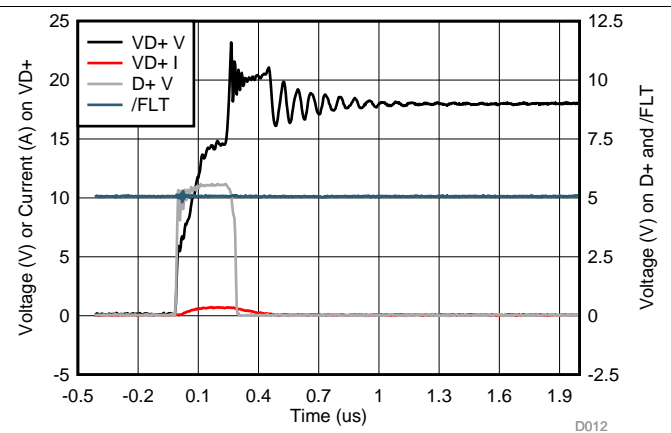


图 13. Data Switch Short-to-18 V Response Waveform

Typical Characteristics (接下页)

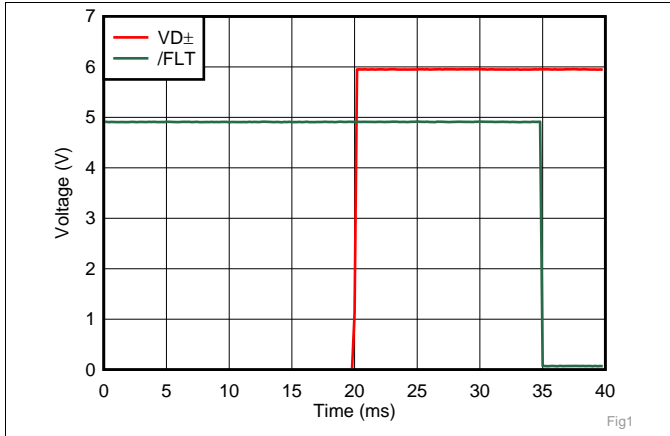


图 14. \overline{FLT} Assertion Time During OVP

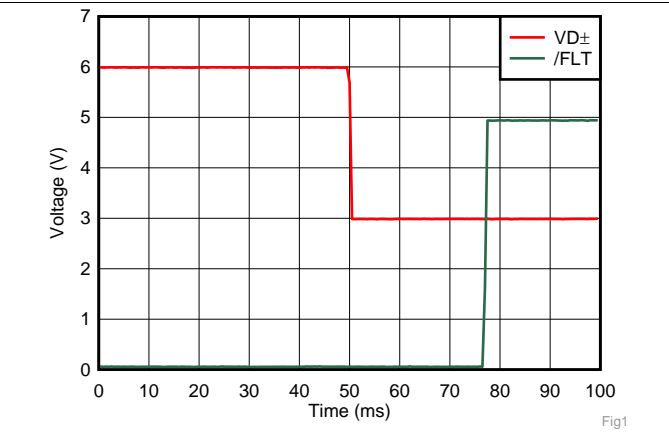


图 15. \overline{FLT} Recover Time After OVP Clear

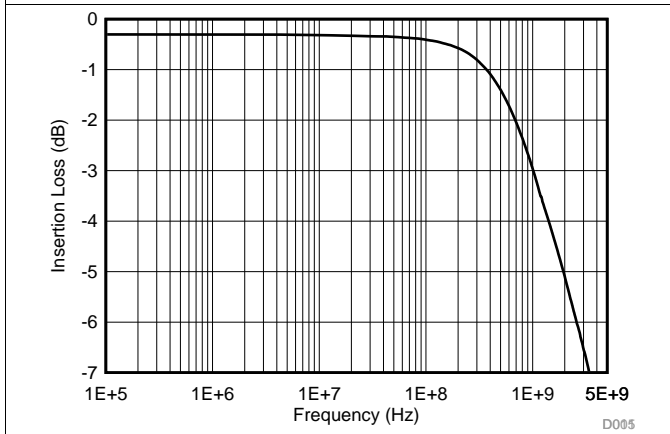


图 16. Data Switch Differential Bandwidth

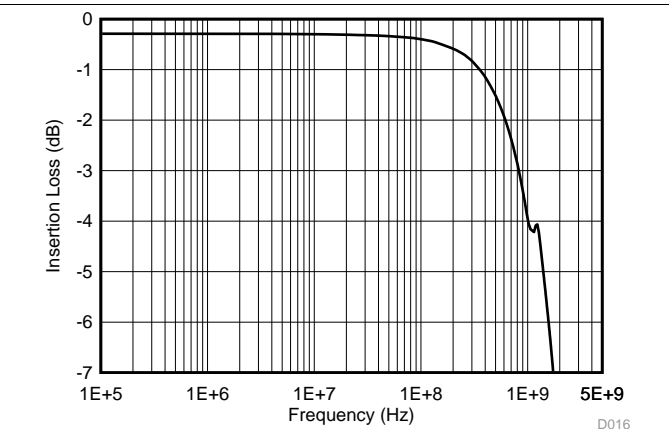


图 17. Data Switch Single-Ended Bandwidth

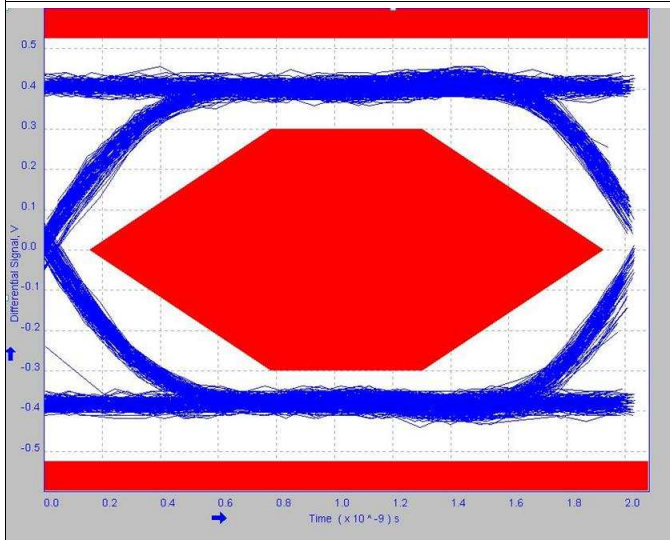


图 18. USB2.0 Eye Diagram (No TPD2S703-Q1)

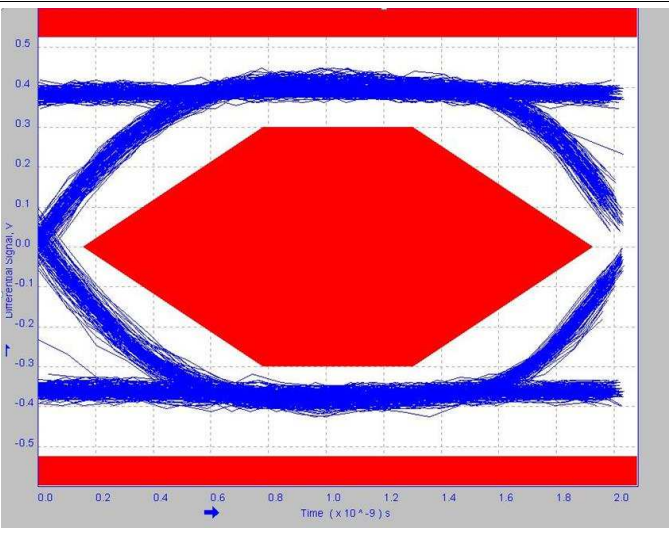
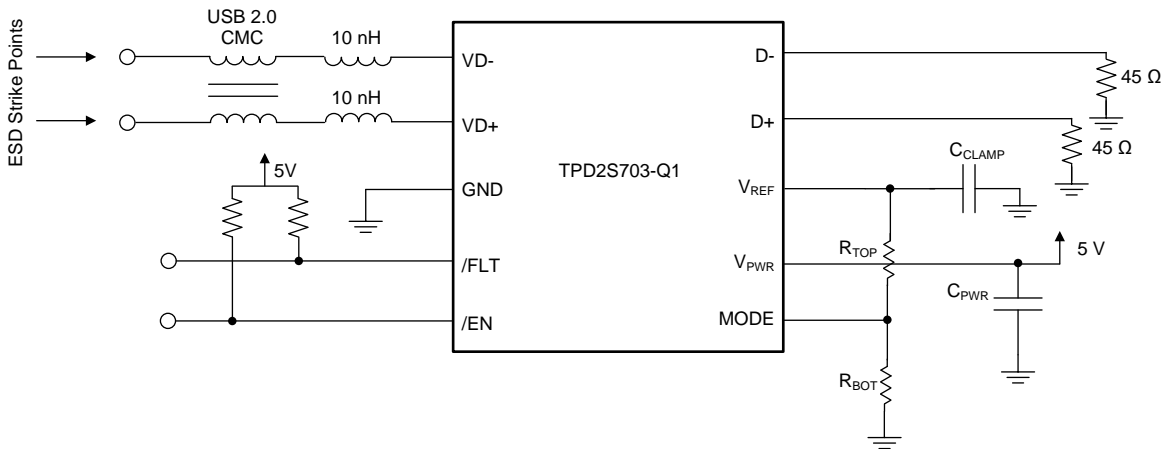


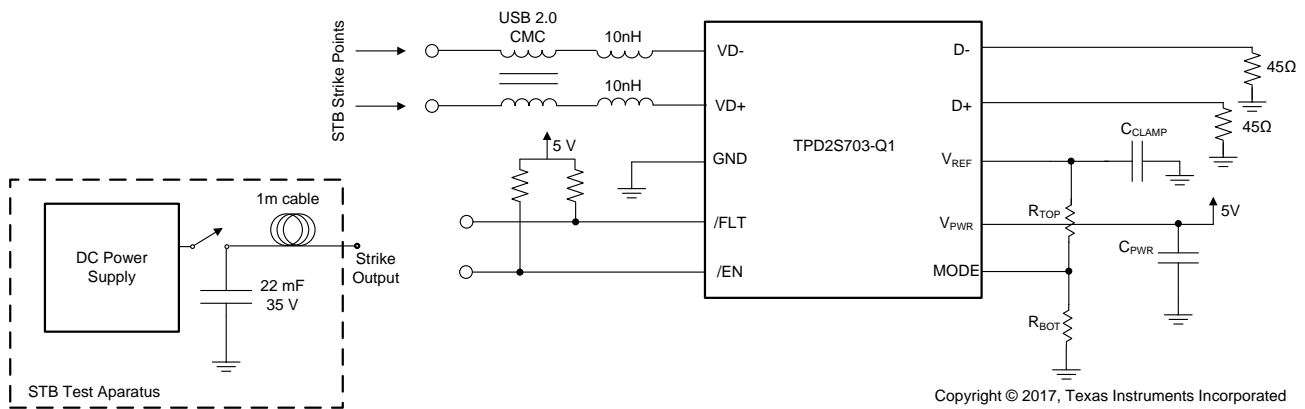
图 19. USB2.0 Eye Diagram (With TPD2S703-Q1)

7 Parameter Measurement Information



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图 20. ESD Setup



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图 21. Short-to-Battery Setup

8 Detailed Description

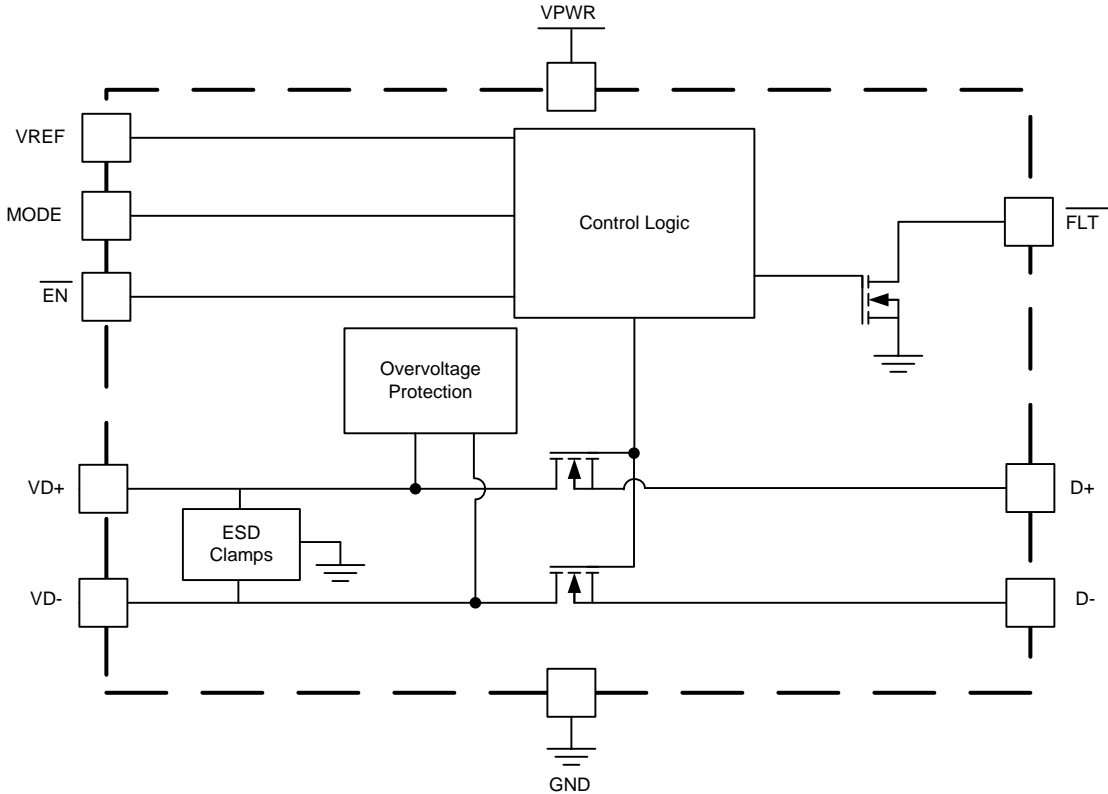
8.1 Overview

The TPD2S703-Q1 is a 2-Channel Data Line Short-to-Battery, Short-to- V_{BUS} , and IEC61000-4-2 ESD protection device for automotive high-speed interfaces like USB2.0. The TPD2S703-Q1 contains two data line nFET switches which ensure safe data communication while protecting the internal system circuits from any overvoltage conditions at the $VD+$ and $VD-$ pins. On these pins, this device can handle overvoltage protection up to 18-V DC. This provides sufficient protection for shorting the data lines to the car battery as well as the USB V_{BUS} rail.

Additionally, the TPD2S703-Q1 has a \overline{FLT} pin which provides an indication when the device sees an overvoltage condition and automatically resets when the overvoltage condition is removed. The TPD2S703-Q1 also integrates IEC ESD clamps on the $VD+$ and $VD-$ pins, thus eliminating the need for external TVS clamp circuits in the application.

The TPD2S703-Q1 has an internal oscillator and charge pump that controls the turnon of the internal nFET switches. The internal oscillator controls the timers that enable the charge pump and resets the open-drain \overline{FLT} output. If $VD+$ and $VD-$ are less than V_{OVP} , the internal charge pump is enabled. After an internal delay, the charge-pump starts-up, turning on the internal nFET switches. At any time, if $VD+$ or $VD-$ rises above V_{OVP} , TPD2S703-Q1 asserts \overline{FLT} pin LOW and the nFET switches are turned off.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 OVP Operation

When the VD+, or VD– voltages rise above V_{OVP} , the internal nFET switches are turned off, protecting the transceiver from overvoltage conditions. The response is very rapid, with the FET switches turning off in less than 1 μ s. Before the OVP condition, the \overline{FLT} pin is High-Z, and is pulled HIGH via an external resistor to indicate there is no fault. Once the OVP condition occurs, the \overline{FLT} pin is asserted LOW. When the VD+, or VD– voltages returns below $V_{OVP} - V_{HYS-OVP}$, the nFET switches are turned on again. When the OVP condition is cleared and the nFETs are completely turned on, the \overline{FLT} is reset to high-Z.

8.3.2 OVP Threshold

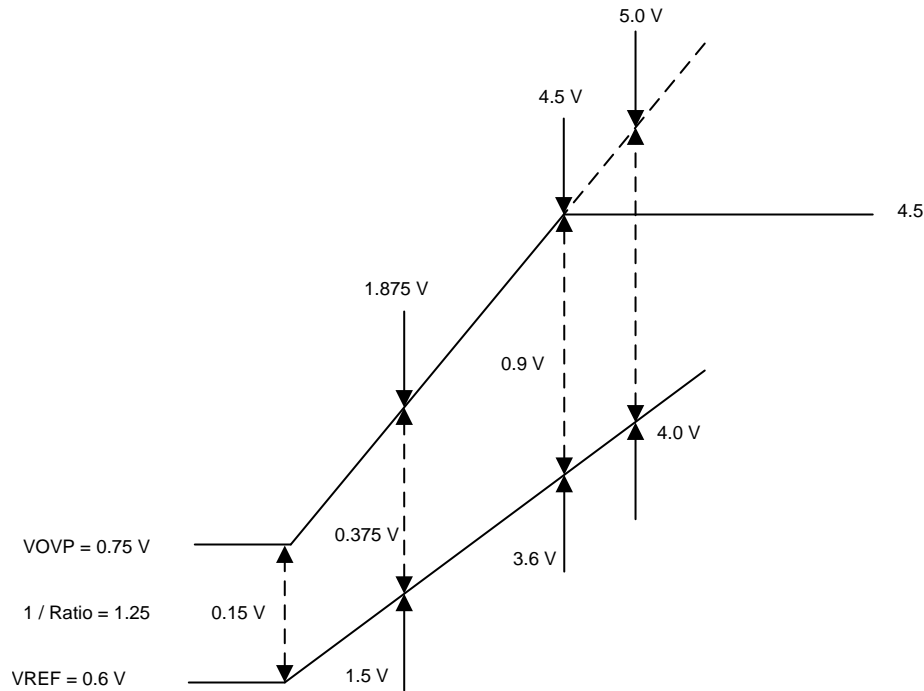


图 22. OVP Threshold

The OVP Threshold V_{OVP} is set by V_{REF} according to 公式 1, 公式 2 and 公式 3.

$$V_{OVP} = 1.25 \times V_{REF} \quad (1)$$

$$V_{REF} \leq 3.6 \text{ V} \quad (2)$$

$$V_{OVP} = 4.5 \text{ V for } V_{REF} > 3.6 \text{ V} \quad (3)$$

公式 1, 公式 2 and 公式 3 yield the typical V_{OVP} values. See the parametric tables for the minimum and maximum values that include variation over temperature and process. 图 22 gives a graphical representation of the relationship between V_{OVP} and V_{REF} .

V_{REF} can be set either by an external regulator (Mode 0) or an internal adjustable regulator (Mode 1). See the [V_{REF} Operation](#) section for more details on how to operate V_{REF} in Mode 0 and Mode 1.

8.3.3 D± Clamping Voltage

The TPD2S703-Q1 provides a differentiated device architecture which allows the system designer to control the clamping voltage the protected transceiver sees from the D+ and D– pins. This architecture allows the system designer to minimize the amount of stress the transceiver sees during Short-to-Battery and ESD events. The clamping voltage that appears on the D+ and D– lines during a short-to-battery or ESD event obeys 公式 4.

$$V_{CLAMP_DP/M} = V_{REF} + V_{BR} + IR_{DYN} \quad (4)$$

Feature Description (接下页)

Where V_{BR} approximately = 0.7 V, IR_{DYN} approximately = 1 V. By adjusting V_{REF} , the clamping voltage of the D+ and D– lines can be adjusted. As V_{REF} also controls the OVP threshold, take care to insure that the V_{REF} setting both satisfies the OVP threshold requirements while simultaneously optimizing system protection on the D+ and D– lines.

The size of the capacitor used on the V_{REF} pin also influences the clamping voltage as transient currents during Short-to-Battery and ESD events flow into the V_{REF} capacitor. This causes the V_{REF} voltage to increase, and likewise the clamping voltage on D_{\pm} according to [公式 4](#). The larger capacitor that is used, the better the clamping performance of the device is going to be. See the parametric tables for the clamping performance of the TPD2S703-Q1 with a 1- μ F capacitor.

8.4 Device Functional Modes

The TPD2S703-Q1 has two modes of operation which vary the way the VREF pin functions. In Mode 0, the VREF pin is connected to an external regulator which sets the voltage on the VREF pin. In Mode 1, the TPD2S703-Q1 uses an adjustable internal regulator to set the VREF voltage. Mode 1 enables the system designer to operate the TPD2S703-Q1 with a single power supply, and have the flexibility to easily set the VREF voltage to any voltage between 0.6 V and 3.8 V with two external resistors.

Typical Application (接下页)

9.2.1 Design Requirements

9.2.1.1 Device Operation

表 1 给出完整的器件功能响应于 $\overline{\text{EN}}$ 引脚，到过电压条件在连接器 (VD_{\pm} 引脚)，到热关断，和到 V_{PWR} ， V_{REF} ，和 MODE 引脚的条件。

表 1. Device Operation Table

Functional Mode	$\overline{\text{EN}}$	MODE	VREF	VPWR	VD $_{\pm}$	TJ	$\overline{\text{FLT}}$	Comments
NORMAL OPERATION								
Mode 0 unpowered 1	X	$R_{\text{bot}} \leq 2.6 \text{ k}\Omega$	X	X	X	X	H	Device unpowered, data switches open
Mode 0 unpowered 2	X	$R_{\text{bot}} \leq 2.6 \text{ k}\Omega$	X	X	X	X	H	Device unpowered, data switches open
Mode 1 unpowered	X	$R_{\text{top}} \parallel R_{\text{bot}} > 14 \text{ k}\Omega$	X	X	X	X	H	Device unpowered, data switches open
Mode 0 disabled	H	$R_{\text{bot}} \leq 2.6 \text{ k}\Omega$	>UVLO	>UVLO	X	<TSD	H	Device disabled, data switches open
Mode 1 disabled	H	$R_{\text{top}} \parallel R_{\text{bot}} > 14 \text{ k}\Omega$	Set by R_{top} and R_{bot}	>UVLO	X	<TSD	H	Device disabled, data switches open, V_{REF} is disabled
Mode 0 enabled	L	$R_{\text{bot}} \leq 2.6 \text{ k}\Omega$	>UVLO	>UVLO	<OVP	<TSD	H	Device enabled, data switches closed, V_{REF} is the value set by the power supply on V_{REF}
Mode 1 enabled	L	$R_{\text{top}} \parallel R_{\text{bot}} > 14 \text{ k}\Omega$	Set by R_{top} and R_{bot}	>UVLO	<OVP	<TSD	H	Device enabled, data switches closed, V_{REF} is the value set by the R_{top} and R_{bot} resistor divider
FAULT CONDITIONS								
Mode 0 thermal shutdown	X	$R_{\text{bot}} \leq 2.6 \text{ k}\Omega$	X	>UVLO	X	>TSD	L	Thermal shutdown, data switches opened, $\overline{\text{FLT}}$ pin asserted
Mode 1 thermal shutdown	X	$R_{\text{top}} \parallel R_{\text{bot}} > 14 \text{ k}\Omega$	Set by R_{top} and R_{bot}	>UVLO	X	>TSD	L	Thermal shutdown, data switches opened, V_{REF} is disabled, $\overline{\text{FLT}}$ pin asserted
Mode 0 OVP fault	L	$R_{\text{bot}} \leq 2.6 \text{ k}\Omega$	>UVLO	>UVLO	>OVP	<TSD	L	Data line overvoltage protection mode. OVP is set relative to the voltage on V_{REF} . Data switches opened, $\overline{\text{FLT}}$ pin asserted
Mode 1 OVP fault	L	$R_{\text{top}} \parallel R_{\text{bot}} > 14 \text{ k}\Omega$	Set by R_{top} and R_{bot}	>UVLO	>OVP	<TSD	L	Data line overvoltage protection mode. OVP is set relative to the voltage on V_{REF} . Data switches opened, fault pin asserted

9.2.2 Detailed Design Procedure

9.2.2.1 V_{REF} Operation

The TPD2S703-Q1 has two modes of operation which vary the way the V_{REF} pin functions. In Mode 0, the V_{REF} pin is connected to an external regulator which sets the voltage on the V_{REF} pin. In Mode 1, the TPD2S703-Q1 uses an adjustable internal regulator to set the V_{REF} voltage. Mode 1 enables the system designer to operate the TPD2S703-Q1 with a single power supply, and have the flexibility to easily set the V_{REF} voltage to any voltage between 0.6 V and 3.8 V with two external resistors.

9.2.2.1.1 Mode 0

To set the device into Mode 0, ensure that R_{bot} , resistance between the MODE pin and ground, is less than 2.6 k Ω . The easiest way to implement Mode 0 is to directly connect the mode pin to GND on your PCB. With this resistance condition met, connect V_{REF} to an external regulator to set the V_{REF} voltage.

9.2.2.1.2 Mode 1

To operate in Mode 1, ensure that $R_{top} \parallel R_{bot}$, resistance between the MODE pin and ground, is greater than 14 k Ω . This is accomplished by insuring $R_{top} \parallel R_{bot} > 14 \text{ k}\Omega$ because when the device is initially powered up, V_{REF} is at ground until the internal circuitry recognizes if the device is in Mode 1 or Mode 2.

In Mode 1, V_{REF} is set by using an internal regulator to set the voltage. Using a resistor divider off of a feedback comparator is how to set V_{REF} , similar to a standard LDO or DC/DC. V_{REF} is set in Mode 1 according to [公式 5](#).

$$V_{REF} = \frac{V_{MODE}(R_{TOP} + R_{BOT})}{R_{BOT}} \quad (5)$$

[公式 5](#) yields the typical value for V_{REF} . When using $\pm 1\%$ resistors R_{TOP} and R_{BOT} , V_{REF} accuracy is going to be $\pm 5\%$. Therefore, the minimum and maximum values for V_{REF} can be calculated off of the typical V_{REF} . The parametric tables above give example R_{TOP} and R_{BOT} resistors to use for standard output V_{REF} voltages for Mode 1.

9.2.2.2 Mode 1 Enable Timing

In Mode 1, when the TPD2S703-Q1 is disabled, the output regulator is disabled, leading V_{REF} to discharge to 0 V through R_{TOP} and R_{BOT} . It is desired for V_{REF} to be at 0 V when the device is disabled to minimize the clamping voltage during a power disabled Short-to-Battery or ESD event. If V_{REF} is at 0 V, this holds D_{\pm} near ground during these fault events.

When enabling the TPD2S703-Q1, V_{REF} is quickly charged up to insure a quick turnon time of the Data FETs. Data FET turnon is gated by V_{REF} reaching 80% of its final voltage plus 150 μs to insure a proper OVP threshold is set before passing data. This prevents false OVPs due to normal operation. Because Data FET turnon is gated by charging the V_{REF} clamping capacitor, the size of the capacitor influences the turnon time of the Data switches. The TPD2S703-Q1's internal regulator uses a constant current source to quickly charge the V_{REF} clamping capacitor, so the charging time of C_{VREF} can easily be calculated with [公式 6](#).

$$t_{CHG_CVREF} = \frac{C_{VREF} \times 0.8 (V_{REF_FINAL})}{I_{CHG_VREF}} \quad (6)$$

Where C_{VREF} is the clamping capacitance on V_{REF} , V_{REF_FINAL} is the final value V_{REF} is set to, and $I_{CHG_VREF} = 22 \text{ mA}$ (typical). If $V_{REF} = 1 \text{ V}$, 0.8 is used in the above equation because 80% of V_{REF} is the amount of time that gates the turnon of the Data FETs. Once t_{CHG_CVREF} is calculated, the typical turnon time of the Data FETs can be calculated from [公式 7](#).

$$t_{ON_EN_MODE1} = t_{CHG_CVREF} + 150 \mu\text{s} \quad (7)$$

9.2.3 Application Curves

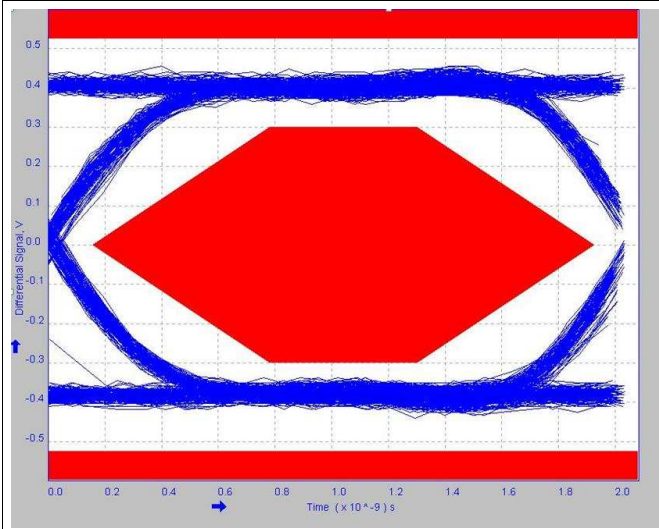


图 24. USB2.0 Eye Diagram (Board Only, Through Path)

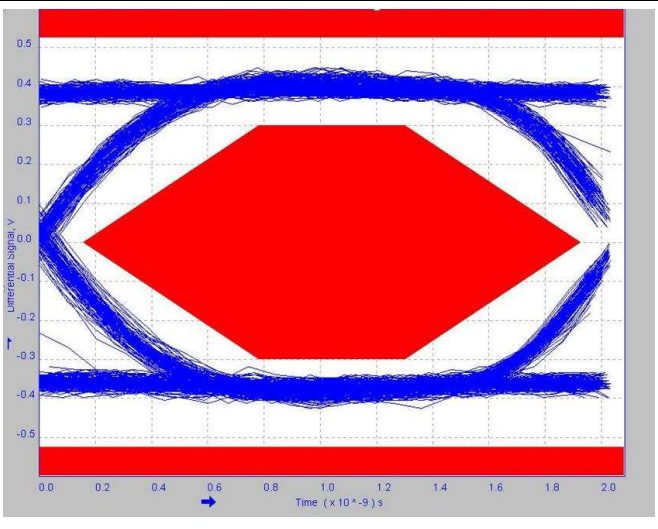


图 25. USB2.0 Eye Diagram (System from Typical Application Schematic)

10 Power Supply Recommendations

10.1 V_{PWR} Path

The V_{PWR} pin provides power to the TPD2S703-Q1. A 10- μ F capacitor is recommended on V_{PWR} as close to the pin as possible for localized decoupling of transients. A supply voltage above the UVLO threshold for V_{PWR} must be supplied for the device to power on.

10.2 V_{REF} Pin

The V_{REF} pin provides a voltage reference for the data switch OVP level as well as a bypass for ESD clamping. A 1- μ F capacitor must be placed as close to the pin as possible and the supply must be set to be above the UVLO threshold for V_{REF} .

11 Layout

11.1 Layout Guidelines

Proper routing and placement maintains signal integrity for high-speed signals. The following guidelines apply to the TPD2S703-Q1:

- Place the bypass capacitors as close as possible to the VPWR and VREF pins. Capacitors must be attached to a solid ground. This minimizes voltage disturbances during transient events such as short-to-battery, ESD, or overcurrent conditions.
- High speed traces (data switch path) must be routed as straight as possible and any sharp bends must be minimized.

Standard ESD recommendations apply to the VD+, VD- pins as well:

- The optimum placement is as close to the connector as possible.
 - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
 - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
 - Electric fields tend to build up on corners, increasing EMI coupling.

11.2 Layout Example

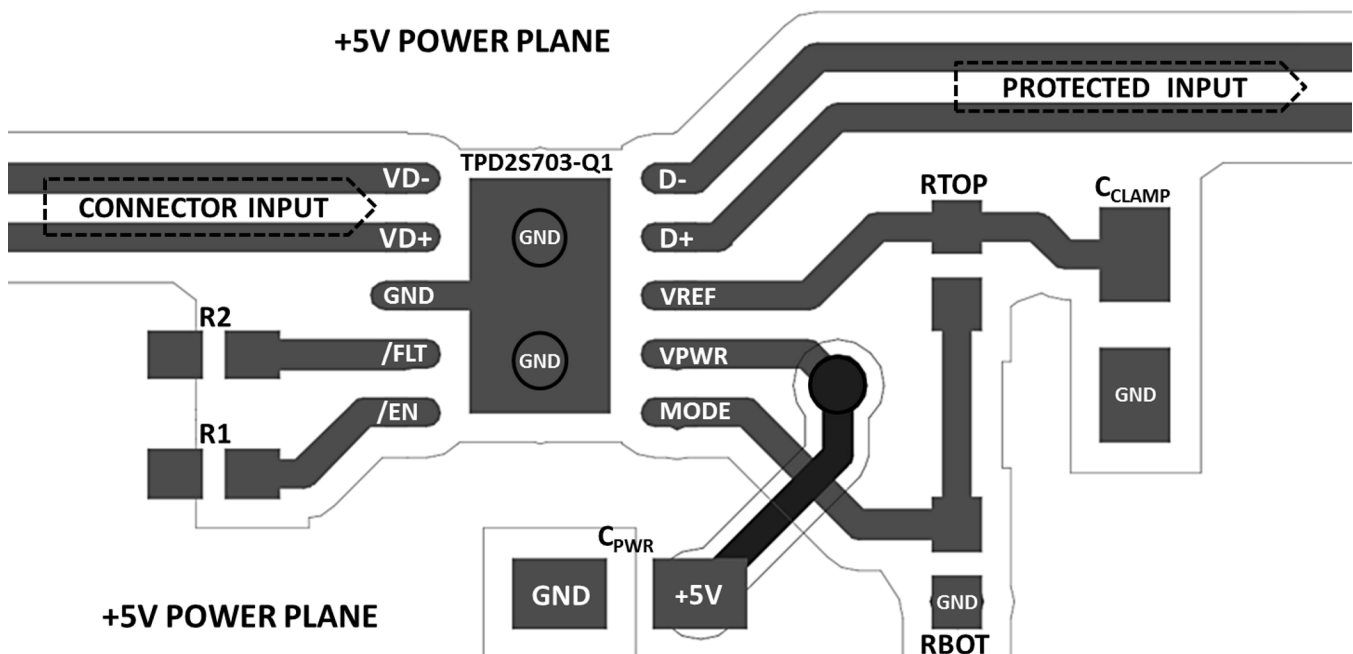


图 26. TPD2S703-Q1 Layout

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

如需相关文档，请参阅：

《TPD2S703-Q1 评估模块用户指南》

12.2 接收文档更新通知

如需接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。请单击右上角的提醒我 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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设计支持 *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.4 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD2S703QDGSRQ1	Active	Production	VSSOP (DGS) 10	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	13Z
TPD2S703QDSKRQ1	Active	Production	SON (DSK) 10	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	14XI

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD2S703QDGSRQ1	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPD2S703QDSKRQ1	SON	DSK	10	3000	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD2S703QDGSRQ1	VSSOP	DGS	10	2500	366.0	364.0	50.0
TPD2S703QDSKRQ1	SON	DSK	10	3000	210.0	185.0	35.0

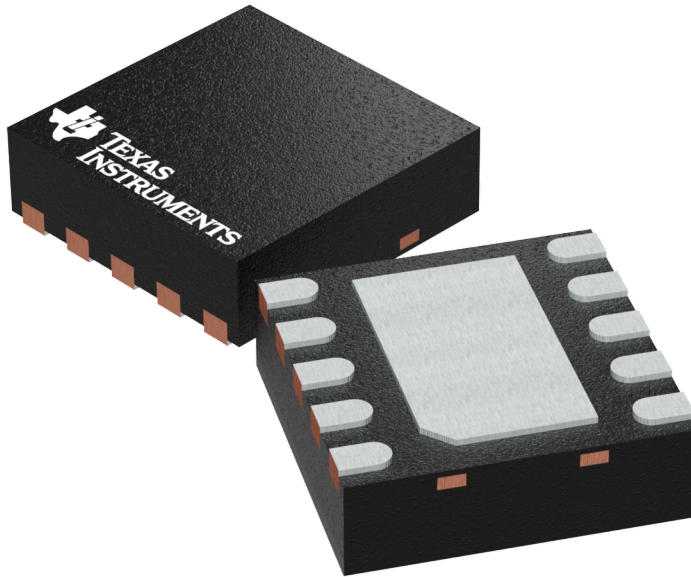
GENERIC PACKAGE VIEW

DSK 10

WSON - 0.8 mm max height

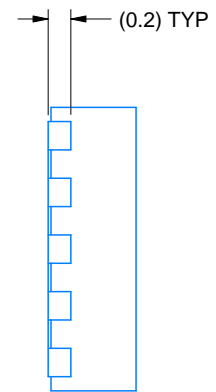
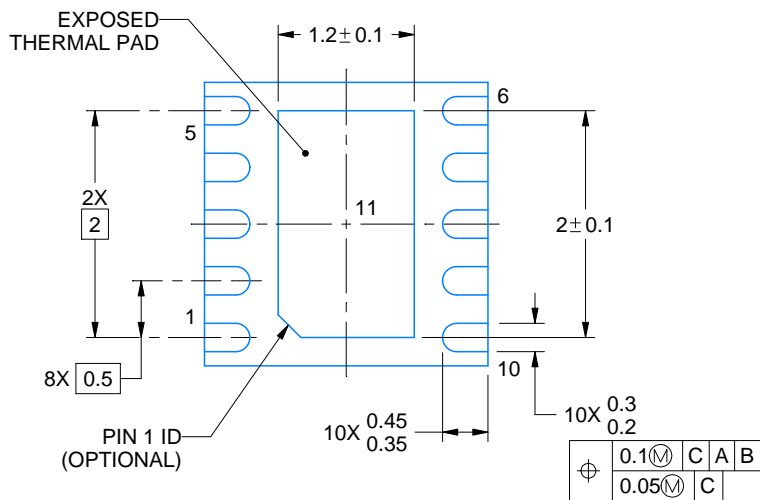
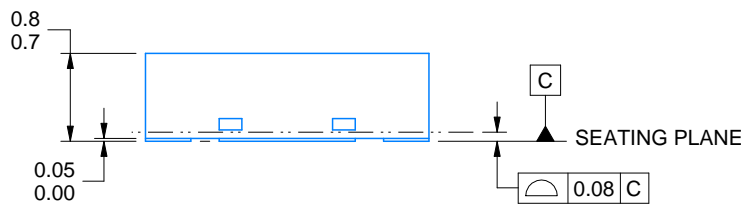
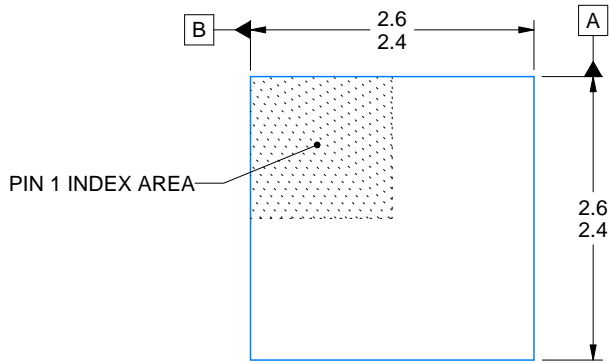
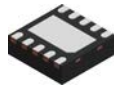
2.5 x 2.5 mm, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4225304/A



4218903/B 10/2020

NOTES:

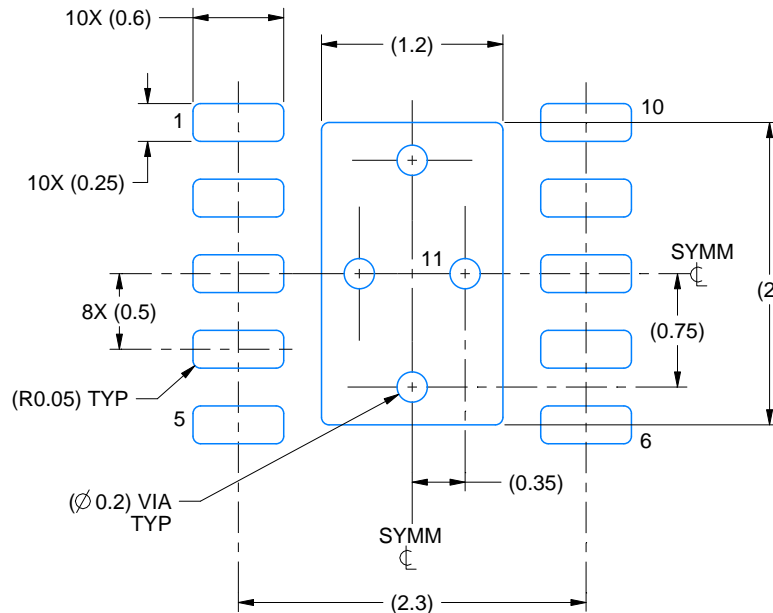
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

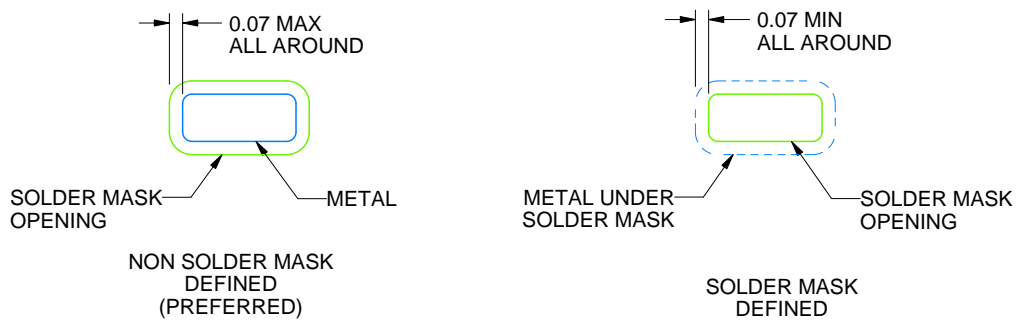
DSK0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218903/B 10/2020

NOTES: (continued)

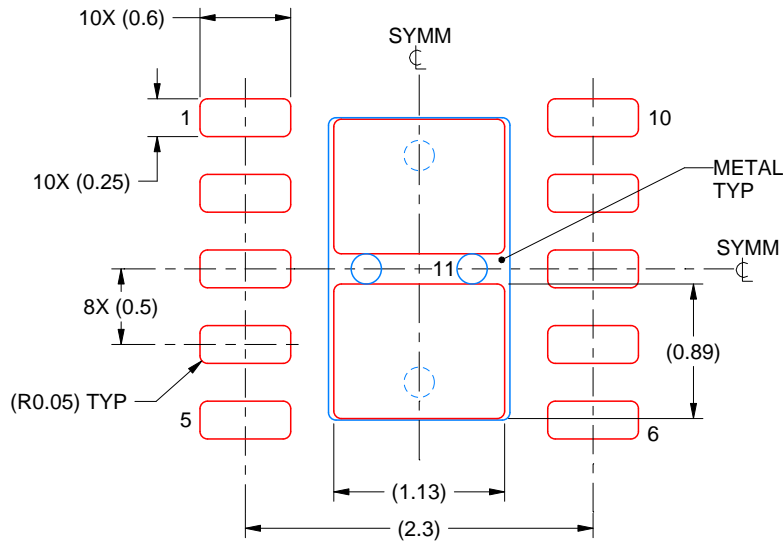
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DSK0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

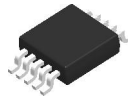
EXPOSED PAD 11
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4218903/B 10/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

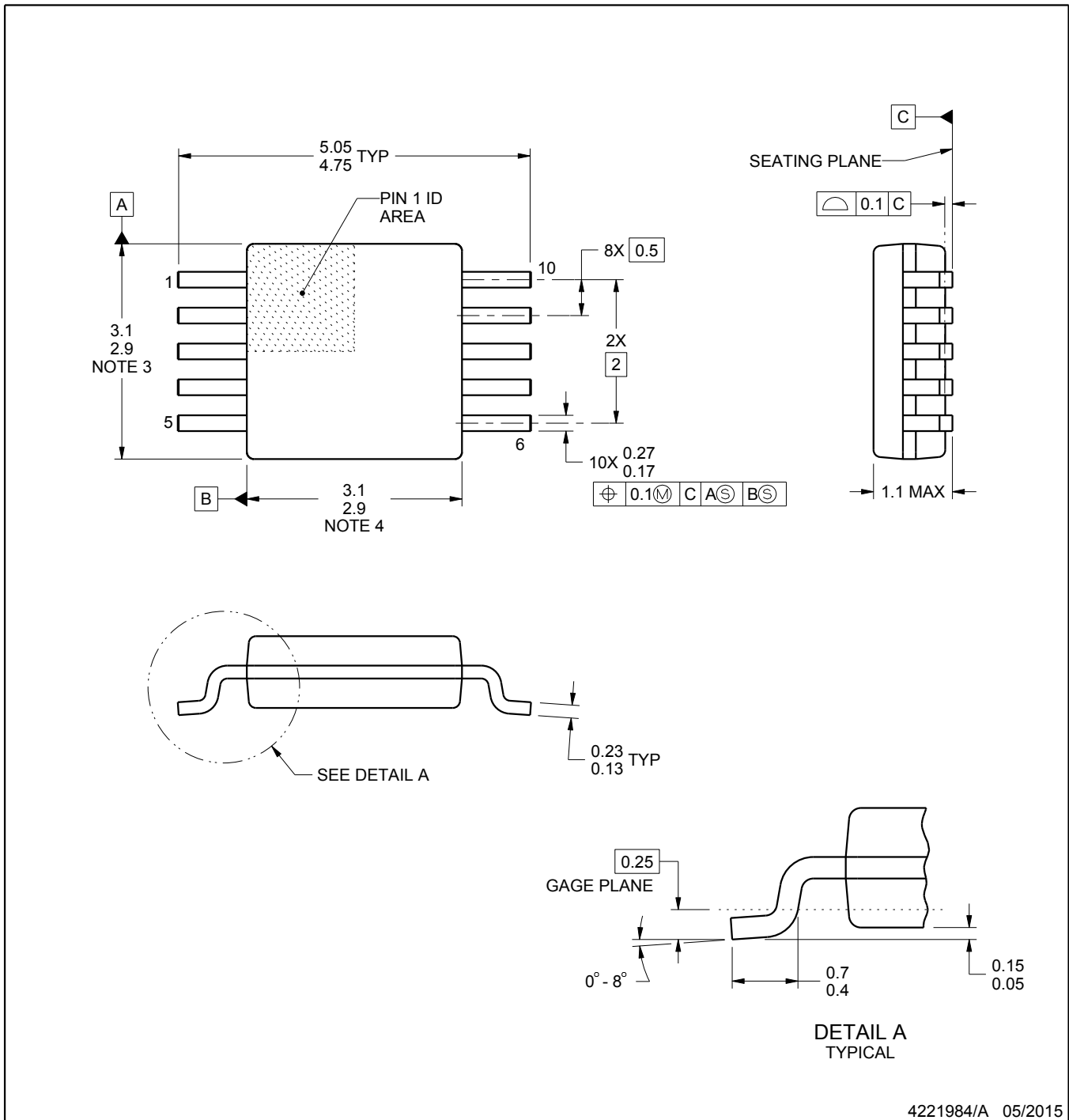
DGS0010A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4221984/A 05/2015

NOTES:

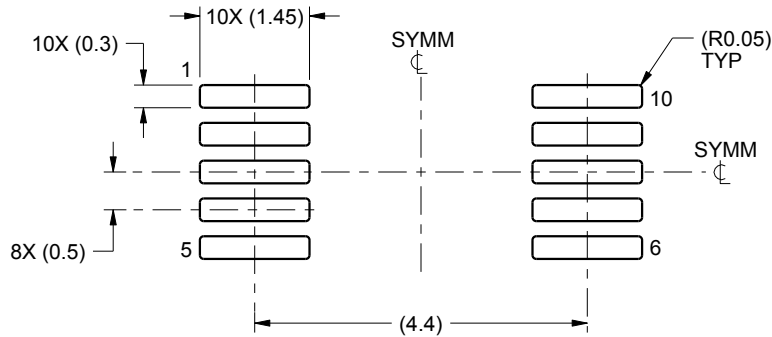
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

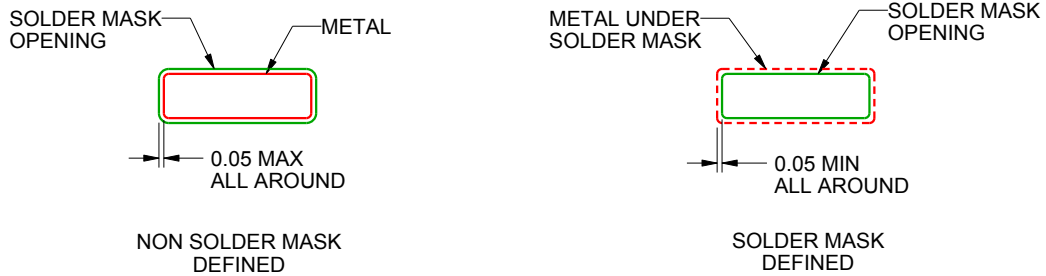
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

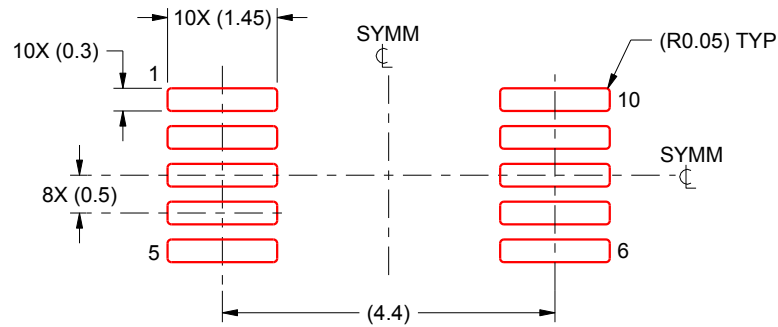
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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