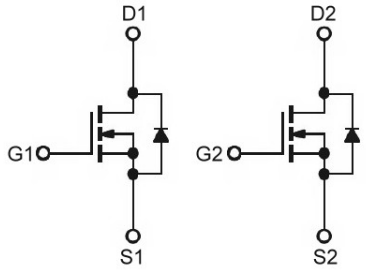
MSH40N30D

Dual N-Channel 40-V (D-S) MOSFET

Description

The device is using trench DMOS technology. This advanced technology has been especially tailored to minimize $R_{DS(ON)}$, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

Graphic Symbol



Features

- $R_{DS(ON)}$ = 9mΩ @ V_{GS} =10V
- Fast switching
- Improve dv/dt Capability
- 100% EAS Guaranteed
- Green Device Available

Typical Applications

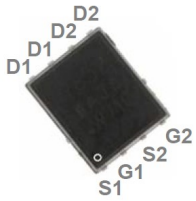
- Notebook
- Load Switch
- Hand-held Device

Package type：PDFN 5X6 Dual

AEC-Q101 qualified

Packing & Order Information

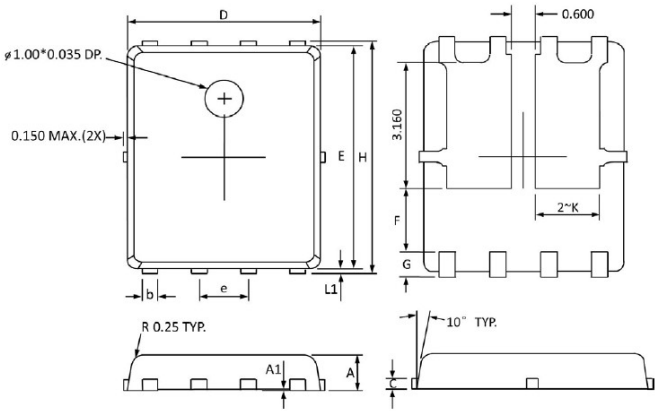
3,000/Reel



AEC-Q101 Qualified
Available

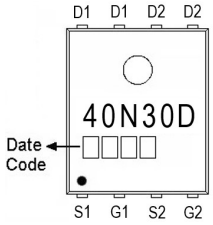
RoHS Compliant

Package Dimension



REF.	Millimeter			REF.	Millimeter		
	Min.	Nom.	Max.		Min.	Nom.	Max.
A	0.90	1.00	1.10	E	5.70	-	5.90
A1	0.00	-	0.05	e	-	1.27	-
b	0.33	-	0.51	H	5.90	-	6.20
c	0.20	-	0.30	G	0.50	-	0.70
D	4.80	-	5.00	L1	0.06	-	0.20
F	1.6 Ref.			K	-	1.60	-

Marking



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MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings			
Symbol	**Parameter**	**Value**	**Units**
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Continuous Drain Current[1] (T_C =25°C)	30	A
	Continuous Drain Current[1] (T_C =100°C)	19	A
I_{DM}	Pulsed Drain Current[1,2]	120	A
I_{AS}	Single Pulse Avalanche Current, L =0.1mH[3]	36	A
E_{AS}	Single Pulse Avalanche Energy, L =0.1mH[3]	64	mJ
P_D	Power Dissipation[4] (T_C =25°C)	46	W
	Power Dissipation[4] – Derate above 25°C	0.37	W/°C
T_J/T_{STG}	Operating Junction and Storage Temperature	-55 to +150	°C

Thermal Resistance Ratings			
Symbol	**Parameter**	**Maximum**	**Units**
$R_{\theta JA}$	Maximum Junction-to-Ambient[1]	62	°C/W
$R_{\theta JC}$	Maximum Junction-to-Case[1]	2.7	°C/W

Electrical Characteristics (T_J=25°C unless otherwise specified)						
Symbol	**Parameter**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Units**
$V_{GS\ (th)}$	Gate Threshold Voltage	V_{DS} =V_{GS}, I_D =250μA	1.0	1.6	2.5	V
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} =0V, I_D =250μA	40	-	-	V
g_{fs}	Forward Transconductance	V_{DS} =10V, I_D =10A	-	13	-	S
I_{GSS}	Gate-Source Leakage Current	V_{DS} =0V, V_{GS} =±20V	-	-	±100	nA
I_{DSS}	Drain-Source Leakage Current	V_{DS} =40V, V_{GS} =0V, T_J =25°C V_{DS} =32V, V_{GS} =0V, T_J =125°C	-	-	1 10	μA
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS} =10V, I_D =8A V_{GS} =4.5V, I_D =4A	- -	7.2 9.5	9 12	mΩ
EAS	Single Pulse Avalanche Energy[5]	V_{DD} =25V, L =0.1mH, I_{AS} =6A	1.8		-	mJ
V_{SD}	Diode Forward Voltage[2]	I_S =1A, V_{GS} =0V, T_J =25°C	-	-	1.0	V
I_S	Continuous Source Current[1,6]	V_G =V_D =0V, Force Current	-	-	30	A
I_{SM}	Pulsed Source Current[2,6]		-	-	60	

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Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Q_g	Total Gate Charge[2]	V_{DS} =20V I_D =8A V_{GS} =4.5V	--	12.2	24	nC
Q_{gs}	Gate-Source Charge		--	3.3	7	
Q_{gd}	Gate-Drain Charge		--	6.7	13	
$t_{d(on)}$	Turn-On Delay Time[2]	V_{DS} =15V I_D =1A V_{GS} =10V R_G =3.3Ω	--	13.2	25	ns
t_r	Rise Time		--	2.2	5	
$t_{d(off)}$	Turn-Off Delay Time		--	72	130	
t_f	Fall Time		--	4.5	10	
C_{ISS}	Input Capacitance	V_{DS} =25V V_{GS} =0V f =1.0MHz	--	1220	2200	pF
C_{OSS}	Output Capacitance		--	130	250	
C_{RSS}	Reverse Transfer Capacitance		--	55	110	
Rg	Gate Resistance	V_{GS} =V_{DS} =0V, f =1.0MHz	--	2.2	--	Ω

Notes

1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.
3. The EAS data shows maximum rating. The test condition is V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=36A.
4. The power dissipation is limited by 150℃ junction temperature.
5. The Min. value is 100% EAS tested guarantee.
6. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

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- **Typical Electrical Characteristics**

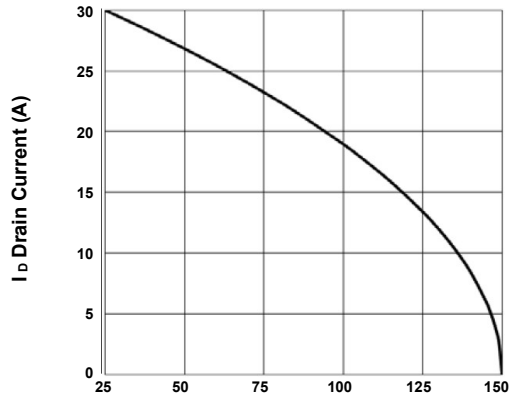

FIG.1-Drain Current vs. T_C

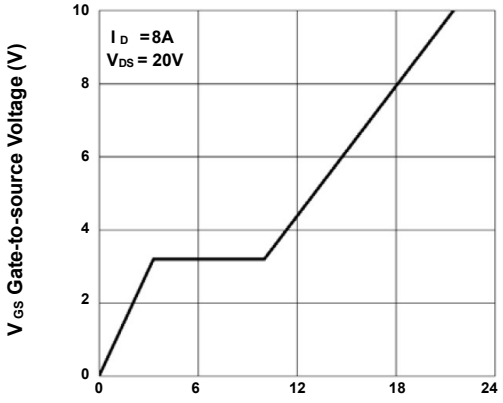

FIG.2-Gate Charge Characteristics

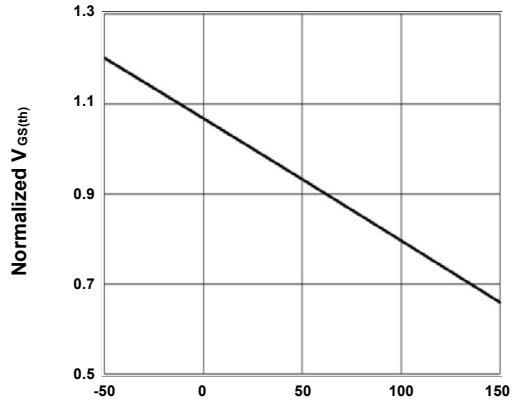

FIG.3-Normalized $V_{GS(th)}$ vs. T_J

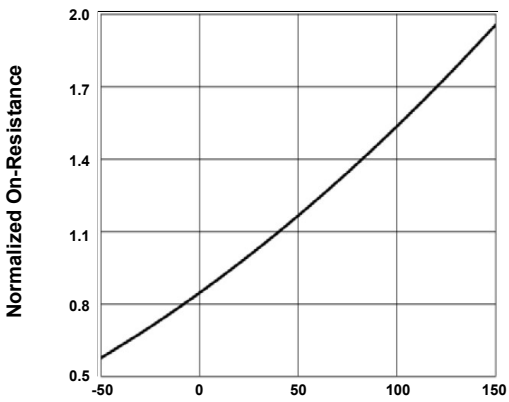

FIG.4-Normalized R_{DSON} vs. T_J

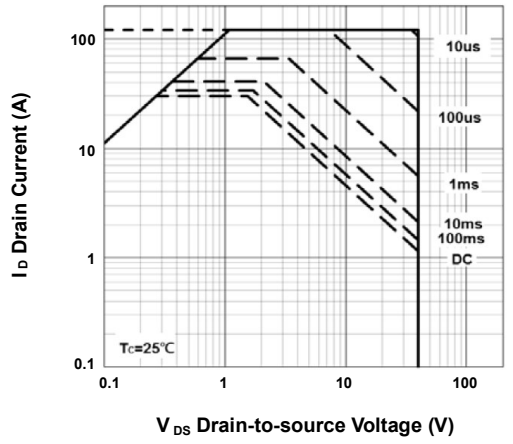

FIG.5-Safe Operating Area

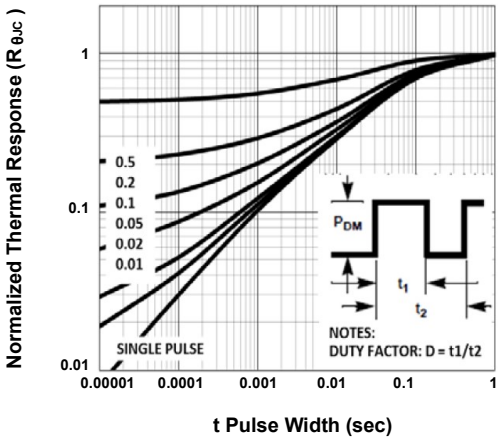

FIG.6-Transient Thermal Impedance

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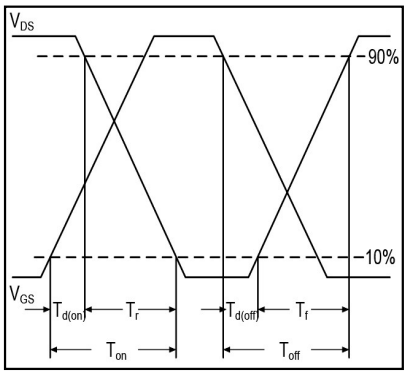

FIG.7-Switching Time Waveform

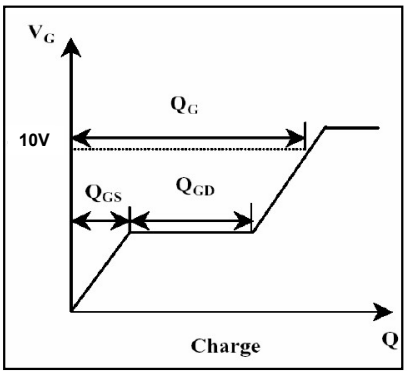

FIG.8-Gate Charge Waveform

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