CDCE62002 Four Output Clock Generator/Jitter Cleaner With Integrated Dual VCOs

1 Features

- Frequency Synthesizer With PLL/VCO and Partially Integrated Loop Filter
- Fully Configurable Outputs Including Frequency and Output Format
- Smart Input Multiplexer Automatically Switches Between One of Two Reference Inputs
- Multiple Operational Modes Include Clock Generation Through Crystal, SERDES Start-Up Mode, Jitter Cleaning, and Oscillator Based Holdover Mode
- Integrated EEPROM Determines Device Configuration at Power Up
- Excellent Jitter Performance
- Integrated Frequency Synthesizer Including PLL, Multiple VCOs, and Loop Filter:
  - Full Programmability Facilitates Phase Noise Performance Optimization Enabling Jitter Cleaner Mode
  - Programmable Charge Pump Gain and Loop Filter Settings
  - Unique Dual-VCO Architecture Supports a Wide Tuning Range 1.750 GHz to 2.356 GHz.
- Universal Output Blocks Support Up to 2 Differential, 4 Single-Ended, or Combinations of Differential or Single-Ended:
  - 0.5 ps RMS (10 kHz to 20 MHz) Output Jitter Performance
  - Low Output Phase Noise: –130 dBc/Hz at 1 MHz Offset, Fc = 491.52 MHz
  - Output Frequency Ranges From 10.94 MHz to 1.175 GHz in Synthesizer Mode
  - LVPECL, LVDS, and LVCMOS
  - Independent Output Dividers Support Divide Ratios for 1, 2, 3, 4, 5, 8, 10, 12, 16, 20, 24, and 32
- Flexible Inputs With Innovative Smart Multiplexer:
  - Two Universal Differential Inputs Accept Frequencies from 1 MHz up to 500 MHz (LVPECL), 500 MHz (LVDS), or 250 MHz (LVCMOS)
  - One Auxiliary Input Accepts Crystals in the Range of 2 MHz to 42 MHz
  - Clock Generator Mode Using Crystal Input
  - Smart Input Multiplexer Can be Configured to Automatically Switch Between Highest Priority Clock Source Available Allowing for Fail-Safe Operation
- Typical Power Consumption 750 mW at 3.3 V
- Integrated EEPROM Stores Default Settings; Therefore, the Device Can Power Up in a Known, Predefined State
- Offered in QFN-32 Package
- ESD Protection Exceeds 2000 V HBM
- Industrial Temperature Range: –40°C to +85°C

2 Applications

- Data Converter and Data Aggregation Clocking
- Wireless Infrastructure
- Switches and Routers
- Medical Electronics
- Military and Aerospace
- Industrial
- Clock Generation and Jitter Cleaning

3 Description

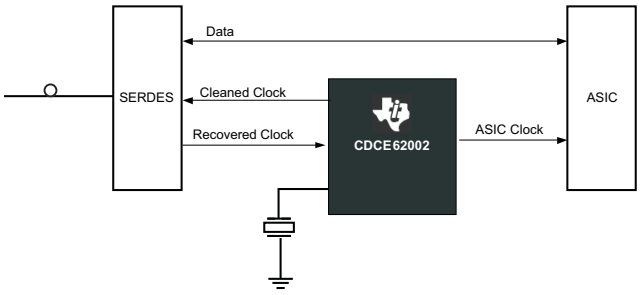
The CDCE62002 device is a high-performance clock generator featuring low output jitter, a high degree of configurability through a SPI interface, and programmable start-up modes determined by on-chip EEPROM. Specifically tailored for clocking data converters and high-speed digital signals, the CDCE62002 achieves jitter performance under 0.5 ps RMS (1).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CDCE62002	VQFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

CDCE62002 Application Example



(1) 10-kHz to 20-MHz integration bandwidth.

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4 Revision History

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- Added figure titles. ... 12
- Updated Figure 18 ... 19
- Updated Figure 20 ... 20
- Corrected description for bits 0 and 1 in *CDCE62002 Register 0 Bit Definitions* ... 36
- Corrected the register bits for LVPECL-AC, LVPECL-DC, LVDS-AC, LVDS-DC reference inputs in *Reference Input AC/DC Input Termination Table* ... 37

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- Added 3 rows in TIMING REQUIREMENTS table, under Duty Cycle row ... 9
- Added a sentence below Equation 3 ... 16
- Changed last row last column in Figure 23 truth table from *Disabled* to *Input Buffer Termination Disabled* ... 20
- Changed in Table 13, second column, 5th and 6th row from 1 to 0 ... 23
- Added a reference to Table 11 and 2 references to Table 12 in Table 6 ... 36
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- Changed changed last row in Table 8 Description column, from "always reads 1" to "May read back to 1 or 0" ... 37

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- Changed the description of Pin 19, TESTSYNC To: Reserved Pin.....resistor. ... 6
- Changed pin 31 From: Power To: A. Power in *Pin Functions* table ... 6
- Changed *Pin Functions* table, Pins 9, 12 to VCC_OUT0. Pins 13 and 16 to VCC_OUT1 ... 6
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- Added SPI OUTPUT row From: PLL To: PLL_LOCK ... 8
- Changed t_r / t_f Max value From: 735 To: 135 ... 9
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- Added Driver Level and Max shunt capacitance to AUXILARY_IN REQUIREMENT in the TIMING REQUIREMENTS table ... 9
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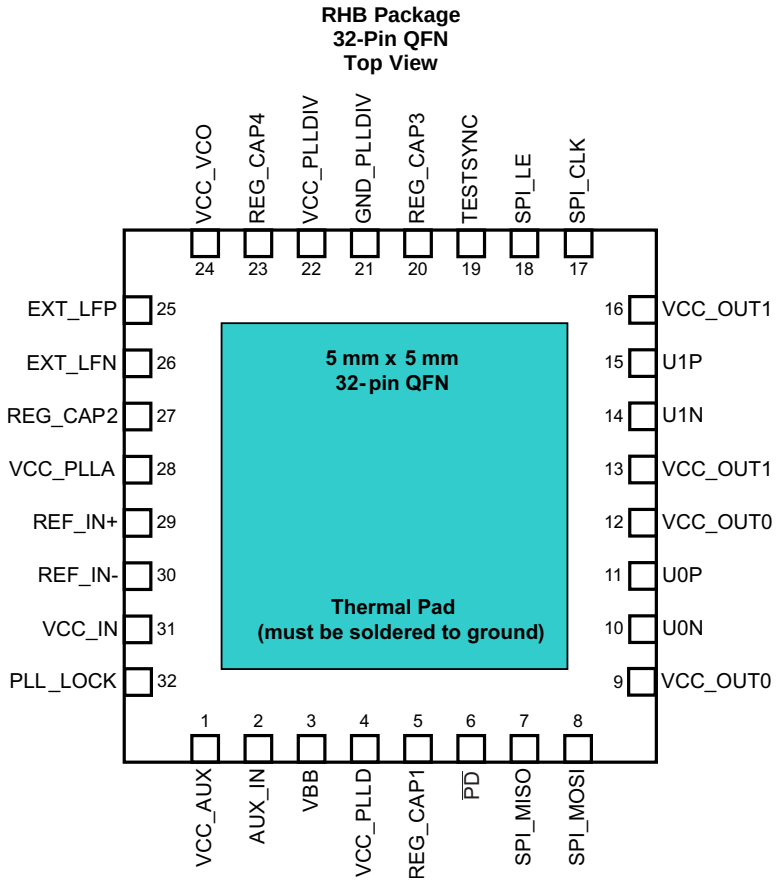
5 Description (continued)

It incorporates a synthesizer block with partially integrated loop filter, a clock distribution block including programmable output formats, and an input block featuring an innovative smart multiplexer. The clock distribution block includes two individually programmable outputs that can be configured to provide different combinations of output formats (LVPECL, LVDS, LVCMOS). Each output can also be programmed to a unique output frequency (ranging from 10.94 MHz to 1.175 GHz (1)). If Both outputs are configured in single-ended mode (such as LVCMOS), the CDCE62002 supports up to four outputs. The input block includes one universal differential inputs which support frequencies up to 500 MHz and an auxiliary input that can be configured to connect to an external AT-Cut crystal through an onboard oscillator block. The smart input multiplexer has two modes of operation, manual and automatic. In manual mode, the user selects the synthesizer reference through the SPI interface. In automatic mode, the input multiplexer will automatically select between the highest priority input clock available.

6 Pin Configuration and Functions



(1) Frequency range depends on operational mode and output format selected.

Pin Functions

PIN		TYPE	DESCRIPTION(1)
NAME	NO.		
AUX_IN	2	I	Auxiliary Input is a Crystal input pin that connect to an internal oscillator circuitry.
EXT_LFN	26	Analog	External Loop Filter Input Negative.
EXT_LFP	25	Analog	External Loop Filter Input Positive
GND	PAD	Ground	Ground is on Thermal PAD. See *Layout Guidelines*
GND_PLLDIV	21	Ground	Ground for PLL Divider circuitry. (short to GND)
$\overline{PD}$	6	I	$\overline{PD}$ or Power-Down Pin is an active low pin and can be activated externally or through the corresponding Bit in SPI Register 2 While $\overline{PD}$ is asserted (low), the device is shut down. When $\overline{PD}$ switches high the EEPROM becomes loaded into the RAM. After the selected input clock signal becomes available, the VCO starts calibration and the PLL aims to achieve lock. All Output dividers become initiated. During self-calibration, the outputs are held static (for example, logical zero). $\overline{PD}$ pin has an internal 150-kΩ pullup resistor. *Note: The SPI_LE signal has to be high in order for the EEPROM to load correctly into RAM on the Rising edge of $\overline{PD}$.*
PLL_LOCK	32	O	PLL Lock indicator
REF_IN+	29	I	Universal Input Buffer (LVPECL, LVDS, LVCMOS) positive input for the Reference Clock.
REF_IN–	30	I	Universal Input Buffer (LVPECL, LVDS,) negative input for the Reference Clock. This pin must be pulled to ground through 1-kΩ resistor when input is selected LVCMOS.
REG_CAP1	5	Analog	Capacitor for the internal Regulator. Connect to a 10-µF Capacitor (Y5V)
REG_CAP2	27	Analog	Capacitor for the internal Regulator. Connect to a 10-µF Capacitor (Y5V)
REG_CAP3	20	Analog	Capacitor for the internal Regulator. Connect to a 10-µF Capacitor (Y5V)
REG_CAP4	23	Analog	Capacitor for the internal Regulator. Connect to a 10-µF Capacitor (Y5V)
SPI_CLK	17	I	LVCMOS input, serial Control Clock Input for the SPI bus interface, with Hysteresis.
SPI_LE	18	I	LVCMOS input, control Latch Enable for Serial Programmable Interface. *Note: The SPI_LE signal has to be high in order for the EEPROM to load correctly on the Rising edge of $\overline{PD}$.* The input has an internal 150-kΩ pull-up resistor
SPI_MISO	7	O	3-state LVCMOS Output that is enabled when SPI_LE is asserted low. It is the serial Data Output to the SPI bus interface.
SPI_MOSI	8	I	LVCMOS input, Master Out Slave In as a serial Control Data Input to CDCE62002 for the SPI bus interface.
TESTSYNC	19	I	Reserved Pin. Pull this pin down to ground using 1-kΩ resistor.
U0P:U0N U1P:U1N	11,10 15,14	O	The outputs of **CDCE62002** are user definable and can be any combination of up to 2 LVPECL outputs, 2 LVDS outputs or up to 4 LVCMOS outputs. The outputs are selectable through SPI interface. The power-up setting is EEPROM configurable.
VBB	3	Analog	Capacitor for the internal termination Voltage. Connect to a 1-µF Capacitor (Y5V)
VCC_AUX	1	A. Power	3.3-V Supply Power for Crystal/Auxiliary Input Buffer Circuitry
VCC_IN	31	A. Power	3.3-V Supply Power for Input Buffer Circuitry
VCC_OUT0	9, 12	Power	3.3-V Supply for the Output Buffers.
VCC_OUT1	13, 16		
VCC_PLLA	28	A. Power	3.3-V Supply Power for the PLL circuitry.
VCC_PLLD	4	Power	3.3-V Supply Power for the PLL circuitry.
VCC_PLLDIV	22	Power	3.3-V Supply Power for the PLL circuitry.
VCC_VCO	24	A. Power	3.3-V Supply Power for the VCO circuitry.

(1) It is furthermore recommended to use a supply filter for each VCC supply domain independently. A minimum requirement is to group the supplies into four independent groups:
VCC_PLLA + VCC_VCO
VCC_PLLD + VCC_PLLDIV
VCC_IN + VCC_AUXIN
VCC_OUT0 + VCC_OUT1
All VCC pins need to be connected for the device to operate properly.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
	Supply voltage VCC (2)	–0.5		V
	Input voltage, V_I (3)	–0.5		V
	Output voltage, V_O (3)	–0.5		V
	Input current (V_I < 0, V_I > VCC)		±20	mA
	Output current for LVPECL/LVCMOS Outputs (0 < V_O < V_{CC})		±50	mA
T_J	Junction temperature		125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All supply voltages have to be supplied simultaneously.
(3) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

7.2 Thermal Information

THERMAL METRIC(1)			CDCE62002 QFN (RGZ) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JEDEC Compliant Board - 3×3 vias on pad)	0-lfm Airflow	35	°C/W
		200-lfm Airflow	28.3	
		400-lfm Airflow	27.2	
$R_{\theta JP}$	Junction-to-pad		1.13	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.3 Electrical Characteristics

recommended operating conditions for the CDCE62002 Device for under the specified Industrial temperature range of –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
POWER SUPPLY						
	Supply voltage, V_{CC_OUT}, V_{CC_PLLDIV}, V_{CC_PLLD}, V_{CC_IN}, and V_{CC_AUX}		3	3.3	3.6	V
	Analog supply voltage, VCC_PLLA, & VCC_VCO		3	3.3	3.6	V
P_{LVPECL}	REF at 30.72 MHz, outputs are LVPECL	Output 1 = 491.52 MHz Output 2 = 245.76 MHz In case of LVCMOS Outputs (1) = 245.76MHz		850		mW
P_{LVDS}	REF at 30.72 MHz, outputs are LVDS			750		mW
P_{LVCMOS}	REF at 30.72 MHz, outputs are LVCMOS			800		mW
P_{OFF}	REF at 30.72 MHz	Outputs are disabled		450		mW
P_{PD}		Device is powered down		40		mW
DIFFERENTIAL INPUT MODE (REF_IN)						
	Differental Input amplitude, (VIN+ – VIN–)		0.1		1.3	V
	Common-mode input voltage, VIC		1.0		V_{CC}–03	V
I_{IH}	Differential input current high (no internal termination)	V_I = V_{CC}, V_{CC} = 3.6 V			20	µA
I_{IL}	Differential input current low (no internal termination)	V_I = 0 V, V_{CC} = 3.6 V	–20			µA
Input Capacitance on REF_IN				3		pF
CRYSTAL INPUT SPECIFICATIONS						
	On-chip load capacitance		8		10	pF
	Equivalent Series Resistance (ESR)				50	Ω

(1) All typical values are at VCC = 3.3 V, temperature = 25°C.

Electrical Characteristics (continued)

recommended operating conditions for the CDCE62002 Device for under the specified Industrial temperature range of –40°C to 85°C

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
LVCMOS INPUT MODE (SPI_CLK,SPI_MOSI,SPI_LE,$\overline{PD}$, REF_IN)							
V_{IL}	Low-level input voltage LVCMOS			0		0.3 V_{CC}	V
V_{IH}	High-level input voltage LVCMOS			0.7 V_{CC}		V_{CC}	V
V_{IK}	LVCMOS input clamp voltage	V_{CC} = 3 V, I_I = –18 mA				–1.2	V
I_{IH}	LVCMOS input current VI =	$V_{CC,}$ V_{CC} = 3.6 V				20	µA
I_{IL}	LVCMOS input (Except REF_IN)	V_I = 0 V, V_{CC} = 3.6 V		–10		–40	µA
I_{IL}	LVCMOS input (REF_IN)	V_I = 0 V, V_{CC} = 3.6 V		–10		10	µA
C_I	Input capacitance (LVCMOS signals)	V_I = 0 V or V_{CC} = 3			3		pF
SPI OUTPUT (MISO) / PLL_LOCK							
I_{OH}	High-level output current	V_{CC} = 3.3 V,	V_O = 1.65 V		–30		mA
I_{OL}	Low-level output current	V_{CC} = 3.3 V,	V_O = 1.65 V		33		mA
V_{OH}	High-level output voltage for LVCMOS outputs	V_{CC} = 3 V,	I_{OH} = –100 µA	V_{CC}–0.5			V
V_{OL}	Low-level output voltage for LVCMOS outputs	V_{CC} = 3 V,	I_{OH} = 100 µA			0.3	V
C_O	Output capacitance o MISO	V_{CC} = 3.3 V; V_O = 0 V or V_{CC}			3		pF
I_{OZH}	3-state output current	V_O = V_{CC}, V_O = 0 V			5		µA
I_{OZL}					–5		µA
EEPROM							
EEcyc	Programming cycle of EEPROM			100	1000		Cycles
EEret	Data retention			10			Years
VBB (INPUT BUFFER INTERNAL TERMINATION VOLTAGE REFERENCE)							
V_{BB}	Input termination voltage	IBB = –0.2 mA, depending on the setting		1.2		1.9	V
INPUT BUFFERS INTERNAL TERMINATION RESISTORS (REF_IN)							
	Termination resistance	Single-ended			5		kΩ
PHASE DETECTOR							
f_{CPmax}	Charge pump frequency			0.04		40	MHz
LVCMOS							
f_{clk}	Output frequency, see Figure 7	Load = 5 pF to GND				250	MHz
V_{OH}	High-level output voltage for LVCMOS outputs	V_{CC} = min to max	I_{OH} = –100 µA	V_{CC}–0.5			V
V_{OL}	Low-level output voltage for LVCMOS outputs	V_{CC} = min to max	I_{OL} = 100 µA			0.3	V
I_{OH}	High-level output current	V_{CC} = 3.3 V	V_O = 1.65 V		–30		mA
I_{OL}	Low-level output current	V_{CC} = 3.3 V	V_O = 1.65 V		33		mA
t_{sko}	Skew, output to output For Y0 to Y1	Both outputs set at 122.88 MHz, reference = 30.72 MHz			75		ps
C_O	Output capacitance on Y0 to Y1	V_{CC} = 3.3 V; V_O = 0 V or V_{CC}			5		pF
I_{OZH}	Tristate LVCMOS output current	V_O = V_{CC}			5		µA
I_{OZL}	Tristate LVCMOS output current	V_O = 0 V			-5		µA
I_{OPDH}	Power-down output current	V_O = V_{CC}				25	µA
I_{OPDL}	Power-down output current	V_O = 0 V				5	µA
Duty cycle	LVCMOS			45%		55%	
$t_{slew-rate}$	Output rise/fall slew rate			3.6	5.2		V/ns
LVDS OUTPUT							
f_{clk}	Output frequency	Configuration load (see Figure 8)		0		800	MHz
|VOD|	Differential output voltage	R_L = 100 Ω		270		550	mV
ΔV_{OD}	LVDS VOD magnitude change					50	mV
V_{OS}	Offset voltage	–40°C to 85°C			1.24		V
ΔV_{OS}	VOS magnitude change				40		mV
	Short-circuit Vout+ to ground	VOUT = 0				27	mA

Electrical Characteristics (continued)

recommended operating conditions for the CDCE62002 Device for under the specified Industrial temperature range of –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
	Short-cicuit Vout- to ground	VOUT = 0			27	mA
$t_{sk(o)}$	Skew, output to output For Y0 to Y1	Both outputs set at 122.88 MHz reference = 30.72 MHz		10		ps
C_O	Output capacitance on Y0 to Y1	V_{CC} = 3.3 V; VO = 0 V or V_{CC}		5		pF
I_{OPDH}	Power-down output current	$V_O = V_{CC}$			25	µA
I_{OPDL}	Power-down output current	V_O = 0 V			5	µA
	Duty cycle		45%		55%	
t_r / t_f	Rise and fall time	20% to 80% of V_{OPP}	110	160	190	ps
LVCMOS-TO-LVDS						
t_{skP_C}	Output skew between LVCMOS and LVDS outputs	V_{CC}/2 to crosspoint	1.4	1.7	2.0	ns
LVPECL OUTPUT						
f_{clk}	Output frequency	Configuration load (see Figure 9 and Figure 10)	0		1175	MHz
V_{OH}	LVPECL high-level output voltage	Load	V_{CC} –1.1		V_{CC} –0.88	V
V_{OL}	LVPECL low-level output voltage	Load	V_{CC} –2.02		V_{CC} –1.48	V
|VOD|	Differential output voltage		510		870	mV
t_{sko}	Skew, output to output For Y0 to Y1	Both outputs set at 122.88 MHz		15		ps
$_{CO}$	Output capacitance on Y0 to Y1	V_{CC} = 3.3 V; VO = 0 V or V_{CC}		5		pF
I_{OPDH}	Power-down output current	$V_O = V_{CC}$			25	µA
I_{OPDL}	Power-down output current	V_O = 0 V			5	µA
	Duty cycle		45%		55%	
t_r / t_f	Rise and fall time	20% to 80% of V_{OPP}	55	75	135	ps
LVDS-TO- LVPECL						
t_{skP_C}	Output skew between LVDS and LVPECL outputs	Crosspoint to Crosspoint	130	200	280	ps
LVCMOS-TO- LVPECL						
t_{skP_C}	Output skew between LVCMOS and LVPECL outputs	V_{CC}/2 to Crosspoint	1.6	1.8	2.2	ns
LVPECL Hi-PERFORMANCE OUTPUT						
V_{OH}	LVPECL high-level output voltage	Load	V_{CC} –1.11		V_{CC} –0.91	V
V_{OL}	LVPECL low-level output voltage	Load	V_{CC} –2.06		V_{CC} –1.84	V
|VOD|	Differential output voltage		670		950	mV
t_r / t_f	Rise and fall time	20% to 80% of V_{OPP}	55	75	135	ps

7.4 Timing Requirements

over recommended ranges of supply voltage, load and operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
REF_IN REQUIREMENTS					
$f_{REF\ –\ Diff\ IN\text{-}DIV}$	Maximum clock frequency applied to reference divider when (Register 0 Bit 9 = 1)			500	MHz
$f_{REF\ –\ Diff\ REF\_DIV}$	Maximum clock frequency applied to reference divider when (Register 0 Bit 9 = 0)			250	MHz
$f_{REF–\ Single}$	For single-ended Inputs (LVCMOS) on REF_IN			250	MHz
Duty Cycle	Duty cycle of REF_IN	40%		60%	
INTERNAL TIMING REQUIREMENTS					
f_{SMUX}	Maximum clock frequency applied to smart MUX input			250	MHz
f_{INDIV}	Maximum clock frequency applied to input divider			200	MHz
AUXILARY_IN REQUIREMENTS					
$f_{REF\ –\ Crystal}$	AT-Cut crystal input	2		42	MHz
	Drive level	0.1			mW

Timing Requirements (continued)

over recommended ranges of supply voltage, load and operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
	Maximum shunt capacitance			7	pF
$\overline{PD}$ REQUIREMENTS					
t_r / t_f	Rise and fall time of the $\overline{PD}$ signal from 20% to 80% of V_{CC}			4	ns

7.5 SPI Bus Timing Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency for the SPI_CLK			20	MHz
t_1	SPI_LE to SPI_CLK setup time	10			ns
t_2	SPI_MOSI to SPI_CLK setup time	10			ns
t_3	SPI_MOSI to SPI_CLK hold time	10			ns
t_4	SPI_CLK high duration	25			ns
t_5	SPI_CLK low duration	25			ns
t_6	SPI_CLK to SPI_LE hold time	10			ns
t_7	SPI_LE pulse width	20			ns
t_8	SPI_CLK to MISO data valid			10	ns
t_9	SPI_LE to SPI_MISO data valid			10	ns

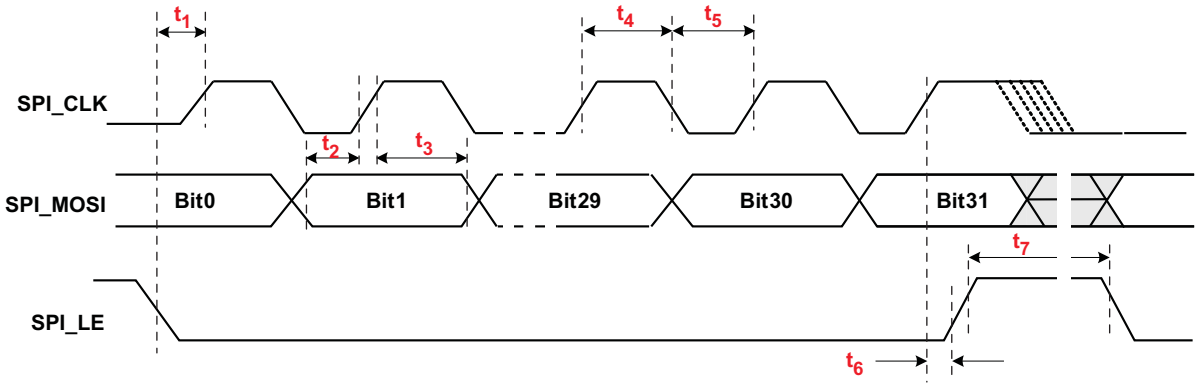


Figure 1. Timing Diagram for SPI Write Command

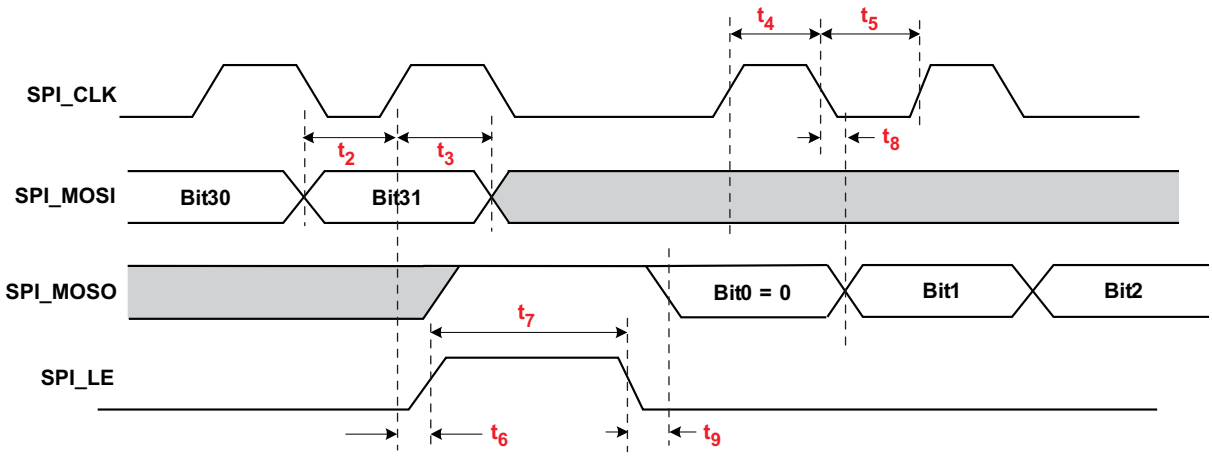


Figure 2. Timing Diagram for SPI Read Command

7.6 Typical Characteristics

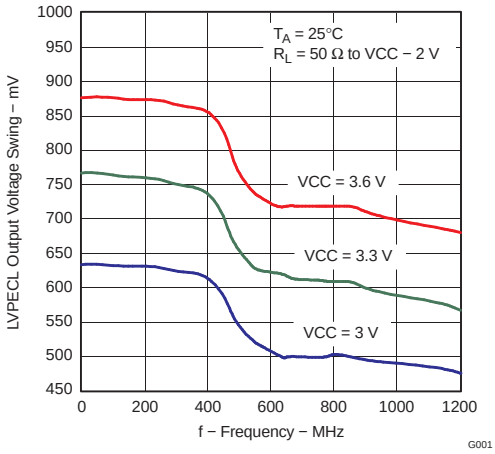


Figure 3. LVPECL Output Voltage Swing vs Frequency

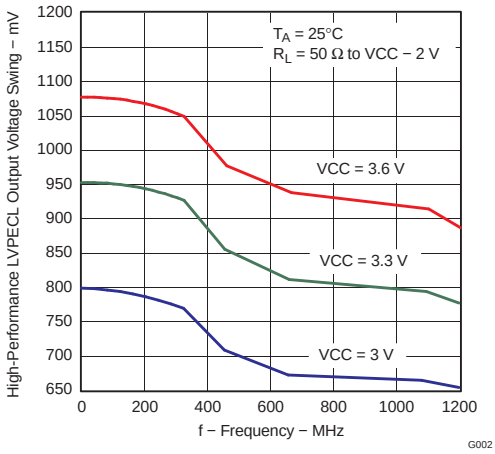


Figure 4. High-Performance LVPECL Output Voltage Swing vs Frequency

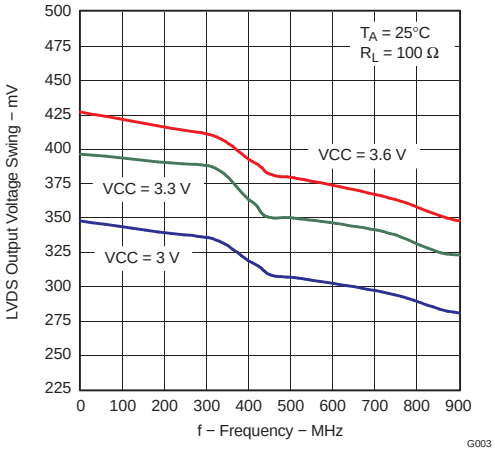


Figure 5. LVDS Output Voltage Swing vs Frequency

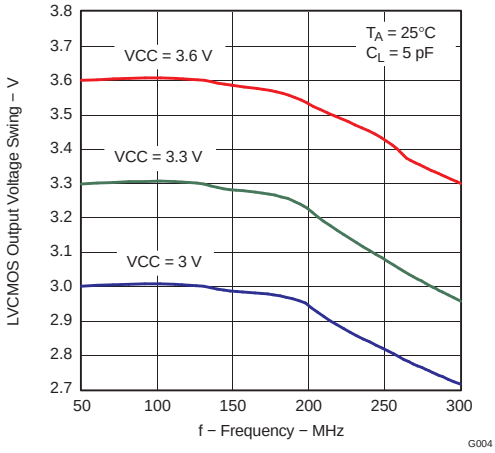


Figure 6. LVCMOS Output Voltage Swing vs Frequency

8 Parameter Measurement Information

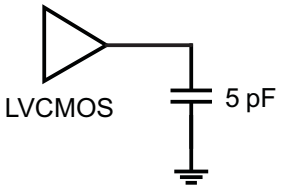


Figure 7. LVCMOS, 5 pF

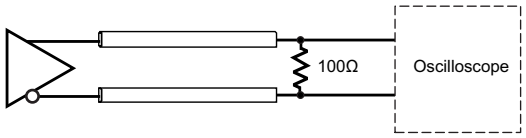


Figure 8. LVDS DC Termination Test

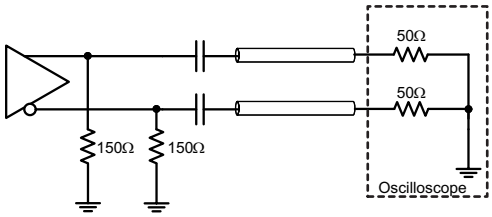


Figure 9. LVPECL AC Termination Test

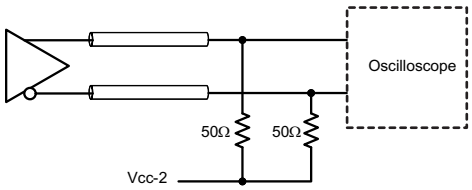


Figure 10. LVPECL DC Termination Test

9 Detailed Description

9.1 Overview

The CDCE62002 comprises of four primary blocks: the interface and control block, the input block, the output block, and the synthesizer block. To determine which settings are appropriate for any specific combination of input and output frequencies, a basic understanding of these blocks is required. The interface and control block determines the state of the CDCE62002 at power up based on the contents of the onboard EEPROM. In addition to the EEPROM, the SPI port is available to configure the CDCE62002 by writing directly to the device registers after power up. The input block selects which of the two input ports is available for use by the synthesizer block. The output block provides two separate clock channels that are fully programmable. The synthesizer block multiplies and filters the input clock selected by the input block.

NOTE

This section of the data sheet provides a high-level description of the features of the CDCE62002 for purpose of understanding its capabilities. For a complete description of device registers and I/O, refer to the *Device Configuration* section.

9.2 Functional Block Diagrams

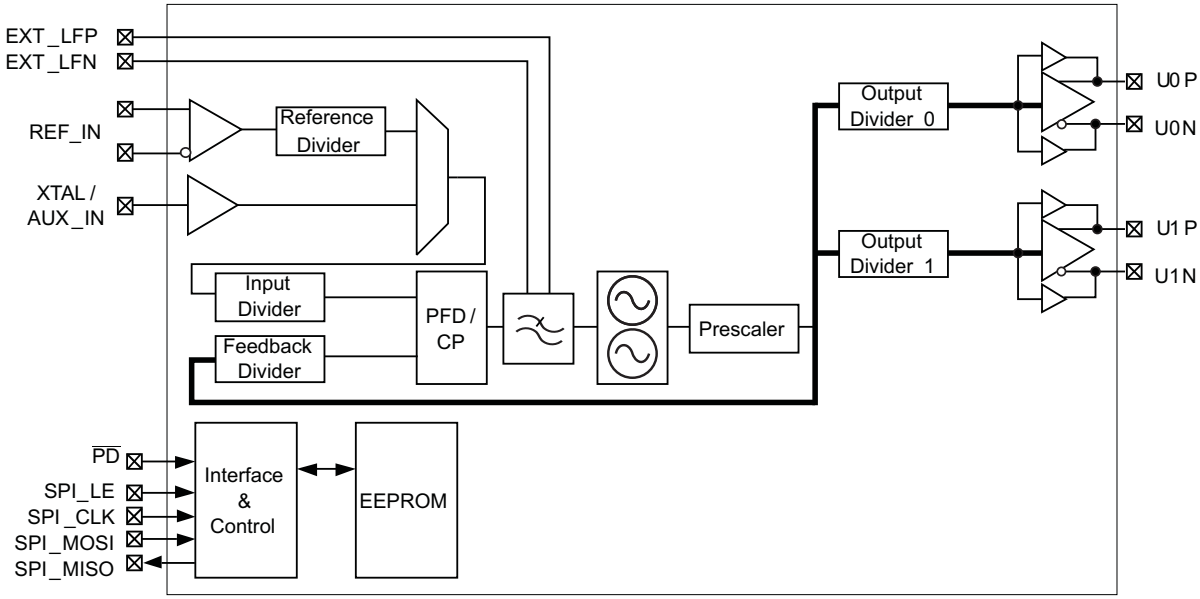


Figure 11. CDCE62002 Block Diagram

Functional Block Diagrams (continued)

9.2.1 Interface and Control Block

The CDCE62002 is a highly flexible and configurable architecture and as such contains a number of registers so that the user may specify device operation. The contents of three 28-bit wide registers implemented in static RAM determine device configuration at all times. On power up, the CDCE62002 copies the contents of the EEPROM into the RAM and the device begins operation based on the default configuration stored in the EEPROM. Systems that do not have a host system to communicate with the CDCE62002 use this method for device configuration.After power up, the host system may overwrite the contents of the RAM through the SPI (Serial Peripheral Interface) port. This enables the configuration and reconfiguration of the CDCE62002 during system operation. Finally, the device offers the ability to copy the contents of the RAM into EEPROM

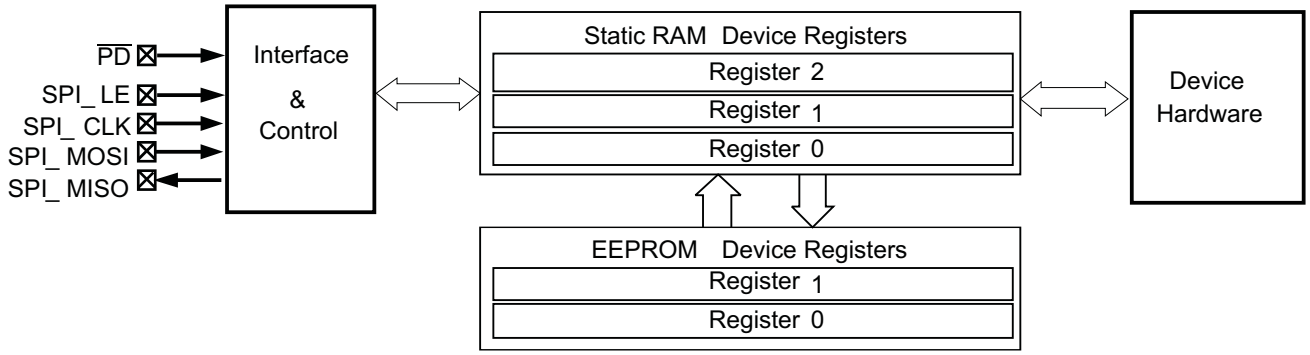


Figure 12. CDCE62002 Interface and Control Block

9.2.2 Input Block

The input block includes one universal input buffer and an auxiliary input. The input block buffers the incoming signals and facilitates signal routing to the Internal synthesizer block through the smart multiplexer (called the smart MUX). The CDCE62002 can divide the REF_IN signal through the dividers present on the inputs of the first stage of the smart MUX.

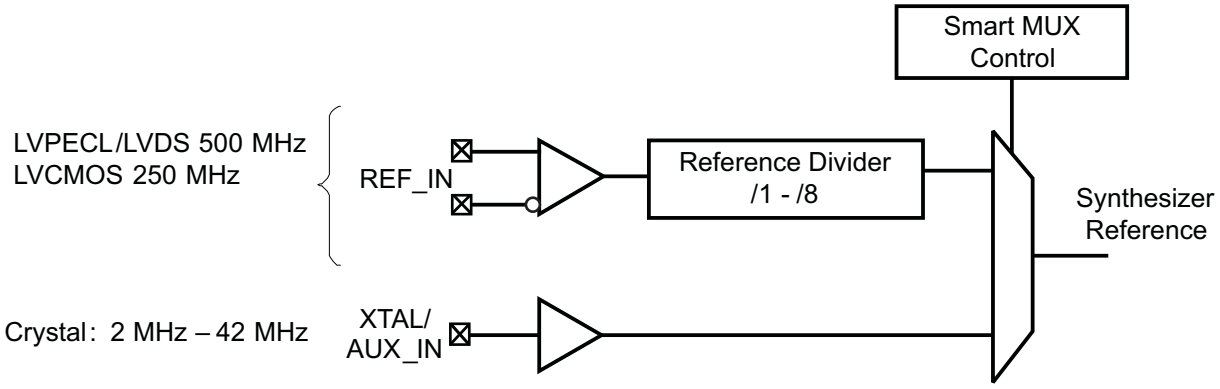


Figure 13. CDCE62002 Input Block

Functional Block Diagrams (continued)

9.2.3 Output Block

Both identical output blocks incorporate a clock divider module (CDM), and a universal output buffer. If an individual clock output channel is not used, then the user should disable the output buffer for the unused channel to save device power. Each channel includes 4-bit in register 0 to control the divide ratio. The output divider supports divide ratios from divide of 1 (bypass the divider) 2, 3, 4, 5, 8, 10, 12, 16, 20, 24, and 32.

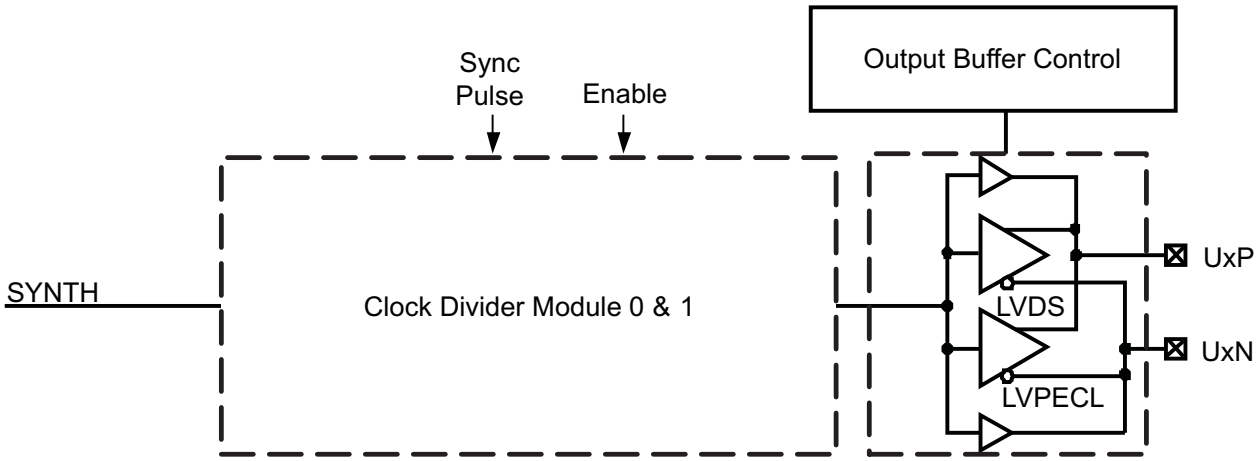


Figure 14. CDCE62002 Output Block

9.2.4 Synthesizer Block

Figure 15 presents a high-level overview of the synthesizer block on the CDCE62002. This block contains the phase-locked loop, internal loop filter, and dual voltage-controlled oscillators. Only one VCO is selected at a time. The loop is closed after a prescaler divider that feeds the output stage the feedback divider.

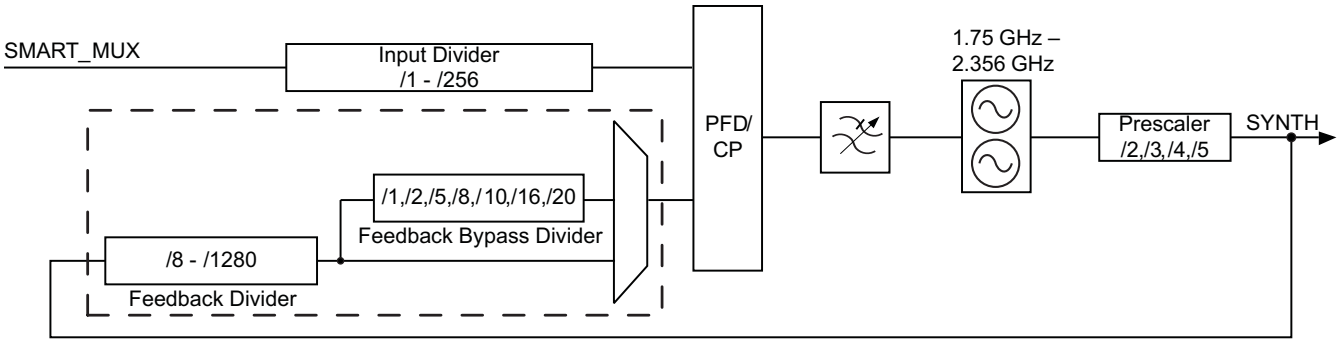


Figure 15. CDCE62002 Synthesizer Block

Functional Block Diagrams (continued)

9.2.5 Computing the Output Frequency

Figure 16 presents the block diagram of the CDCE62002 synthesizer highlighting the clock path for a single output. It also identifies the following regions containing dividers comprising the complete clock path:

- R: Is the Reference divider values.
- O: The output divider value (see *Output Block* for more details)
- I: The input divider value (see *Synthesizer Block* for more details)
- P: The Prescaler divider value (see *Synthesizer Block* of more details)
- F: The cumulative divider value of all dividers falling within the feedback divider (see *Synthesizer Block* for more details)

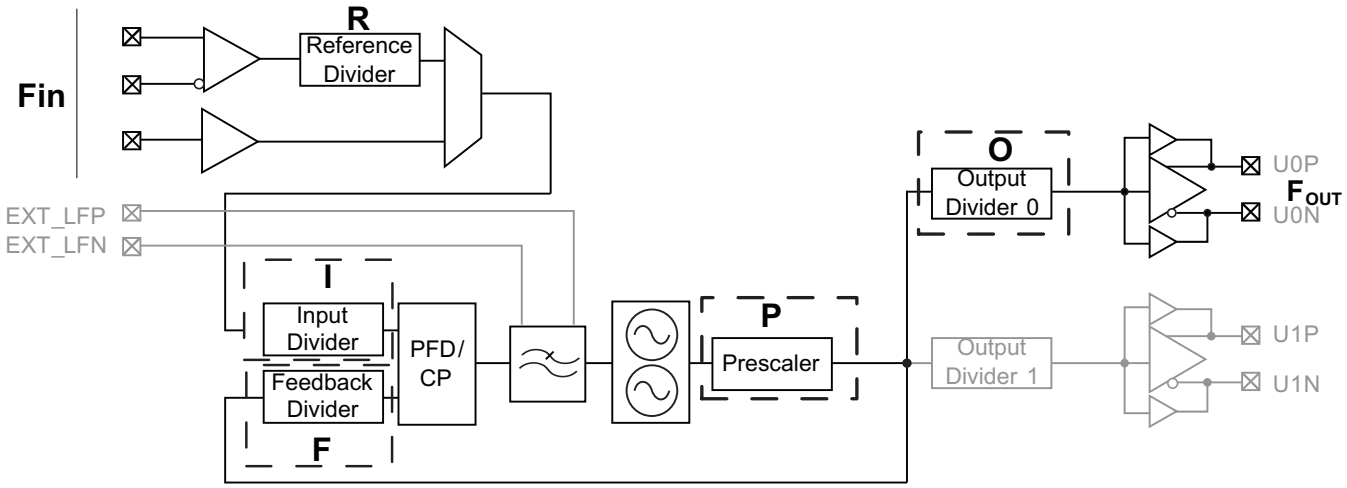


Figure 16. CDCE62002 Clock Path – Synthesizer

With respect to Figure 16, any output frequency generated by the CDCE62002 relates to the input frequency connected to the Synthesizer Block by Equation 1:

$$F_{OUT} = F_{IN} \cdot \frac{F}{R \cdot I \cdot O} \quad (1)$$

Equation 1 holds true subject to the constraints in Equation 2:

$$1.750\text{GHz} < O \cdot P \cdot F_{OUT} < 2.356\text{GHz} \quad (2)$$

And the comparison frequency F_{COMP},

$$40.0\ \text{kHz} \le F_{COMP} \le 40\ \text{MHz}$$

Where:

$$F_{COMP} = \frac{F_{IN}}{R \cdot I} \quad (3)$$

When AUX_IN is selected as the input, R can be set to 1 in Equation 1 and Equation 3.

9.3 Feature Description

9.3.1 Phase Noise Analysis

Table 1. Phase Noise for 30.72-MHz External Reference

Phase Noise Specifications under following configuration: VCO = 1966.08 MHz, REF_IN = 30.72 MHz, PFD Frequency = 30.72 MHz, Charge Pump Current = 1.5-mA Loop BW = 400 kHz at 3.3 V and 25°C.						
PHASE NOISE AT	**REFERENCE 30.72 MHz**	**LVPECL-HP 491.52 MHz**	**LVPECL 491.52 MHz**	**LVDS 491.52 MHz**	**LVCMOS 122.88 MHz**	**UNIT**
10Hz	–108	–84	–84	–85	–97	dBc/Hz
100Hz	–130	–98	–98	–97	–111	dBc/Hz
1kHz	–134	–106	–106	–106	–118	dBc/Hz
10kHz	–152	–118	–118	–118	–130	dBc/Hz
100kHz	–156	–121	–121	–121	–133	dBc/Hz
1MHz	–157	–131	–131	–130	–142	dBc/Hz
10MHz	—	–146	–146	–145	–151	dBc/Hz
20MHz	—	–146	–146	–145	–151	dBc/Hz
Jitter(RMS) 10k~20MHz	195 (10k~1MHz)	319	316	332.2	372.1	fs

Table 2. Phase Noise for 25-MHz Crystal Reference

Phase Noise Specifications under following configuration: VCO = 2000.00 MHz, AUX_IN-REF = 25.00 MHz, PFD Frequency = 25.00 MHz, Charge Pump Current = 1.5-mA Loop BW = 400 kHz 3.3V and 25°C.				
PHASE NOISE AT	**LVPECL-HP 500.00 MHz**	**LVDS 250.00 MHz**	**LVCMOS 125.00 MHz**	**UNIT**
10Hz	–72	–72	–79	dBc/Hz
100Hz	–97	–97	–103	dBc/Hz
1kHz	–111	–111	–118	dBc/Hz
10kHz	–120	–120	–126	dBc/Hz
100kHz	–124	–124	–130	dBc/Hz
1MHz	–136	–136	–142	dBc/Hz
10MHz	–147	–147	–151	dBc/Hz
20MHz	–148	–148	–151	dBc/Hz
Jitter(RMS) 10k~20MHz	426	426	443	fs

9.3.2 Output-to-Output Isolation

Table 3. Output-to-Output Isolation

			WORST SPUR	**UNIT**
The Output to Output Isolation was tested at 3.3-V supply and 25°C ambient temperature (Default Configuration):				
Output 1	Measured Channel	**In LVDS Signaling at 125 MHz**	–70	dB
Output 0	*Aggressor Channel*	*LVPECL 156.25 MHz*		

9.3.3 Device Control

Figure 17 provides a conceptual explanation of the CDCE62002 Device operation. Table 4 defines how the device behaves in each of the operational states.

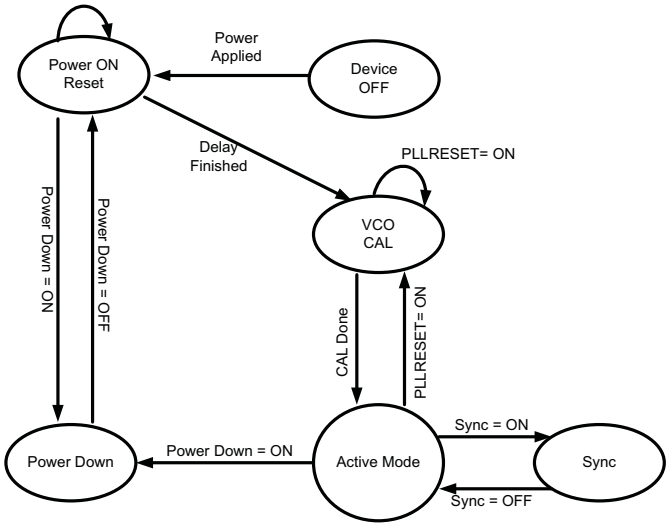


Figure 17. CDCE62002 Device State Control Diagram

Table 4. CDCE62002 Device State Definitions

STATE	DEVICE BEHAVIOR	ENTERED VIA	EXITED VIA	SPI PORT STATUS	PLL STATUS	OUTPUT DIVIDER STATUS	OUTPUT BUFFER STATUS
Power-On Reset	After device power supply reaches approximately 2.35 V, the contents of EEPROM are copied into the Device Registers, thereby initializing the device hardware.	Power applied to the device or upon exit from Power-Down State through the $\overline{PD}$ pin set HIGH.	Power-On-Reset and EEPROM loading delays are finished OR the $\overline{PD}$ pin is set LOW.	OFF	Disabled	Disabled	OFF
VCO CAL	The voltage-controlled oscillator is calibrated based on the PLL settings and the incoming reference clock. After the VCO has been calibrated, the device enters Active Mode automatically.	Delay process in the Power-On Reset State is finished or PLLRESET=ON	Calibration Process in completed	ON	Enabled	Disabled	OFF
Active Mode	Normal Operation	CAL Done (VCO calibration process finished) or Sync = OFF (from Sync State).	Power Down or PLLRESET=ON	ON	Enabled	Disabled or Enabled	Disabled or Enabled
Power Down	Used to shut down all hardware and Resets the device after exiting the Power-Down State. Therefore, the EEPROM contents will eventually be copied into RAM after the Power-Down State is exited.	$\overline{PD}$ pin is pulled LOW.	$\overline{PD}$ pin is pulled HIGH.	ON	Disabled	Disabled	Disabled
Sync	Sync synchronizes both outputs dividers so that they begin counting at the same time	$\overline{Sync}$ Bit in device register 2 bit 8 is set LOW	$\overline{Sync}$ bit in device register 2 bit 8 is set HIGH	ON	Enabled	Disabled	Disabled

9.3.4 External Control Pins

Power Down ($\overline{PD}$)

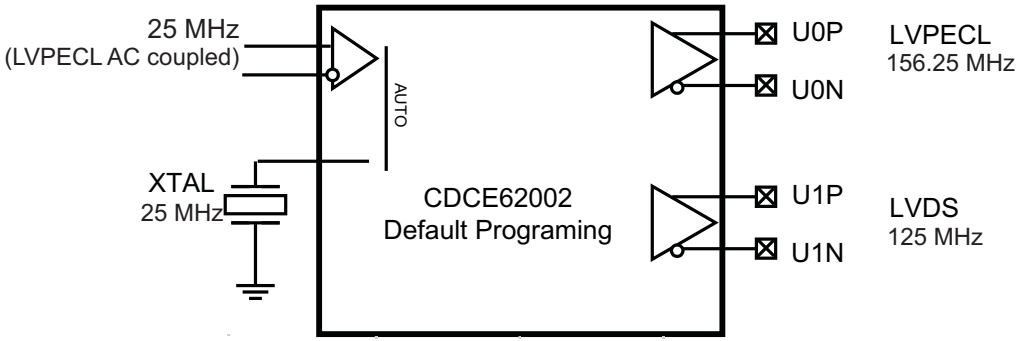
When pulled LOW, $\overline{PD}$ activates the power-down state which shuts down all hardware and resets the device. Restoring $\overline{PD}$ high will cause the CDCE62002 to exit the power-down state. This causes the device to behave as if it has been powered up including copying the EEPROM contents into RAM. $\overline{PD}$ pin also has a shadowed $\overline{PD}$ bit residing in Register 2 Bit 7. When asserted Low it puts the device in power-down mode, but it does not load the EEPROM when the bits is disserted.

NOTE

The SPI_LE signal has to be high in order for the EEPROM to load correctly into RAM on the Rising edge of PD Pin.

9.3.4.1 Factory Default Programming

The CDCE62002 is factory pre-programmed to work with 25-MHz input from the reference input or from the auxiliary input with auto switching enabled. An internal PFD of 6.25 MHz and about 400-KHz loop bandwidth. Output 0 is pre-programmed as an LVPECL driver to output 156.25 MHz and output 1 is pre-programmed as LVDS driver to output 125 MHz.



EEPROM	Register Content
Register 0	72A000E0
Register 1	8389A061

Figure 18. CDCE62002 Default Factory Programming

9.3.5 Input Block

The input block includes one universal input buffers, an auxiliary input, and a smart multiplexer.

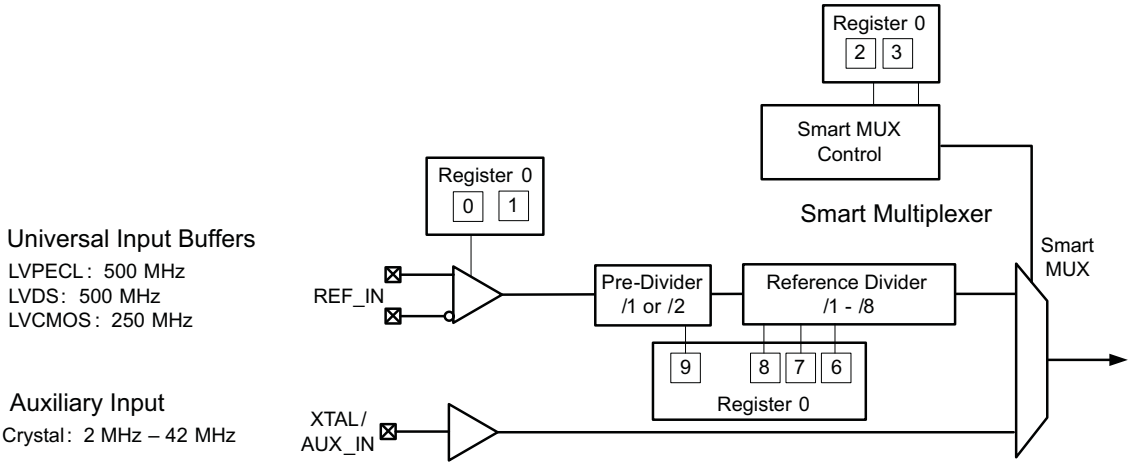


Figure 19. CDCE62002 Input Block With References to Registers

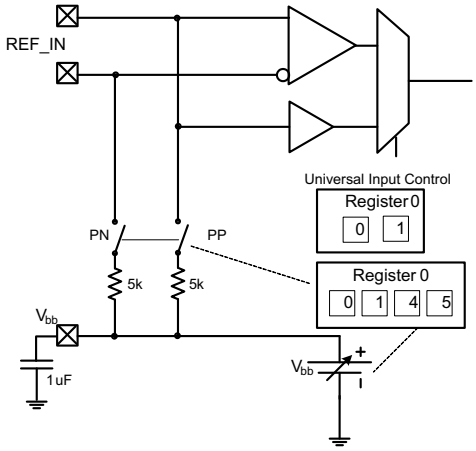
The CDCE62002 provides a reference divider that divides the clock exiting reference (REF_IN) input buffer.

Table 5. CDCE62002 Reference Divider Settings

BIT NAME →	REFERENCE DIVIDER				TOTAL DIVIDE RATIO
	REFDIVIDE3	REFDIVIDE2	REFDIVIDE1	REFDIVIDE0	
REGISTER BIT →	0.9	0.8	0.7	0.6	
	0	0	0	0	/1
	0	0	0	1	/2
	0	0	1	0	/3
	0	0	1	1	/4
	0	1	0	0	/5
	0	1	0	1	/6
	0	1	1	0	/7
	0	1	1	1	/8
	1	0	0	0	/2
	1	0	0	1	/4
	1	0	1	0	/6
	1	0	1	1	/8
	1	1	0	0	/10
	1	1	0	1	/12
	1	1	1	0	/14
	1	1	1	1	/16

9.3.5.1 Reference Input Buffer

Figure 20 shows the key elements of a universal input buffer (UIB). A UIB supports multiple formats along with different termination and coupling schemes. The CDCE62002 implements the UIB by including onboard switched termination, a programmable bias voltage generator, and a multiplexer. The CDCE62002 provides a high degree of configurability on the UIB to facilitate most existing clock input formats. REF_IN only provides biasing internally. TI recommends terminating it externally if needed.

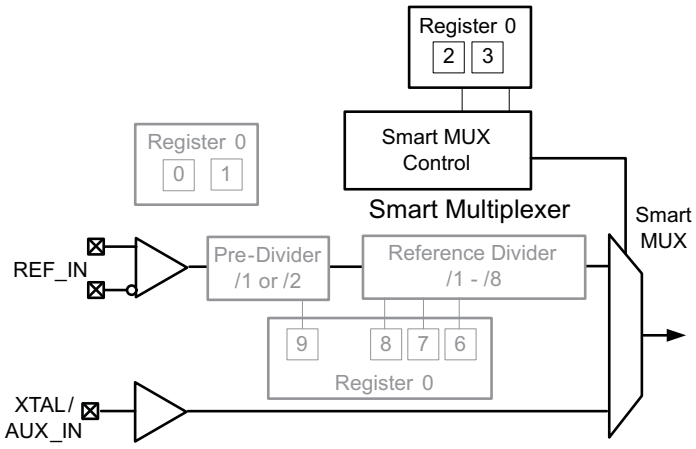


TERMSEL	INBUFSELY	INBUFSELX	ACDCSEL	P	N	VBB	Input buffer Mode
0	1	0	0	ON	ON	1.9V	LVPECL – AC coupled
			1			1.2V	note (1)
	0	1	0			1.2V	LVDS – AC coupled
			1			1.2V	LVDS – DC coupled
	1	1	X	OFF	OFF	---	LVCMOS
1	X	X	X			---	Input Buffer Termination Disabled

note (1): This setting is not recommended.

Figure 20. CDCE62002 Universal Input Buffer

9.3.5.2 Smart Multiplexer Dividers



Setting		Smart Mux Mode
REFSEL	AUXSEL	
0.2	0.3	
0	0	Reserved
1	0	REF Select
0	1	AUX Select
1	1	Auto Select

Figure 21. CDCE62002 Smart Multiplexer

In auto select mode the smart Mux switches automatically between reference input and auxiliary input with a preference to the reference input. In order for the smart MUX to function correctly the frequency after the reference divider and the auxiliary input signal frequency should be within 20% of each other or one of them should be zero or ground. In REF select mode, TI recommends connecting AUX_IN to GND with a 1-k pulldown resistor. In AUX Select mode, TI recommends pulling the REF_INp high and REF_INn low with a 1-k resistor each.

9.3.5.3 Auxiliary Input Port

The auxiliary input on the CDCE62002 is designed to connect to an AT-Cut Crystal with a total load capacitance of 8 pF to 10 pF. One side of the crystal connects to ground while the other side connects to the auxiliary input of the device. The circuit accepts crystals from 2 to 42 MHz. See the Crystal Input Interface section for crystal load selection.

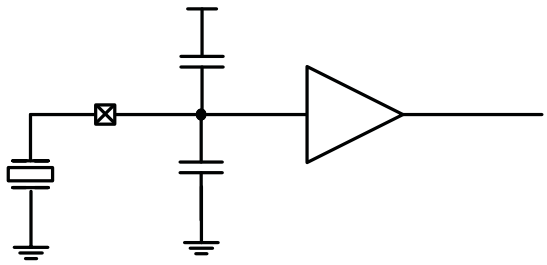


Figure 22. CDCE62002 Auxiliary Input Port

9.3.5.4 Output Block

The output block includes two identical output channels. Each output channel comprises of a clock divider module, and a universal output buffer as shown in Figure 23.

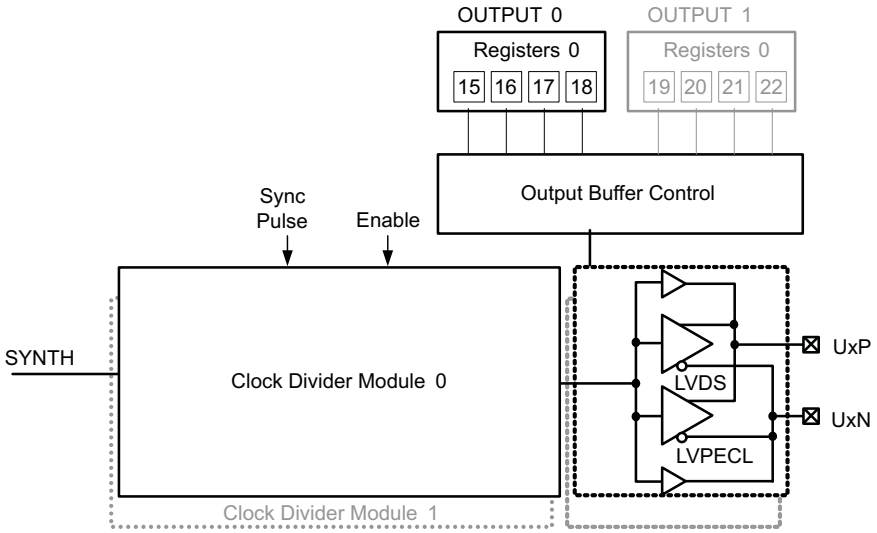


Figure 23. CDCE62002 Output Channel

Table 6. CDCE62002 Output Divider Settings

	OUTPUT DIVIDERS SETTING				DIVIDE RATIO
DIVIDER 0 →	0.18	0.17	0.16	0.15	
DIVIDER 1 →	0.22	0.21	0.20	0.19	
	0	0	0	0	Disabled
	0	0	0	1	/1
	0	0	1	0	/2
	0	0	1	1	/3
	0	1	0	0	/4
	0	1	0	1	/5
	0	1	1	0	/6
	0	1	1	1	Disabled
	1	0	0	0	/8
	1	0	0	1	Disabled
	1	0	1	0	/10
	1	0	1	1	/20
	1	1	0	0	/12
	1	1	0	1	/24
	1	1	1	0	/16
	1	1	1	1	/32

9.3.5.5 Synthesizer Block

Figure 24 provides an overview of the CDCE62002 synthesizer block. The synthesizer block provides a phase-locked loop, a partially integrated programmable loop filter, and two voltage-controlled oscillators (VCO). The synthesizer block generates an output clock called *SYNTH* and drives it onto the Internal clock distribution bus.

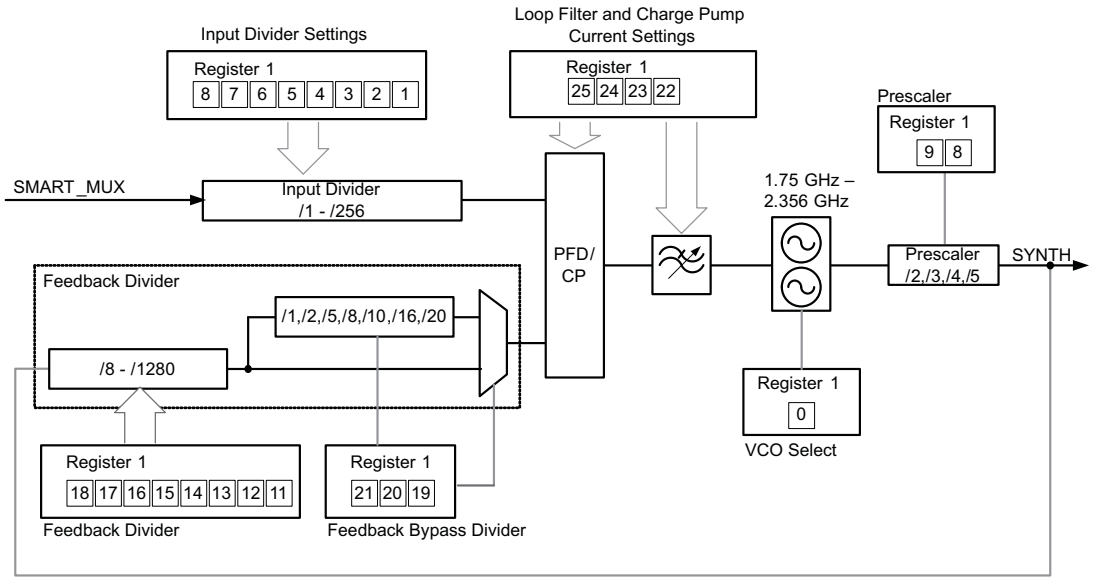


Figure 24. CDCE62002 Synthesizer Block

9.3.5.6 Input Divider

The input divider divides the clock signal selected by the smart multiplexer and presents the divided signal to the phase frequency detector / charge pump of the frequency synthesizer.

Table 7. CDCE62002 Input Divider Settings

INPUT DIVIDER SETTINGS								DIVIDE RATIO
SELINDIV7	SELINDIV6	SELINDIV5	SELINDIV4	SELINDIV3	SELINDIV2	SELINDIV1	SELINDIV0	
1.8	1.7	1.6	1.5	1.4	1.3	1.2	1.1	
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
0	0	0	0	0	0	1	1	4
0	0	0	0	0	1	0	0	5
0	0	0	0	0	1	0	1	6
–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–
1	1	1	1	1	1	1	1	256

9.3.5.7 Feedback and Feedback Bypass Divider

Table 8 shows how to configure the feedback divider for various divide values:

Table 8. CDCE62002 Feedback Divider Settings

FEEDBACK DIVIDER								DIVIDE RATIO
SELFBDIV7	SELFBDIV6	SELFBDIV5	SELFBDIV4	SELFBDIV3	SELFBDIV2	SELFBDIV1	SELFBDIV0	
1.18	1.17	1.16	1.15	1.14	1.13	1.12	1.11	
0	0	0	0	0	0	0	0	8
0	0	0	0	0	0	0	1	12
0	0	0	0	0	0	1	0	16
0	0	0	0	0	0	1	1	20
0	0	0	0	0	1	0	1	24
0	0	0	0	0	1	1	0	32
0	0	0	0	1	0	0	1	36
0	0	0	0	0	1	1	1	40
0	0	0	0	1	0	1	0	48
0	0	0	1	1	0	0	0	56
0	0	0	0	1	0	1	1	60
0	0	0	0	1	1	1	0	64
0	0	0	1	0	1	0	1	72
0	0	0	0	1	1	1	1	80
0	0	0	1	1	0	0	1	84
0	0	0	1	0	1	1	0	96
0	0	0	1	0	0	1	1	100
0	1	0	0	1	0	0	1	108
0	0	0	1	1	0	1	0	112
0	0	0	1	0	1	1	1	120
0	0	0	1	1	1	1	0	128
0	0	0	1	1	0	1	1	140
0	0	1	1	0	1	0	1	144
0	0	0	1	1	1	1	1	160
0	0	1	1	1	0	0	1	168
0	1	0	0	1	0	1	1	180
0	0	1	1	0	1	1	0	192
0	0	1	1	0	0	1	1	200
0	1	0	1	0	1	0	1	216
0	0	1	1	1	0	1	0	224
0	0	1	1	0	1	1	1	240
0	1	0	1	1	0	0	1	252
0	0	1	1	1	1	1	0	256
0	0	1	1	1	0	1	1	280
0	1	0	1	0	1	1	0	288
0	1	0	1	0	0	1	1	300
0	0	1	1	1	1	1	1	320
0	1	0	1	1	0	1	0	336
0	1	0	1	0	1	1	1	360
0	1	0	1	1	1	1	0	384
1	1	0	1	1	0	0	0	392
0	1	1	1	0	0	1	1	400

Table 8. CDCE62002 Feedback Divider Settings (continued)

FEEDBACK DIVIDER								DIVIDE RATIO
SELFBDIV7	SELFBDIV6	SELFBDIV5	SELFBDIV4	SELFBDIV3	SELFBDIV2	SELFBDIV1	SELFBDIV0	
1.18	1.17	1.16	1.15	1.14	1.13	1.12	1.11	
0	1	0	1	1	0	1	1	420
1	0	1	1	0	1	0	1	432
0	1	1	1	1	0	1	0	448
0	1	0	1	1	1	1	1	480
1	0	0	1	0	0	1	1	500
1	0	1	1	1	0	0	1	504
0	1	1	1	1	1	1	0	512
0	1	1	1	1	0	1	1	560
1	0	1	1	0	1	1	0	576
1	1	0	1	1	0	0	1	588
1	0	0	1	0	1	1	1	600
0	1	1	1	1	1	1	1	640
1	0	1	1	1	0	1	0	672
1	0	0	1	1	0	1	1	700
1	0	1	1	0	1	1	1	720
1	0	1	1	1	1	1	0	768
1	1	0	1	1	0	1	0	784
1	0	0	1	1	1	1	1	800
1	0	1	1	1	0	1	1	840
1	1	0	1	1	1	1	0	896
1	0	1	1	1	1	1	1	960
1	1	0	1	1	0	1	1	980
1	1	1	1	1	1	1	0	1024
1	1	0	1	1	1	1	1	1120
1	1	1	1	1	1	1	1	1280

Table 9 shows how to configure the Feedback Bypass Divider.

Table 9. CDCE62002 Feedback Bypass Divider Settings

FEEDBACK BYPASS DIVIDER			DIVIDE RATIO
SELBPDIV2	SELBPDIV1	SELBPDIV0	
1.21	1.20	1.19	
0	0	0	2
0	0	1	5
0	1	0	8
0	1	1	10
1	0	0	16
1	0	1	20
1	1	0	RESERVED
1	1	1	1(bypass)

9.3.5.7.1 VCO Select

Table 10 illustrates how to control the dual voltage controlled oscillators.

Table 10. CDCE62002 VCO Select

BIT NAME →	VCO SELECT SELVCO	VCO CHARACTERISTICS		
REGISTER NAME →	1.0	VCO RANGE	Fmin (MHz)	Fmax (MHz)
	0	Low	1750	2046
	1	High	2040	2356

9.3.5.7.2 Prescaler

Table 11 shows how to configure the prescaler.

Table 11. CDCE62002 Prescaler Settings

SETTINGS		DIVIDE RATIO
SELPRESCB	SELPRESCA	
1.10	1.9	
0	0	5
1	0	4
0	1	3
1	1	2

9.3.5.7.3 Loop Filter

Figure 25 depicts the loop filter topology of the CDCE62002. It facilitates both internal and external implementations providing optimal flexibility.

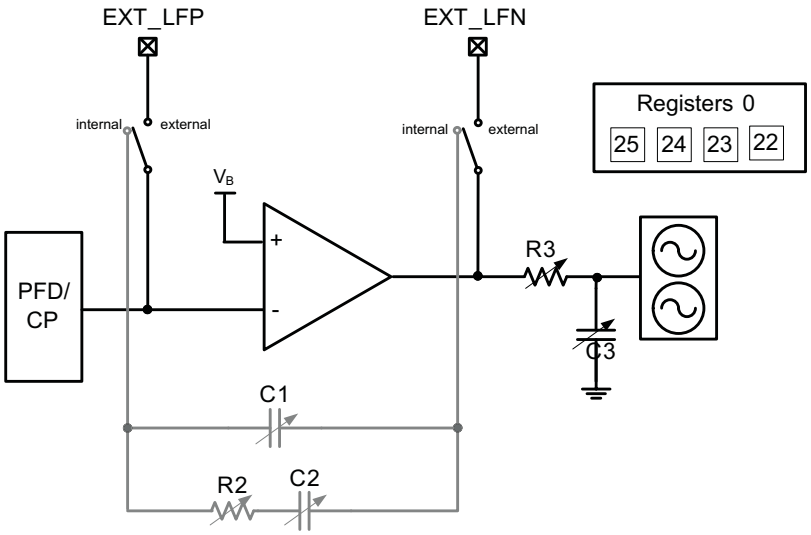


Figure 25. CDCE62002 Loop Filter Topology

9.3.5.8 Internal Loop Filter Component Configuration

Figure 25 illustrates the switching between four fixed internal loop filter settings and the external loop filter setting. Table 12 shows that the CDCE62002 has 16 settings different settings for the loop filter. Four of the settings are internal and twelve are external.

Table 12. CDCE62002 Loop Filter Settings

LFRCSEL										Charge Pump
3	2	1	0	Loop Filter	C1	C2	R2	R3	C3	Current
0	0	0	0	Internal	1.5 pF	473.5 pF	4.0k	5k	2.5 pF	1.5 mA
0	0	0	1	Internal	1.5 pF	473.5 pF	4.0k	5k	2.5 pF	400 µA
0	0	1	0	Internal	1.5 pF	473.5 pF	2.7k	5k	2.5 pF	250 µA
0	0	1	1	Internal	1.5 pF	473.5 pF	2.7k	5k	2.5 pF	150 µA
0	1	0	0	External	X	X	X	20k	112 pF	1.0 mA
0	1	0	1	External	X	X	X	20k	112 pF	2.0 mA
0	1	1	0	External	X	X	X	20k	112 pF	3.0 mA
0	1	1	1	External	X	X	X	20k	112 pF	3.75 mA
1	0	0	0	External	X	X	X	10k	100 pF	1.0 mA
1	0	0	1	External	X	X	X	10k	100 pF	2.0 mA
1	0	1	0	External	X	X	X	10k	100 pF	3.0 mA
1	0	1	1	External	X	X	X	10k	100 pF	3.75 mA
1	1	0	0	External	X	X	X	5k	100 pF	1.0 mA
1	1	0	1	External	X	X	X	5k	64 pF	2.0 mA
1	1	1	0	External	X	X	X	5k	48 pF	3.0 mA
1	1	1	1	External	X	X	X	5k	38 pF	3.75 mA

9.3.6 Lock Detect

The CDCE62002 provides a lock detect indicator circuit that can be detected on an external Pin PLL_LOCK (Pin 32) and internally by reading PLLLOCKPIN bit (6) in Register 2.

Two signals whose phase difference is less than a prescribed amount are *locked* otherwise they are *unlocked*. The phase frequency detector / charge pump compares the clock provided by the input divider and the feedback divider; using the input divider as the phase reference. The lock detect circuit implements a programmable lock detect window. Table 13 shows an overview of how to configure the lock detect feature. The PLL_LOCK pin will possibly jitter several times between lock and out of lock until the PLL achieves a stable lock. If desired, choosing a wide loop bandwidth and a high number of successive clock cycles virtually eliminates this characteristic. PLL_LOCK will return to out of lock, if just one cycle is outside the lock detect window or if a cycle slip occurs.

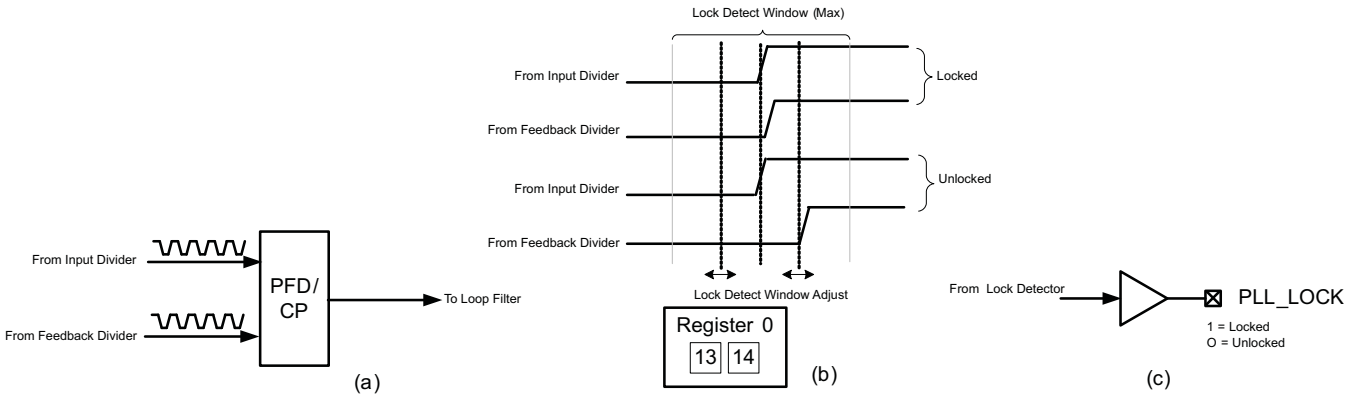


Figure 26. CDCE62002 Lock Detect

Table 13. CDCE62002 Lock Detect Control

	LOCK DETECT		LOCK DETECT WINDOW
BIT NAME →	**LOCKW(1)**	**LOCKW(0)**	
REGISTER NAME →	**0.13**	**0.14**	
	0	0	2.1 ns
	0	1	4.6 ns
	1	0	7.2 ns
	1	1	19.9 ns

9.3.7 Crystal Input Interface

In fundamental mode, TI recommends the oscillation mode of operation for the input crystal and parallel resonance is the recommended type of circuit for the crystal.

A crystal load capacitance refers to all capacitances in the oscillator feedback loop. It is equal to the amount of capacitance seen between the terminals of the crystal in the circuit. For parallel resonant mode circuits, the correct load capacitance is necessary to ensure the oscillation of the crystal within the expected parameters.

The CDCE62002 implements an input crystal oscillator circuitry, known as the Colpitts oscillator, and requires one pad of the crystal to interface with the AUX_IN pin; the other pad of the crystal is tied to ground. In this crystal interface, it is important to account for all sources of capacitance when calculating the correct value for the discrete capacitor component, CL, for a design.

The CDCE62002 has been characterized with 10-pF parallel resonant crystals. The input crystal oscillator stage in the CDCE62002 is designed to oscillate at the correct frequency for all parallel resonant crystals with low-pull capability and rated with a load capacitance that is equal to the sum of the on-chip load capacitance at the AUX_IN pin (10-pF), crystal stray capacitance, and board parasitic capacitance between the crystal and AUX_IN pin.

The normalized frequency error of the crystal, as a result of load capacitance mismatch, can be calculated as Equation 4:

$$\frac{\Delta f}{f} = \frac{C_S}{2\left(C_{L,R} + C_O\right)} - \frac{C_S}{2\left(C_{L,A} + C_O\right)}$$

where

- C_S is the motional capacitance of the crystal
- C_0 is the shunt capacitance of the crystal
- $C_{L,R}$ is the rated load capacitance for the crystal
- $C_{L,A}$ is the actual load capacitance in the implemented PCB for the crystal
- Δf is the frequency error of the crystal
- f is the rated frequency of the crystal (4)

The first three parameters can be obtained from the crystal vendor.

To minimize the frequency error of the crystal to meet application requirements, the difference between the rated load capacitance and the actual load capacitance must be minimized and a crystal with low-pull capability (low CS) must be used.

For example, if an application requires less than ±50-ppm frequency error and a crystal with less than ±50-ppm frequency tolerance is picked, the characteristics are as follows: C_0 = 7 pF, C_S = 10 pF, and $C_{L,R}$ = 12 pF. To meet the required frequency error, calculate $C_{L,A}$ using Equation 4 to be 17 pF. Subtracting $C_{L,R}$ from $C_{L,A}$, results in 5 pF; take care during printed-circuit board (PCB) layout with the crystal and the CDCE62002 to ensure that the sum of the crystal stray capacitance and board parasitic capacitance is less than the calculated 5 pF.

Good layout practices are fundamental to the correct operation and reliability of the oscillator. It is critical to place the crystal components very close to the XIN pin to minimize routing distances. Long traces in the oscillator circuit are a very common source of problems. Do not route other signals across the oscillator circuit. Also, make sure power and high-frequency traces are routed as far away as possible to avoid crosstalk and noise coupling. Avoid the use of vias; if the routing becomes very complex, it is better to use 0-Ω resistors as bridges to go over other signals. Vias in the oscillator circuit must only be used for connections to the ground plane. Do not share ground connections; instead, make a separate connection to ground for each component that requires grounding. If possible, place multiple vias in parallel for each connection to the ground plane. Especially in the Colpitts oscillator configuration, the oscillator is very sensitive to capacitance in parallel with the crystal. Therefore, the layout must be designed to minimize stray capacitance across the crystal to less than 5 pF total under all circumstances to ensure proper crystal oscillation. Be sure to take into account both PCB and crystal stray capacitance.

9.3.8 VCO Calibration

The CDCE62002 includes two on-chip LC oscillator-based VCOs with low phase noise covering a frequency range of 1.75 GHz to 2.356 GHz. The VCO must be calibrated to ensure proper operation over the valid device operating conditions. VCO calibration is controlled by the reference clock input. This calibration requires that the PLL be set up properly to lock the PLL loop and that the reference clock input be present.

The device enters self-calibration of the VCO automatically at power up, after the registers have been loaded from the EEPROM and an input clock signal is detected. If there is no input clock available during power up, the VCO will wait for reference clock before starting calibration.

If the input signal is not valid during self-calibration, it is necessary to re-initiate VCO calibration after the input clock signal stabilizes.

NOTE

Re-calibration is also necessary anytime a PLL setting is changed (e.g. divider ratios in the PLL or loop filter settings are adjusted).

VCO calibration can be initiated by writing to register 2 bits 7, 13 and 20.

Table 14. VCO Calibration Method Through Register Programming

CALSELECT Reg 2.13	PLLRESET 2.20	PD 2.7	VCO CALIBRATION MECHANISM(1)
1	1-0-1	1	VCO calibration starts at PLLRESET toggling low-to-high. The outputs turn off for the duration of the calibration, which is a few ns.
0	X	1-0-1	Device is powered down when $\overline{PD}$ is toggle 1-to-0. All outputs are disabled while $\overline{PD}$ is zero. After asserting $\overline{PD}$ from zero to one the VCO becomes calibrated and immediately afterwards the device outputs turn on.

(1) A VCO calibration is also initiated if the external PD pin is toggle high-low-high. In this case all EEPROM registers become reloaded into the device and the CALSELECT bit is reset to 0.

9.3.9 Start-Up Time Estimation

The CDCE62002 startup time can be estimated based on the parameters defined in Table 15 and graphically shown in Figure 27.

Table 15. Start-up Time Dependencies

PARAMETER		DESCRIPTION	METHOD OF DETERMINATION
t_{pul}	Power-up time (low limit)	Power-supply rise time to low limit of power-on-reset (POR) trip point	Time required for power supply to ramp to 2.27 V
t_{puh}	Power-up time (high limit)	Power-supply rise time to high limit of power-on-reset (POR) trip point	Time required for power supply to ramp to 2.64 V
t_{rsu}	Reference start-up time	After POR releases, the Colpitts oscillator is enabled. This start-up time is required for the oscillator to generate the requisite signal levels for the delay block to be clocked by the reference input	500 µs best-case and 800 µs worst-case (This is only for crystal connected to AUX_IN)
t_{delay}	Delay time	Internal delay time generated from the clock. This delay provides time for the oscillator to stabilize.	t_{delay} = 16384 x t_{id} t_{id} = period of input clock to the input divider
t_{VCO_CAL}	VCO calibration time	VCO calibration time generated from the PFD clock. This process selects the operating point for the VCO based on the PLL settings.	t_{VCO_CAL} = 550 x t_{PFD} t_{PFD} = period of the PFD clock
t_{PLL_LOCK}	PLL lock time	Time required for PLL to lock within ±10 ppm of reference frequency	t_{PLL_LOCK} = 3/LBW LBW = PLL Loop Bandwidth

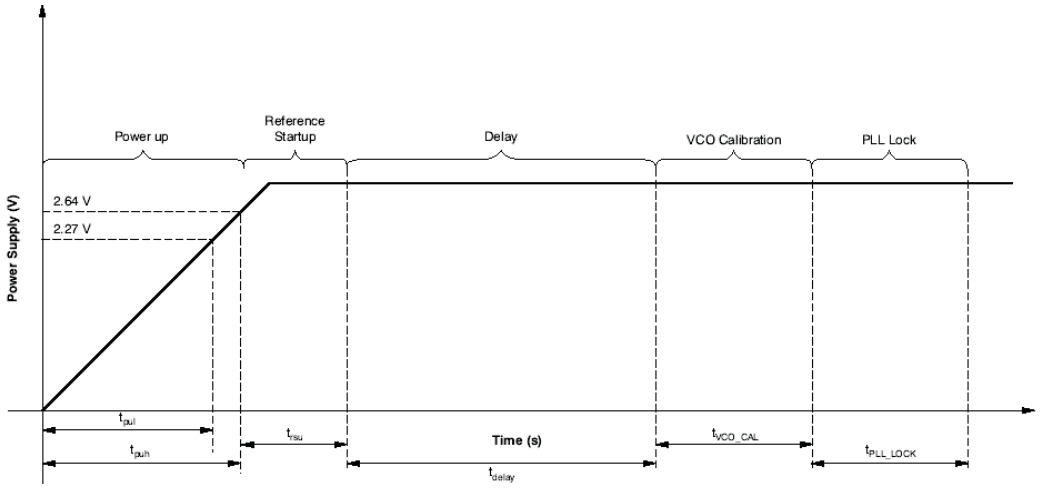


Figure 27. Start-Up Time dependencies

9.4 Device Functional Modes

9.4.1 Clock Generator

The CDCE62002 can generate 1 to 4 low noise clocks from a single crystal or crystal oscillator as follows:

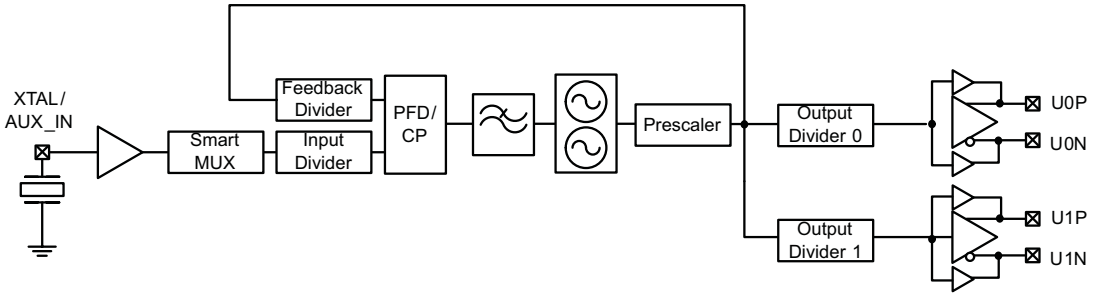


Figure 28. CDCE62002 as a Clock Generator

9.4.2 SERDES Start-Up and Clock Cleaner

The CDCE62002 can serve as a SERDES device companion by providing a crystal based reference for the SERDES device to lock to receive data stream and when the SERDES locks to the data and outputs the recovered clock the CDCE62002 can switch and use the recovered clock and serve as a jitter cleaner.

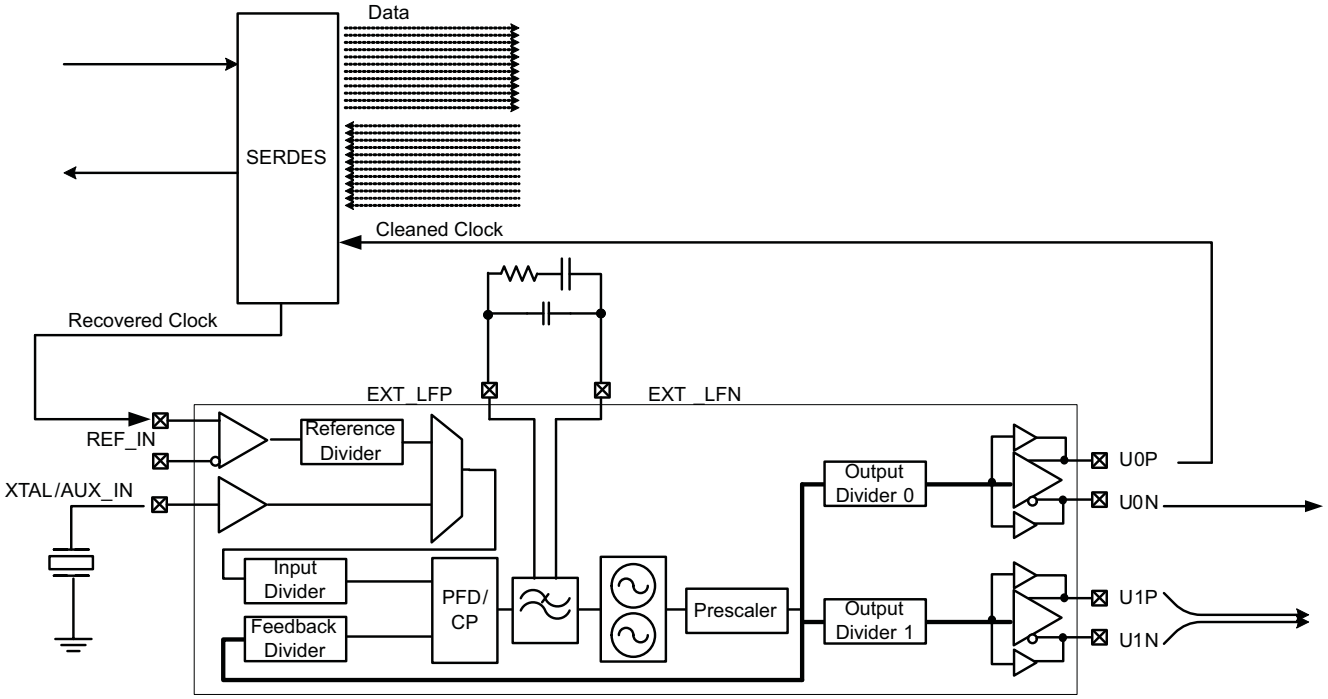


Figure 29. CDCE62002 Clocking SERDES

Because the jitter of the recovered clock can be above 100 ps (RMS), the output jitter from CDCE62002 can be as low and 6 ps (RMS) depending on the external loop filter configuration.

Device Functional Modes (continued)

9.4.3 Clocking ADCS With the CDCE62002

High-speed analog to digital converters incorporate high input bandwidth on both the analog port and the sample clock port. Often the input bandwidth far exceeds the sample rate of the converter. Engineers regularly implement receiver chains that take advantage of the characteristics of bandpass sampling. This implementation trend often causes engineers working in communications system design to encounter the term *clock-limited performance*. Therefore, it is important to understand the impact of clock jitter on ADC performance. Equation 5 shows the relationship of data converter signal to noise ratio (SNR) to total jitter:

$$SNR_{jitter} = 20\log_{10}\left[\frac{1}{2\pi f_{in} jitter_{total}}\right] \quad (5)$$

Total jitter comprises two components: the intrinsic aperture jitter of the converter and the jitter of the sample clock:

$$jitter_{total} = \sqrt{(jitter_{ADC})^2 + (jitter_{CLK})^2} \quad (6)$$

With respect to an ADC with N-bits of resolution, ignoring total jitter, ADC quantization error, and input noise, Equation 7 shows the relationship between resolution and SNR:

$$SNR_{ADC} = 6.02N + 1.76 \quad (7)$$

Figure 30 plots Equation 5 and Equation 7 for constant values of total jitter. When used in conjunction with most ADCs, the CDCE62002 supports a total jitter performance value of <1 ps.

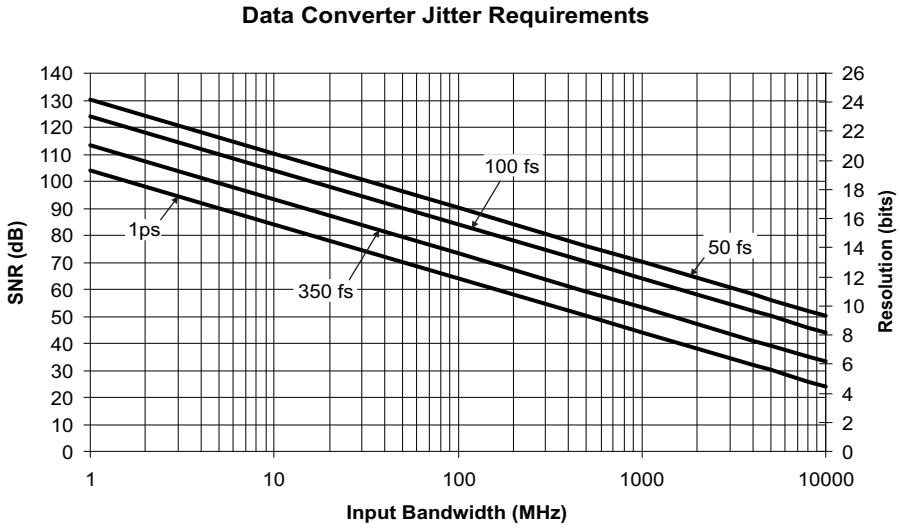


Figure 30. Data Converter Jitter Requirements

9.5 Programming

9.5.1 Interface and Control Block

The interface and control block includes a SPI interface, one control pin, a non-volatile memory array in which the device stores default configuration data, and an array of device registers implemented in static RAM. This RAM, also called the device registers, configures all hardware within the CDCE62002.

9.5.1.1 SPI (Serial Peripheral Interface)

The serial interface of CDCE62002 is a simple bidirectional SPI interface for writing and reading to and from the device registers. It implements a low speed serial communications link in a master/slave topology in which the CDCE62002 is a slave. The SPI consists of four signals:

- **SPI_CLK:**Serial Clock (Output from Master) – the CDCE62002 and the master host clock data in and out on the rising edge of SPI_CLK. Data transitions therefore occur on the falling edge of the clock. (LVCMOS Input Buffer)
- **SPI_MOSI:** Master Output Slave Input (LVCMOS Input Buffer).
- **SPI_MISO:** Master Input Slave Output (Open Drain LVCMOS Buffer)
- **SPI_LE:** Latch Enable (Output from Master). The falling edge of SPI_LE initiates a transfer. If SPI_LE is high, no data transfer can take place. (LVCMOS Input Buffer).

9.5.1.2 SPI Interface Master

The Interface master can be designed using a FPGA or a microcontroller. The CDCE62002 acts as a slave to the SPI master and only supports non-consecutive read and write command. The SPI clock should start and stop with respect to the SPI_LE signal as shown in Figure 31 SPI_MOSI, SPI_CLK and SPI_LE are generated by the SPI Master. SPI_MISO is generated by the SPI slave the CDCE62002.

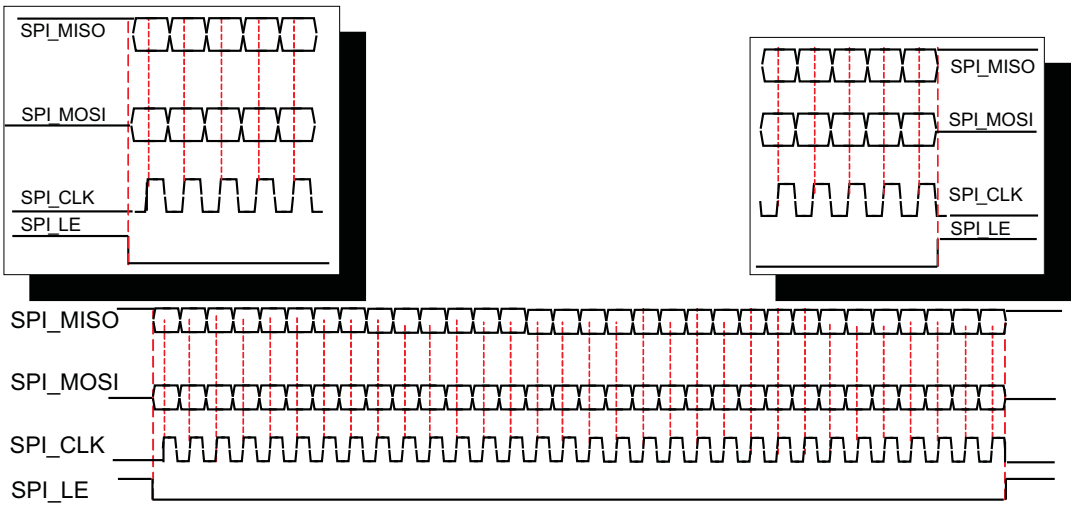


Figure 31. CDCE62002 SPI Read/Write Command

9.5.1.3 SPI Consecutive Read/Write Cycles to the CDCE62002

Figure 32 Illustrates how two consecutive SPI cycles are performed between a SPI Master and the CDCE62002 SPI Slave.

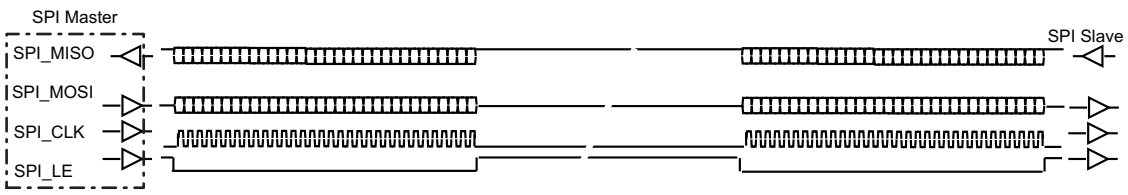


Figure 32. Consecutive Read/Write Cycles

Programming (continued)

9.5.1.4 Writing to the CDCE62002

Figure 33 illustrates a Write to RAM operation. Notice that the latching of the first data bit in the data stream (Bit 0) occurs on the first rising edge of SPI_CLK after SPI_LE transitions from a high to a low. For the CDCE62002, data transitions occur on the falling edge of SPI_CLK. A rising edge on SPI_LE signals to the CDCE62002 that the transmission of the last bit in the stream (Bit 31) has occurred.

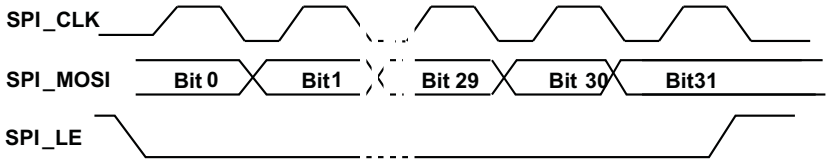


Figure 33. CDCE62002 SPI Write Operation

9.5.1.5 Reading from the CDCE62002

Figure 34 shows how the CDCE62002 executes a read command. The SPI master first issues a read command to initiate a data transfer from the CDCE62002 back to the host (see SPI Bus Timing Characteristics). This command specifies the address of the register of interest. By transitioning SPI_LE from a low to a high, the CDCE62002 resolves the address specified in the appropriate bits of the data field. The host drives SPI_LE low and the CDCE62002 presents the data present in the register specified in the read command on SPI_MISO.

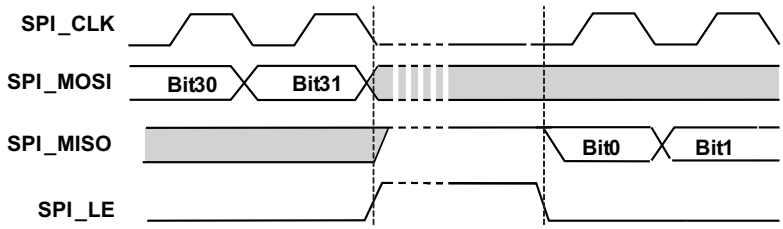


Figure 34. CDCE62002 SPI Read Operation

9.5.1.6 Writing to EEPROM

After the CDCE62002 detects a power-up and completes a reset cycle, the device copies the contents of the on-chip EEPROM into the device registers. (SPI_LE signal has to be HIGH in order for the EEPROM to load correctly during the rising edge of power_down signal).

The host issues a special commands shown in Figure 35 to copy the contents of device registers 0 and 1into EERPOM.

- Copy RAM to EEPROM – unlock, execution of this command can happen many times.

After the command is initiated, power must remain stable and the host must not access the CDCE62002 for at least 50 ms to allow the EEPROM to complete the write cycle and to avoid the possibility of EEPROM corruption.

9.5.1.7 CDCE62002 SPI Command Structure

The CDCE62002 supports three commands issued by the master through the SPI:

- Write to RAM
- Read Command
- Copy RAM to EEPROM – unlock

Figure 35 provides a summary of the CDCE62002 SPI command structure. The host (master) constructs a Write to RAM command by specifying the appropriate register address in the address field and appends this value to the beginning of the data field. Therefore, a valid command stream must include 32 bits, transmitted LSB first. The host must issue a read command to initiate a data transfer from the CDCE62002 back to the host. This command specifies the address of the register of interest in the data field.

Programming (continued)

			Data Field (28 Bits)																										Addr Field (4 Bits)			
Register	Operation	NVM	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	3	2	1	0
0	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	0
1	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	1
2	Status/Control	No	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	1	0
Instruction	Read Command	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	A	A	A	A	1	1	1	0
Instruction	RAM EEPROM	Unlock	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

NOTE: 'A' indicates address bits.

Figure 35. CDCE62002 SPI Command Structure

9.5.2 Device Configuration

The *Feature Description* section described four different functional blocks contained within the CDCE62002. Figure 36 depicts these blocks along with a high-level functional block diagram of the circuit elements comprising each block. The balance of this section focuses on a detailed discussion of each functional block from the perspective of how to configure them.

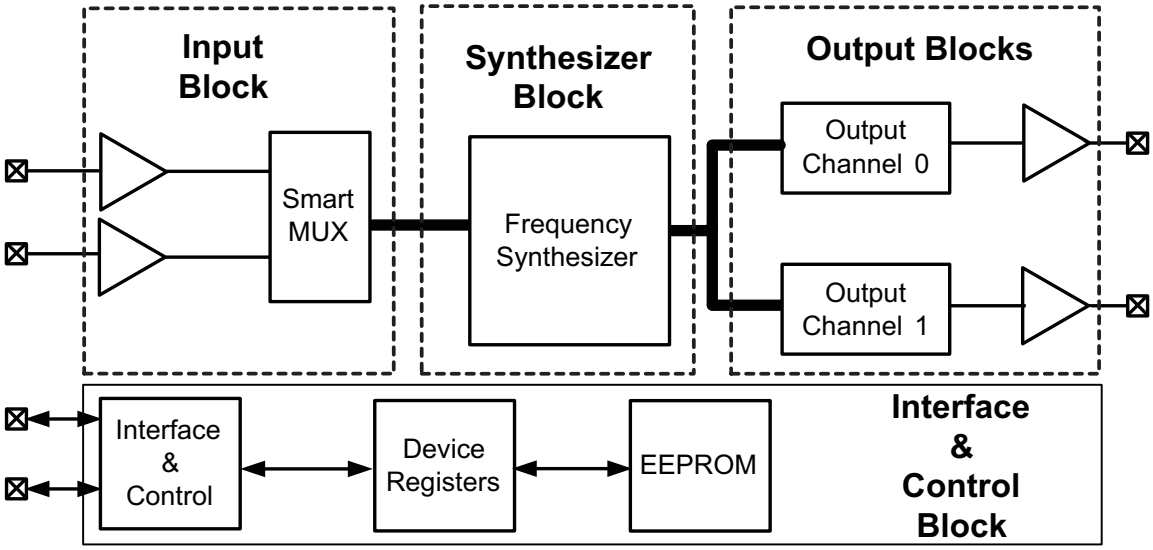


Figure 36. CDCE62002 Circuit Blocks

9.6 Register Maps

9.6.1 Device Registers: Register 0 Address 0x00

Table 16. CDCE62002 Register 0 Bit Definitions

REGISTER BIT	BIT NAME	RELATED BLOCK	DESCRIPTION / FUNCTION	
0	INBUFSELX	INBUFSELX	Input Buffer Select (LVPECL,LVDS or LVCMOS) XY(00) Disabled, (01) LVDS, (10) LVPECL, (11) LVCMOS The VBB internal Biasing will be determined from this setting	EEPROM
1	INBUFSELY	INBUFSELY		EEPROM
2	REFSEL	Smart MUX Bits(2,3)	*See specific section for more detailed description and configuration setup.* 00 – RESERVED 10 – REF_IN Select 01– AUX_IN Select 11 – Auto Select (Reference then AUX)	EEPROM
3	AUXSEL			EEPROM
4	ACDCSEL	Input Buffers	If Set to 1 DC Termination, If set to “0” AC Termination	EEPROM
5	TERMSEL	Input Buffers	If Set to 0 Input Buffer Internal Termination Enabled	EEPROM
6	REFDIVIDE 0		Reference Divider Settings (Refer to Table 5) *See specific section for more detailed description and configuration setup.*	EEPROM
7	REFDIVIDE 1			EEPROM
8	REFDIVIDE 2			EEPROM
9	REFDIVIDE 3			EEPROM
10	RESERVED		Always Set to 0	EEPROM
11	*I70TEST*	*TEST*	*Set to 0 for Normal Operation.*	EEPROM
12	*ATETEST*	*TEST*	*Set to 0 for Normal Operation.*	EEPROM
13	LOCKW(0)	PLL Lock	Lock-detect window Bit 0	EEPROM
14	LOCKW(1)	PLL Lock	Lock-detect window Bit 1	EEPROM
15	OUT0DIVRSEL0	Output 0	Output 0 Divider Settings (Refer to Table 6) *See specific section for more detailed description and configuration setup.*	EEPROM
16	OUT0DIVRSEL1	Output 0		EEPROM
17	OUT0DIVRSEL2	Output 0		EEPROM
18	OUT0DIVRSEL3	Output 0		EEPROM
19	OUT1DIVRSEL0	Output 1	Output 1 Divider Settings (Refer to Table 6) *See specific section for more detailed description and configuration setup.*	EEPROM
20	OUT1DIVRSEL1	Output 1		EEPROM
21	OUT1DIVRSEL2	Output 1		EEPROM
22	OUT1DIVRSEL3	Output 1		EEPROM
23	HIPERORMANCE	Output 0 & 1	High Performance, If this Bit is set to 1: – Increases the Bias in the device to achieve Best Phase Noise on the Output Divider – It changes the LVPECL Buffer to Hi Swing in LVPECL. – It increases the current consumption by 20mA (Typical) – This setting only applies to LVPECL output buffers. If none of these two outputs are LVPECL, this bit should be set to zero.	EEPROM
24	OUTBUFSEL0X	Output 0	Output Buffer mode select for OUTPUT 0 . (X,Y)=00:Disabled, 01:LVCMOS, 10:LVDS, 11:LVPECL	EEPROM
25	OUTBUFSEL0Y	Output 0		EEPROM
26	OUTBUFSEL1X	Output 1	Output Buffer mode select for OUTPUT 1 . (X,Y)=00:Disabled, 01:LVCMOS, 10:LVDS, 11:LVPECL	EEPROM
27	OUTBUFSEL1Y	Output 1		EEPROM

Table 17. Reference Input AC/DC Input Termination Table

REFERENCE INPUT	REGISTER BITS				VBB VOLTAGE	REF+ TERMINATION	REF– TERMINATION
INTERNAL TERMINATION	0	1	4	5	GENERATOR	5kΩ to VBB	5kΩ to VBB
External Termination	X	X	X	1	—	OPEN	OPEN
Disabled	0	0	X	X	—	OPEN	OPEN
LVCMOS	1	1	X	0	—	OPEN	OPEN
LVPECL-AC	1	0	0	0	1.9 V	CLOSED	CLOSED
LVPECL-DC	1	0	1	0	1.0 V	CLOSED	CLOSED
LVDS-AC	0	1	0	0	1.2 V	CLOSED	CLOSED
LVDS-DC	0	1	1	0	1.2 V	CLOSED	CLOSED

9.6.2 Device Registers: Register 1 Address 0x01

Table 18. CDCE62002 Register 1 Bit Definitions

REGISTER BIT	BIT NAME	RELATED BLOCK	DESCRIPTION / FUNCTION	
0	SELVCO	VCO Core	VCO Select – See Table 10 for details	EEPROM
1	SELINDIV0	VCO Core	Input Divider Settings (Refer to Table 7) *See specific section for more detailed description and configuration setup.*	EEPROM
2	SELINDIV1	VCO Core		EEPROM
3	SELINDIV2	VCO Core		EEPROM
4	SELINDIV3	VCO Core		EEPROM
5	SELINDIV4	VCO Core		EEPROM
6	SELINDIV5	VCO Core		EEPROM
7	SELINDIV6	VCO Core		EEPROM
8	SELINDIV7	VCO Core		EEPROM
9	SELPRESCA	VCO Core	PRESCALER Setting. (Refer to Table 11) *See specific section for more detailed description and configuration setup.*	EEPROM
10	SELPRESCB	VCO Core		EEPROM
11	SELFBDIV0	VCO Core	FEEDBACK DIVIDER Setting (Refer to Table 8) *See specific section for more detailed description and configuration setup.*	EEPROM
12	SELFBDIV1	VCO Core		EEPROM
13	SELFBDIV2	VCO Core		EEPROM
14	SELFBDIV3	VCO Core		EEPROM
15	SELFBDIV4	VCO Core		EEPROM
16	SELFBDIV5	VCO Core		EEPROM
17	SELFBDIV6	VCO Core		EEPROM
18	SELFBDIV7	VCO Core		EEPROM
19	SELBPDIV0	VCO Core	BYPASS DIVIDER Setting (Refer to Table 9) *See specific section for more detailed description and configuration setup.*	EEPROM
20	SELBPDIV1	VCO Core		EEPROM
21	SELBPDIV2	VCO Core		EEPROM
22	LFRCSEL0	VCO Core	Loop Filter & Charge Pump Control Setting (Refer to Table 12) *See specific section for more detailed description and configuration setup.*	EEPROM
23	LFRCSEL1	VCO Core		EEPROM
24	LFRCSEL2	VCO Core		EEPROM
25	LFRCSEL3	VCO Core		EEPROM
26	RESERVED	Status	TI Use Only; set 0	EEPROM
27	RESERVED	Status	Read Only; May read back to 1 or 0; set '1' while writing	EEPROM

9.6.3 Device Registers: Register 2 Address 0x02

Table 19. CDCE62002 Register 2 Bit Definitions

REGISTER BIT	BIT NAME	RELATED BLOCK	DESCRIPTION / FUNCTION	
0	RESERVED	Diagnostics	*TI Test Registers. For TI Use Only*	RAM
1	RESERVED	Diagnostics	*TI Test Registers. For TI Use Only*	RAM
2	RESERVED	Diagnostics	*TI Test Registers. For TI Use Only*	RAM
3	RESERVED	Diagnostics	*TI Test Registers. For TI Use Only*	RAM
4	RESERVED	Diagnostics	*TI Test Registers. For TI Use Only*	RAM
5	RESERVED	Diagnostics	*TI Test Registers. For TI Use Only*	RAM
6	PLLLOCKPIN	Status	Read only: Status of the PLL Lock Pin Driven by the device. PLL Lock = 1	RAM
7	$\overline{\text{PD}}$	Control	Power-down mode “On” when set to 0, Off when set to “1” is normal operation ($\overline{\text{PD}}$ bit does not load the EEPROM into RAM when set to "1").	RAM
8	$\overline{\text{SYNC}}$	Control	If toggled 1-0-1 this bit forces “$\overline{\text{SYNC}}$“ resynchronize the Output Dividers.	RAM
9	RESERVED	Diagnostics	*TI Test Registers. For TI Use Only*	RAM
10	VERSION0	Read Only		RAM
11	VERSION1	Read Only		RAM
12	VERSION2	Read Only		RAM
13	CALSELECT	VCO Core	This bit selects the VCO calibration mode. If CALSELECT = 0 , toggling PD# bit (Register 2 bit 7) will calibrate the VCO. When CALSELECT = 1, toggling the PLLRESET bit (Register 2 bit 20) will calibrate the VCO. Default value = 0	RAM
14	RESERVED	Diagnostics	*TI Test Registers. For TI Use Only*	RAM
15	RESERVED	Diagnostics	*TI Test Registers. For TI Use Only*	RAM
16	RESERVED	Diagnostics	*TI Test Registers. For TI Use Only*	RAM
17	RESERVED	Diagnostics	*TI Test Registers. For TI Use Only*	RAM
18	RESERVED	Diagnostics	*TI Test Registers. For TI Use Only*	RAM
19	RESERVED	Diagnostics	*TI Test Registers. For TI Use Only*	RAM
20	PLLRESET	Diagnostics	When CALSELECT=1 this bit forces a VCO calibration when toggled 1-0-1. If CALSELECT=0 this bit is ignored.	RAM
21	*TITSTCFG0*	Diagnostics	*TI Test Registers. For TI Use Only*	RAM
22	*TITSTCFG1*	Diagnostics	*TI Test Registers. For TI Use Only*	RAM
23	*TITSTCFG2*	Diagnostics	*TI Test Registers. For TI Use Only*	RAM
24	*TITSTCFG3*	Diagnostics	*TI Test Registers. For TI Use Only*	RAM
25	RESERVED	Diagnostics	*TI Test Registers. For TI Use Only*	RAM
26	RESERVED	Diagnostics	*TI Test Registers. For TI Use Only*	RAM
27	RESERVED	Diagnostics	*TI Test Registers. For TI Use Only*	RAM

10 Power Supply Recommendations

The CDCE62002 is a high-performance device; therefore pay careful attention to device configuration and printed-circuit board layout with respect to power consumption. Table 20 provides the power consumption for the individual blocks within the CDCE62002. To estimate total power consumption, calculate the sum of the products of the number of blocks used and the power dissipated of each corresponding block.

Table 20. CDCE62002 Power Consumption

INTERNAL BLOCK (Power at 3.3 V)	POWER DISSIPATED PER BLOCK (mW)	NUMBER OF BLOCKS PER DEVICE
Input circuit	32	1
PLL and VCO core	333	1
Output divider	92	2
Output buffer (LVPECL)	150	2
Output buffer (LVDS)	95	2
Output buffer (LVCMOS)	62	4

This power estimate determines the degree of thermal management required for a specific design. Observing good thermal layout practices enables the thermal pad on the backside of the 32-pin VQFN package to provide a good thermal path between the die contained within the package and the ambient air. This thermal pad also serves as the ground connection the device; therefore, a low inductance connection to the ground plane is essential.

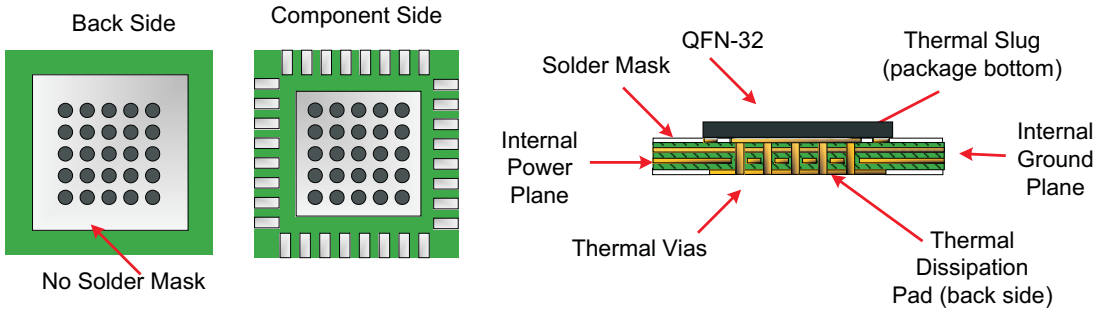


Figure 37. CDCE62002 Recommended PCB Layout

11 Layout

11.1 Layout Guidelines

Figure 38 shows a conceptual layout focusing on power supply bypass capacitor placement. If the capacitors are mounted on the back side, 0402 components can be employed; however, soldering to the thermal dissipation pad can be difficult. If the capacitors are mounted on the component side, 0201 components must be used to facilitate signal routing. In either case, the connections between the capacitor and the power supply terminal on the device must be kept as short as possible.

11.2 Layout Example

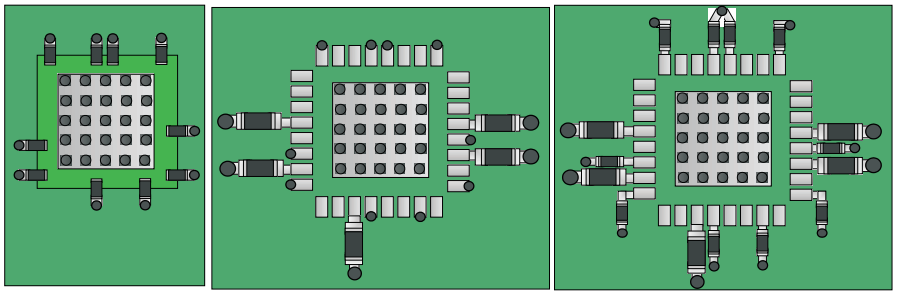


Figure 38. CDCE62002 Power Supply Bypassing

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

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12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Package

The CDCE62002 is packaged in a 32-Pin Lead Free “Green” Plastic Quad Flatpack Package with enhanced bottom thermal pad for heat dissipation. The Texas Instruments Package Designator is; RHB (S-PQFP-N32). Please refer to the Mechanical Data appendix at the end of this document for more information.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDCE62002RHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDCE 62002
CDCE62002RHBR.Z	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDCE 62002
CDCE62002RHBT	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDCE 62002
CDCE62002RHBT.Z	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDCE 62002

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

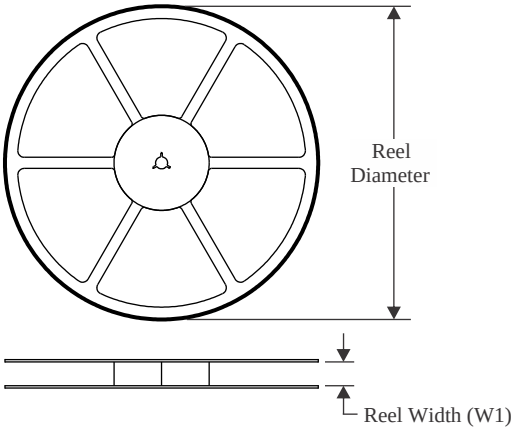
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

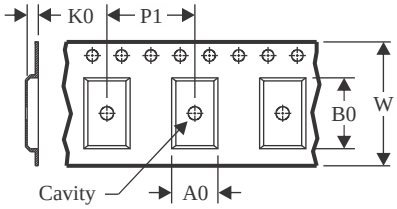
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

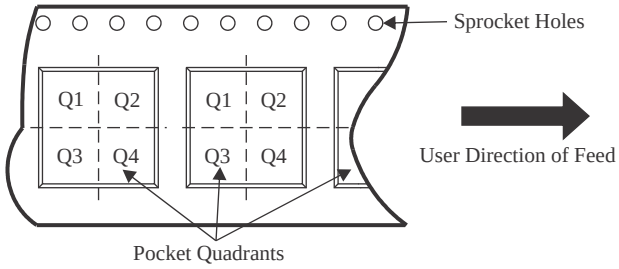


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

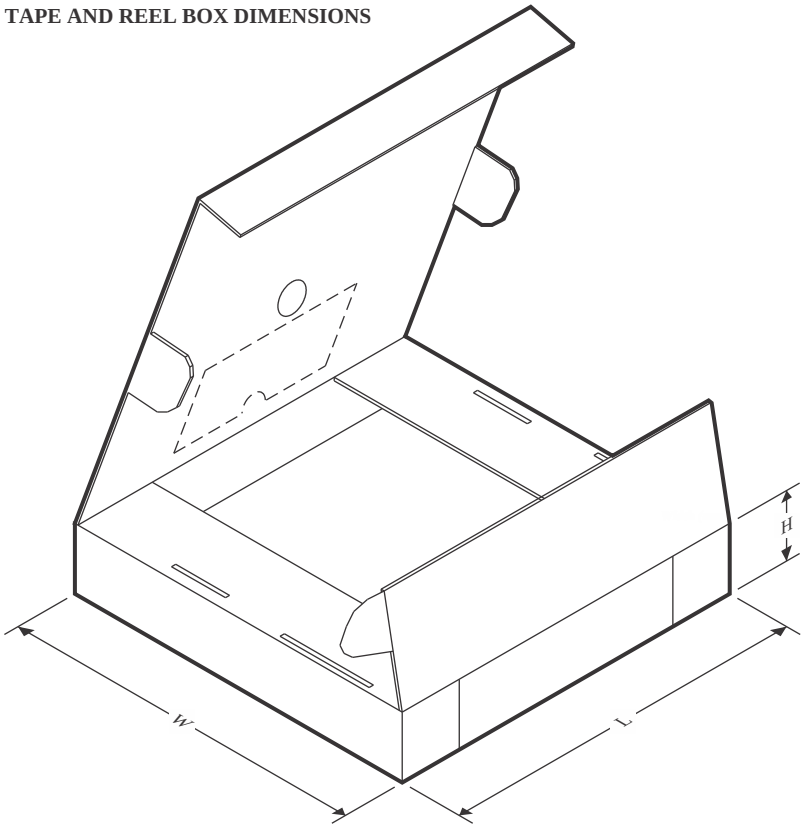
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCE62002RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCE62002RHBR	VQFN	RHB	32	3000	350.0	350.0	43.0

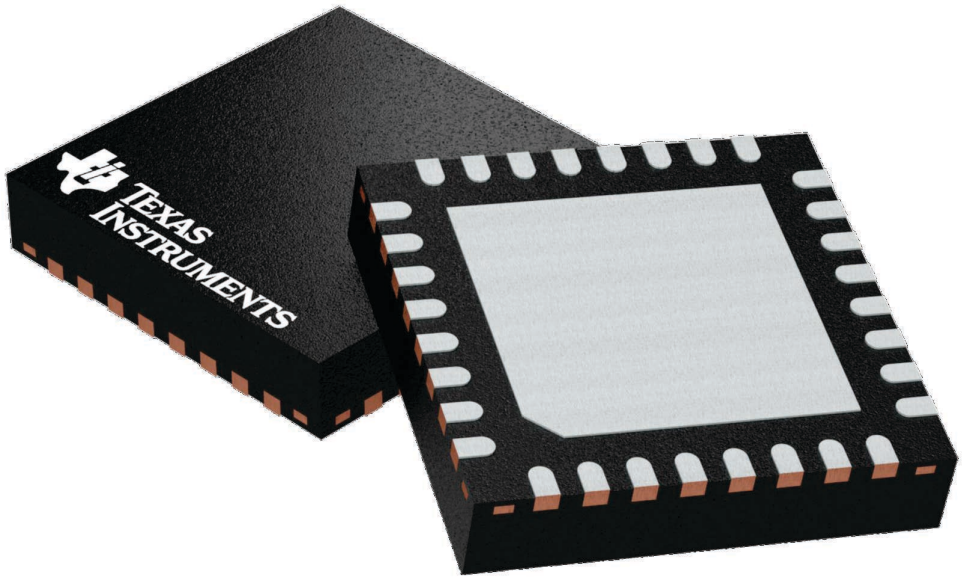
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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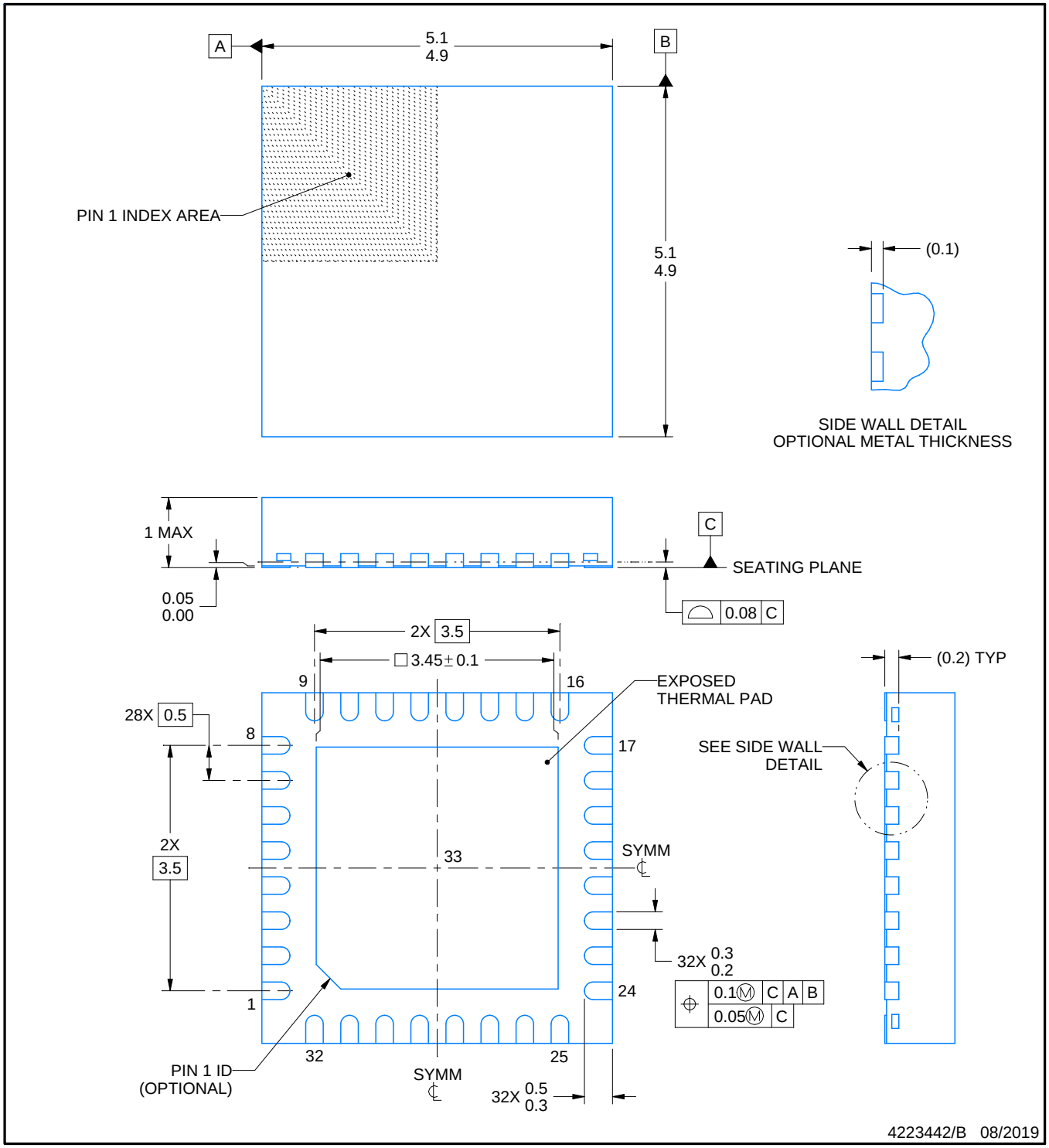
RHB0032E

PACKAGE OUTLINE

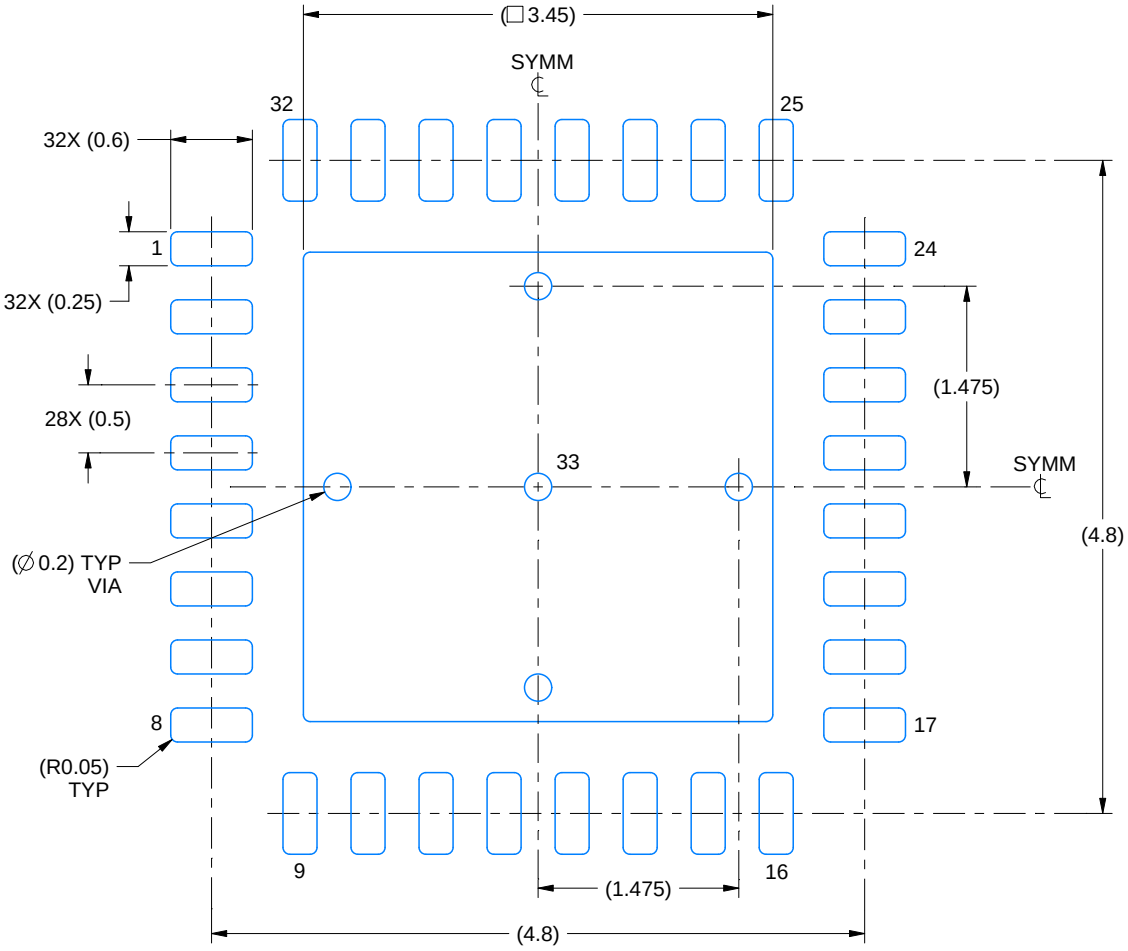
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

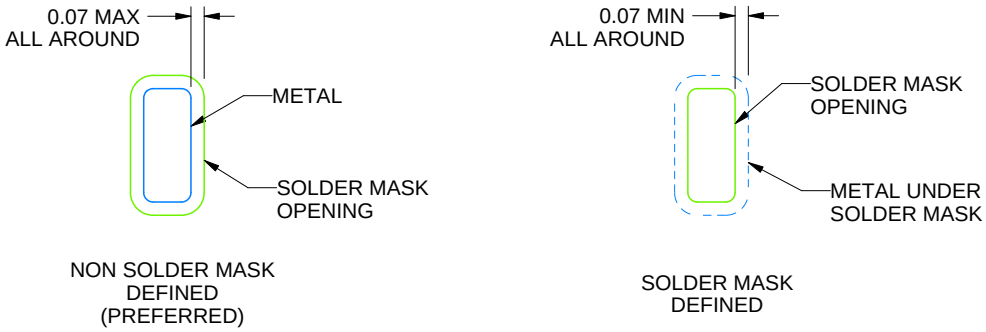


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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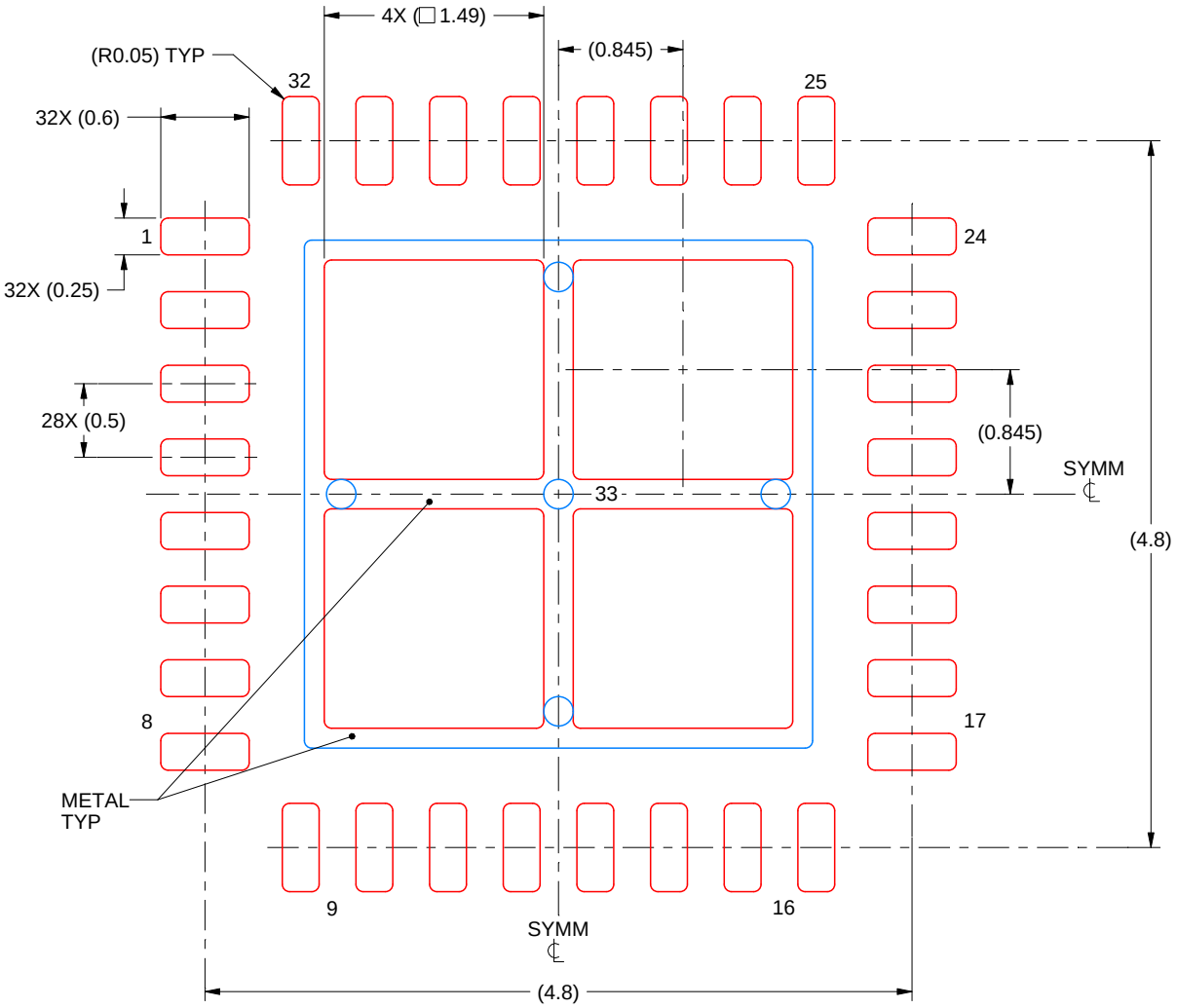
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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