

Silicon Carbide Power MOSFET N-Channel Enhancement Mode

Features

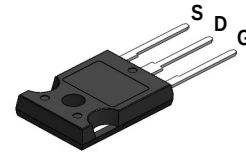
- 3rd Generation SiC MOSFET technology
- High blocking voltage with low on-resistance
- High speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant

Typical Applications

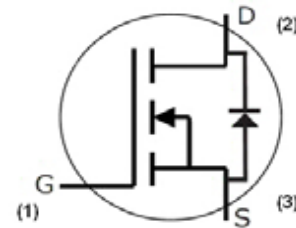
- EV charging
- Server power supplies
- Solar PV inverters
- UPS
- DC/DC converters

Benefits

- Higher system efficiency
- Reduced cooling requirements
- Increased power density
- Increased system switching frequency
- Easy to parallel and simple to drive
- Enable new hard switching PFC topologies (Totem-Pole)



T0-247-3



ORDERING INFORMATION

HT39N650ADZ

$T_A = -40^\circ$ to 175° C for all packages

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			650	V	$T_c = 25^\circ\text{C}$	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+19		Transient	
Operational Gate-Source Voltage	$V_{GS op}$		-4/15			Static	Note 1
DC Continuous Drain Current	I_D			39	A	$V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}, T_J \leq 175^\circ\text{C}$	Fig. 19 Note 2
				20		$V_{GS} = 15\text{ V}, T_c = 100^\circ\text{C}, T_J \leq 175^\circ\text{C}$	
Pulsed Drain Current	I_{DM}			99		t_{pmax} limited by T_{Jmax} $V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}$	Fig. 22
Power Dissipation	P_D			150	W	$T_c = 25^\circ\text{C}, T_J = 175^\circ\text{C}$	Fig. 20
Operating Junction and Storage Temperature	T_J, T_{stg}			-40 to +175	$^\circ\text{C}$		
Solder Temperature	T_L			260		According to JEDEC J-STD-020	
Mounting Torque	M_D			1 8.8	Nm lbf-in	M3 or 6-32 screw	

Note (1): Recommended turn-on gate voltage is 15V with $\pm 5\%$ regulation tolerance, see Application Note PRD-04814 for additional details

Note (2): Verified by design

Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.3	3.6	V	$V_{DS} = V_{GS}, I_D = 5 \text{ mA}$	Fig. 11
		—	1.9	—		$V_{DS} = V_{GS}, I_D = 5 \text{ mA}, T_J = 175^\circ\text{C}$	
Zero Gate Voltage Drain Current	I_{DSS}	—	1	50	μA	$V_{DS} = 650 \text{ V}, V_{GS} = 0 \text{ V}$	
Gate-Source Leakage Current	I_{GSS}	—	10	250	nA	$V_{GS} = 15 \text{ V}, V_{DS} = 0 \text{ V}$	
Drain-Source On-State Resistance	$R_{DS(on)}$	42	60	79	m Ω	$V_{GS} = 15 \text{ V}, I_D = 13.2 \text{ A}$	Fig. 4, 5, 6
		—	80	—		$V_{GS} = 15 \text{ V}, I_D = 13.2 \text{ A}, T_J = 175^\circ\text{C}$	
Transconductance	g_{fs}	—	10	—	S	$V_{DS} = 20 \text{ V}, I_{DS} = 13.2 \text{ A}$	Fig. 7
			9			$V_{DS} = 20 \text{ V}, I_{DS} = 13.2 \text{ A}, T_J = 175^\circ\text{C}$	
Input Capacitance	C_{iss}	—	1020	—	pF	$V_{GS} = 0 \text{ V}, V_{DS} = 600 \text{ V}$ $f = 1 \text{ Mhz}$ $V_{AC} = 25 \text{ mV}$	Fig. 17, 18
Output Capacitance	C_{oss}	—	80	—			
Reverse Transfer Capacitance	C_{rss}	—	9	—			
Effective Output Capacitance (Energy Related)	$C_{o(er)}$	—	95	—		$V_{GS} = 0 \text{ V}, V_{DS} = 0 \text{ V to } 400 \text{ V}$	Note 3
Effective Output Capacitance (Time Related)	$C_{o(tr)}$	—	132	—			
C_{oss} Stored Energy	E_{oss}	—	15	—	μJ	$V_{DS} = 600 \text{ V}, f = 1 \text{ Mhz}$	Fig. 16
Turn-On Switching Energy (Body Diode)	E_{on}	—	110	—		$V_{DS} = 400 \text{ V}, V_{GS} = -4 \text{ V/15 V}, I_D = 13.2 \text{ A},$ $R_{G(ext)} = 2.5 \Omega, L = 135 \mu\text{H}, T_J = 175^\circ\text{C}$ FWD = Internal Body Diode of MOSFET	Fig. 25
Turn Off Switching Energy (Body Diode)	E_{off}	—	22	—			
Turn-On Switching Energy (External Sic Diode)	E_{on}	—	63	—			
Turn Off Switching Energy (External Sic Diode)	E_{off}	—	28	—			
Turn-On Delay Time	$t_{d(on)}$	—	9	—	ns	$V_{DD} = 400 \text{ V}, V_{GS} = -4 \text{ V/15 V}$ $I_D = 13.2 \text{ A}, R_{G(ext)} = 2.5 \Omega,$ $L = 135 \mu\text{H}$ Timing relative to V_{DS} Inductive load	Fig. 26
Rise Time	t_r	—	20	—			
Turn-Off Delay Time	$t_{d(off)}$	—	17	—			
Fall Time	t_f	—	8	—			
Internal Gate Resistance	$R_{G(int)}$	—	3	—	Ω	$f = 1 \text{ MHz}, V_{AC} = 25 \text{ mV}$	
Gate to Source Charge	Q_{gs}	—	14	—	nC	$V_{DS} = 400 \text{ V}, V_{GS} = -4 \text{ V/15 V}$ $I_D = 13.2 \text{ A}$ Per IEC60747-8-4 pg 21	Fig. 12
Gate to Drain Charge	Q_{gd}	—		—			
Total Gate Charge	Q_g	—	46	—			

Note:

³ $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

$C_{o(tr)}$, a lumped capacitance that gives same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Reverse Diode Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Notes
Diode Forward Voltage	V_{SD}	5.1	—	V	$V_{GS} = -4\text{ V}, I_{SD} = 6.6\text{ A}, T_J = 25^\circ\text{C}$	Fig. 8, 9, 10
		4.8	—		$V_{GS} = -4\text{ V}, I_{SD} = 6.6\text{ A}, T_J = 175^\circ\text{C}$	
Continuous Diode Forward Current	I_S	—	23	A	$V_{GS} = -4\text{ V}, T_c = 25^\circ\text{C}$	
Diode pulse Current	I_{SM}	—	99		$V_{GS} = -4\text{ V}$, pulse width t_p limited by T_{jmax}	
Reverse Recovery Time	t_{rr}	20	—	ns	$V_{GS} = -4\text{ V}, I_{SD} = 13.2\text{ A}, V_R = 400\text{ V}$ $di_F/dt = 1200\text{ A}/\mu\text{s}, T_J = 175^\circ\text{C}$	
Reverse Recovery Charge	Q_{rr}	190	—	nC		
Peak Reverse Recovery Current	I_{RRM}	16	—	A		
Reverse Recovery Time	t_{rr}	29	—	ns	$V_{GS} = -4\text{ V}, I_{SD} = 13.2\text{ A}, V_R = 400\text{ V}$ $di_F/dt = 750\text{ A}/\mu\text{s}, T_J = 175^\circ\text{C}$	
Reverse Recovery Charge	Q_{rr}	181	—	nC		
Peak Reverse Recovery Current	I_{RRM}	9	—	A		

Thermal Characteristics

Parameter	Symbol	Typ.	Unit	Note
Thermal Resistance from Junction to Case	$R_{\theta JC}$	0.99	$^\circ\text{C}/\text{W}$	Fig. 21
Thermal Resistance From Junction to Ambient	$R_{\theta JA}$	40		

Typical Performance

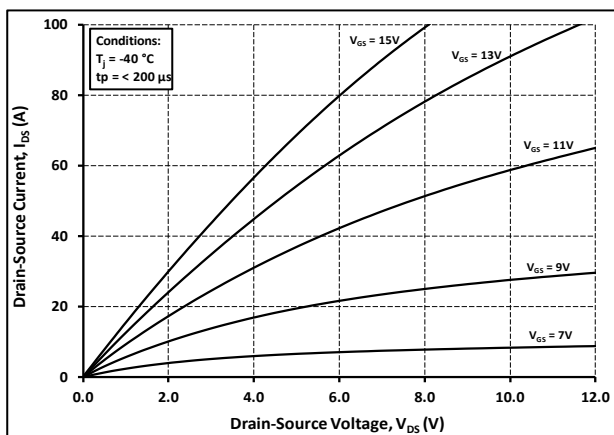


Figure 1. Output Characteristics $T_j = -40^{\circ}\text{C}$

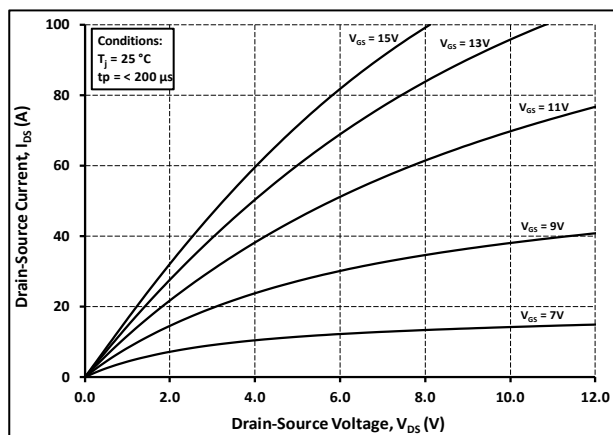


Figure 2. Output Characteristics $T_j = 25^{\circ}\text{C}$

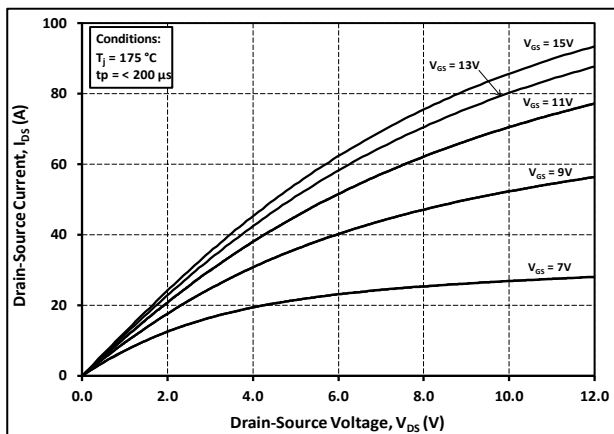


Figure 3. Output Characteristics $T_j = 175^{\circ}\text{C}$

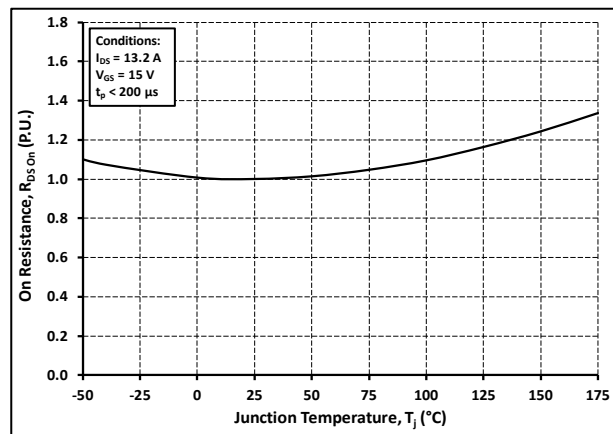


Figure 4. Normalized On-Resistance vs. Temperature

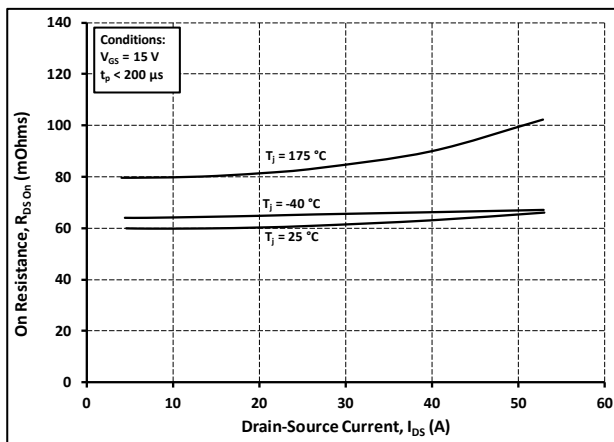


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

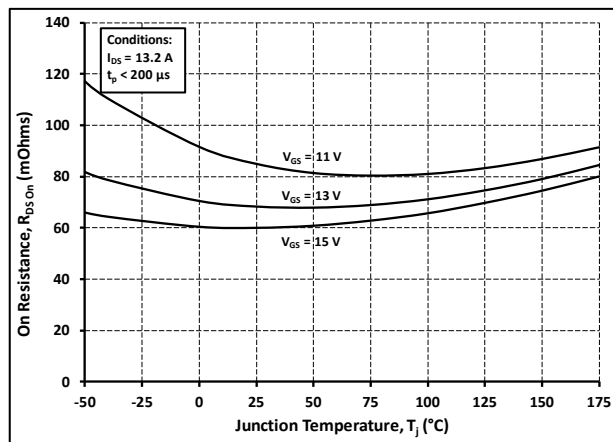


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

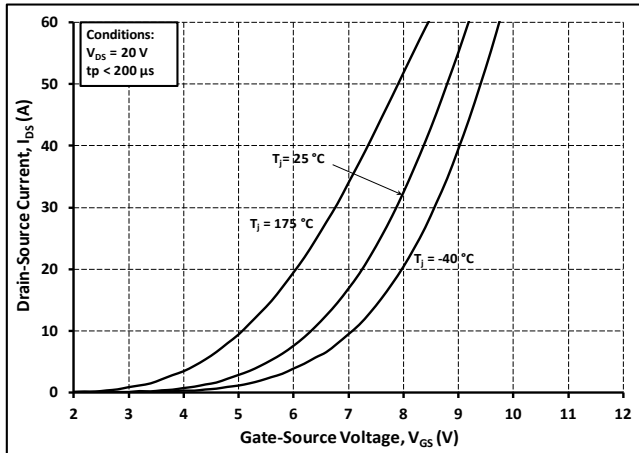


Figure 7. Transfer Characteristic for Various Junction Temperatures

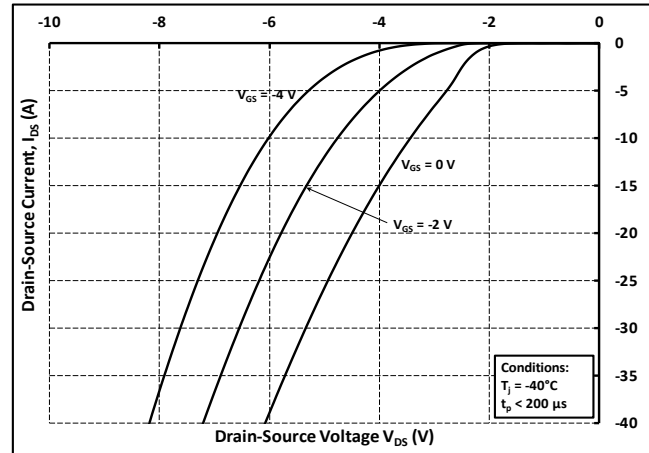


Figure 8. Body Diode Characteristic at -40°C

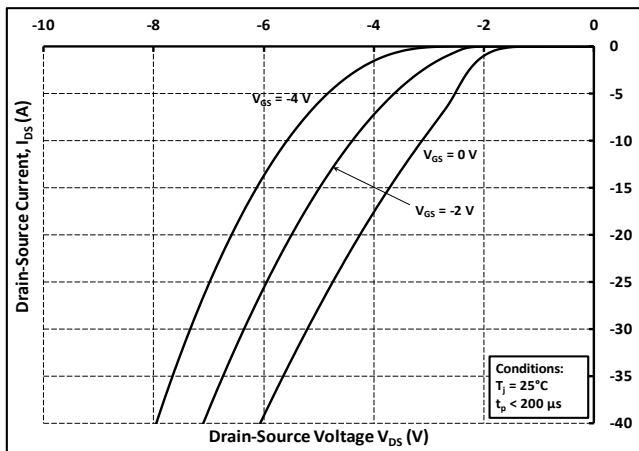


Figure 9. Body Diode Characteristic at 25°C

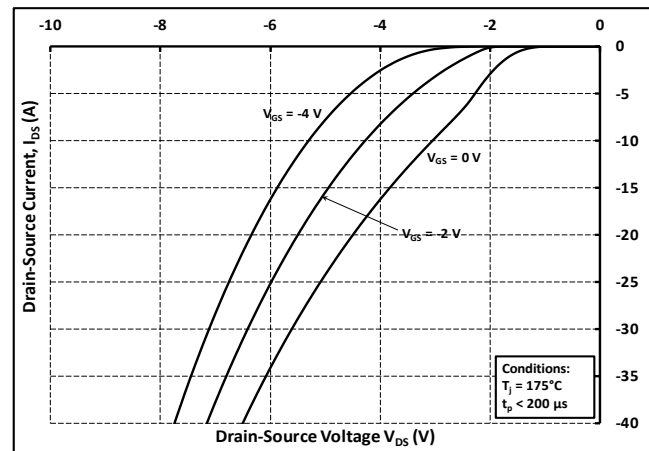


Figure 10. Body Diode Characteristic at 175°C

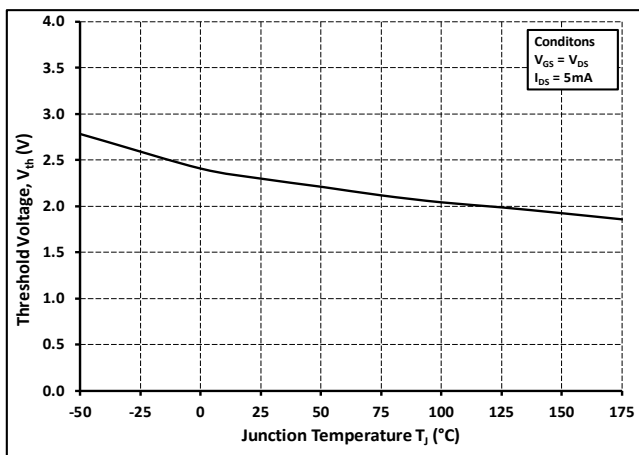


Figure 11. Threshold Voltage vs. Temperature

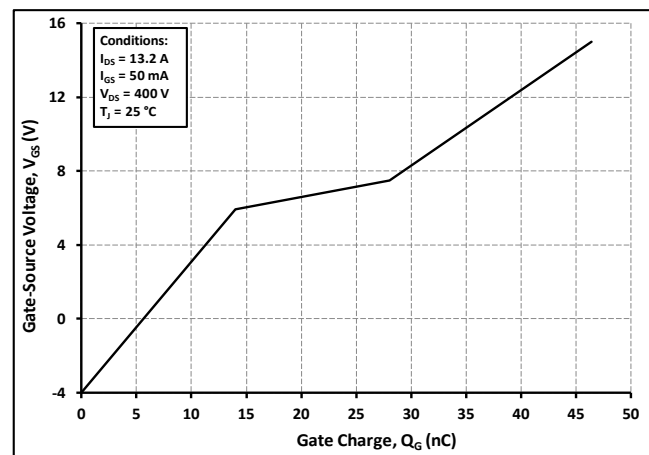


Figure 12. Gate Charge Characteristics

Typical Performance

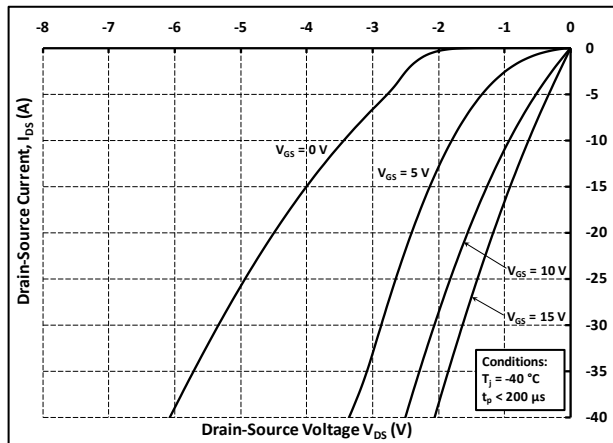


Figure 13. 3rd Quadrant Characteristic at -40°C

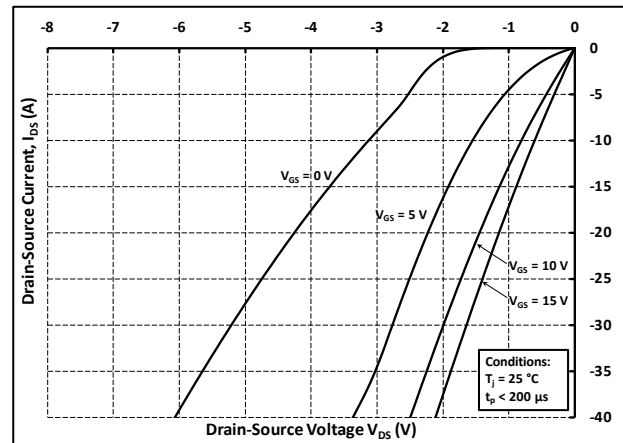


Figure 14. 3rd Quadrant Characteristic at 25°C

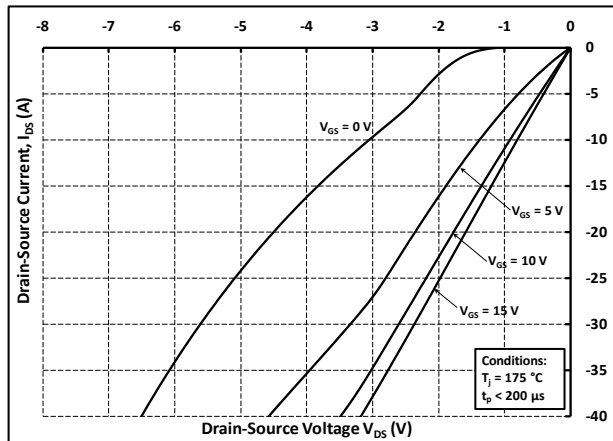


Figure 15. 3rd Quadrant Characteristic at 175°C

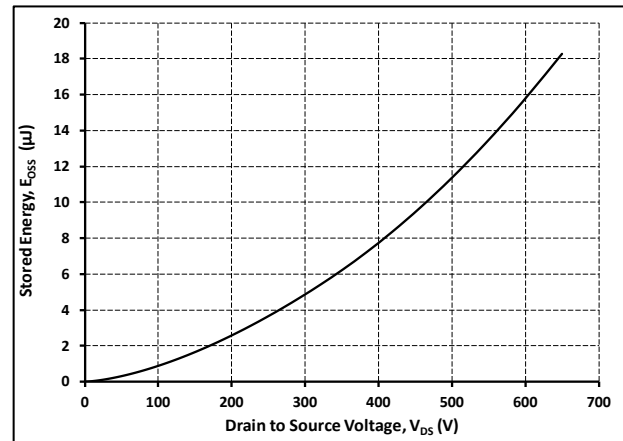


Figure 16. Output Capacitor Stored Energy

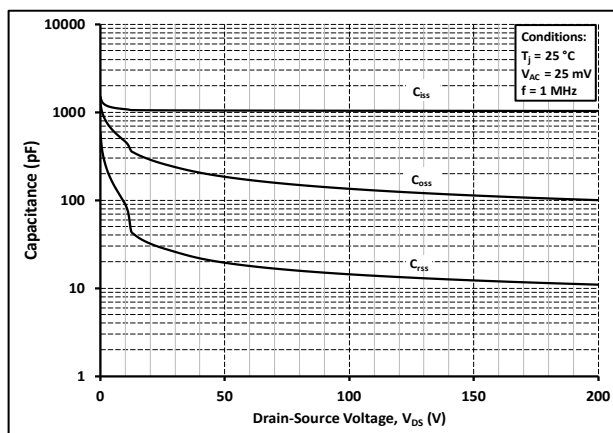


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

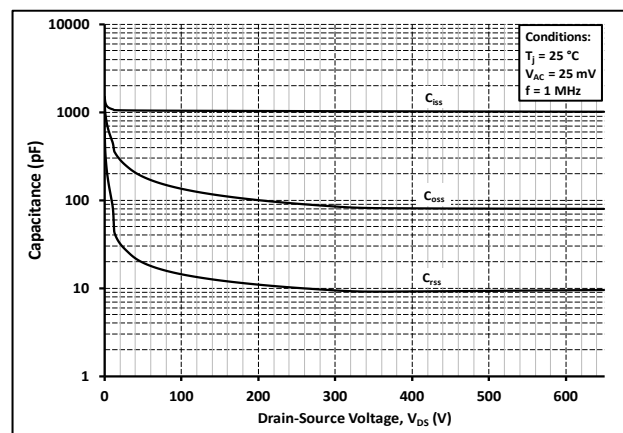


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 650V)

Typical Performance

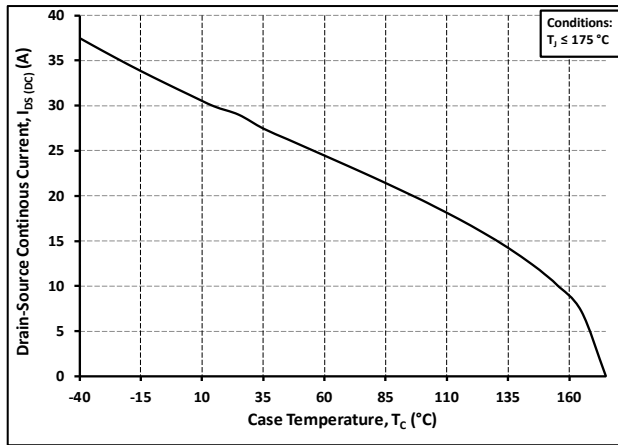


Figure 19. Continuous Drain Current Derating vs. Case Temperature

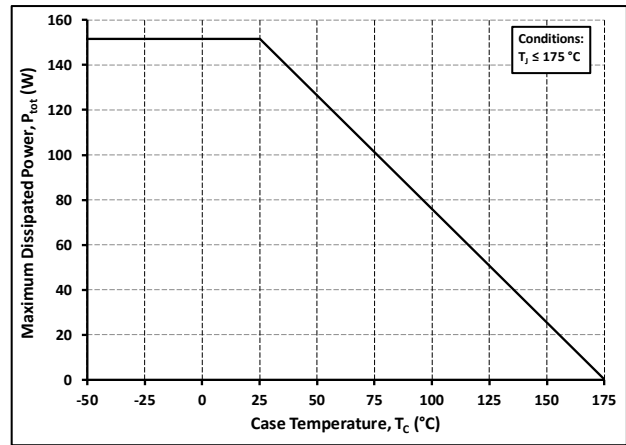


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

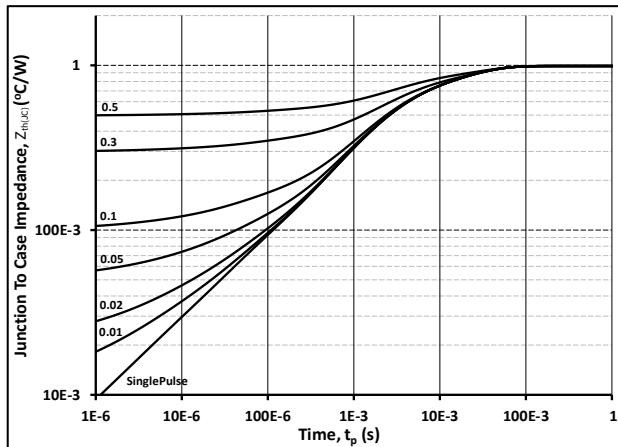


Figure 21. Transient Thermal Impedance (Junction - Case)

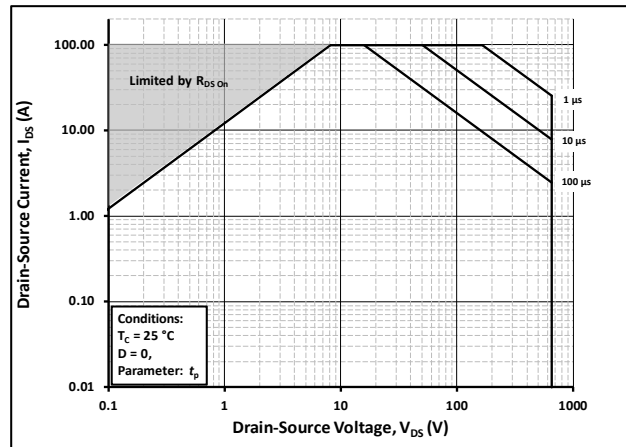


Figure 22. Safe Operating Area

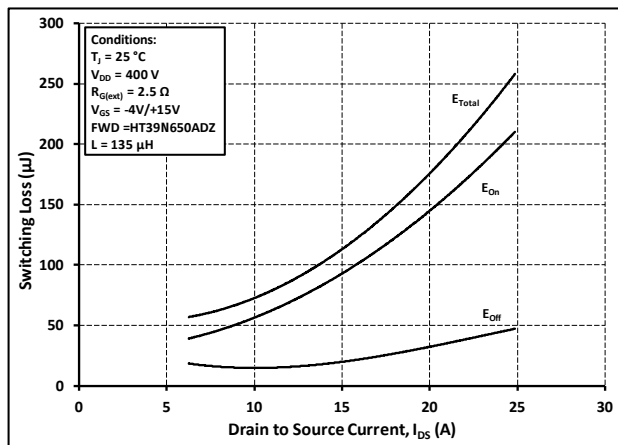


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 400V$)

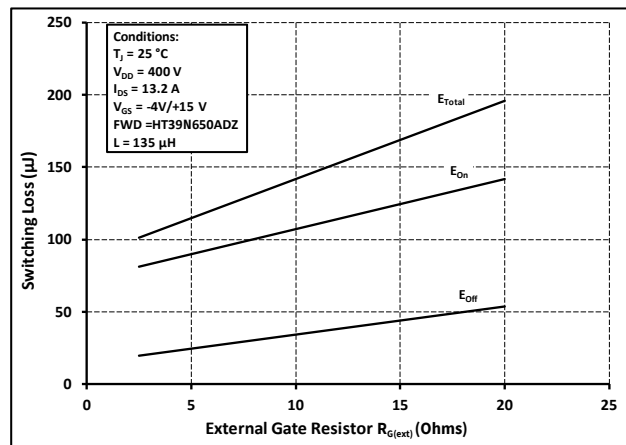


Figure 24. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

Typical Performance

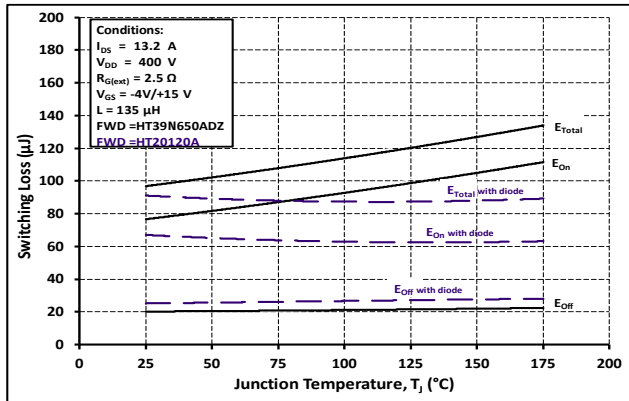


Figure 25. Clamped Inductive Switching Energy vs. Temperature

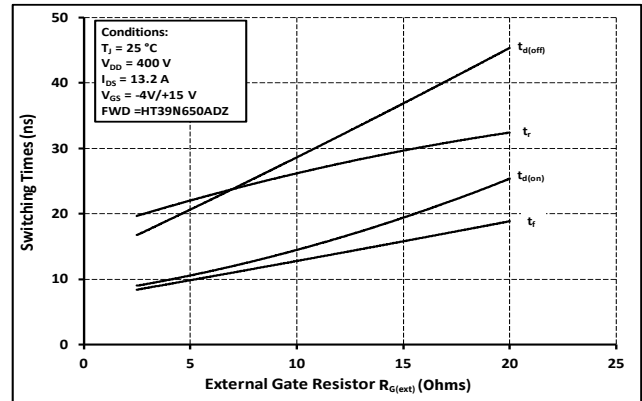


Figure 26. Switching Times vs. $R_{G(ext)}$

Test Circuit Schematic

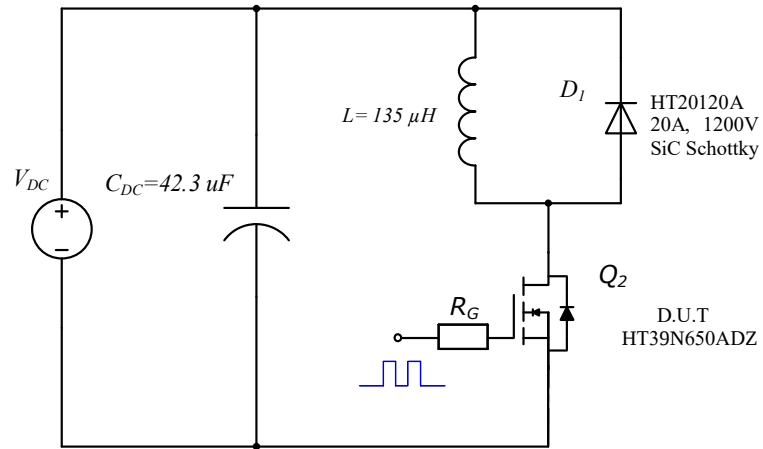


Figure 27. Clamped Inductive Switching Waveform Test Circuit

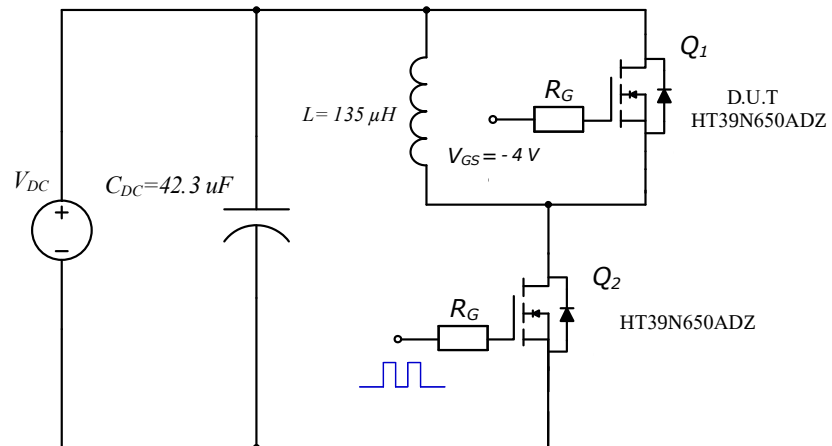
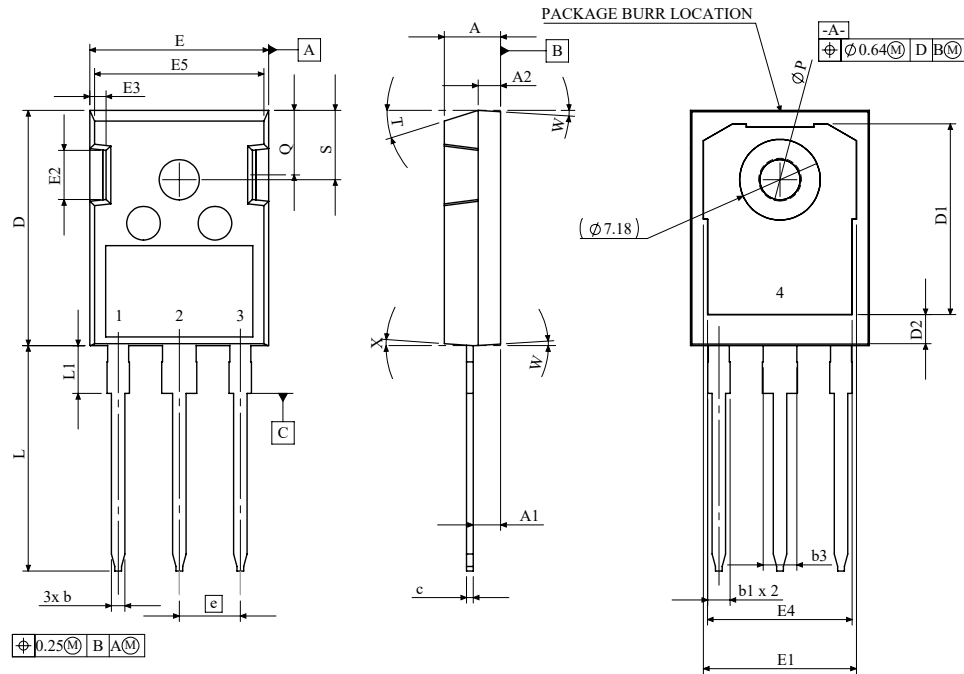


Figure 28. Body Diode Recovery Test Circuit

Package Dimensions

Package: TO-247-3



SYMBOL	MIN (mm)	MAX (mm)
A	4.83	5.21
A1	2.27	2.52
A2	1.91	2.16
b	1.07	1.33
b1	1.91	2.41
b3	2.87	3.38
c	0.55	0.74
D	20.75	21.05
D1	16	17.4
D2	2.86	3.26
E	15.75	16.13
E1	13.5	14.55
E2	3.68	5.1
E3	1	1.9
E4	12.38	13.43
E5	14.65	15.05
e	5.44 BSC	
L	19.73	20.48
L1	3.97	4.69
Ø P	3.18	4.06
Q	5.42	5.96
S	5.85	6.49
T	17.5° REF.	
W	3.5° REF.	
X	4° REF.	

1	GATE
2	DRAIN
3	SOURCE
4	DRAIN

NOTES:

1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. BURR OR MOLD FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

Recommended Solder Pad Layout

