# CC2652PSIP 具有集成式功率放大器的 SimpleLink™ 多协议 2.4GHz 无线系统级封装

## 1 特性

### 无线微控制器

- 功能强大的 48MHz Arm® Cortex®-M4F 处理器
- 352KB 闪存程序存储器
- 256KB ROM，用于协议和库函数
- 8KB 高速缓存 SRAM
- 具有奇偶校验功能的 80KB 超低泄漏 SRAM，可实现高度可靠运行
- 动态多协议管理器 (DMM) 驱动程序
- 可编程无线电包括对 2-(G)FSK、4-(G)FSK、MSK、OOK、低功耗 Bluetooth® 5.2、IEEE 802.15.4 PHY 和 MAC 的支持
- 支持无线升级 (OTA)

### 超低功耗传感器控制器

- 具有 4KB SRAM 的自主 MCU
- 采样、存储和处理传感器数据
- 快速唤醒进入低功耗运行
- 软件定义外设；电容式触控、流量计、LCD

### 低功耗

- MCU 功耗：
  - 3.5mA 有源模式，CoreMark
  - 74 µA/MHz（运行 CoreMark 时）
  - 1 µA 待机模式，RTC，80KB RAM
  - 160nA 关断模式，引脚唤醒
- 超低功耗传感器控制器功耗：
  - 2MHz 模式下为 30.1 µA
  - 24MHz 模式下为 808 µA
- 无线电功耗：
  - RX：7.3mA（在 2.4GHz 条件下）
  - TX：7.9mA（在 0dBm 条件下）
  - TX：10.9mA（在 +5dBm 条件下）
  - TX：33mA（在 +10dBm 条件下）

### 无线协议支持

- Thread、Zigbee®、Matter
- 低功耗 *Bluetooth*® 5.2
- SimpleLink™ TI 15.4-stack
- 专有系统

### 高性能无线电

- 低功耗 Bluetooth® 125kbps 时（LE 编码 PHY）敏感度为 -103dBm
- 高达 +10dBm 的输出功率，具有温度补偿

### 法规遵从性

- 经过监管认证，满足全球无线电频率要求：
  - ETSI RED（欧洲）/RER（英国）
  - ISED（加拿大）
  - FCC（美国）

### MCU 外设

- 数字外设可连接至 30 个 GPIO 中的任何一个
- 四个 32 位或八个 16 位通用计时器
- 12 位 ADC、200ksps、8 通道
- 8 位 DAC
- 两个比较器
- 可编程电流源
- 两个 UART、两个 SSI、$I^2C$、$I^2S$
- 实时时钟 (RTC)
- 集成温度和电池监控器

### 安全驱动工具

- AES 128 位和 256 位加密加速计
- ECC 和 RSA 公钥硬件加速器
- SHA2 加速器（最高到 SHA-512 的全套装）
- 真随机数发生器 (TRNG)

### 开发工具和软件

- LP-CC2652PSIP 开发套件
- SimpleLink™ CC13xx 和 CC26xx 软件开发套件 (SDK)
- 用于简单无线电配置的 SmartRF™ Studio
- 用于构建低功耗检测应用的 Sensor Controller Studio
- SysConfig 系统配置工具

### 工作温度范围

- 片上降压直流/直流转换器
- 1.8V 至 3.8V 单电源电压
- $T_j$：-40°C 至 +105°C

### 封装

- 7mm × 7mm MOT（30 个 GPIO）
- 符合 RoHS 标准的封装

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

## 2 应用

- 2400MHz 至 2480MHz ISM 和 SRD 系统 [1]
- 楼宇自动化
  - 楼宇安防系统 – 运动检测器、电子智能锁、门窗传感器、车库门系统、网关
  - HVAC – 恒温器、无线环境传感器、HVAC 系统控制器、网关
  - 防火安全系统 – 烟雾和热量探测器、火警控制面板 (FACP)
  - 升降机和自动扶梯 – 升降机和自动扶梯的电梯主控板
- 工业运输 – 资产跟踪
- 工厂自动化和控制
- 医疗
- 通信设备
  - 有线网络 – 无线 LAN 或 Wi-Fi 接入点、边缘路由器 、小型企业路由器
- 个人电子产品
  - 便携式电子产品 – 射频智能遥控器
  - 家庭影院和娱乐 – 智能扬声器、智能显示器、机顶盒
  - 游戏 – 电子玩具和机器人玩具
  - 可穿戴设备（非医用） – 智能追踪器、智能服装

## 3 说明

SimpleLink™ CC2652PSIP 是一款具有系统级封装 (SiP) 认证模块的多协议 2.4GHz 无线微控制器 (MCU)，支持以下协议：Thread、Zigbee®、低功耗 *Bluetooth*® 5.2、IEEE 802.15.4、支持 IPv6 的智能对象 (6LoWPAN) 和专有系统，包括 TI 15.4-Stack (2.4GHz) 和通过动态多协议管理器 (DMM) 驱动器实现的并发多协议。该器件经过优化，可用于楼宇安防系统、HVAC、医疗、有线网络、便携式电子产品、家庭影院和娱乐以及联网外设市场中的低功耗无线通信和高级检测。该器件的突出特性包括：

- 小型 7mm x 7mm 的系统级封装认证模块，2.4GHz，具有直流/直流元件、平衡-非平衡变压器和晶体振荡器
- SimpleLink™ CC13xx 和 CC26xx 软件开发套件 (SDK) 以灵活的方式支持各种协议栈。
- 在 +10dBm 条件下实现纽扣电池供电，发送电流消耗为 33 mA。
- 延长无线应用的电池寿命，完全 RAM 保持时低待机电流为 1µA。
- 支持工业温度，在 105ºC 下最低待机电流为 11µA。
- 通过可编程、自主式超低功耗传感器控制器 CPU 实现高级感应，具有快速唤醒功能。例如，传感器控制器能够在 1µA 系统电流下进行 1Hz ADC 采样。
- 低 SER（软错误率）FIT（时基故障），可延长运行寿命，不会对工业市场造成干扰，SRAM 奇偶校验功能始终开启，可防止潜在辐射事件导致的损坏。
- 软件控制的专用无线电控制器 (Arm® Cortex®-M0) 提供灵活的低功耗射频收发器功能，支持多个物理层和射频标准。
- 出色的无线电敏感度和稳健性（选择性与阻断）性能，适用于低功耗 *Bluetooth* ®，125kbps 时（LE 编码 PHY）为 -103dBm。

CC2652PSIP 器件是 SimpleLink™ MCU 平台的一部分，该平台包括 Wi-Fi®、低功耗*蓝牙*、Thread、Zigbee、Sub-1 GHz MCU 和主机 MCU，它们共用一个通用、易于使用的开发环境，其中包含单核软件开发套件 (SDK) 和丰富的工具集。借助一次性集成的 SimpleLink™ 平台，可以将产品组合中的任何器件组合添加至您的设计中，从而在设计要求变更时实现 100% 的代码重用。如需更多信息，请访问 SimpleLink™ MCU 平台。

**器件信息**

| 器件型号(1) | 封装 | 封装尺寸（标称值） |
|---|---|---|
| CC2652PSIPMOTR | QFM (73) | 7.00mm × 7.00mm |

(1) 如需所有可用器件的最新器件、封装和订购信息，请参阅节 13 中的“封装选项附录”或访问 TI 网站。

[1] 请参阅*射频内核*获取有关支持的协议标准、调制格式和数据速率的更多详细信息。


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# 4 Functional Block Diagram

图 4-1 shows the functional block diagram of the CC2652PSIP module.

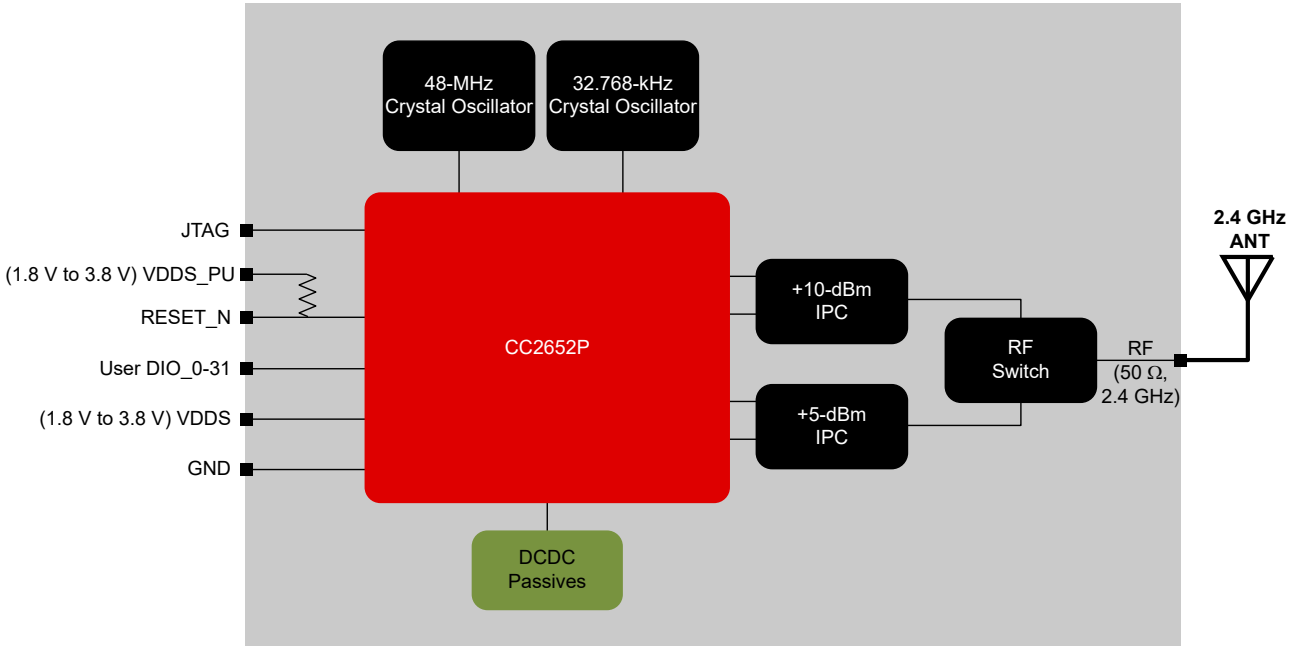



**图 4-1. CC2652PSIP Block Diagram**

图 4-2 shows an overview of the CC2652PSIP hardware.

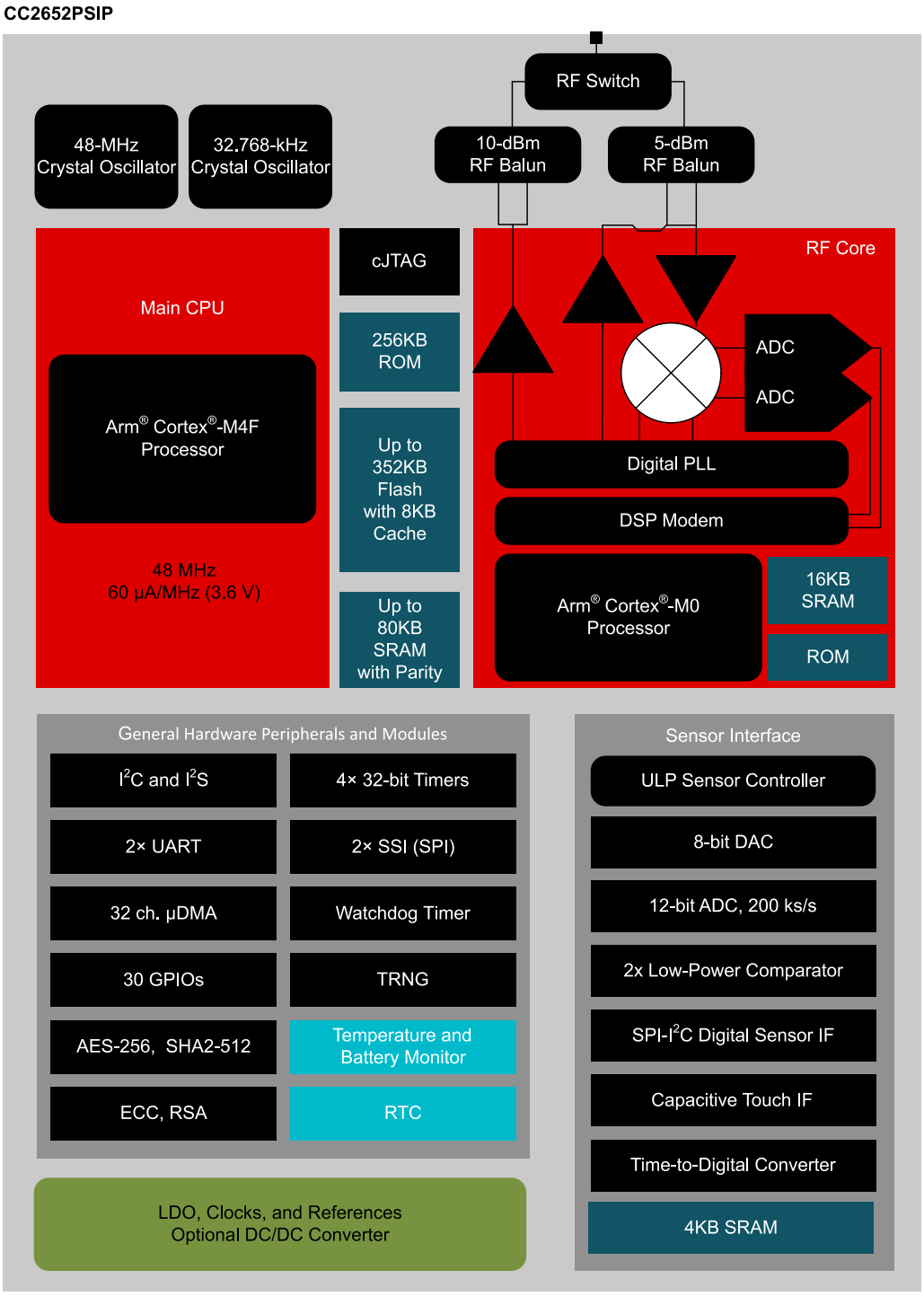



**图 4-2. CC2652PSIP Hardware Overview**


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# Table of Contents

**1 特性** ..... 1
**2 应用** ..... 2
**3 说明** ..... 2
**4 Functional Block Diagram** ..... 3
**5 Revision History** ..... 5
**6 Device Comparison** ..... 6
**7 Terminal Configuration and Functions** ..... 7
7.1 Pin Diagram ..... 7
7.2 Signal Descriptions – SIP Package ..... 8
7.3 Connections for Unused Pins and Modules ..... 9
**8 Specifications** ..... 10
8.1 Absolute Maximum Ratings ..... 10
8.2 ESD Ratings ..... 10
8.3 Recommended Operating Conditions ..... 10
8.4 Power Supply and Modules ..... 10
8.5 Power Consumption - Power Modes ..... 11
8.6 Power Consumption - Radio Modes ..... 12
8.7 Nonvolatile (Flash) Memory Characteristics ..... 12
8.8 Thermal Resistance Characteristics ..... 12
8.9 RF Frequency Bands ..... 13
8.10 Bluetooth Low Energy - Receive (RX) ..... 14
8.11 Bluetooth Low Energy - Transmit (TX) ..... 17
8.12 Zigbee and Thread - IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps) - RX ..... 18
8.13 Zigbee and Thread - IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps) - TX ..... 19
8.14 Timing and Switching Characteristics ..... 19
8.15 Peripheral Characteristics ..... 24
8.16 Typical Characteristics ..... 31
**9 Detailed Description** ..... 39
9.1 Overview ..... 39
9.2 System CPU ..... 39
9.3 Radio (RF Core) ..... 40
9.4 Memory ..... 40
9.5 Sensor Controller ..... 42
9.6 Cryptography ..... 43
9.7 Timers ..... 44
9.8 Serial Peripherals and I/O ..... 45
9.9 Battery and Temperature Monitor ..... 45
9.10 µDMA ..... 45
9.11 Debug ..... 45
9.12 Power Management ..... 46
9.13 Clock Systems ..... 47
9.14 Network Processor ..... 47
9.15 Device Certification and Qualification ..... 48
9.16 Module Markings ..... 50
9.17 End Product Labeling ..... 50
9.18 Manual Information to the End User ..... 50
**10 Application, Implementation, and Layout** ..... 51
10.1 Application Information ..... 51
10.2 Device Connection and Layout Fundamentals ..... 52
10.3 PCB Layout Guidelines ..... 52
10.4 Reference Designs ..... 56
**11 Environmental Requirements and SMT Specifications** ..... 57
11.1 PCB Bending ..... 57
11.2 Handling Environment ..... 57
11.3 Storage Condition ..... 57
11.4 PCB Assembly Guide ..... 57
11.5 Baking Conditions ..... 58
11.6 Soldering and Reflow Condition ..... 59
**12 Device and Documentation Support** ..... 60
12.1 Device Nomenclature ..... 60
12.2 Tools and Software ..... 60
12.3 Documentation Support ..... 63
12.4 支持资源 ..... 63
12.5 Trademarks ..... 63
12.6 Electrostatic Discharge Caution ..... 64
12.7 术语表 ..... 64
**13 Mechanical, Packaging, and Orderable Information** ..... 65
13.1 Packaging Information ..... 65

## 5 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision A (May 2022) to Revision B (September 2022) | Page |
|---|---|
| • 将开发套件更新为 LP-CC2652PSIP | 1 |
| • Added RER (UK) to module comparison table | 6 |
| • Corrected channel 16 to channel 26 in footnotes; 节 8.13 | 10 |
| • Updated power limits based on allowable antenna gain in footnotes; 节 8.13 | 10 |
| • List of certifications updated to include RER (UK) | 48 |
| • Updated device nomenclature figure to remove X | 60 |
| • Corrected development kit to be CC2652PSIP | 60 |

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## 6 Device Comparison

| Device | RADIO SUPPORT | | | | | | | | | | FLASH (KB) | RAM + Cache (KB) | GPIO | PACKAGE SIZE | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Sub-1 GHz Prop. | 2.4 GHz Prop. | Wireless M-Bus | Wi-SUN® | Sidewalk | *Bluetooth*® LE | ZigBee | Thread | Multiprotocol | +20 dBm PA | | | | 4 x 4 mm VQFN (32) | 5 x 5 mm VQFN (32) | 5 x 5 mm VQFN (40) | 7 x 7 mm VQFN (48) |
| CC1310 | X | | X | | | | | | | | 32-128 | 16-20 + 8 | 10-30 | X | X | | X |
| CC1311R3 | X | | X | | | | | | | | 352 | 32 + 8 | 22-30 | | | X | X |
| CC1311P3 | X | | X | | | | | | | X | 352 | 32 + 8 | 26 | | | | X |
| CC1312R | X | | X | X | | | | | | | 352 | 80 + 8 | 30 | | | | X |
| CC1312R7 | X | | X | X | X | | | | X | | 704 | 144 + 8 | 30 | | | | X |
| CC1352R | X | X | X | X | | X | X | X | X | | 352 | 80 + 8 | 28 | | | | X |
| CC1352P | X | X | X | X | | X | X | X | X | X | 352 | 80 + 8 | 26 | | | | X |
| CC1352P7 | X | X | X | X | X | X | X | X | X | X | 704 | 144 + 8 | 26 | | | | X |
| CC2640R2F | | | | | | X | | | | | 128 | 20 + 8 | 10-31 | X | X | | X |
| CC2642R | | | | | | X | | | | | 352 | 80 + 8 | 31 | | | | X |
| CC2642R-Q1 | | | | | | X | | | | | 352 | 80 + 8 | 31 | | | | X |
| CC2651R3 | | X | | | | X | X | | | | 352 | 32 + 8 | 23-31 | | | X | X |
| CC2651P3 | | X | | | | X | X | | | X | 352 | 32 + 8 | 22-26 | | | X | X |
| CC2652R | | X | | | | X | X | X | X | | 352 | 80 + 8 | 31 | | | | X |
| CC2652RB | | X | | | | X | X | X | X | | 352 | 80 + 8 | 31 | | | | X |
| CC2652R7 | | X | | | | X | X | X | X | | 704 | 144 + 8 | 31 | | | | X |
| CC2652P | | X | | | | X | X | X | X | X | 352 | 80 + 8 | 26 | | | | X |
| CC2652P7 | | X | | | | X | X | X | X | X | 704 | 144 + 8 | 26 | | | | X |

| Module | ANTENNA | | RADIO SUPPORT | | | CERTIFICATIONS | | | | FLASH (KB) | RAM + Cache (KB) | GPIO | PACKAGE SIZE | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | External | Integrated | *Bluetooth*® LE | ZigBee | +10 dBm PA | FCC/IC | CE | RER (UK) | Japan | | | | 7 x 7 QFM (73) | 7 x 7 QFM (59) | 16.9 x 11.0 QFM (29) |
| CC2650MODA | | X | X | X | | X | X | | X | 128 | 20+8 | 15 | | | X |
| CC2651R3SIPA | X | X | X | X | | X | X | X | | 352 | 32 + 8 | 32 | | X | |
| CC2652RSIP | X | | X | X | | X | X | X | | 352 | 80 + 8 | 32 | X | | |
| CC2652PSIP | X | | X | X | X | X | X | X | | 352 | 80 + 8 | 30 | X | | |


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# 7 Terminal Configuration and Functions

## 7.1 Pin Diagram

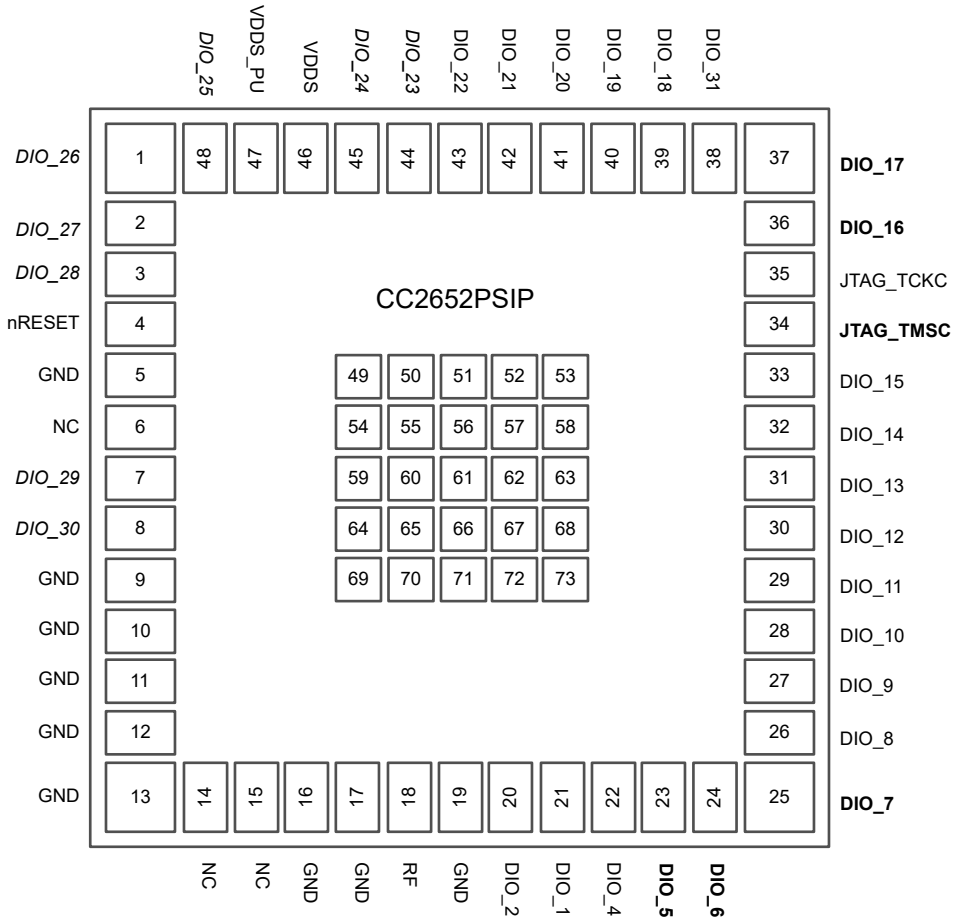



**图 7-1. MOT (7-mm × 7-mm) Pinout, 0.5-mm Pitch (Top View)**

The following I/O pins marked in 图 7-1 in **bold** have high-drive capabilities:

- Pin 23, DIO_5
- Pin 24, DIO_6
- Pin 25, DIO_7
- Pin 34, JTAG_TMSC
- Pin 36, DIO_16
- Pin 37, DIO_17

The following I/O pins marked in 图 7-1 in *italics* have analog capabilities:

- Pin 1, DIO_26
- Pin 2, DIO_27
- Pin 3, DIO_28
- Pin 7, DIO_29
- Pin 8, DIO_30
- Pin 44, DIO_23
- Pin 45, DIO_24
- Pin 48, DIO_25

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## 7.2 Signal Descriptions – SIP Package

表 7-1. Signal Descriptions – SIP Package

| PIN | | I/O | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO. | | | |
| DIO_1 | 21 | I/O | Digital | GPIO |
| DIO_10 | 28 | I/O | Digital | GPIO |
| DIO_11 | 29 | I/O | Digital | GPIO |
| DIO_12 | 30 | I/O | Digital | GPIO |
| DIO_13 | 31 | I/O | Digital | GPIO |
| DIO_14 | 32 | I/O | Digital | GPIO |
| DIO_15 | 33 | I/O | Digital | GPIO |
| DIO_16 | 36 | I/O | Digital | GPIO, JTAG_TDO, high-drive capability |
| DIO_17 | 37 | I/O | Digital | GPIO, JTAG_TDI, high-drive capability |
| DIO_18 | 39 | I/O | Digital | GPIO |
| DIO_19 | 40 | I/O | Digital | GPIO |
| DIO_2 | 20 | I/O | Digital | GPIO |
| DIO_20 | 41 | I/O | Digital | GPIO |
| DIO_21 | 42 | I/O | Digital | GPIO |
| DIO_22 | 43 | I/O | Digital | GPIO |
| DIO_23 | 44 | I/O | Digital or Analog | GPIO, analog capability |
| DIO_24 | 45 | I/O | Digital or Analog | GPIO, analog capability |
| DIO_25 | 48 | I/O | Digital or Analog | GPIO, analog capability |
| DIO_26 | 1 | I/O | Digital or Analog | GPIO, analog capability |
| DIO_27 | 2 | I/O | Digital or Analog | GPIO, analog capability |
| DIO_28 | 3 | I/O | Digital or Analog | GPIO, analog capability |
| DIO_29 | 7 | I/O | Digital or Analog | GPIO, analog capability |
| DIO_30 | 8 | I/O | Digital or Analog | GPIO, analog capability |
| DIO_31(1) | 38 | I/O | Digital | Supports only peripheral functionality. Does not support general purpose I/O functionality. |
| DIO_4 | 22 | I/O | Digital | GPIO |
| DIO_5 | 23 | I/O | Digital | GPIO, high-drive capability |
| DIO_6 | 24 | I/O | Digital | GPIO, high-drive capability |
| DIO_7 | 25 | I/O | Digital | GPIO, high-drive capability |
| DIO_8 | 26 | I/O | Digital | GPIO |
| DIO_9 | 27 | I/O | Digital | GPIO |
| GND | 5 | — | — | GND |
| GND | 9 | — | — | GND |
| GND | 10 | — | — | GND |
| GND | 11 | — | — | GND |
| GND | 12 | — | — | GND |
| GND | 13 | — | — | GND |
| GND | 16 | — | — | GND |
| GND | 17 | — | — | GND |
| GND | 19 | — | — | GND |
| GND | 49-73 | — | — | GND |
| NC | 6 | — | — | No Connect |
| NC | 14 | — | — | No Connect |


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表 7-1. Signal Descriptions – SIP Package (continued)

| PIN | | I/O | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO. | | | |
| NC | 15 | — | — | No Connect |
| nRESET | 4 | I | Digital | Reset, active low. Internal pullup resistor to VDDS_PU |
| RF | 18 | — | RF | 50 ohm RF port |
| JTAG_TCKC | 35 | I | Digital | JTAG_TCKC |
| JTAG_TMSC | 34 | I/O | Digital | JTAG_TMSC, high-drive capability |
| VDDS | 46 | — | Power | 1.8-V to 3.8-V main SIP supply |
| VDDS_PU | 47 | — | Power | Power to reset internal pullup resistor |

(1) PORT_ID = 0x00 is not supported. See the SimpleLink™ CC13x2, CC26x2 Wireless MCU Technical Reference Manual for further details.

## 7.3 Connections for Unused Pins and Modules

表 7-2. Connections for Unused Pins – SIP Package

| FUNCTION | SIGNAL NAME | PIN NUMBER | ACCEPTABLE PRACTICE(1) | PREFERRED PRACTICE(1) |
|---|---|---|---|---|
| GPIO | DIO_n | 1-3<br>7-8<br>20-33<br>36-45<br>48 | NC or GND | NC |
| No Connects | NC | 6, 14-15 | NC | NC |

(1) NC = No connect

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# 8 Specifications

## 8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| VDDS(3) | Supply voltage | | –0.3 | 4.1 | V |
| | Voltage on any digital pin(4) (5) | | –0.3 | VDDS + 0.3, max 4.1 | V |
| $V_{in}$ | Voltage on ADC input | Voltage scaling enabled | –0.3 | VDDS | V |
| | | Voltage scaling disabled, internal reference | –0.3 | 1.49 | |
| | | Voltage scaling disabled, VDDS as reference | –0.3 | VDDS / 2.9 | |
| | Input level, RF pin | | | 5 | dBm |
| $T_{stg}$ | Storage temperature | | –40 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ground, unless otherwise noted.
(3) VDDS_DCDC, VDDS2 and VDDS3 must be at the same potential as VDDS.
(4) Including analog capable DIOs.
(5) Injection current is not supported on any GPIO pin

## 8.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{ESD}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS001(1) | All pins | ±1000 | V |
| | | Charged device model (CDM), per JESD22-C101(2) | All pins | ±500 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Operating junction temperature(1) | –40 | 105 | °C |
| Operating supply voltage (VDDS) | 1.8 | 3.8 | V |
| Rising supply voltage slew rate | 0 | 100 | mV/µs |
| Falling supply voltage slew rate | 0 | 20 | mV/µs |

(1) For thermal resistance characteristics refer to Section 8.8.

## 8.4 Power Supply and Modules

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| VDDS Power-on-Reset (POR) threshold | | 1.1 | | 1.5 | V |
| VDDS Brown-out Detector (BOD) | Rising threshold | | 1.77 | | V |
| VDDS Brown-out Detector (BOD), before initial boot (1) | Rising threshold | | 1.70 | | V |
| VDDS Brown-out Detector (BOD) | Falling threshold | | 1.75 | | V |

(1) Brown-out Detector is trimmed at initial boot, value is kept until device is reset by a POR reset or the nRESET pin


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## 8.5 Power Consumption - Power Modes

When measured on the CC2652xSIP-EM reference design with $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V with DC/DC enabled unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| **Core Current Consumption** | | | | |
| $I_{core}$ | Reset and Shutdown | Reset. nRESET pin asserted or VDDS below power-on-reset threshold(1) | 30 | µA |
| | | Shutdown. No clocks running, no retention | 160 | nA |
| | Standby without cache retention | RTC running, CPU, 80KB RAM and (partial) register retention. RCOSC_LF | 0.99 | µA |
| | | RTC running, CPU, 80KB RAM and (partial) register retention XOSC_LF | 1.15 | µA |
| | Standby with cache retention | RTC running, CPU, 80KB RAM and (partial) register retention. RCOSC_LF | 3.36 | µA |
| | | RTC running, CPU, 80KB RAM and (partial) register retention. XOSC_LF | 3.47 | µA |
| | Idle | Supply Systems and RAM powered RCOSC_HF | 708 | µA |
| | Active | MCU running CoreMark at 48 MHz RCOSC_HF | 3.5 | mA |
| **Peripheral Current Consumption** | | | | |
| $I_{peri}$ | Peripheral power domain | Delta current with domain enabled | 102 | µA |
| | Serial power domain | Delta current with domain enabled | 7.56 | |
| | RF Core | Delta current with power domain enabled, clock enabled, RF core idle | 221 | |
| | µDMA | Delta current with clock enabled, module is idle | 67.1 | |
| | Timers | Delta current with clock enabled, module is idle(4) | 85.1 | |
| | I2C | Delta current with clock enabled, module is idle | 10.6 | |
| | I2S | Delta current with clock enabled, module is idle | 27.6 | |
| | SSI | Delta current with clock enabled, module is idle | 90.2 | |
| | UART | Delta current with clock enabled, module is idle(2) | 175.9 | |
| | CRYPTO (AES) | Delta current with clock enabled, module is idle(3) | 26.9 | |
| | PKA | Delta current with clock enabled, module is idle | 88.9 | |
| | TRNG | Delta current with clock enabled, module is idle | 37.4 | |
| **Sensor Controller Engine Consumption** | | | | |
| $I_{SCE}$ | Active mode | 24 MHz, infinite loop | 808 | µA |
| | Low-power mode | 2 MHz, infinite loop | 30.1 | |

(1) CC2652xSIP integrates a 100 kΩ pull-up resistor on nRESET
(2) Only one UART running
(3) Only one SSI running
(4) Only one GPTimer running

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## 8.6 Power Consumption - Radio Modes

When measured on the CC2652xSIP-EM reference design with $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V with DC/DC enabled unless otherwise noted.
High-power PA connected to $V_{DDS}$ unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| | Radio receive current | 2440 MHz | 7.3 | mA |
| | Radio transmit current<br>2.4 GHz PA (Bluetooth Low Energy) | 0 dBm output power setting<br>2440 MHz | 7.9 | mA |
| | | +5 dBm output power setting<br>2440 MHz | 10.9 | mA |
| | Radio transmit current<br>High-power PA, 10 dBm configuration | +10 dBm output power setting<br>2440 MHz VDDR = 1.67 V | 33.0 | mA |

## 8.7 Nonvolatile (Flash) Memory Characteristics

Over operating free-air temperature range and $V_{DDS}$ = 3.0 V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Flash sector size | | | 8 | | KB |
| Supported flash erase cycles before failure, full bank(1) (5) | | 30 | | | k Cycles |
| Supported flash erase cycles before failure, single sector(2) | | 60 | | | k Cycles |
| Maximum number of write operations per row before sector erase(3) | | | | 83 | Write Operations |
| Flash retention | 105 °C | 11.4 | | | Years |
| Flash sector erase current | Average delta current | | 9.7 | | mA |
| Flash sector erase time(4) | Zero cycles | | 10 | | ms |
| | 30k cycles | | | 4000 | ms |
| Flash write current | Average delta current, 4 bytes at a time | | 5.3 | | mA |
| Flash write time(4) | 4 bytes at a time | | 21.6 | | µs |

(1) A full bank erase is counted as a single erase cycle on each sector
(2) Up to 4 customer-designated sectors can be individually erased an additional 30k times beyond the baseline bank limitation of 30k cycles
(3) Each wordline is 2048 bits (or 256 bytes) wide. This limitation corresponds to sequential memory writes of 4 (3.1) bytes minimum per write over a whole wordline. If additional writes to the same wordline are required, a sector erase is required once the maximum number of write operations per row is reached.
(4) This number is dependent on Flash aging and increases over time and erase cycles
(5) Aborting flash during erase or program modes is not a safe operation.

## 8.8 Thermal Resistance Characteristics

| THERMAL METRIC(1) | | PACKAGE<br>MOT (SIP)<br>73 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 48.7 | °C/W(2) |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 12.4 | °C/W(2) |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 32.2 | °C/W(2) |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.40 | °C/W(2) |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 32.0 | °C/W(2) |

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) °C/W = degrees Celsius per watt.


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## 8.9 RF Frequency Bands

Over operating free-air temperature range (unless otherwise noted).

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Frequency bands | 2360 | | 2500 | MHz |

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## 8.10 Bluetooth Low Energy - Receive (RX)

Measured on the CC2652xSIP-EM reference design with $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, $f_{RF}$= 2440 MHz with DC/DC enabled and high power PA connected to $V_{DDS}$ unless otherwise noted.
All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **125 kbps (LE Coded)** | | | | | |
| Receiver sensitivity | Differential mode. BER = $10^{-3}$ | | –103 | | dBm |
| Receiver saturation | Differential mode. BER = $10^{-3}$ | | >5 | | dBm |
| Frequency error tolerance | Difference between the incoming carrier frequency and the internally generated carrier frequency | | > (–300 / 300) | | kHz |
| Data rate error tolerance | Difference between incoming data rate and the internally generated data rate (37-byte packets) | | > (–320 / 240) | | ppm |
| Data rate error tolerance | Difference between incoming data rate and the internally generated data rate (255-byte packets) | | > (–100 / 100) | | ppm |
| Co-channel rejection(1) | Wanted signal at –79 dBm, modulated interferer in channel, BER = $10^{-3}$ | | –1.5 | | dB |
| Selectivity, ±1 MHz(1) | Wanted signal at –79 dBm, modulated interferer at ±1 MHz, BER = $10^{-3}$ | | 8 / 4.5(2) | | dB |
| Selectivity, ±2 MHz(1) | Wanted signal at –79 dBm, modulated interferer at ±2 MHz, BER = $10^{-3}$ | | 44 / 37(2) | | dB |
| Selectivity, ±3 MHz(1) | Wanted signal at –79 dBm, modulated interferer at ±3 MHz, BER = $10^{-3}$ | | 46 / 44(2) | | dB |
| Selectivity, ±4 MHz(1) | Wanted signal at –79 dBm, modulated interferer at ±4 MHz, BER = $10^{-3}$ | | 44 / 46(2) | | dB |
| Selectivity, ±6 MHz(1) | Wanted signal at –79 dBm, modulated interferer at ±6 MHz, BER = $10^{-3}$ | | 48 / 44(2) | | dB |
| Selectivity, ±7 MHz | Wanted signal at –79 dBm, modulated interferer at ⩾ ±7 MHz, BER = $10^{-3}$ | | 51 / 45(2) | | dB |
| Selectivity, Image frequency(1) | Wanted signal at –79 dBm, modulated interferer at image frequency, BER = $10^{-3}$ | | 37 | | dB |
| Selectivity, Image frequency ±1 MHz(1) | Note that Image frequency + 1 MHz is the Co- channel – 1 MHz. Wanted signal at –79 dBm, modulated interferer at ±1 MHz from image frequency, BER = $10^{-3}$ | | 4.5 / 44 (2) | | dB |
| **500 kbps (LE Coded)** | | | | | |
| Receiver sensitivity | Differential mode. BER = $10^{-3}$ | | –98 | | dBm |
| Receiver saturation | Differential mode. BER = $10^{-3}$ | | > 5 | | dBm |
| Frequency error tolerance | Difference between the incoming carrier frequency and the internally generated carrier frequency | | > (–300 / 300) | | kHz |
| Data rate error tolerance | Difference between incoming data rate and the internally generated data rate (37-byte packets) | | > (–350 / 350) | | ppm |
| Data rate error tolerance | Difference between incoming data rate and the internally generated data rate (255-byte packets) | | > (–150 / 175) | | ppm |
| Co-channel rejection(1) | Wanted signal at –72 dBm, modulated interferer in channel, BER = $10^{-3}$ | | –3.5 | | dB |
| Selectivity, ±1 MHz(1) | Wanted signal at –72 dBm, modulated interferer at ±1 MHz, BER = $10^{-3}$ | | 8 / 4(2) | | dB |
| Selectivity, ±2 MHz(1) | Wanted signal at –72 dBm, modulated interferer at ±2 MHz, BER = $10^{-3}$ | | 43 / 35(2) | | dB |
| Selectivity, ±3 MHz(1) | Wanted signal at –72 dBm, modulated interferer at ±3 MHz, BER = $10^{-3}$ | | 46 / 46(2) | | dB |
| Selectivity, ±4 MHz(1) | Wanted signal at –72 dBm, modulated interferer at ±4 MHz, BER = $10^{-3}$ | | 45 / 47(2) | | dB |
| Selectivity, ±6 MHz(1) | Wanted signal at –72 dBm, modulated interferer at ⩾ ±6 MHz, BER = $10^{-3}$ | | 46 / 45(2) | | dB |
| Selectivity, ±7 MHz | Wanted signal at –72 dBm, modulated interferer at ⩾ ±7 MHz, BER = $10^{-3}$ | | 49 / 45(2) | | dB |


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Measured on the CC2652xSIP-EM reference design with $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, $f_{RF}$= 2440 MHz with DC/DC enabled and high power PA connected to $V_{DDS}$ unless otherwise noted.
All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Selectivity, Image frequency(1) | Wanted signal at – 72 dBm, modulated interferer at image frequency, BER = $10^{-3}$ | | 35 | | dB |
| Selectivity, Image frequency ±1 MHz(1) | Note that Image frequency + 1 MHz is the Co- channel – 1 MHz. Wanted signal at – 72 dBm, modulated interferer at ±1 MHz from image frequency, BER = $10^{-3}$ | | 4 / 46(2) | | dB |
| **1 Mbps (LE 1M)** | | | | | |
| Receiver sensitivity | Differential mode. BER = $10^{-3}$ | | – 96 | | dBm |
| Receiver saturation | Differential mode. BER = $10^{-3}$ | | > 5 | | dBm |
| Frequency error tolerance | Difference between the incoming carrier frequency and the internally generated carrier frequency | | > ( – 350 / 350) | | kHz |
| Data rate error tolerance | Difference between incoming data rate and the internally generated data rate (37-byte packets) | | > ( – 650 / 750) | | ppm |
| Co-channel rejection(1) | Wanted signal at – 67 dBm, modulated interferer in channel, BER = $10^{-3}$ | | – 6 | | dB |
| Selectivity, ±1 MHz(1) | Wanted signal at – 67 dBm, modulated interferer at ±1 MHz, BER = $10^{-3}$ | | 7 / 4(2) | | dB |
| Selectivity, ±2 MHz(1) | Wanted signal at – 67 dBm, modulated interferer at ±2 MHz,BER = $10^{-3}$ | | 39 / 33(2) | | dB |
| Selectivity, ±3 MHz(1) | Wanted signal at – 67 dBm, modulated interferer at ±3 MHz, BER = $10^{-3}$ | | 36 / 40(2) | | dB |
| Selectivity, ±4 MHz(1) | Wanted signal at – 67 dBm, modulated interferer at ±4 MHz, BER = $10^{-3}$ | | 36 / 45(2) | | dB |
| Selectivity, ±5 MHz or more(1) | Wanted signal at – 67 dBm, modulated interferer at ⩾ ±5 MHz, BER = $10^{-3}$ | | 40 | | dB |
| Selectivity, image frequency(1) | Wanted signal at – 67 dBm, modulated interferer at image frequency, BER = $10^{-3}$ | | 33 | | dB |
| Selectivity, image frequency ±1 MHz(1) | Note that Image frequency + 1 MHz is the Co- channel – 1 MHz. Wanted signal at – 67 dBm, modulated interferer at ±1 MHz from image frequency, BER = $10^{-3}$ | | 4 / 41(2) | | dB |
| Out-of-band blocking(3) | 30 MHz to 2000 MHz | | – 10 | | dBm |
| Out-of-band blocking | 2003 MHz to 2399 MHz | | – 18 | | dBm |
| Out-of-band blocking | 2484 MHz to 2997 MHz | | – 12 | | dBm |
| Out-of-band blocking | 3000 MHz to 12.75 GHz | | – 2 | | dBm |
| Intermodulation | Wanted signal at 2402 MHz, – 64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level | | – 42 | | dBm |
| Spurious emissions, 30 to 1000 MHz(4) | Measurement in a 50-Ω single-ended load. | | < – 59 | | dBm |
| Spurious emissions, 1 to 12.75 GHz(4) | Measurement in a 50-Ω single-ended load. | | < – 47 | | dBm |
| RSSI dynamic range | | | 70 | | dB |
| RSSI accuracy | | | ±4 | | dB |
| **2 Mbps (LE 2M)** | | | | | |
| Receiver sensitivity | Differential mode. Measured at SMA connector, BER = $10^{-3}$ | | – 90 | | dBm |
| Receiver saturation | Differential mode. Measured at SMA connector, BER = $10^{-3}$ | | > 5 | | dBm |
| Frequency error tolerance | Difference between the incoming carrier frequency and the internally generated carrier frequency | | > ( – 500 / 500) | | kHz |
| Data rate error tolerance | Difference between incoming data rate and the internally generated data rate (37-byte packets) | | > ( – 700 / 750) | | ppm |
| Co-channel rejection(1) | Wanted signal at – 67 dBm, modulated interferer in channel,BER = $10^{-3}$ | | – 7 | | dB |

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Measured on the CC2652xSIP-EM reference design with $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, $f_{RF}$= 2440 MHz with DC/DC enabled and high power PA connected to $V_{DDS}$ unless otherwise noted.
All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Selectivity, ±2 MHz(1) | Wanted signal at –67 dBm, modulated interferer at ±2 MHz, Image frequency is at –2 MHz, BER = $10^{-3}$ | | 8 / 4(2) | | dB |
| Selectivity, ±4 MHz(1) | Wanted signal at –67 dBm, modulated interferer at ±4 MHz, BER = $10^{-3}$ | | 36 / 34(2) | | dB |
| Selectivity, ±6 MHz(1) | Wanted signal at –67 dBm, modulated interferer at ±6 MHz, BER = $10^{-3}$ | | 37 / 36(2) | | dB |
| Selectivity, image frequency(1) | Wanted signal at –67 dBm, modulated interferer at image frequency, BER = $10^{-3}$ | | 4 | | dB |
| Selectivity, image frequency ±2 MHz(1) | Note that Image frequency + 2 MHz is the Co-channel. Wanted signal at –67 dBm, modulated interferer at ±2 MHz from image frequency, BER = $10^{-3}$ | | –7 / 36(2) | | dB |
| Out-of-band blocking(3) | 30 MHz to 2000 MHz | | –16 | | dBm |
| Out-of-band blocking | 2003 MHz to 2399 MHz | | –21 | | dBm |
| Out-of-band blocking | 2484 MHz to 2997 MHz | | –15 | | dBm |
| Out-of-band blocking | 3000 MHz to 12.75 GHz | | –12 | | dBm |
| Intermodulation | Wanted signal at 2402 MHz, –64 dBm. Two interferers at 2408 and 2414 MHz respectively, at the given power level | | –38 | | dBm |

(1) Numbers given as I/C dB
(2) X / Y, where X is +N MHz and Y is –N MHz
(3) Excluding one exception at $F_{wanted}$ / 2, per Bluetooth Specification
(4) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)


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## 8.11 Bluetooth Low Energy - Transmit (TX)

Measured on the CC2652xSIP-EM reference design with $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, $f_{RF}$= 2440 MHz with DC/DC enabled and high power PA connected to $V_{DDS}$ unless otherwise noted.
All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **General Parameters** | | | | | | |
| Max output power, high power PA, 10 dBm configuration(1) (2) | Differential mode, delivered to a single-ended 50 Ω load through a balun | | | 10.5 | | dBm |
| Output power programmable range high power PA, 10 dBm configuration | Differential mode, delivered to a single-ended 50 Ω load through a balun | | | 5 | | dB |
| Max output power, regular PA | Differential mode, delivered to a single-ended 50 Ω load through a balun | | | 5 | | dBm |
| Output power programmable range, regular PA | Differential mode, delivered to a single-ended 50 Ω load through a balun | | | 26 | | dB |
| **Spurious emissions and harmonics** | | | | | | |
| Spurious emissions, high-power PA, 10 dBm configuration(2) | f < 1 GHz, outside restricted bands | +10 dBm setting | | < -36 | | dBm |
| | f < 1 GHz, restricted bands ETSI | | | < -54 | | dBm |
| | f < 1 GHz, restricted bands FCC | | | < -55 | | dBm |
| | f > 1 GHz, including harmonics | | | -41 | | dBm |
| Harmonics, high-power PA, 10 dBm configuration(1) | Second harmonic | | | < -42 | | dBm |
| | Third harmonic | | | < -42 | | dBm |
| Spurious emissions, regular PA | f < 1 GHz, outside restricted bands | +5 dBm setting | | < –36 | | dBm |
| | f < 1 GHz, restricted bands ETSI | | | < –54 | | dBm |
| | f < 1 GHz, restricted bands FCC | | | < –55 | | dBm |
| | f > 1 GHz, including harmonics | | | < –42 | | dBm |
| Harmonics, regular PA | Second harmonic | | | < -42 | | dBm |
| | Third harmonic | | | < -42 | | dBm |

(1) To meet the FCC 15.247 Part 15 (US) harmonic requirement at full output power, the max allowable antenna gain is 1.9 dBi. Output power is limited to 9 dBm when using a max antenna gain of 3.3 dBi.
(2) To meet the ETSI EN 300 328 (Europe) 10 dBm/MHz Power Spectral Density (PSD) requirement, output power is limited to 7 dBm and 6 dBm when using a max antenna gain of 1.9 dBi and 3.3 dBi, respectively.

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## 8.12 Zigbee and Thread - IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps) - RX

Measured on the CC2652xSIP-EM reference design with $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, $f_{RF}$= 2440 MHz with DC/DC enabled and high power PA connected to $V_{DDS}$ unless otherwise noted.
All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **General Parameters** | | | | | |
| Receiver sensitivity | PER = 1% | | –98 | | dBm |
| Receiver saturation | PER = 1% | | > 5 | | dBm |
| Adjacent channel rejection | Wanted signal at –82 dBm, modulated interferer at ±5 MHz, PER = 1% | | 36 | | dB |
| Alternate channel rejection | Wanted signal at –82 dBm, modulated interferer at ±10 MHz, PER = 1% | | 57 | | dB |
| Channel rejection, ±15 MHz or more | Wanted signal at –82 dBm, undesired signal is IEEE 802.15.4 modulated channel, stepped through all channels 2405 to 2480 MHz, PER = 1% | | 59 | | dB |
| Blocking and desensitization, 5 MHz from upper band edge | Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 57 | | dB |
| Blocking and desensitization, 10 MHz from upper band edge | Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 62 | | dB |
| Blocking and desensitization, 20 MHz from upper band edge | Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 62 | | dB |
| Blocking and desensitization, 50 MHz from upper band edge | Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 65 | | dB |
| Blocking and desensitization, –5 MHz from lower band edge | Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 59 | | dB |
| Blocking and desensitization, –10 MHz from lower band edge | Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 59 | | dB |
| Blocking and desensitization, –20 MHz from lower band edge | Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 63 | | dB |
| Blocking and desensitization, –50 MHz from lower band edge | Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 65 | | dB |
| Spurious emissions, 30 MHz to 1000 MHz | Measurement in a 50-Ω single-ended load | | –66 | | dBm |
| Spurious emissions, 1 GHz to 12.75 GHz | Measurement in a 50-Ω single-ended load | | –53 | | dBm |
| Frequency error tolerance | Difference between the incoming carrier frequency and the internally generated carrier frequency | | > 350 | | ppm |
| Symbol rate error tolerance | Difference between incoming symbol rate and the internally generated symbol rate | | > 1000 | | ppm |
| RSSI dynamic range | | | 95 | | dB |
| RSSI accuracy | | | ±4 | | dB |


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## 8.13 Zigbee and Thread - IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps) - TX

Measured on the CC2652xSIP-EM reference design with $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, $f_{RF}$= 2440 MHz with DC/DC enabled and high power PA connected to $V_{DDS}$ unless otherwise noted.
All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **General Parameters** | | | | | | |
| Max output power, high power PA, 10 dBm configuration(1) (2) | Differential mode, delivered to a single-ended 50-Ω load through a balun | | | 10.0 | | dBm |
| Output power programmable range, high power PA, 10 dBm configuration | Differential mode, delivered to a single-ended 50-Ω load through a balun | | | 5 | | dB |
| Max output power, regular PA (3) | Differential mode, delivered to a single-ended 50-Ω load through a balun | | | 5 | | dBm |
| Output power programmable range, regular PA | Differential mode, delivered to a single-ended 50-Ω load through a balun | | | 26 | | dB |
| **Spurious emissions and harmonics** | | | | | | |
| Spurious emissions, high-power PA, 10 dBm configuration(1) | f < 1 GHz, outside restricted bands | +10 dBm setting | | < -36 | | dBm |
| | f < 1 GHz, restricted bands ETSI | | | < -47 | | dBm |
| | f < 1 GHz, restricted bands FCC | | | < -55 | | dBm |
| | f > 1 GHz, including harmonics | | | -42 | | dBm |
| Harmonics, high-power PA, 10 dBm configuration | Second harmonic | | | < -42 | | dBm |
| | Third harmonic | | | < -42 | | dBm |
| Spurious emissions, regular PA (3) | f < 1 GHz, outside restricted bands | +5 dBm setting | | < -36 | | dBm |
| | f < 1 GHz, restricted bands ETSI | | | < -47 | | dBm |
| | f < 1 GHz, restricted bands FCC | | | < -55 | | dBm |
| | f > 1 GHz, including harmonics | | | < –42 | | dBm |
| Harmonics, regular PA (3) | Second harmonic | | | < -42 | | dBm |
| | Third harmonic | | | < -42 | | dBm |
| **IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps)** | | | | | | |
| Error vector magnitude, high power PA, 10 dBm configuration | +10 dBm setting | | | 2 | | % |
| Error vector magnitude, Regular PA | +5 dBm setting | | | 2 | | % |

(1) For FCC 15.247 Part 15 (US) Channel 26 is disabled and not available for use.
(2) To meet the ETSI EN 300 328 (Europe) 10 dBm/MHz Power Spectral Density (PSD) requirement, output power is limited to 7 dBm and 6 dBm when using a max antenna gain of 1.9 dBi and 3.3 dBi, respectively.
(3) To meet the FCC 15.247 Part 15 (US) Band Edge requirement, Channel 26 output power is limited to 2 dBm and 0 dBm when using a max antenna gain of 3.3 dBi and 5.3 dBi, respectively.

## 8.14 Timing and Switching Characteristics

### 8.14.1 Reset Timing

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| nRESET low duration | 1 | | | µs |

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### 8.14.2 Wakeup Timing

Measured over operating free-air temperature with $V_{DDS}$ = 3.0 V (unless otherwise noted). The times listed here do not include software overhead.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| MCU, Reset to Active(1) | | | 850 - 4000 | | µs |
| MCU, Shutdown to Active(1) | | | 850 - 4000 | | µs |
| MCU, Standby to Active | | | 165 | | µs |
| MCU, Active to Standby | | | 36 | | µs |
| MCU, Idle to Active | | | 14 | | µs |

(1) The wakeup time is dependent on remaining charge on VDDR capacitor when starting the device, and thus how long the device has been in Reset or Shutdown before starting up again.

### 8.14.3 Clock Specifications

#### *8.14.3.1 48 MHz Crystal Oscillator (XOSC_HF)*

Measured on a CC2652xSIP-EM reference design with integrated 48 MHz crystal including parameters based on external manufacturer's crystal specification at $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V at initial time, unless otherwise noted.

| | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Crystal frequency | | 48 | | MHz |
| Start-up time(1) | | 200 | | µs |
| Initial crystal frequency tolerance(2) | -16 | | 18 | ppm |
| Crystal aging at 10 years(2) | -4 | | 2 | ppm/year |

(1) Start-up time using the TI-provided power driver. Start-up time may increase if driver is not used.
(2) External manufacturer's crystal specification

#### *8.14.3.2 48 MHz RC Oscillator (RCOSC_HF)*

Measured on a CC2652xSIP-EM reference design with $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Frequency | | 48 | | MHz |
| Uncalibrated frequency accuracy | | ±1 | | % |
| Calibrated frequency accuracy(1) | | ±0.25 | | % |
| Start-up time | | 5 | | µs |

(1) Accuracy relative to the calibration source (XOSC_HF)

#### *8.14.3.3 2 MHz RC Oscillator (RCOSC_MF)*

Measured on a CC2652xSIP-EM reference design with $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Calibrated frequency | | 2 | | MHz |
| Start-up time | | 5 | | µs |

#### *8.14.3.4 32.768 kHz Crystal Oscillator (XOSC_LF)*

Measured on a CC2652xSIP-EM reference design with integrated 32.768 kHz crystal including parameters based on external manufacturer's crystal specification at $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V at initial time, unless otherwise noted.

| | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Crystal frequency | | 32.768 | | kHz |
| Initial crystal frequency tolerance(1) | -20 | | 20 | ppm |
| Crystal aging at 1st year(1) | -3 | | 3 | ppm/year |

(1) External manufacturer's crystal specification


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#### *8.14.3.5 32 kHz RC Oscillator (RCOSC_LF)*

Measured on a CC2652xSIP-EM reference design with $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Calibrated frequency | | 32.8 (1) | | kHz |
| Temperature coefficient. | | 50 | | ppm/°C |

(1) When using RCOSC_LF as source for the low frequency system clock (SCLK_LF), the accuracy of the SCLK_LF-derived Real Time Clock (RTC) can be improved by measuring RCOSC_LF relative to XOSC_HF and compensating for the RTC tick speed. This functionality is available through the TI-provided Power driver.

### 8.14.4 Synchronous Serial Interface (SSI) Characteristics

#### *8.14.4.1 Synchronous Serial Interface (SSI) Characteristics*

over operating free-air temperature range (unless otherwise noted)

| PARAMETER NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| S1 | $t_{clk_per}$ | SSIClk cycle time | 12 | | 65024 | System Clocks (2) |
| S2(1) | $t_{clk_high}$ | SSIClk high time | | 0.5 | | $t_{clk_per}$ |
| S3(1) | $t_{clk_low}$ | SSIClk low time | | 0.5 | | $t_{clk_per}$ |

(1) Refer to SSI timing diagrams Figure 8-1, Figure 8-2, and Figure 8-3.
(2) When using the TI-provided Power driver, the SSI system clock is always 48 MHz.

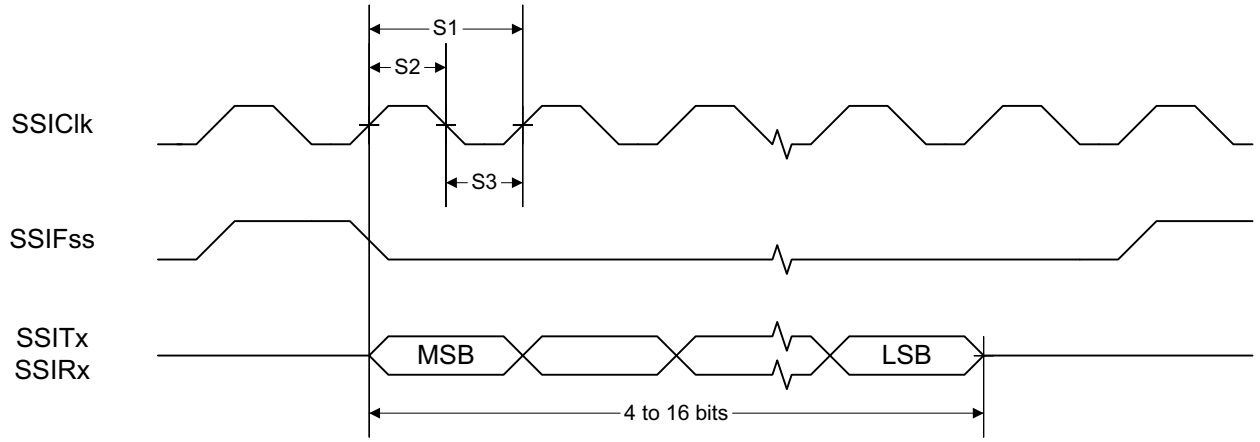



**图 8-1. SSI Timing for TI Frame Format (FRF = 01), Single Transfer Timing Measurement**

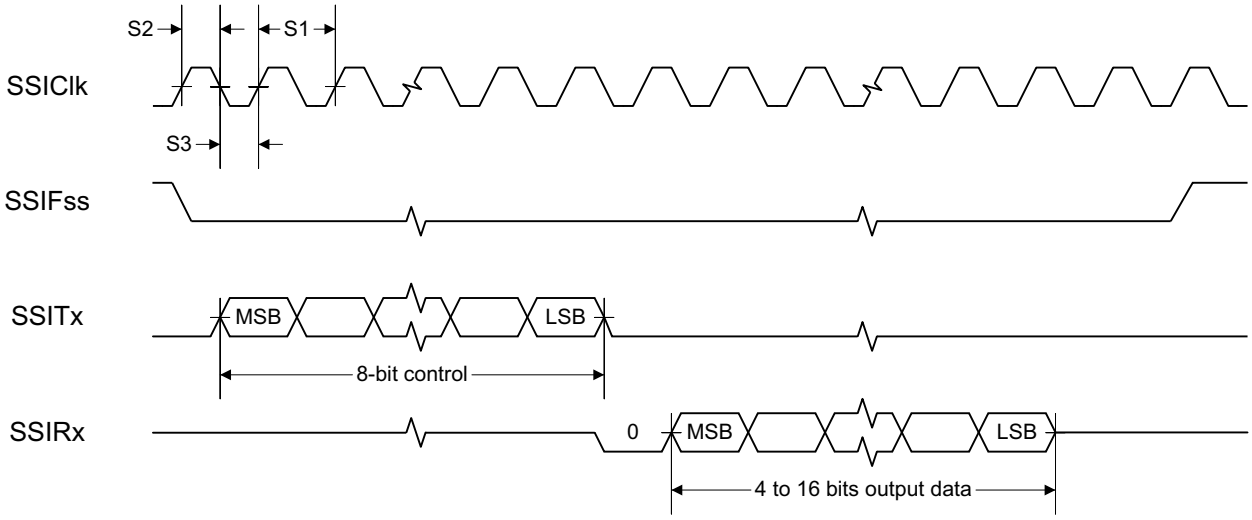



**图 8-2. SSI Timing for MICROWIRE Frame Format (FRF = 10), Single Transfer**

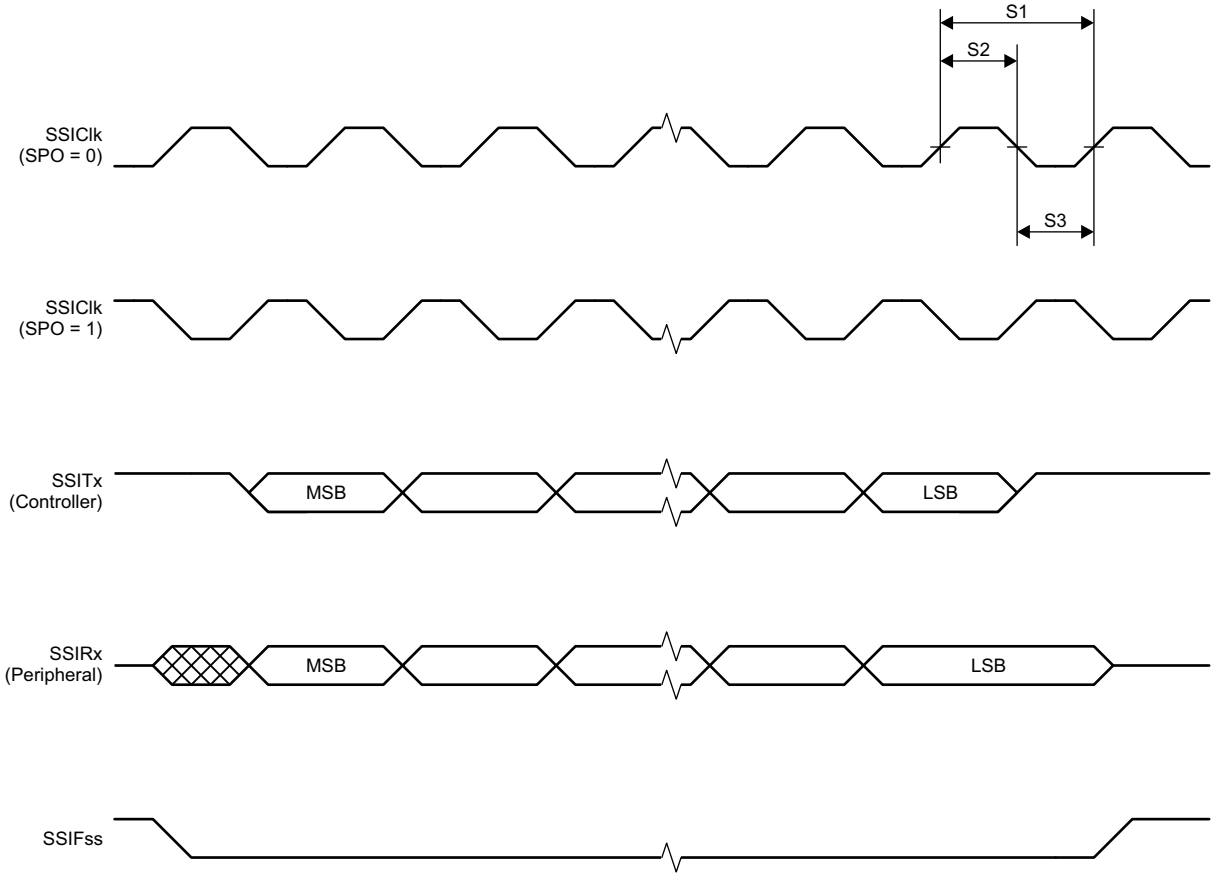



**图 8-3. SSI Timing for SPI Frame Format (FRF = 00), With SPH = 1**


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### 8.14.5 UART

**表 8-1. UART Characteristics**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| UART rate | | | 3 | MBaud |

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## 8.15 Peripheral Characteristics

### 8.15.1 ADC

#### *Analog-to-Digital Converter (ADC) Characteristics*

$T_c$ = 25 °C, $V_{DDS}$ = 3.0 V and voltage scaling enabled, unless otherwise noted.(1)
Performance numbers require use of offset and gain adjustements in software by TI-provided ADC drivers.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Input voltage range | | 0 | | VDDS | V |
| | Resolution | | | 12 | | Bits |
| | Sample Rate | | | | 200 | ksps |
| | Offset | Internal 4.3 V equivalent reference(2) | | –0.24 | | LSB |
| | Gain error | Internal 4.3 V equivalent reference(2) | | 7.14 | | LSB |
| DNL(4) | Differential nonlinearity | | | >–1 | | LSB |
| INL | Integral nonlinearity | | | ±4 | | LSB |
| ENOB | Effective number of bits | Internal 4.3 V equivalent reference(2), 200 kSamples/s, 9.6 kHz input tone | | 9.8 | | Bits |
| | | Internal 4.3 V equivalent reference(2), 200 kSamples/s, 9.6 kHz input tone, DC/DC enabled | | 9.8 | | |
| | | VDDS as reference, 200 kSamples/s, 9.6 kHz input tone | | 10.1 | | |
| | | Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone | | 11.1 | | |
| | | Internal reference, voltage scaling disabled, 14-bit mode, 200 kSamples/s, 600 Hz input tone (5) | | 11.3 | | |
| | | Internal reference, voltage scaling disabled, 15-bit mode, 200 kSamples/s, 150 Hz input tone (5) | | 11.6 | | |
| THD | Total harmonic distortion | Internal 4.3 V equivalent reference(2), 200 kSamples/s, 9.6 kHz input tone | | –65 | | dB |
| | | VDDS as reference, 200 kSamples/s, 9.6 kHz input tone | | –70 | | |
| | | Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone | | –72 | | |
| SINAD, SNDR | Signal-to-noise and distortion ratio | Internal 4.3 V equivalent reference(2), 200 kSamples/s, 9.6 kHz input tone | | 60 | | dB |
| | | VDDS as reference, 200 kSamples/s, 9.6 kHz input tone | | 63 | | |
| | | Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone | | 68 | | |
| SFDR | Spurious-free dynamic range | Internal 4.3 V equivalent reference(2), 200 kSamples/s, 9.6 kHz input tone | | 70 | | dB |
| | | VDDS as reference, 200 kSamples/s, 9.6 kHz input tone | | 73 | | |
| | | Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone | | 75 | | |
| | Conversion time | Serial conversion, time-to-output, 24 MHz clock | | 50 | | Clock Cycles |
| | Current consumption | Internal 4.3 V equivalent reference(2) | | 0.42 | | mA |
| | Current consumption | VDDS as reference | | 0.6 | | mA |
| | Reference voltage | Equivalent fixed internal reference (input voltage scaling enabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1 | | 4.3(2) (3) | | V |
| | Reference voltage | Fixed internal reference (input voltage scaling disabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1. This value is derived from the scaled value (4.3 V) as follows: $V_{ref}$ = 4.3 V × 1408 / 4095 | | 1.48 | | V |
| | Reference voltage | VDDS as reference, input voltage scaling enabled | | VDDS | | V |
| | Reference voltage | VDDS as reference, input voltage scaling disabled | | VDDS / 2.82(3) | | V |


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$T_c$ = 25 °C, $V_{DDS}$ = 3.0 V and voltage scaling enabled, unless otherwise noted.(1)
Performance numbers require use of offset and gain adjustements in software by TI-provided ADC drivers.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Input impedance | 200 kSamples/s, voltage scaling enabled. Capacitive input, Input impedance depends on sampling frequency and sampling time | | >1 | | MΩ |

(1) Using IEEE Std 1241-2010 for terminology and test methods
(2) Input signal scaled down internally before conversion, as if voltage range was 0 to 4.3 V
(3) Applied voltage must be within Absolute Maximum Ratings (see Section 8.1 ) at all times
(4) No missing codes
(5) ADC_output = Σ(4^n samples ) >> n, n = desired extra bits

## 8.15.2 DAC

### *8.15.2.1 Digital-to-Analog Converter (DAC) Characteristics*

$T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **General Parameters** | | | | | | |
| | Resolution | | | 8 | | Bits |
| $V_{DDS}$ | Supply voltage | Any load, any $V_{REF}$, pre-charge OFF, DAC charge-pump ON | 1.8 | | 3.8 | V |
| | | External Load(4), any $V_{REF}$, pre-charge OFF, DAC charge-pump OFF | 2.0 | | 3.8 | |
| | | Any load, $V_{REF}$ = DCOUPL, pre-charge ON | 2.6 | | 3.8 | |
| $F_{DAC}$ | Clock frequency | Buffer ON (recommended for external load) | 16 | | 250 | kHz |
| | | Buffer OFF (internal load) | 16 | | 1000 | |
| | Voltage output settling time | $V_{REF}$ = VDDS, buffer OFF, internal load | | 13 | | 1 / $F_{DAC}$ |
| | | $V_{REF}$ = VDDS, buffer ON, external capacitive load = 20 pF(3) | | 13.8 | | |
| | External capacitive load | | | 20 | 200 | pF |
| | External resistive load | | 10 | | | MΩ |
| | Short circuit current | | | | 400 | µA |
| $Z_{MAX}$ | Max output impedance Vref = VDDS, buffer ON, CLK 250 kHz | VDDS = 3.8 V, DAC charge-pump OFF | | 51.1 | | kΩ |
| | | VDDS = 3.0 V, DAC charge-pump ON | | 53.1 | | |
| | | VDDS = 3.0 V, DAC charge-pump OFF | | 54.3 | | |
| | | VDDS = 2.0 V, DAC charge-pump ON | | 48.7 | | |
| | | VDDS = 2.0 V, DAC charge-pump OFF | | 70.2 | | |
| | | VDDS = 1.8 V, DAC charge-pump ON | | 49.4 | | |
| | | VDDS = 1.8 V, DAC charge-pump OFF | | 79.2 | | |
| **Internal Load - Continuous Time Comparator / Low Power Clocked Comparator** | | | | | | |
| DNL | Differential nonlinearity | $V_{REF}$ = VDDS, load = Continuous Time Comparator or Low Power Clocked Comparator $F_{DAC}$ = 250 kHz | | ±1 | | LSB(1) |
| | Differential nonlinearity | $V_{REF}$ = VDDS, load = Continuous Time Comparator or Low Power Clocked Comparator $F_{DAC}$ = 16 kHz | | ±1.2 | | |
| | Offset error(2) Load = Continuous Time Comparator | $V_{REF}$ = VDDS = 3.8 V | | ±0.64 | | LSB(1) |
| | | $V_{REF}$ = VDDS= 3.0 V | | ±0.81 | | |
| | | $V_{REF}$ = VDDS = 1.8 V | | ±1.27 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge ON | | ±3.43 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge OFF | | ±2.88 | | |
| | | $V_{REF}$ = ADCREF | | ±2.37 | | |

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$T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Offset error(2) Load = Low Power Clocked Comparator | $V_{REF}$ = VDDS= 3.8 V | | ±0.78 | | LSB(1) |
| | | $V_{REF}$ = VDDS = 3.0 V | | ±0.77 | | |
| | | $V_{REF}$ = VDDS= 1.8 V | | ±3.46 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge ON | | ±3.44 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge OFF | | ±4.70 | | |
| | | $V_{REF}$ = ADCREF | | ±4.11 | | |
| | Max code output voltage variation(2) Load = Continuous Time Comparator | $V_{REF}$ = VDDS = 3.8 V | | ±1.53 | | LSB(1) |
| | | $V_{REF}$ = VDDS = 3.0 V | | ±1.71 | | |
| | | $V_{REF}$ = VDDS= 1.8 V | | ±2.10 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge ON | | ±6.00 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge OFF | | ±3.85 | | |
| | | $V_{REF}$ = ADCREF | | ±5.84 | | |
| | Max code output voltage variation(2) Load = Low Power Clocked Comparator | $V_{REF}$ = VDDS= 3.8 V | | ±2.92 | | LSB(1) |
| | | $V_{REF}$ =VDDS= 3.0 V | | ±3.06 | | |
| | | $V_{REF}$ = VDDS= 1.8 V | | ±3.91 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge ON | | ±7.84 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge OFF | | ±4.06 | | |
| | | $V_{REF}$ = ADCREF | | ±6.94 | | |
| | Output voltage range(2) Load = Continuous Time Comparator | $V_{REF}$ = VDDS = 3.8 V, code 1 | | 0.03 | | V |
| | | $V_{REF}$ = VDDS = 3.8 V, code 255 | | 3.62 | | |
| | | $V_{REF}$ = VDDS= 3.0 V, code 1 | | 0.02 | | |
| | | $V_{REF}$ = VDDS= 3.0 V, code 255 | | 2.86 | | |
| | | $V_{REF}$ = VDDS= 1.8 V, code 1 | | 0.01 | | |
| | | $V_{REF}$ = VDDS = 1.8 V, code 255 | | 1.71 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge OFF, code 1 | | 0.01 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge OFF, code 255 | | 1.21 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge ON, code 1 | | 1.27 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge ON, code 255 | | 2.46 | | |
| | | $V_{REF}$ = ADCREF, code 1 | | 0.01 | | |
| | | $V_{REF}$ = ADCREF, code 255 | | 1.41 | | |
| | Output voltage range(2) Load = Low Power Clocked Comparator | $V_{REF}$ = VDDS = 3.8 V, code 1 | | 0.03 | | V |
| | | $V_{REF}$ = VDDS= 3.8 V, code 255 | | 3.61 | | |
| | | $V_{REF}$ = VDDS= 3.0 V, code 1 | | 0.02 | | |
| | | $V_{REF}$ = VDDS= 3.0 V, code 255 | | 2.85 | | |
| | | $V_{REF}$ = VDDS = 1.8 V, code 1 | | 0.01 | | |
| | | $V_{REF}$ = VDDS = 1.8 V, code 255 | | 1.71 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge OFF, code 1 | | 0.01 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge OFF, code 255 | | 1.21 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge ON, code 1 | | 1.27 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge ON, code 255 | | 2.46 | | |
| | | $V_{REF}$ = ADCREF, code 1 | | 0.01 | | |
| | | $V_{REF}$ = ADCREF, code 255 | | 1.41 | | |
| **External Load** | | | | | | |
| INL | Integral nonlinearity | $V_{REF}$ = VDDS, $F_{DAC}$ = 250 kHz | | ±1 | | LSB(1) |
| | | $V_{REF}$ = DCOUPL, $F_{DAC}$ = 250 kHz | | ±1 | | |
| | | $V_{REF}$ = ADCREF, $F_{DAC}$ = 250 kHz | | ±1 | | |
| DNL | Differential nonlinearity | $V_{REF}$ = VDDS, $F_{DAC}$ = 250 kHz | | ±1 | | LSB(1) |


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$T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Offset error | $V_{REF}$ = VDDS= 3.8 V | | ±0.35 | | LSB(1) |
| | | $V_{REF}$ = VDDS= 3.0 V | | ±0.50 | | |
| | | $V_{REF}$ = VDDS = 1.8 V | | ±0.75 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge ON | | ±1.55 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge OFF | | ±1.30 | | |
| | | $V_{REF}$ = ADCREF | | ±1.10 | | |
| | Max code output voltage variation | $V_{REF}$ = VDDS= 3.8 V | | ±1.00 | | LSB(1) |
| | | $V_{REF}$ = VDDS= 3.0 V | | ±1.00 | | |
| | | $V_{REF}$ = VDDS= 1.8 V | | ±1.00 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge ON | | ±3.45 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge OFF | | ±2.10 | | |
| | | $V_{REF}$ = ADCREF | | ±1.90 | | |
| | Output voltage range Load = Low Power Clocked Comparator | $V_{REF}$ = VDDS = 3.8 V, code 1 | | 0.03 | | V |
| | | $V_{REF}$ = VDDS = 3.8 V, code 255 | | 3.59 | | |
| | | $V_{REF}$ = VDDS = 3.0 V, code 1 | | 0.02 | | |
| | | $V_{REF}$ = VDDS= 3.0 V, code 255 | | 2.82 | | |
| | | $V_{REF}$ = VDDS= 1.8 V, code 1 | | 0.01 | | |
| | | $V_{REF}$ = VDDS = 1.8 V, code 255 | | 1.70 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge OFF, code 1 | | 0.01 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge OFF, code 255 | | 1.21 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge ON, code 1 | | 1.27 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge ON, code 255 | | 2.46 | | |
| | | $V_{REF}$ = ADCREF, code 1 | | 0.01 | | |
| | | $V_{REF}$ = ADCREF, code 255 | | 1.42 | | |

(1) 1 LSB ($V_{REF}$ 3.8 V/3.0 V/1.8 V/DCOUPL/ADCREF) = 14.10 mV/11.13 mV/6.68 mV/4.67 mV/5.48 mV
(2) Includes comparator offset
(3) A load > 20 pF will increases the settling time
(4) Keysight 34401A Multimeter

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## 8.15.3 Temperature and Battery Monitor

### *8.15.3.1 Temperature Sensor*

Measured on a Texas Instruments reference design with $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Resolution | | | 2 | | °C |
| Accuracy | -40 °C to 0 °C | | ±4.0 | | °C |
| Accuracy | 0 °C to 105 °C | | ±2.5 | | °C |
| Supply voltage coefficient(1) | | | 3.6 | | °C/V |

(1) The temperature sensor is automatically compensated for VDDS variation when using the TI-provided driver.

### *8.15.3.2 Battery Monitor*

Measured on a Texas Instruments reference design with $T_c$ = 25 °C, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Resolution | | | 25 | | mV |
| Range | | 1.8 | | 3.8 | V |
| Integral nonlinearity (max) | | | 23 | | mV |
| Accuracy | VDDS = 3.0 V | | 22.5 | | mV |
| Offset error | | | -32 | | mV |
| Gain error | | | -1 | | % |


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## 8.15.4 Comparators

### 8.15.4.1 Low-Power Clocked Comparator

$T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Input voltage range | | 0 | | $V_{DDS}$ | V |
| Clock frequency | | | SCLK_LF | | |
| Internal reference voltage(1) | Using internal DAC with VDDS as reference voltage, DAC code = 0 - 255 | | 0.024 - 2.865 | | V |
| Offset | Measured at $V_{DDS}$ / 2, includes error from internal DAC | | ±5 | | mV |
| Decision time | Step from – 50 mV to 50 mV | | 1 | | Clock Cycle |

(1) The comparator can use an internal 8 bits DAC as its reference. The DAC output voltage range depends on the reference voltage selected. See Section 8.15.2.1

### 8.15.4.2 Continuous Time Comparator

$T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Input voltage range(1) | | 0 | | $V_{DDS}$ | V |
| Offset | Measured at $V_{DDS}$ / 2 | | ±5 | | mV |
| Decision time | Step from – 10 mV to 10 mV | | 0.78 | | µs |
| Current consumption | Internal reference | | 8.6 | | µA |

(1) The input voltages can be generated externally and connected throughout I/Os or an internal reference voltage can be generated using the DAC

## 8.15.5 Current Source

### 8.15.5.1 Programmable Current Source

$T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Current source programmable output range (logarithmic range) | | | 0.25 - 20 | | µA |
| Resolution | | | 0.25 | | µA |

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## 8.15.6 GPIO

### *8.15.6.1 GPIO DC Characteristics*

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **$T_A$ = 25 °C, $V_{DDS}$ = 1.8 V** | | | | | |
| GPIO VOH at 8 mA load | IOCURR = 2, high-drive GPIOs only | | 1.56 | | V |
| GPIO VOL at 8 mA load | IOCURR = 2, high-drive GPIOs only | | 0.24 | | V |
| GPIO VOH at 4 mA load | IOCURR = 1 | | 1.59 | | V |
| GPIO VOL at 4 mA load | IOCURR = 1 | | 0.21 | | V |
| GPIO pullup current | Input mode, pullup enabled, Vpad = 0 V | | 73 | | µA |
| GPIO pulldown current | Input mode, pulldown enabled, Vpad = VDDS | | 19 | | µA |
| GPIO low-to-high input transition, with hysteresis | IH = 1, transition voltage for input read as 0 → 1 | | 1.08 | | V |
| GPIO high-to-low input transition, with hysteresis | IH = 1, transition voltage for input read as 1 → 0 | | 0.73 | | V |
| GPIO input hysteresis | IH = 1, difference between 0 → 1 and 1 → 0 points | | 0.35 | | V |
| **$T_A$ = 25 °C, $V_{DDS}$ = 3.0 V** | | | | | |
| GPIO VOH at 8 mA load | IOCURR = 2, high-drive GPIOs only | | 2.59 | | V |
| GPIO VOL at 8 mA load | IOCURR = 2, high-drive GPIOs only | | 0.42 | | V |
| GPIO VOH at 4 mA load | IOCURR = 1 | | 2.63 | | V |
| GPIO VOL at 4 mA load | IOCURR = 1 | | 0.40 | | V |
| **$T_A$ = 25 °C, $V_{DDS}$ = 3.8 V** | | | | | |
| GPIO pullup current | Input mode, pullup enabled, Vpad = 0 V | | 282 | | µA |
| GPIO pulldown current | Input mode, pulldown enabled, Vpad = VDDS | | 110 | | µA |
| GPIO low-to-high input transition, with hysteresis | IH = 1, transition voltage for input read as 0 → 1 | | 1.97 | | V |
| GPIO high-to-low input transition, with hysteresis | IH = 1, transition voltage for input read as 1 → 0 | | 1.55 | | V |
| GPIO input hysteresis | IH = 1, difference between 0 → 1 and 1 → 0 points | | 0.42 | | V |
| **$T_A$ = 25 °C** | | | | | |
| VIH | Lowest GPIO input voltage reliably interpreted as a *High* | $0.8*V_{DDS}$ | | | V |
| VIL | Highest GPIO input voltage reliably interpreted as a *Low* | | | $0.2*V_{DDS}$ | V |


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## 8.16 Typical Characteristics

All measurements in this section are done with $T_c$ = 25 °C and $V_{DDS}$ = 3.0 V, unless otherwise noted. See *Recommended Operating Conditions* for device limits. Values exceeding these limits are for reference only.

### 8.16.1 MCU Current

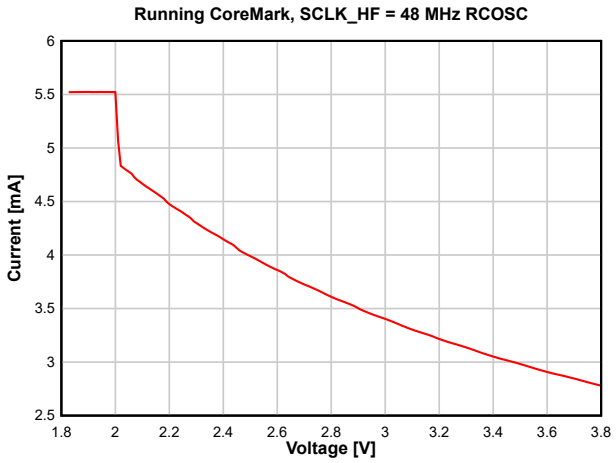



图 8-4. Active Mode (MCU) Current vs. Supply Voltage (VDDS)

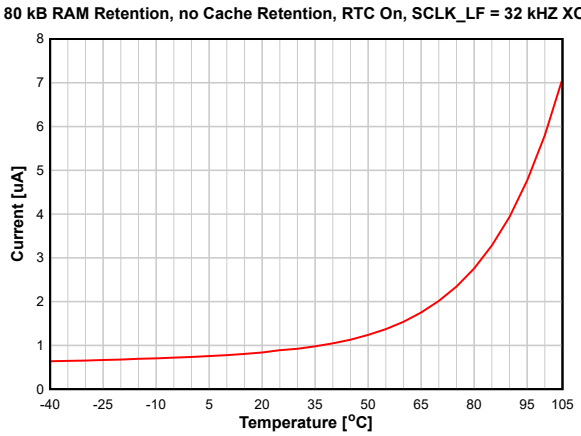



图 8-5. Standby Mode (MCU) Current vs. Temperature

### 8.16.2 RX Current

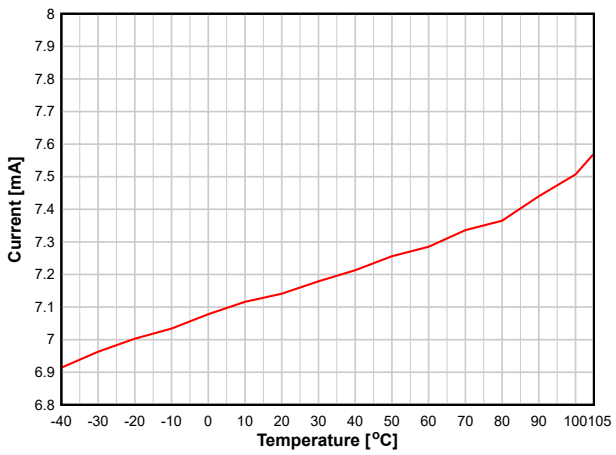



图 8-6. RX Current vs. Temperature (BLE 1 Mbps, 2.44 GHz)

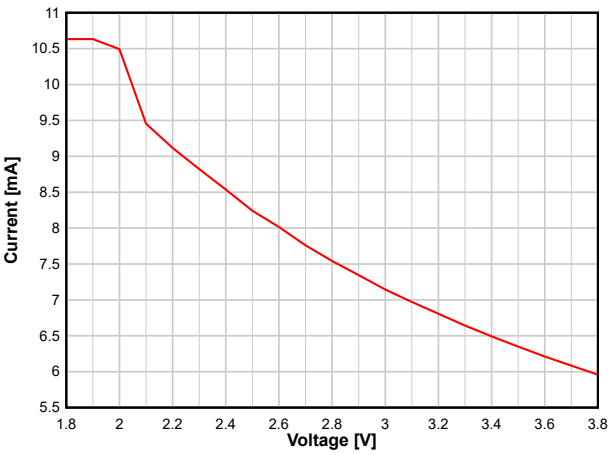



图 8-7. RX Current vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz)

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### 8.16.3 TX Current

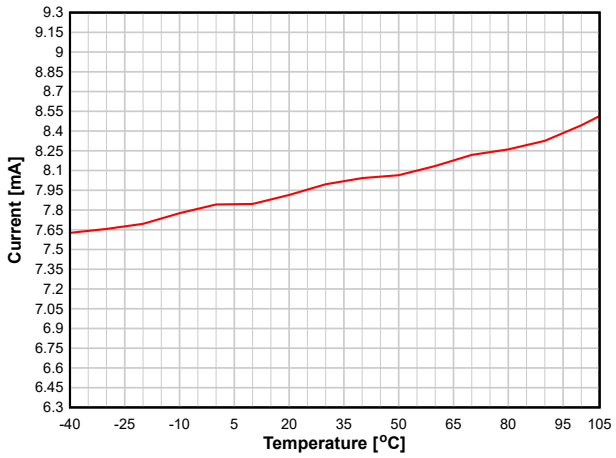



图 8-8. TX Current vs. Temperature (BLE 1 Mbps, 2.44 GHz, 0 dBm)

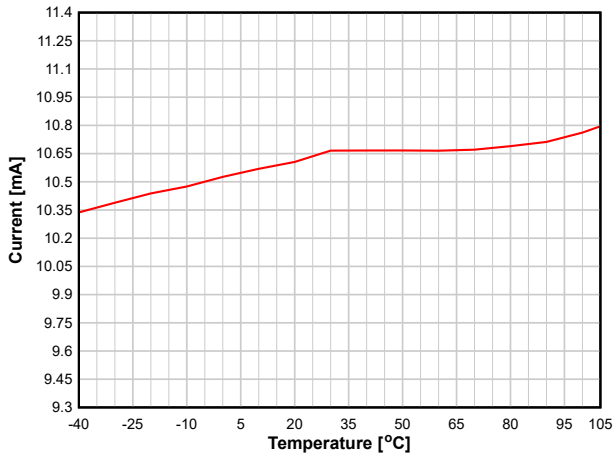



图 8-9. TX Current vs. Temperature (BLE 1 Mbps, 2.44 GHz, +5 dBm)

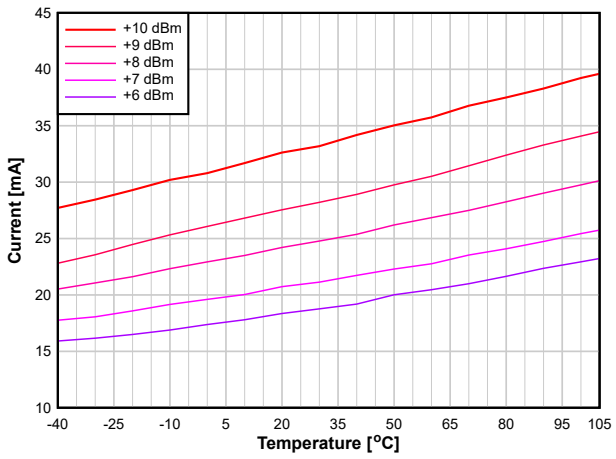



图 8-10. TX Current vs. Temperature (BLE 1 Mbps, 2.44 GHz, +10 dBm)

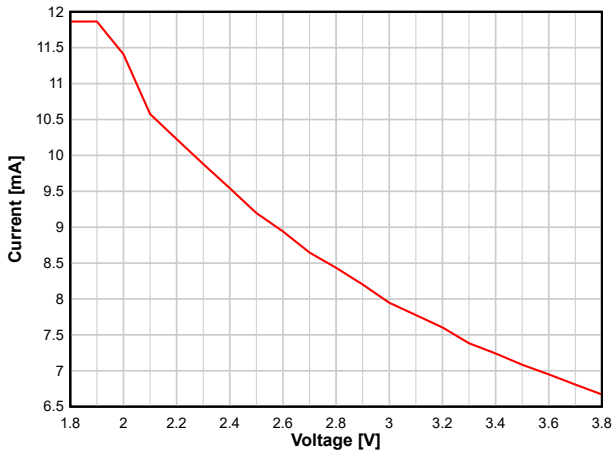



图 8-11. TX Current vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz, 0 dBm)

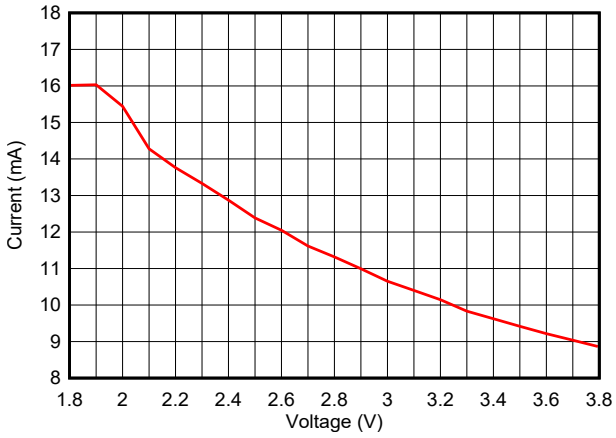



图 8-12. TX Current vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz, +5 dBm)

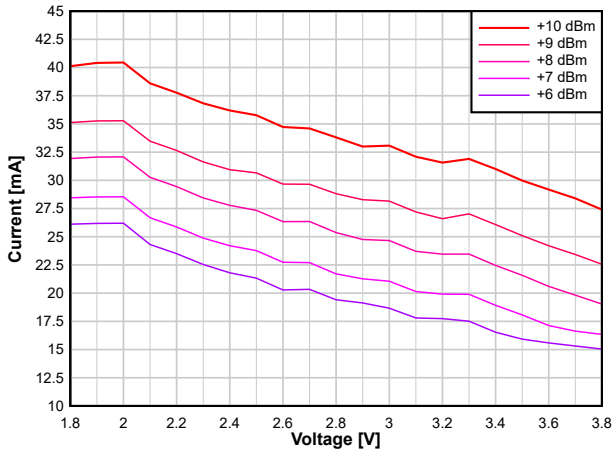



图 8-13. TX Current vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz, +10 dBm PA)

shows typical TX current and output power for different output power settings.


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表 8-2. Typical TX Current and Output Power

| CC2652PSIP at 2.44 GHz, VDDS = 3.0 V (Measured on CC2652XSIP_EM) | | | |
|---|---|---|---|
| **txPower** | **TX Power Setting (SmartRF Studio)** | **Typical Output Power [dBm]** | **Typical Current Consumption [mA]** |
| 0x0014475E | 10 | 9.80 | 33.06 |
| 0x00143957 | 9 | 9.05 | 28.08 |
| 0x0014592A | 8 | 8.31 | 24.67 |
| 0x00144723 | 7 | 7.34 | 21.09 |
| 0x00104120 | 6 | 6.51 | 18.67 |

表 8-3. Typical TX Current and Output Power

| CC2652PSIP at 2.44 GHz, VDDS = 3.0 V (Measured on CC2652XSIP_EM) | | | |
|---|---|---|---|
| **txPower** | **TX Power Setting (SmartRF Studio)** | **Typical Output Power [dBm]** | **Typical Current Consumption [mA]** |
| 0x6C3E | 5 | 4.27 | 10.67 |
| 0x8A2A | 4 | 3.70 | 10.04 |
| 0x581B | 3 | 2.72 | 9.28 |
| 0x3863 | 2 | 1.68 | 8.80 |
| 0x26A3 | 1 | 0.71 | 8.38 |
| 0x269E | 0 | -0.28 | 7.96 |
| 0x26E0 | -3 | -3.04 | 7.19 |
| 0x0ED8 | -5 | -5.10 | 6.65 |
| 0x08E5 | -6 | -6.32 | 6.41 |
| 0x08D0 | -9 | -9.28 | 5.94 |
| 0x08CF | -10 | -9.96 | 5.85 |
| 0x00CC | -12 | -12.11 | 5.61 |
| 0c00C9 | -15 | -15.29 | 5.34 |
| 0c08C7 | -18 | -18.79 | 5.12 |
| 0c08C6 | -20 | -20.25 | 5.05 |

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### 8.16.4 RX Performance

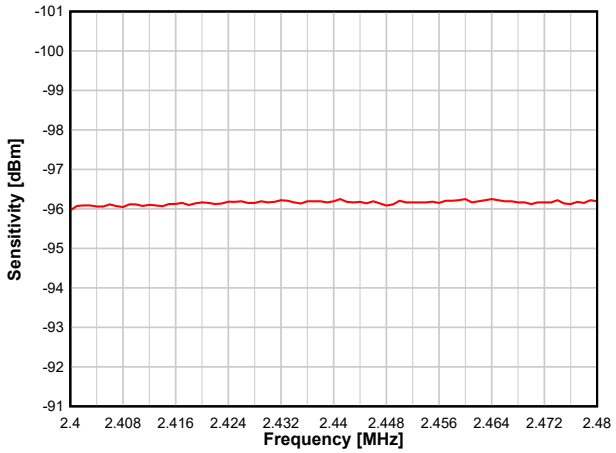



图 8-14. Sensitivity vs. Frequency (BLE 1 Mbps)

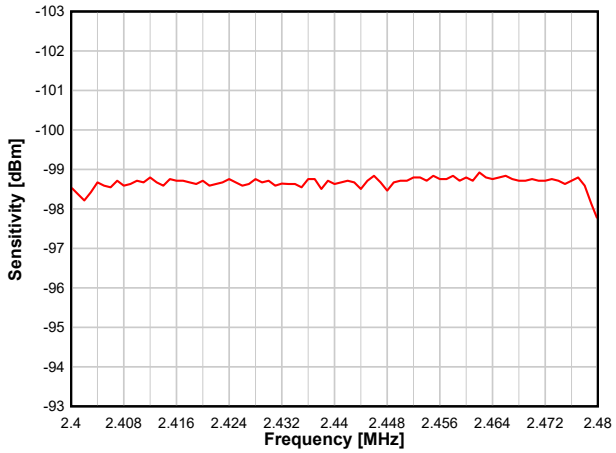



图 8-15. Sensitivity vs. Frequency (250 kbps)

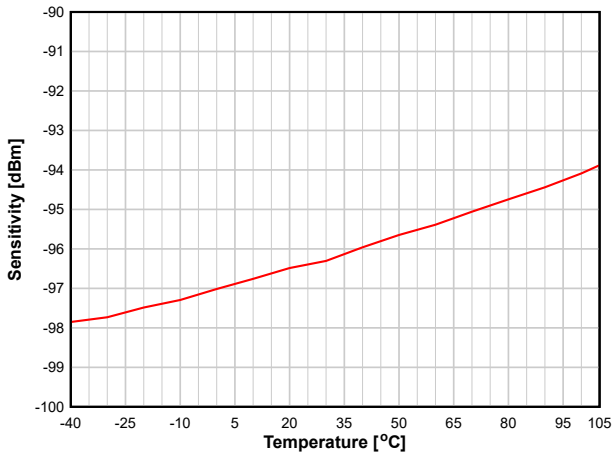



图 8-16. Sensitivity vs. Temperature (BLE 1 Mbps, 2.44 GHz)

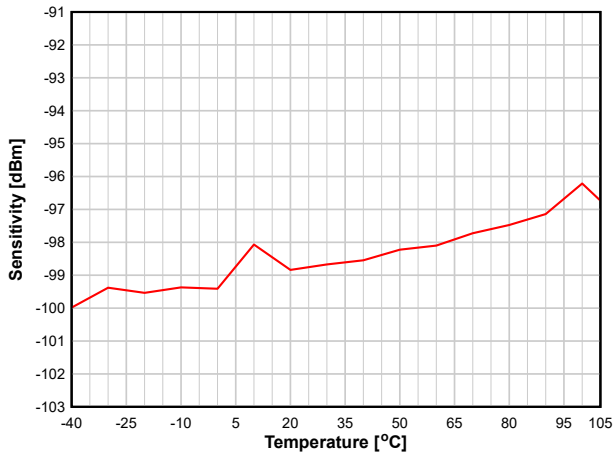



图 8-17. Sensitivity vs. Temperature (250 kbps, 2.44 GHz)

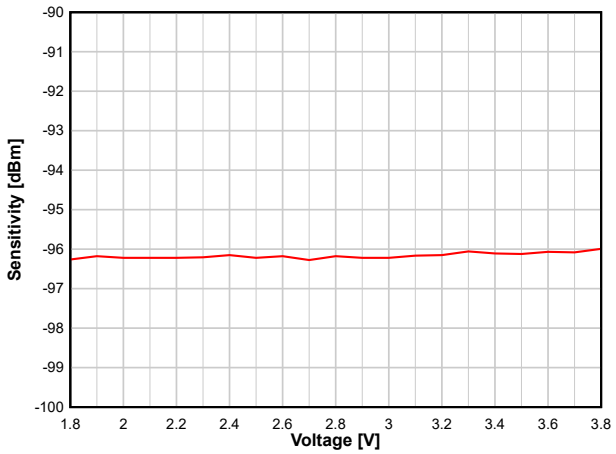



图 8-18. Sensitivity vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz)

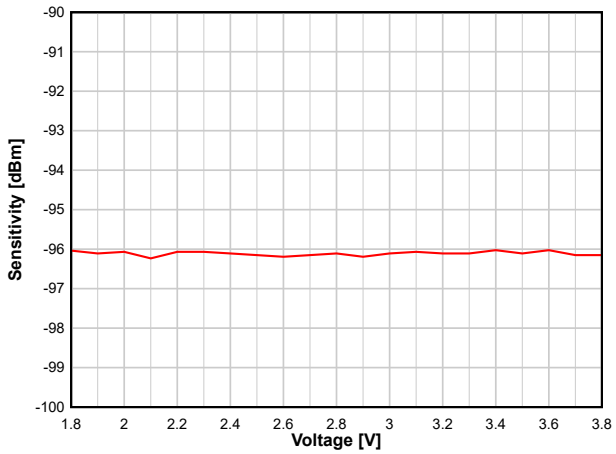



图 8-19. Sensitivity vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz, DCDC Off)


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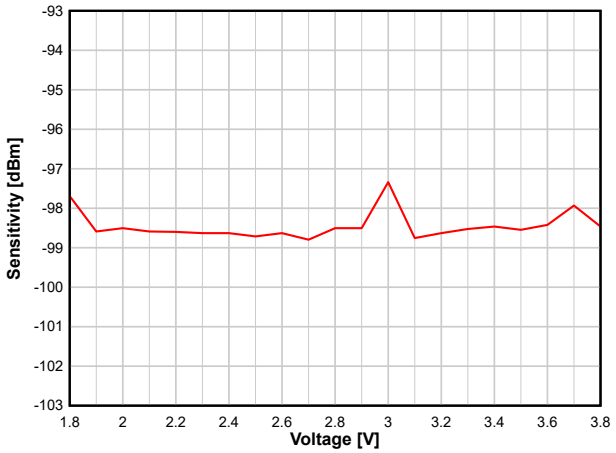



**图 8-20. Sensitivity vs. Supply Voltage (VDDS) (250 kbps, 2.44 GHz)**

### 8.16.5 TX Performance

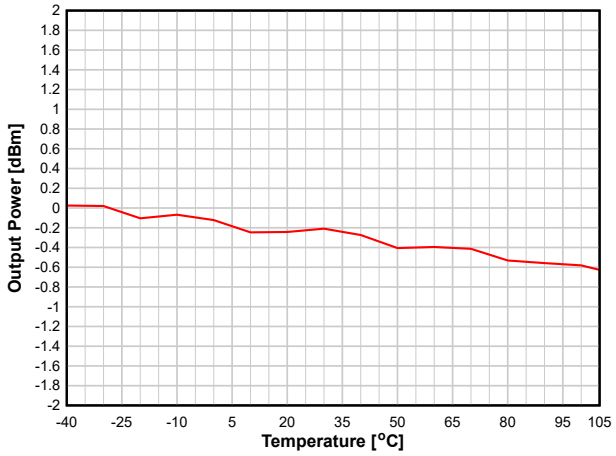



图 8-21. Output Power vs. Temperature (BLE 1 Mbps, 2.44 GHz, 0 dBm)

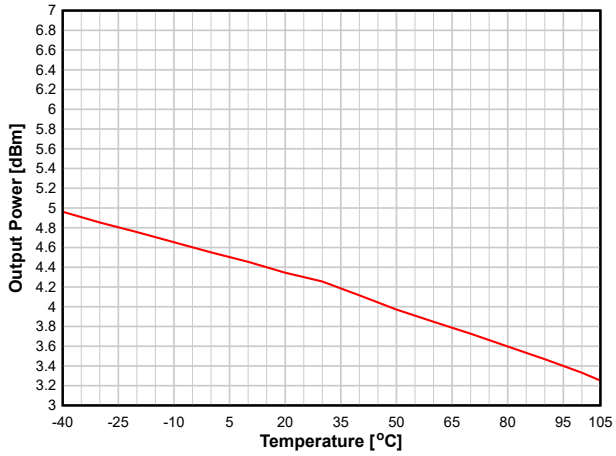



图 8-22. Output Power vs. Temperature (BLE 1 Mbps, 2.44 GHz, +5 dBm)

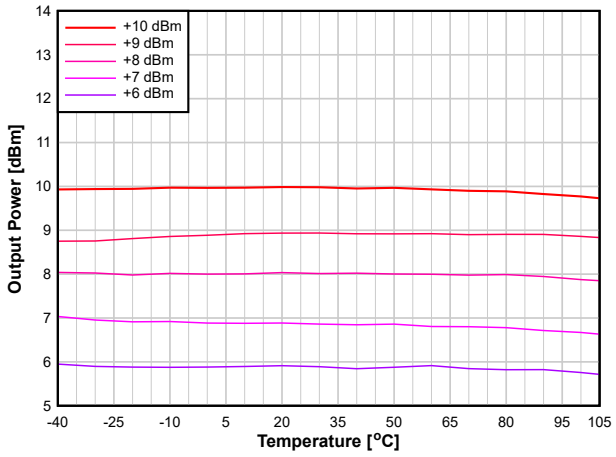



图 8-23. Output Power vs. Temperature (BLE 1 Mbps, 2.44 GHz, +10 dBm)

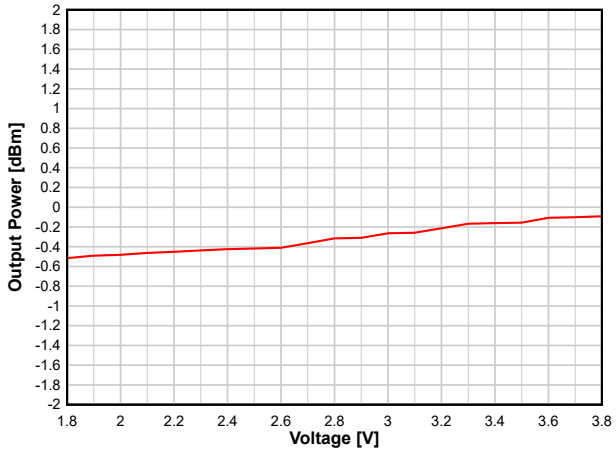



图 8-24. Output Power vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz, 0 dBm)

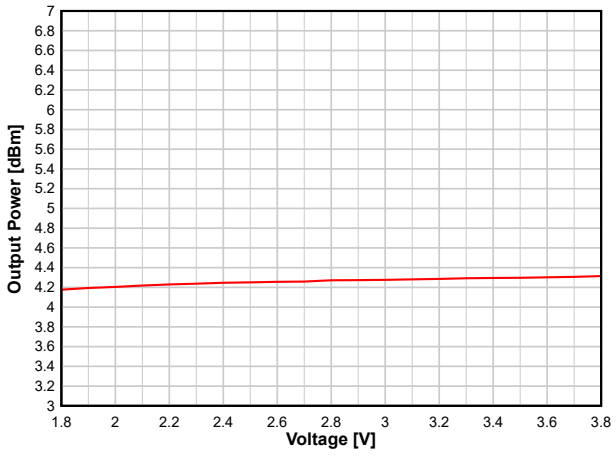



图 8-25. Output Power vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz, +5 dBm)

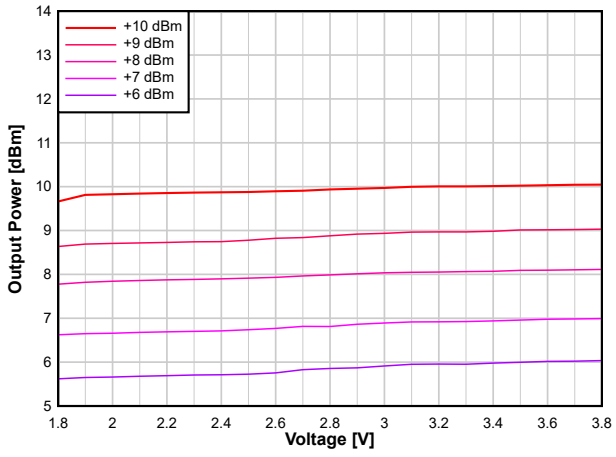



图 8-26. Output Power vs. Supply Voltage (VDDS) (2.44 GHz, +10 dBm PA)


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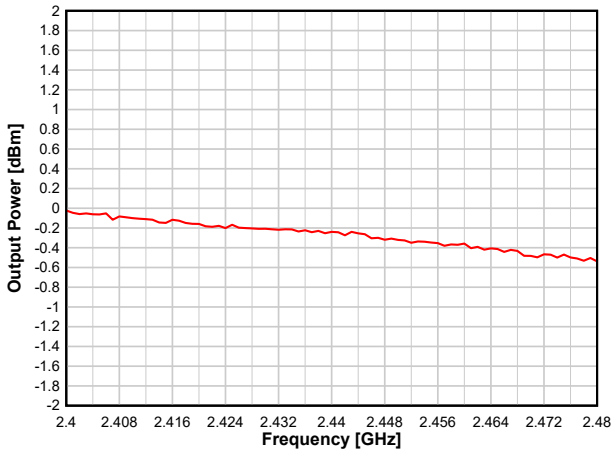



图 8-27. Output Power vs. Frequency (BLE 1 Mbps, 0 dBm)

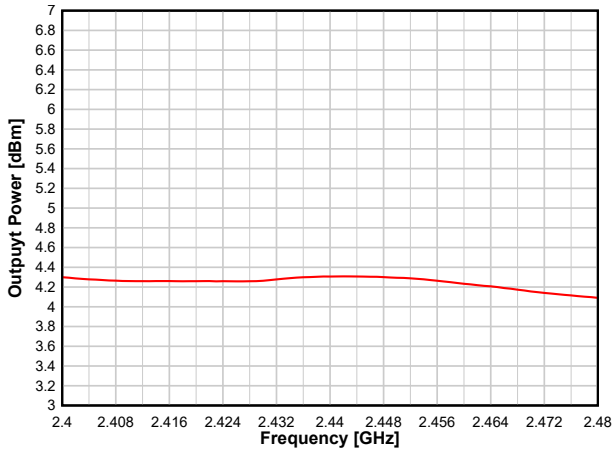



图 8-28. Output Power vs. Frequency (BLE 1 Mbps, +5 dBm)

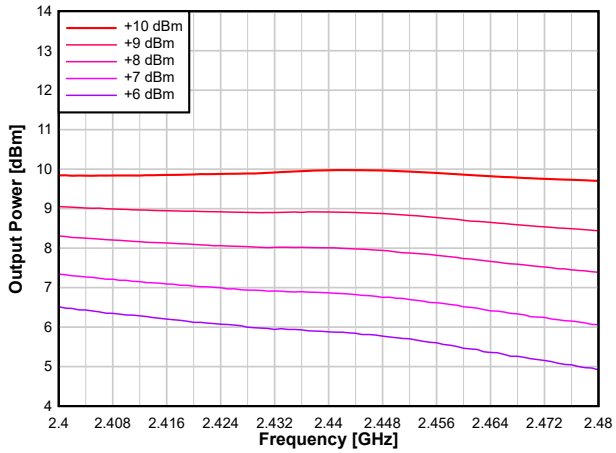



图 8-29. Output Power vs. Frequency (BLE 1Mbps, +10 dBm PA)

### 8.16.6 ADC Performance

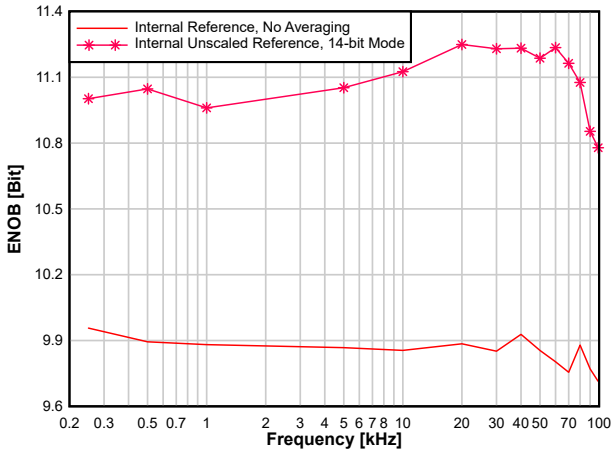



图 8-30. ENOB vs. Input Frequency

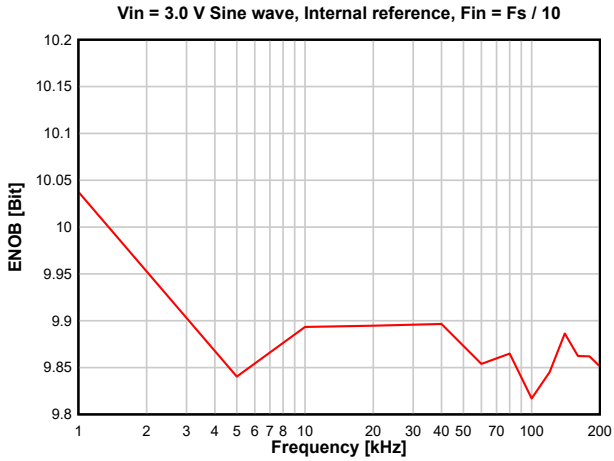



图 8-31. ENOB vs. Sampling Frequency

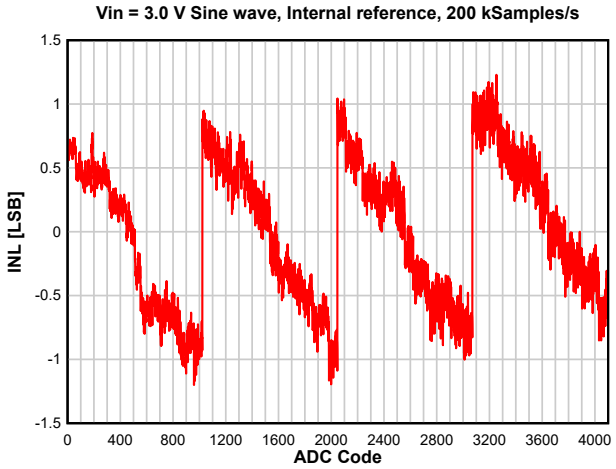



图 8-32. INL vs. ADC Code

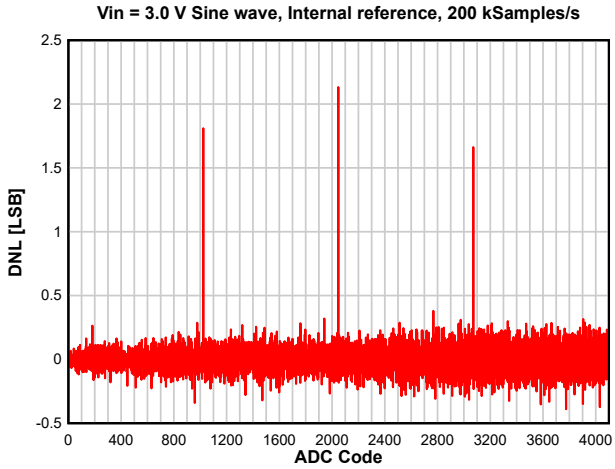



图 8-33. DNL vs. ADC Code

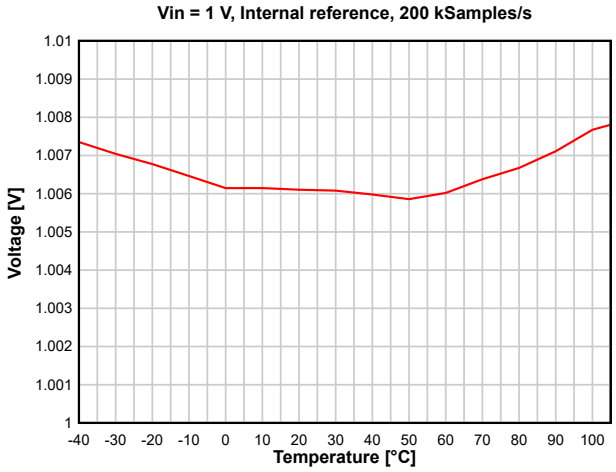



图 8-34. ADC Accuracy vs. Temperature

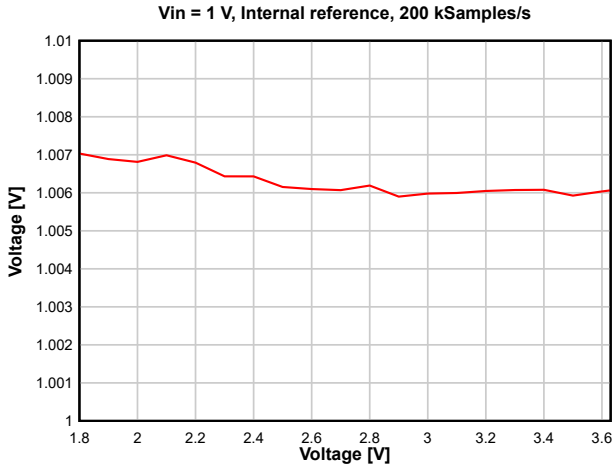



图 8-35. ADC Accuracy vs. Supply Voltage (VDDS)


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# 9 Detailed Description

## 9.1 Overview

节 4 shows the core modules of the CC2652PSIP device.

## 9.2 System CPU

The CC2652PSIP SimpleLink™ Wireless MCU contains an Arm® Cortex®-M4F system CPU, which runs the application and the higher layers of radio protocol stacks.

The system CPU is the foundation of a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

Its features include the following:

- ARMv7-M architecture optimized for small-footprint embedded applications
- Arm Thumb®-2 mixed 16- and 32-bit instruction set delivers the high performance expected of a 32-bit Arm core in a compact memory size
- Fast code execution permits increased sleep mode time
- Deterministic, high-performance interrupt handling for time-critical applications
- Single-cycle multiply instruction and hardware divide
- Hardware division and fast digital-signal-processing oriented multiply accumulate
- Saturating arithmetic for signal processing
- IEEE 754-compliant single-precision Floating Point Unit (FPU)
- Memory Protection Unit (MPU) for safety-critical applications
- Full debug with data matching for watchpoint generation
  - Data Watchpoint and Trace Unit (DWT)
  - JTAG Debug Access Port (DAP)
  - Flash Patch and Breakpoint Unit (FPB)
- Trace support reduces the number of pins required for debugging and tracing
  - Instrumentation Trace Macrocell Unit (ITM)
  - Trace Port Interface Unit (TPIU) with asynchronous serial wire output (SWO)
- Optimized for single-cycle flash memory access
- Tightly connected to 8-KB 4-way random replacement cache for minimal active power consumption and wait states
- Ultra-low-power consumption with integrated sleep modes
- 48 MHz operation
- 1.25 DMIPS per MHz

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## 9.3 Radio (RF Core)

The RF Core is a highly flexible and future proof radio module which contains an Arm Cortex-M0 processor that interfaces the analog RF and base-band circuitry, handles data to and from the system CPU side, and assembles the information bits in a given packet structure. The RF core offers a high level, command-based API to the main CPU that configurations and data are passed through. The Arm Cortex-M0 processor is not programmable by customers and is interfaced through the TI-provided RF driver that is included with the SimpleLink Software Development Kit (SDK).

The RF core can autonomously handle the time-critical aspects of the radio protocols, thus offloading the main CPU, which reduces power and leaves more resources for the user application. Several signals are also available to control external circuitry such as RF switches or range extenders autonomously.

Multiprotocol solutions are enabled through time-sliced access of the radio, handled transparently for the application through the TI-provided RF driver and dual-mode manager.

The various physical layer radio formats are partly built as a software defined radio where the radio behavior is either defined by radio ROM contents or by non-ROM radio formats delivered in form of firmware patches with the SimpleLink SDKs. This allows the radio platform to be updated for support of future versions of standards even with over-the-air (OTA) updates while still using the same silicon.

### 9.3.1 Bluetooth 5.2 Low Energy

The RF Core offers full support for Bluetooth 5.2 Low Energy, including the high-sped 2-Mbps physical layer and the 500-kbps and 125-kbps long range PHYs (Coded PHY) through the TI provided Bluetooth 5.2 stack or through a high-level Bluetooth API. The Bluetooth 5.2 PHY and part of the controller are in radio and system ROM, providing significant savings in memory usage and more space available for applications.

The new high-speed mode allows data transfers up to 2 Mbps, twice the speed of Bluetooth 4.2 and five times the speed of Bluetooth 4.0, without increasing power consumption. In addition to faster speeds, this mode offers significant improvements for energy efficiency and wireless coexistence with reduced radio communication time.

Bluetooth 5.2 also enables unparalleled flexibility for adjustment of speed and range based on application needs, which capitalizes on the high-speed or long-range modes respectively. Data transfers are now possible at 2 Mbps, enabling development of applications using voice, audio, imaging, and data logging that were not previously an option using Bluetooth low energy. With high-speed mode, existing applications deliver faster responses, richer engagement, and longer battery life. Bluetooth 5.2 enables fast, reliable firmware updates.

### 9.3.2 802.15.4 (Thread, Zigbee, 6LoWPAN)

Through a dedicated IEEE radio API, the RF Core supports the 2.4-GHz IEEE 802.15.4-2011 physical layer (2 Mchips per second Offset-QPSK with DSSS 1:8), used in Thread, Zigbee, and 6LoWPAN protocols. The 802.15.4 PHY and MAC are in radio and system ROM. TI also provides royalty-free protocol stacks for Thread and Zigbee as part of the SimpleLink SDK, enabling a robust end-to-end solution.

## 9.4 Memory

The up to 352-KB nonvolatile (Flash) memory provides storage for code and data. The flash memory is in-system programmable and erasable. The last flash memory sector must contain a Customer Configuration section (CCFG) that is used by boot ROM and TI provided drivers to configure the device. This configuration is done through the ccfg.c source file that is included in all TI provided examples.

The ultra-low leakage system static RAM (SRAM) is split into up to five 16-KB blocks and can be used for both storage of data and execution of code. Retention of SRAM contents in Standby power mode is enabled by default and included in Standby mode power consumption numbers. Parity checking for detection of bit errors in memory is built-in, which reduces chip-level soft errors and thereby increases reliability. System SRAM is always initialized to zeroes upon code execution from boot.

To improve code execution speed and lower power when executing code from nonvolatile memory, a 4-way nonassociative 8-KB cache is enabled by default to cache and prefetch instructions read by the system CPU. The cache can be used as a general-purpose RAM by enabling this feature in the Customer Configuration Area (CCFG).


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There is a 4-KB ultra-low leakage SRAM available for use with the Sensor Controller Engine which is typically used for storing Sensor Controller programs, data and configuration parameters. This RAM is also accessible by the system CPU. The Sensor Controller RAM is not cleared to zeroes between system resets.

The ROM includes a TI-RTOS kernel and low-level drivers, as well as significant parts of selected radio stacks, which frees up flash memory for the application. The ROM also contains a serial (SPI and UART) bootloader that can be used for initial programming of the device.

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## 9.5 Sensor Controller

The Sensor Controller contains circuitry that can be selectively enabled in both Standby and Active power modes. The peripherals in this domain can be controlled by the Sensor Controller Engine, which is a proprietary power-optimized CPU. This CPU can read and monitor sensors or perform other tasks autonomously; thereby significantly reducing power consumption and offloading the system CPU.

The Sensor Controller Engine is user programmable with a simple programming language that has syntax similar to C. This programmability allows for sensor polling and other tasks to be specified as sequential algorithms rather than static configuration of complex peripheral modules, timers, DMA, register programmable state machines, or event routing.

The main advantages are:

- Flexibility - data can be read and processed in unlimited manners while still ensuring ultra-low power
- 2 MHz low-power mode enables lowest possible handling of digital sensors
- Dynamic reuse of hardware resources
- 40-bit accumulator supporting multiplication, addition and shift
- Observability and debugging options

Sensor Controller Studio is used to write, test, and debug code for the Sensor Controller. The tool produces C driver source code, which the System CPU application uses to control and exchange data with the Sensor Controller. Typical use cases may be (but are not limited to) the following:

- Read analog sensors using integrated ADC or comparators
- Interface digital sensors using GPIOs, SPI, UART, or $I^2C$ ($I^2C$ and UART are bit-banged)
- Capacitive sensing
- Waveform generation
- Very low-power pulse counting (flow metering)
- Key scan

The peripherals in the Sensor Controller include the following:

- The low-power clocked comparator can be used to wake the system CPU from any state in which the comparator is active. A configurable internal reference DAC can be used in conjunction with the comparator. The output of the comparator can also be used to trigger an interrupt or the ADC.
- Capacitive sensing functionality is implemented through the use of a constant current source, a time-to-digital converter, and a comparator. The continuous time comparator in this block can also be used as a higher-accuracy alternative to the low-power clocked comparator. The Sensor Controller takes care of baseline tracking, hysteresis, filtering, and other related functions when these modules are used for capacitive sensing.
- The ADC is a 12-bit, 200-ksamples/s ADC with eight inputs and a built-in voltage reference. The ADC can be triggered by many different sources including timers, I/O pins, software, and comparators.
- The analog modules can connect to up to eight different GPIOs
- Dedicated SPI controller with up to 6 MHz clock speed

The peripherals in the Sensor Controller can also be controlled from the main application processor.


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## 9.6 Cryptography

The CC2652PSIP device comes with a wide set of modern cryptography-related hardware accelerators, drastically reducing code footprint and execution time for cryptographic operations. It also has the benefit of being lower power and improves availability and responsiveness of the system because the cryptography operations runs in a background hardware thread.
Together with a large selection of open-source cryptography libraries provided with the Software Development Kit (SDK), this allows for secure and future proof IoT applications to be easily built on top of the platform. The hardware accelerator modules are:

- **True Random Number Generator (TRNG)** module provides a true, nondeterministic noise source for the purpose of generating keys, initialization vectors (IVs), and other random number requirements. The TRNG is built on 24 ring oscillators that create unpredictable output to feed a complex nonlinear-combinatorial circuit.
- **Secure Hash Algorithm 2 (SHA-2)** with support for SHA224, SHA256, SHA384, and SHA512
- **Advanced Encryption Standard (AES)** with 128 and 256 bit key lengths
- **Public Key Accelerator** - Hardware accelerator supporting mathematical operations needed for elliptic curves up to 512 bits and RSA key pair generation up to 1024 bits.

Through use of these modules and the TI provided cryptography drivers, the following capabilities are available for an application or stack:

- **Key Agreement Schemes**
  - Elliptic curve Diffie – Hellman with static or ephemeral keys (ECDH and ECDHE)
  - Elliptic curve Password Authenticated Key Exchange by Juggling (ECJ-PAKE)
- **Signature Generation**
  - Elliptic curve Diffie-Hellman Digital Signature Algorithm (ECDSA)
- **Curve Support**
  - Short Weierstrass form (full hardware support), such as:
    - NIST-P224, NIST-P256, NIST-P384, NIST-P521
    - Brainpool-256R1, Brainpool-384R1, Brainpool-512R1
    - secp256r1
  - Montgomery form (hardware support for multiplication), such as:
    - Curve25519
- **SHA2 based MACs**
  - HMAC with SHA224, SHA256, SHA384, or SHA512
- Block cipher mode of operation
  - AESCCM
  - AESGCM
  - AESECB
  - AESCBC
  - AESCBC-MAC
- **True random number generation**

Other capabilities, such as RSA encryption and signatures as well as Edwards type of elliptic curves such as Curve1174 or Ed25519, can also be implemented using the provided hardware accelerators but are not part of the TI SimpleLink SDK for the CC2652PSIP device.

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## 9.7 Timers

A large selection of timers are available as part of the CC2652PSIP device. These timers are:

- **Real-Time Clock (RTC)**

  A 70-bit 3-channel timer running on the 32 kHz low frequency system clock (SCLK_LF)
  This timer is available in all power modes except Shutdown. The timer can be calibrated to compensate for frequency drift when using the LF RCOSC as the low frequency system clock. If an external LF clock with frequency different from 32.768 kHz is used, the RTC tick speed can be adjusted to compensate for this. When using TI-RTOS, the RTC is used as the base timer in the operating system and should thus only be accessed through the kernel APIs such as the Clock module. The real time clock can also be read by the Sensor Controller Engine to timestamp sensor data and also has dedicated capture channels. By default, the RTC halts when a debugger halts the device.
- **General Purpose Timers (GPTIMER)**

  The four flexible GPTIMERs can be used as either 4× 32 bit timers or 8× 16 bit timers, all running on up to 48 MHz. Each of the 16- or 32-bit timers support a wide range of features such as one-shot or periodic counting, pulse width modulation (PWM), time counting between edges and edge counting. The inputs and outputs of the timer are connected to the device event fabric, which allows the timers to interact with signals such as GPIO inputs, other timers, DMA and ADC. The GPTIMERs are available in Active and Idle power modes.
- **Sensor Controller Timers**

  The Sensor Controller contains 3 timers:

  AUX Timer 0 and 1 are 16-bit timers with a $2^N$ prescaler. Timers can either increment on a clock or on each edge of a selected tick source. Both one-shot and periodical timer modes are available.

  AUX Timer 2 is a 16-bit timer that can operate at 24 MHz, 2 MHz or 32 kHz independent of the Sensor Controller functionality. There are 4 capture or compare channels, which can be operated in one-shot or periodical modes. The timer can be used to generate events for the Sensor Controller Engine or the ADC, as well as for PWM output or waveform generation.
- **Radio Timer**

  A multichannel 32-bit timer running at 4 MHz is available as part of the device radio. The radio timer is typically used as the timing base in wireless network communication using the 32-bit timing word as the network time. The radio timer is synchronized with the RTC by using a dedicated radio API when the device radio is turned on or off. This ensures that for a network stack, the radio timer seems to always be running when the radio is enabled. The radio timer is in most cases used indirectly through the trigger time fields in the radio APIs and should only be used when running the accurate 48 MHz high frequency crystal is the source of SCLK_HF.
- **Watchdog timer**

  The watchdog timer is used to regain control if the system operates incorrectly due to software errors. It is typically used to generate an interrupt to and reset of the device for the case where periodic monitoring of the system components and tasks fails to verify proper functionality. The watchdog timer runs on a 1.5 MHz clock rate and cannot be stopped once enabled. The watchdog timer pauses to run in Standby power mode and when a debugger halts the device.


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## 9.8 Serial Peripherals and I/O

The SSIs are synchronous serial interfaces that are compatible with SPI, MICROWIRE, and TI's synchronous serial interfaces. The SSIs support both SPI controller and peripheral up to 4 MHz. The SSI modules support configurable phase and polarity.

The UARTs implement universal asynchronous receiver and transmitter functions. They support flexible baud-rate generation up to a maximum of 3 Mbps.

The $I^2S$ interface is used to handle digital audio and can also be used to interface pulse-density modulation microphones (PDM).

The $I^2C$ interface is also used to communicate with devices compatible with the $I^2C$ standard. The $I^2C$ interface can handle 100 kHz and 400 kHz operation, and can serve as both controller and peripheral.

The I/O controller (IOC) controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a flexible manner. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function, and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull or open-drain. Five GPIOs have high-drive capabilities, which are marked in **bold** in 节 7. All digital peripherals can be connected to any digital pin on the device.

For more information, see the SimpleLink™ CC13xx and CC26xx Software Development Kit (SDK).

## 9.9 Battery and Temperature Monitor

A combined temperature and battery voltage monitor is available in the CC2652PSIP device. The battery and temperature monitor allows an application to continuously monitor on-chip temperature and supply voltage and respond to changes in environmental conditions as needed. The module contains window comparators to interrupt the system CPU when temperature or supply voltage go outside defined windows. These events can also be used to wake up the device from Standby mode through the Always-On (AON) event fabric.

## 9.10 µDMA

The device includes a direct memory access (µDMA) controller. The µDMA controller provides a way to offload data-transfer tasks from the system CPU, thus allowing for more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform a transfer between memory and peripherals. The µDMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory when the peripheral is ready to transfer more data.

Some features of the µDMA controller include the following (this is not an exhaustive list):

- Highly flexible and configurable channel operation of up to 32 channels
- Transfer modes: memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits
- Ping-pong mode for continuous streaming of data

## 9.11 Debug

The on-chip debug support is done through a dedicated cJTAG (IEEE 1149.7) or JTAG (IEEE 1149.1) interface. The device boots by default into cJTAG mode and must be reconfigured to use 4-pin JTAG.

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## 9.12 Power Management

To minimize power consumption, the CC2652PSIP supports a number of power modes and power management features (see 表 9-1).

**表 9-1. Power Modes**

| MODE | SOFTWARE CONFIGURABLE POWER MODES | | | | RESET PIN HELD |
|---|---|---|---|---|---|
| | ACTIVE | IDLE | STANDBY | SHUTDOWN | |
| **CPU** | Active | Off | Off | Off | Off |
| **Flash** | On | Available | Off | Off | Off |
| **SRAM** | On | On | Retention | Off | Off |
| **Supply System** | On | On | Duty Cycled | Off | Off |
| Register and CPU retention | Full | Full | Partial | No | No |
| SRAM retention | Full | Full | Full | No | No |
| 48 MHz high-speed clock (SCLK_HF) | XOSC_HF or RCOSC_HF | XOSC_HF or RCOSC_HF | Off | Off | Off |
| 2 MHz medium-speed clock (SCLK_MF) | RCOSC_MF | RCOSC_MF | Available | Off | Off |
| 32 kHz low-speed clock (SCLK_LF) | XOSC_LF or RCOSC_LF | XOSC_LF or RCOSC_LF | XOSC_LF or RCOSC_LF | Off | Off |
| Peripherals | Available | Available | Off | Off | Off |
| Sensor Controller | Available | Available | Available | Off | Off |
| Wake-up on RTC | Available | Available | Available | Off | Off |
| Wake-up on pin edge | Available | Available | Available | Available | Off |
| Wake-up on reset pin | On | On | On | On | On |
| Brownout detector (BOD) | On | On | Duty Cycled | Off | Off |
| Power-on reset (POR) | On | On | On | Off | Off |
| Watchdog timer (WDT) | Available | Available | Paused | Off | Off |

In **Active** mode, the application system CPU is actively executing code. Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source (see 表 9-1).

In **Idle** mode, all active peripherals can be clocked, but the Application CPU core and memory are not clocked and no code is executed. Any interrupt event brings the processor back into active mode.

In **Standby** mode, only the always-on (AON) domain is active. An external wake-up event, RTC event, or Sensor Controller event is required to bring the device back to active mode. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In **Shutdown** mode, the device is entirely turned off (including the AON domain and Sensor Controller), and the I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a *wake from shutdown pin* wakes up the device and functions as a reset trigger. The CPU can differentiate between reset in this way and reset-by-reset pin or power-on reset by reading the reset status register. The only state retained in this mode is the latched I/O state and the flash memory contents.


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The Sensor Controller is an autonomous processor that can control the peripherals in the Sensor Controller independently of the system CPU. This means that the system CPU does not have to wake up, for example to perform an ADC sampling or poll a digital sensor over SPI, thus saving both current and wake-up time that would otherwise be wasted. The Sensor Controller Studio tool enables the user to program the Sensor Controller, control its peripherals, and wake up the system CPU as needed. All Sensor Controller peripherals can also be controlled by the system CPU.

备注

The power, RF and clock management for the CC2652PSIP device require specific configuration and handling by software for optimized performance. This configuration and handling is implemented in the TI-provided drivers that are part of the CC2652PSIP software development kit (SDK). Therefore, TI highly recommends using this software framework for all application development on the device. The complete SDK with TI-RTOS (optional), device drivers, and examples are offered free of charge in source code.

## 9.13 Clock Systems

The CC2652PSIP device has several internal system clocks.

The 48 MHz SCLK_HF is used as the main system (MCU and peripherals) clock. This can be driven by the internal 48 MHz RC Oscillator (RCOSC_HF) or in-package 48 MHz crystal (XOSC_HF). Note that the radio operation runs off the included, in-package 48 MHz crystal within the module.

SCLK_MF is an internal 2 MHz clock that is used by the Sensor Controller in low-power mode and also for internal power management circuitry. The SCLK_MF clock is always driven by the internal 2 MHz RC Oscillator (RCOSC_MF).

SCLK_LF is the 32.768 kHz internal low-frequency system clock. It can be used by the Sensor Controller for ultra-low-power operation and is also used for the RTC and to synchronize the radio timer before or after Standby power mode. SCLK_LF can be driven by the internal 32.8 kHz RC Oscillator (RCOSC_LF) or the included, in-package 32.768 kHz crystal within the module.

When using the included, in-package crystal within the module, or the internal RC oscillator, the device can output the 32 kHz SCLK_LF signal to other devices, thereby reducing the overall system cost.

## 9.14 Network Processor

Depending on the product configuration, the CC2652PSIP device can function as a wireless network processor (WNP - a device running the wireless protocol stack with the application running on a separate host MCU), or as a system-on-chip (SoC) with the application and protocol stack running on the system CPU inside the device.

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

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## 9.15 Device Certification and Qualification

The CC2652PSIP module from TI is certified for FCC, IC/ISED, ETSI/CE and UK as lised in 表 9-2. Moreover, the module is a Bluetooth Qualified Design by the Bluetooth Special Interest Group (Bluetooth SIG). TI Customers that build products based on the TI CC2652PSIP module can save in testing cost and time per product family.

**备注**

The FCC and IC IDs, as well as the UK and CE markings, must be located in both the user manual and on the packaging. Due to the small size of the module (7 mm x 7 mm), placing the IDs and markings in a type size large enough to be legible without the aid of magnification is impractical.

**表 9-2. CC2652PSIP List of Certifications**

| Regulatory Body | Specification | ID (IF APPLICABLE) |
|---|---|---|
| FCC (USA) | Part 15C + MPE FCC RF Exposure (Bluetooth) | ZAT-CC2652PSIP |
| | Part 15C + MPE FCC RF Exposure (802.15.4) | |
| IC/ISED (Canada) | RSS-102 (MPE) and RSS-247 (Bluetooth) | 451H-CC2652PSIP |
| | RSS-102 (MPE) and RSS-247 (802.15.4) | |
| ETSI/CE (Europe) & RER (UK) | EN 300328 v2.2.2 (2019-07) (Bluetooth) | — |
| | EN 300328 v2.2.2 (2019-07) (802.15.4) | — |
| | EN 62311:2020 and EN 50655:2017 (MPE) | — |
| | EN 301 489-1 v2.2.3 (2019-11) | — |
| | EN 301489-17 v3.2.4 (2020-09) | — |
| | EN 62368-1:2020/A11:2020 | — |

### 9.15.1 FCC Certification and Statement

**CAUTION**

**FCC RF Radiation Exposure Statement:**

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying RF exposure limits. This transmitter must not be co-located or operating with any other antenna or transmitter.

The CC2652PSIPMOT module from TI is certified for FCC as a single-modular transmitter. The module is an FCC-certified radio module that carries a modular grant.

You are cautioned that changes or modifications not expressly approved by the party responsible for compliance could void the user’s authority to operate the equipment.

This device is planned to comply with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference.
- This device must accept any interference received, including interference that may cause undesired operation of the device.


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### 9.15.2 IC/ISED Certification and Statement

**CAUTION**

**IC RF Radiation Exposure Statement:**

To comply with IC RF exposure requirements, this device and its antenna must not be co-located or operating in conjunction with any other antenna or transmitter.

Pour se conformer aux exigences de conformité RF canadienne l'exposition, cet appareil et son antenne ne doivent pas étre co-localisés ou fonctionnant en conjonction avec une autre antenne ou transmetteur.

The CC2652PSIPMOT module from TI is certified for IC as a single-modular transmitter. The CC2652PSIPMOT module from TI is meets IC modular approval and labeling requirements. The IC follows the same testing and rules as the FCC regarding certified modules in authorized equipment.

This device complies with Industry Canada licence-exempt RSS standards.

Operation is subject to the following two conditions:

- This device may not cause interference.
- This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence.

L'exploitation est autorisée aux deux conditions suivantes:

- L'appareil ne doit pas produire de brouillage
- L'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

### 9.15.3 ETSI/CE Certification

The CC2652PSIPMOT module from TI is CE certified with certifications to the appropriate EU radio and EMC directives summarized in the Declaration of Conformity and evidenced by the CE mark. The module is tested and certified against the Radio Equipment Directive (RED).

See the full text of the for the EU Declaration of Conformity for the CC2652PSIPMOT device.

### 9.15.4 UK Certification

The CC2652PSIPMOT module from TI is UK certified with certifications to the appropriate UK radio and EMC directives summarized in the Declaration of Conformity and evidenced by the UK mark. The module is tested and certified against the Radio Equipment Regulations 2017.

See the full text of the for the UK Declaration of Conformity for the CC2652PSIPMOT device.

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## 9.16 Module Markings

图 9-1 shows the top-side marking for the CC2652PSIP module.

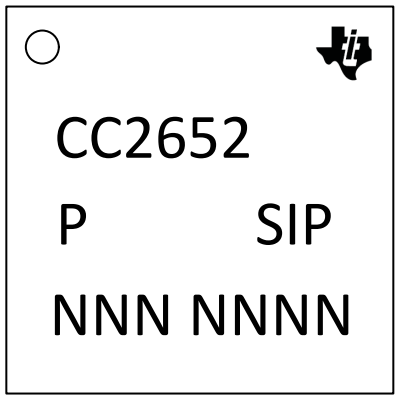



**图 9-1. Top-Side Marking**

表 9-3 lists the CC2652PSIP module markings.

**表 9-3. Module Descriptions**

| MARKING | DESCRIPTION |
|---|---|
| CC2652 | Generic Part Number |
| P | Model |
| SIP | SIP = Module type, X = pre-release |
| NNN NNNN | LTC (Lot Trace Code) |

## 9.17 End Product Labeling

The CC2652PSIPMOT module complies with the FCC single modular FCC grant, FCC ID: .**ZAT-CC2652PSIP**. The host system using this module must display a visible label indicating the following text:

Contains FCC ID: **ZAT-CC2652PSIP**

The CC2652PSIPMOT module complies with the IC single modular IC grant, IC: **451H-CC2652PSIP**. The host system using this module must display a visible label indicating the following text:

Contains IC: **451H-CC2652PSIP**

For more information on end product labeling and a sample label, please see section 4 of the OEM Integrators Guide

## 9.18 Manual Information to the End User

The OEM integrator must be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module.

The end user manual must include all required regulatory information and warnings as shown in this manual.


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# 10 Application, Implementation, and Layout

**备注**

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 10.1 Application Information

### 10.1.1 Typical Application Circuit

图 10-1 shows the typical application schematic using the CC2652PSIP module. For the full reference schematic, download the LP-CC2652PSIP Design Files.

**备注**

The following guidelines are recommended for implementation of the RF design:

- Ensure an RF path is designed with a characteristic impedance of 50 Ω.
- Tuning of the antenna impedance matching network is recommended after manufacturing of the PCB to account for PCB parasitics. Please refer to CC13xx/CC26xx Hardware Configuration and PCB Design Considerations; section 5.1 for further information.

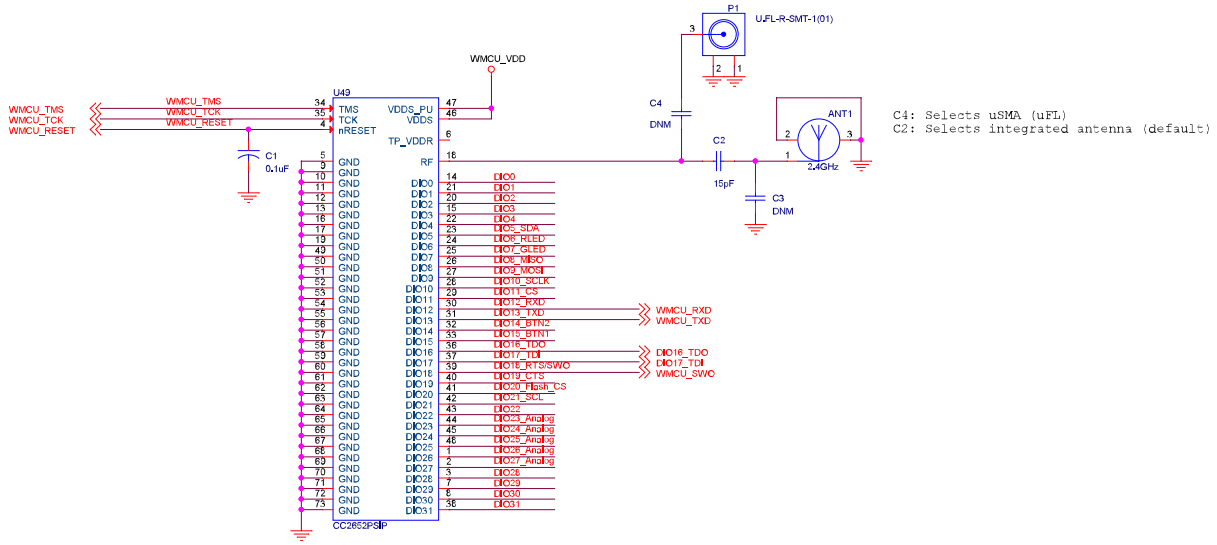



**图 10-1. CC2652PSIP Typical Application Schematic**

表 10-1 provides the bill of materials for a typical application using the CC2652PSIP module in 图 10-1.

For full operation reference design, see the LP-CC2652PSIP Design Files

**表 10-1. Bill of Materials**

| QTY | PART REFERENCE | VALUE | MANUFACTURER | PART NUMBER | DESCRIPTION |
|---|---|---|---|---|---|
| 1 | ANT1 | 2.4 GHz Ant | Texas Instruments | N/A | Refer to 2.4-GHz Inverted F Antenna for details of the antenna implementation and PCB requirements. |
| 1 | C1 | 0.1 µF | Murata | GRT033C81E104KE01D | Capacitor, ceramic, 0.1 µF, 25 V, ±10%, X6S, 0201 |
| 1 | C2 | 15 pF | Murata | GRM0332C1H150JA01D | Capacitor, ceramic, 1 pF, 50 V, ±5%, C0G/NP0, 0201 |
| 1 | P1 | U.FL | Hirose | U.FL-R-SMT-1(01) | U.FL (UMCC) connector receptacle, male pin 50 Ω, surface mount solder |
| 1 | U49 | CC2652PSIP | Texas Instruments | CC2652PSIPMOT | SimpleLink™ multiprotocol 2.4-GHz wireless MCU with integrated power amplifier |

## 10.2 Device Connection and Layout Fundamentals

### 10.2.1 Reset

In order to meet the module power-on-reset requirements, an external 0.1 µF capacitor is required on the nRESET pin during power ON. In addition, VDDS (Pin 46) and VDDS_PU (Pin 47) should be connected together. If the reset signal is not based upon a power-on-reset and is derived from an external MCU, then the external capacitor will not be needed and VDDS_PU (Pin 47) should be No Connect (NC). Please refer to 图 10-1 for the recommended circuit implementation and 表 10-1 for the recommended 0.1 µF capacitor.

### 10.2.2 Unused Pins

All unused pins can be left unconnected without the concern of having leakage current. Please refer to 节 7.3 for more details.

## 10.3 PCB Layout Guidelines

This section details the PCB guidelines to speed up the PCB design using the CC2652PSIP module. The integrator of the CC2652PSIP modules must comply with the PCB layout recommendations described in the following subsections to minimize the risk with regulatory certifications for the FCC, IC/ISED, ETSI/CE. Moreover, TI recommends customers to follow the guidelines described in this section to achieve similar performance to that obtained with the TI reference design.

### 10.3.1 General Layout Recommendations

Ensure that the following general layout recommendations are followed:

- Have a solid ground plane and ground vias under the module for stable system and thermal dissipation.
- Do not run signal traces underneath the module on a layer where the module is mounted.


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### 10.3.2 RF Layout Recommendations

It is critical that the RF section be laid out correctly to ensure optimal module performance. A poor layout can cause low-output power and sensitivity degradation. 图 10-2 shows the RF placement and routing of the CC2652PSIP module with the 2.4-GHz inverted F antenna.

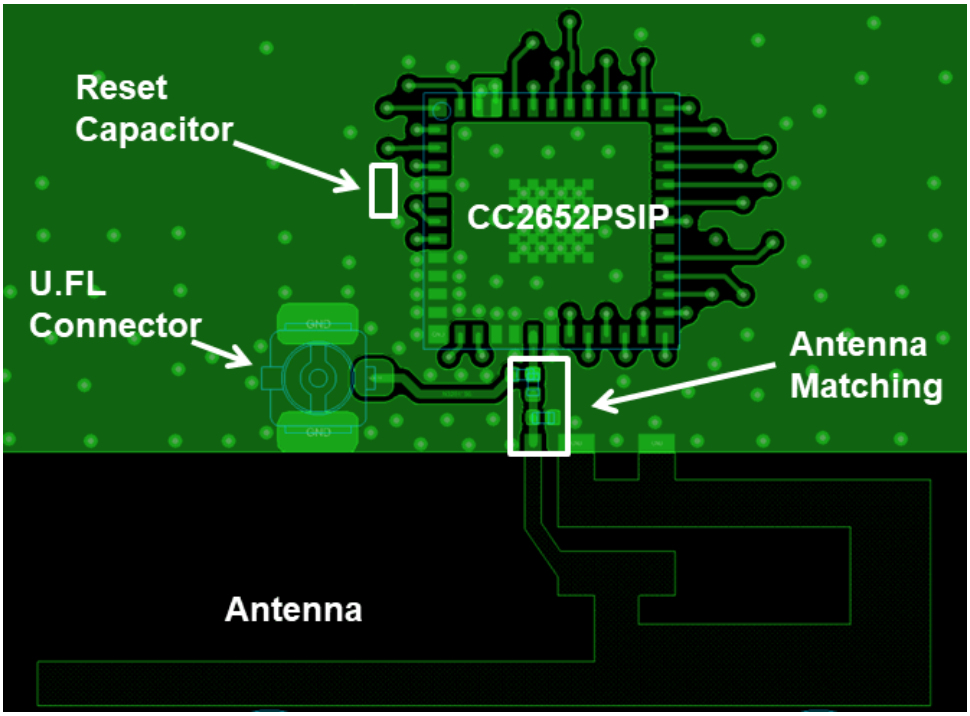



**图 10-2. Module Layout Guidelines**

Follow these RF layout recommendations for the CC2652PSIP module:

- RF traces must have a chararcterisitc impedance of 50-Ω.
- There must be no traces or ground under the antenna section.
- RF traces must have via stitching on the ground plane beside the RF trace on both sides.
- RF traces must be as short as possible.
- The module must be as close to the PCB edge in consideration of the product enclosure and type of antenna being used.

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#### 10.3.2.1 Antenna Placement and Routing

The antenna is the element used to convert the guided waves on the PCB traces to the free space electromagnetic radiation. The placement and layout of the antenna are the keys to increased range and data rates. 表 10-2 provides a summary of the antenna guidelines to follow with the CC2652PSIP module.

**表 10-2. Antenna Guidelines**

| SR NO. | GUIDELINES |
|---|---|
| 1 | Place the antenna on an edge of the PCB. |
| 2 | Ensure that no signals are routed across the antenna elements on any PCB layer. |
| 3 | Most antennas, including the PCB antenna used on the LaunchPad™, require ground clearance on all the layers of the PCB. Ensure that the ground is cleared on inner layers as well. |
| 4 | Ensure that there is provision to place matching components for the antenna. These must be tuned for best return loss when the complete board is assembled. Any plastics or casing must also be mounted while tuning the antenna because this can impact the impedance. |
| 5 | Ensure that the antenna characteristic impedance is 50-Ω as the module is designed for a 50-Ω system. |
| 6 | In case of printed antenna, ensure that the simulation is performed considering the soldermask thickness. |
| 7 | For good RF performance ensrue that the Voltge Standing Wave Ration (VSWR) is less than 2 across the frequency band of interest. |
| 9 | The feed point of the antenna is required to be grounded. This is only for the antenna type used on the CC2652PSIP LaunchPad™. See the specific antenna data sheets for the recommendations. |

表 10-3 lists the recommended antennas to use with the CC2652PSIP module. Other antennas may be available for use with the CC2652PSIP module. Please refer to to the CC2652RSIP OEM integrators guide for a list of approved antennas (and antenna types) that can be used with the CC2652RSIP module.

**表 10-3. Recommended Components**

| CHOICE | ANTENNA | MANUFACTURER | NOTES |
|---|---|---|---|
| 1 | 2.4-GHz Inverted F Antenna | Texas Instruments | Refer to 2.4-GHz Inverted F Antenna for details of the Antenna implementation and PCB requirements. |


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### *10.3.2.2 Transmission Line Considerations*

The RF signal from the module is routed to the antenna using a Coplanar Waveguide with ground (CPW-G) structure. CPW-G structure offers the maximum amount of isolation and the best possible shielding to the RF lines. In addition to the ground on the L1 layer, placing GND vias along the line also provides additional shielding.

图 10-3 shows a cross section of the coplanar waveguide with the critical dimensions.

图 10-4 shows the top view of the coplanar waveguide with GND and via stitching.

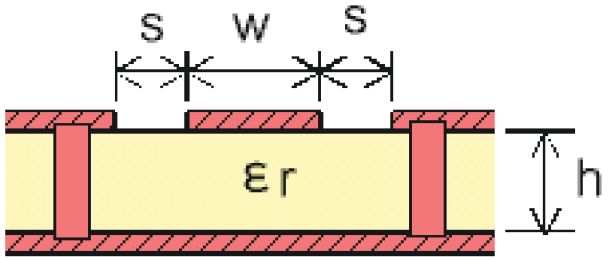



**图 10-3. Coplanar Waveguide (Cross Section)**

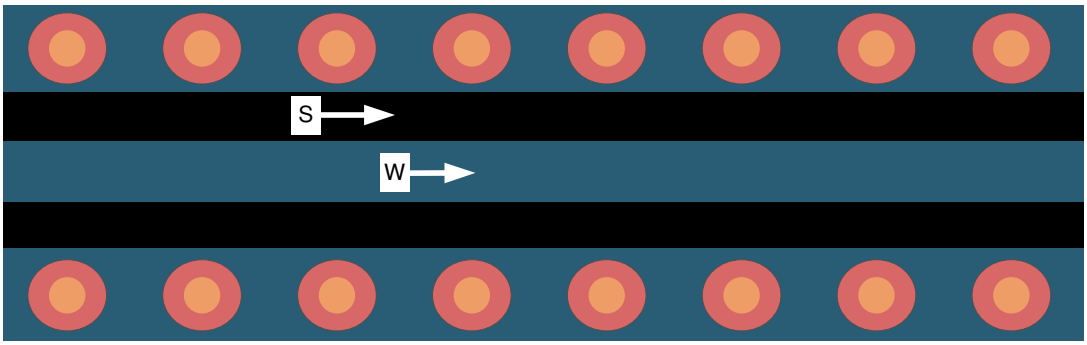



**图 10-4. CPW With GND and Via Stitching (Top View)**

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The recommended values for a 4-layer PCB board is provided in 表 10-4.

**表 10-4. Recommended PCB Values for 4-Layer Board (L1 to L2 = 0.175 mm)**

| PARAMETER | VALUE | UNITS |
|---|---|---|
| W | 0.300 | mm |
| S | 0.500 | mm |
| H | 0.175 | mm |
| Er (FR-4 substrate) | 4.0 | F/m |

## 10.4 Reference Designs

The following reference designs should be followed closely when implementing designs using the CC2652PSIP device.

Special attention must be paid to RF component placement, decoupling capacitors and DCDC regulator components, as well as ground connections for all of these.

| | |
|---|---|
| CC2652xSIP-EM Design Files | The CC2652xSIP-EM reference design provides schematic, layout and production files for the characterization board used for deriving the performance number found in this document. |
| LP-CC2652PSIP Design Files | The CC2652PSIP LaunchPad Design Files contain detailed schematics and layouts to build application specific boards using the CC2652PSIP module. This Launchpad Design is also used as the referenced for the CC2652RSIP module as it is pin-to-pin compatable with the CC2652RSIP module. |
| Sub-1 GHz and 2.4 GHz Antenna Kit for LaunchPad ™ Development Kit and SensorTag | The antenna kit allows real-life testing to identify the optimal antenna for your application. The antenna kit includes 16 antennas for frequencies from 169 MHz to 2.4 GHz, including:<br>• PCB antennas<br>• Helical antennas<br>• Chip antennas<br>• Dual-band antennas for 868 MHz and 915 MHz combined with 2.4 GHz<br>The antenna kit includes a JSC cable to connect to the Wireless MCU LaunchPad Development Kits and SensorTags. |


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# 11 Environmental Requirements and SMT Specifications

## 11.1 PCB Bending

The PCB follows IPC-A-600J for PCB twist and warpage < 0.75% or 7.5 mil per inch.

## 11.2 Handling Environment

### 11.2.1 Terminals

The product is mounted with motherboard through land-grid array (LGA). To prevent poor soldering, do not make skin contact with the LGA portion.

### 11.2.2 Falling

The mounted components will be damaged if the product falls or is dropped. Such damage may cause the product to malfunction.

## 11.3 Storage Condition

### 11.3.1 Moisture Barrier Bag Before Opened

A moisture barrier bag must be stored in a temperature of less than 30°C with humidity under 85% RH. The calculated shelf life for the dry-packed product will be 24 months from the date the bag is sealed.

### 11.3.2 Moisture Barrier Bag Open

Humidity indicator cards must be blue, < 30%.

## 11.4 PCB Assembly Guide

The wireless MCU modules are packaged in a substrate base Leadless Quad Flatpack (QFM) package. The modules are designed with pull back leads for easy PCB layout and board mounting.

### 11.4.1 PCB Land Pattern & Thermal Vias

We recommended a solder mask defined land pattern to provide a consistent soldering pad dimension in order to obtain better solder balancing and solder joint reliability. PCB land pattern are 1:1 to module soldering pad dimension. Thermal vias on PCB connected to other metal plane are for thermal dissipation purpose. It is critical to have sufficient thermal vias to avoid device thermal shutdown. Recommended vias size are 0.2mm and position not directly under solder paste to avoid solder dripping into the vias.

### 11.4.2 SMT Assembly Recommendations

The module surface mount assembly operations include:

- Screen printing the solder paste on the PCB
- Monitor the solder paste volume (uniformity)
- Package placement using standard SMT placement equipment
- X-ray pre-reflow check - paste bridging
- Reflow
- X-ray post-reflow check - solder bridging and voids

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### 11.4.3 PCB Surface Finish Requirements

A uniform PCB plating thickness is key for high assembly yield. For an electroless nickel immersion gold finish, the gold thickness should range from 0.05 µm to 0.20 µm to avoid solder joint embrittlement. Using a PCB with Organic Solderability Preservative (OSP) coating finish is also recommended as an alternative to Ni-Au.

### 11.4.4 Solder Stencil

Solder paste deposition using a stencil-printing process involves the transfer of the solder paste through pre-defined apertures with the application of pressure. Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of package is highly recommended to improve board assembly yields.

### 11.4.5 Package Placement

Packages can be placed using standard pick and place equipment with an accuracy of ±0.05 mm. Component pick and place systems are composed of a vision system that recognizes and positions the component and a mechanical system that physically performs the pick and place operation. Two commonly used types of vision systems are:

- A vision system that locates a package silhouette
- A vision system that locates individual pads on the interconnect pattern

The second type renders more accurate placements but tends to be more expensive and time consuming. Both methods are acceptable since the parts align due to a self-centering features of the solder joint during solder reflow. It is recommended to avoid solder bridging to 2 mils into the solder paste or with minimum force to avoid causing any possible damage to the thinner packages.

### 11.4.6 Solder Joint Inspection

After surface mount assembly, transmission X-ray should be used for sample monitoring of the solder attachment process. This identifies defects such as solder bridging, shorts, opens, and voids. It is also recommended to use side view inspection in addition to X-rays to determine if there are "Hour Glass" shaped solder and package tilting existing. The "Hour Glass" solder shape is not a reliable joint. 90° mirror projection can be used for side view inspection.

### 11.4.7 Rework and Replacement

TI recommends removal of modules by rework station applying a profile similar to the mounting process. Using a heat gun can sometimes cause damage to the module by overheating.

### 11.4.8 Solder Joint Voiding

TI recommends to control solder joint voiding to be less than 30% (per IPC-7093). Solder joint voids could be reduced by baking of components and PCB, minimized solder paste exposure duration, and reflow profile optimization.

## 11.5 Baking Conditions

Products require baking before mounting if:

- Humidity indicator cards read > 30%
- Temp < 30°C, humidity < 70% RH, over 96 hours

Baking condition: 90°C, 12 to 24 hours

Baking times: 1 time


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## 11.6 Soldering and Reflow Condition

- Heating method: Conventional convection or IR convection
- Temperature measurement: Thermocouple d = 0.1 mm to 0.2 mm CA (K) or CC (T) at soldering portion or equivalent method
- Solder paste composition: SAC305
- Allowable reflow soldering times: 2 times based on the reflow soldering profile (see 图 11-1)
- Temperature profile: Reflow soldering will be done according to the temperature profile (see 图 11-1)
- Peak temperature: 260°C

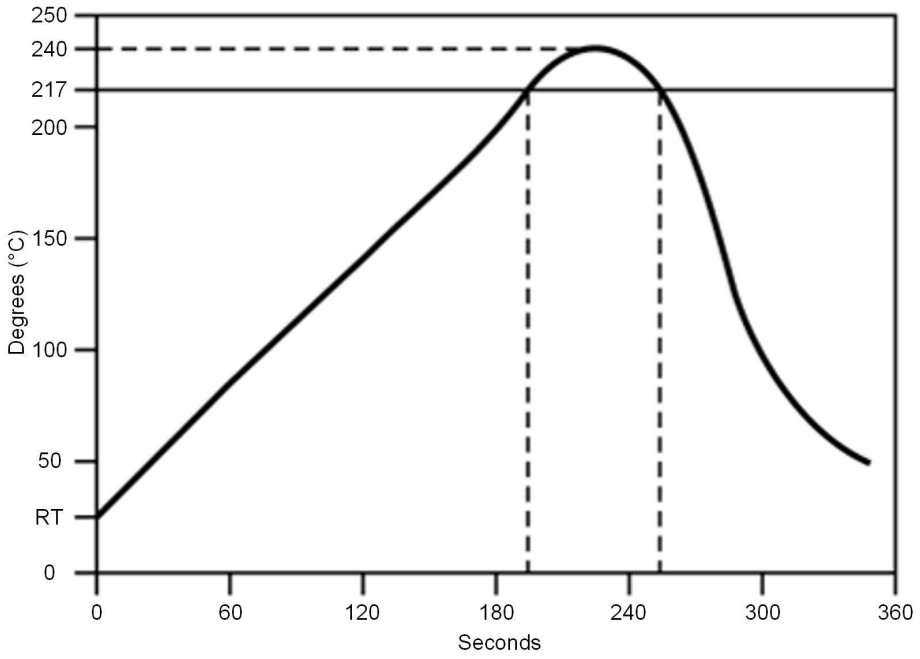



**图 11-1. Temperature Profile for Evaluation of Solder Heat Resistance of a Component (at Solder Joint)**

**表 11-1. Temperature Profile**

| Profile Elements | Convection or IR(1) |
|---|---|
| Peak temperature range | 235 to 240°C typical (260°C maximum) |
| Pre-heat / soaking (150 to 200°C) | 60 to 120 seconds |
| Time above melting point | 60 to 90 seconds |
| Time with 5°C to peak | 30 seconds maximum |
| Ramp up | < 3°C / second |
| Ramp down | < -6°C / second |

(1) For details, refer to the solder paste manufacturer's recommendation.

**备注**

TI does not recommend the use of conformal coating or similar material on the SimpleLink™ module. This coating can lead to localized stress on the solder connections inside the module and impact the module reliability. Use caution during the module assembly process to the final PCB to avoid the presence of foreign material inside the module.

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# 12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed as follows.

## 12.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to all part numbers and/or date-code. Each device has one of three prefixes/identifications: X, P, or null (no prefix) (for example, XCC2652PSIP is in preview; therefore, an X prefix/identification is assigned).

Device development evolutionary flow:

**X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

**P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

**null** Production version of the silicon die that is fully qualified.

Production devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *RGZ*).

For orderable part numbers of *CC2652PSIP* devices in the RGZ (7-mm x 7-mm) package type, see the *Package Option Addendum* of this document, the Device Information in 节 3, the TI website (www.ti.com), or contact your TI sales representative.

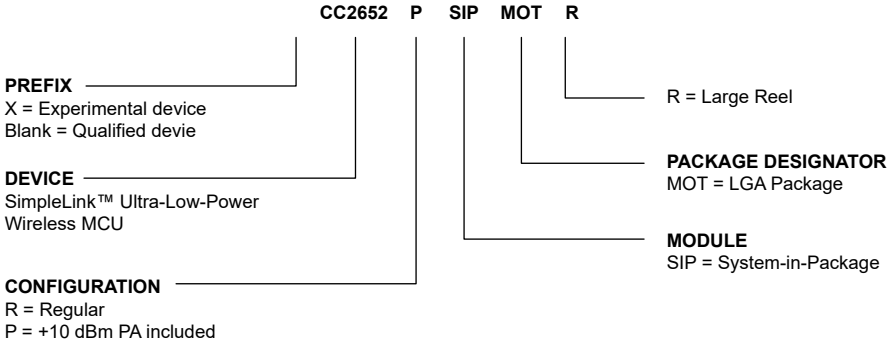



**图 12-1. Device Nomenclature**

## 12.2 Tools and Software

The CC2652PSIP device is supported by a variety of software and hardware development tools.

**Development Kit**

CC2652PSIP LaunchPad™ Development Kit

The CC2652PSIP LaunchPad™ Development Kit enables development of high-performance wireless applications that benefit from low-power operation. The kit features the CC2652PSIP SimpleLink Wireless system-in-Package, which allows you to quickly evaluate and prototype 2.4-GHz wireless applications such as Bluetooth 5 Low Energy, Zigbee and Thread, plus combinations of these. The kit works with the LaunchPad ecosystem, easily enabling additional functionality like sensors, display and more. The built-in EnergyTrace™


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software is an energy-based code analysis tool that measures and displays the application's energy profile and helps to optimize it for ultra-low-power consumption.

## Software

SimpleLink™ CC13XX-CC26XX SDK

The SimpleLink CC13XX-CC26XX Software Development Kit (SDK) provides a complete package for the development of wireless applications on the CC13X2 / CC26X2 family of devices. The SDK includes a comprehensive software package for the CC2652PSIP device, including the following protocol stacks:

- Bluetooth Low Energy 4 and 5.2
- Thread (based on OpenThread)
- Zigbee 3.0
- TI 15.4-Stack - an IEEE 802.15.4-based star networking solution for Sub-1 GHz and 2.4 GHz
- EasyLink - a large set of building blocks for building proprietary RF software stacks
- Multiprotocol support - concurrent operation between stacks using the Dynamic Multiprotocol Manager (DMM)

The SimpleLink CC13XX-CC26XX SDK is part of TI's SimpleLink MCU platform, offering a single development environment that delivers flexible hardware, software and tool options for customers developing wired and wireless applications. For more information about the SimpleLink MCU Platform, visit http://www.ti.com/simplelink.

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## Development Tools

**Code Composer Studio™ Integrated Development Environment (IDE)**

Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse® software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

CCS has support for all SimpleLink Wireless MCUs and includes support for EnergyTrace™ software (application energy usage profiling). A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK.

Code Composer Studio is provided free of charge when used in conjunction with the XDS debuggers included on a LaunchPad Development Kit.

**Code Composer Studio™ Cloud IDE**

Code Composer Studio (CCS) Cloud is a web-based IDE that allows you to create, edit and build CCS and Energia™ projects. After you have successfully built your project, you can download and run on your connected LaunchPad. Basic debugging, including features like setting breakpoints and viewing variable values is now supported with CCS Cloud.

**IAR Embedded Workbench® for Arm®**

IAR Embedded Workbench® is a set of development tools for building and debugging embedded system applications using assembler, C and C++. It provides a completely integrated development environment that includes a project manager, editor, and build tools. IAR has support for all SimpleLink Wireless MCUs. It offers broad debugger support, including XDS110, IAR I-jet™ and Segger J-Link™. A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK. IAR is also supported out-of-the-box on most software examples provided as part of the SimpleLink SDK.

A 30-day evaluation or a 32 KB size-limited version is available through iar.com.

**SmartRF™ Studio**

SmartRF™ Studio is a Windows® application that can be used to evaluate and configure SimpleLink Wireless MCUs from Texas Instruments. The application will help designers of RF systems to easily evaluate the radio at an early stage in the design process. It is especially useful for generation of configuration register values and for practical testing and debugging of the RF system. SmartRF Studio can be used either as a standalone application or together with applicable evaluation boards or debug probes for the RF device. Features of the SmartRF Studio include:

- Link tests - send and receive packets between nodes
- Antenna and radiation tests - set the radio in continuous wave TX and RX states
- Export radio configuration code for use with the TI SimpleLink SDK RF driver
- Custom GPIO configuration for signaling and control of external switches

**Sensor Controller Studio**

Sensor Controller Studio is used to write, test and debug code for the Sensor Controller peripheral. The tool generates a Sensor Controller Interface driver, which is a set of C source files that are compiled into the System CPU application. These source files also contain the Sensor Controller binary image and allow the System CPU application to control and exchange data with the Sensor Controller. Features of the Sensor Controller Studio include:

- Ready-to-use examples for several common use cases
- Full toolchain with built-in compiler and assembler for programming in a C-like programming language


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- Provides rapid development by using the integrated sensor controller task testing and debugging functionality, including visualization of sensor data and verification of algorithms

CCS UniFlash — CCS UniFlash is a standalone tool used to program on-chip flash memory on TI MCUs. UniFlash has a GUI, command line, and scripting interface. CCS UniFlash is available free of charge.

### 12.2.1 SimpleLink™ Microcontroller Platform

The SimpleLink microcontroller platform sets a new standard for developers with the broadest portfolio of wired and wireless Arm® MCUs (System-on-Chip) in a single software development environment. Delivering flexible hardware, software and tool options for your IoT applications. Invest once in the SimpleLink software development kit and use throughout your entire portfolio. Learn more on ti.com/simplelink.

## 12.3 Documentation Support

To receive notification of documentation updates on data sheets, errata, application notes and similar, navigate to the device product folder on ti.com/product/CC2652PSIP. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the MCU, related peripherals, and other technical collateral is listed as follows.

**TI Resource Explorer**

TI Resource Explorer — Software examples, libraries, executables, and documentation are available for your device and development board.

**Errata**

*CC2652PSIP Silicon Errata* — The silicon errata describes the known exceptions to the functional specifications for each silicon revision of the device and description on how to recognize a device revision.

**Application Reports**

All application reports for the CC2652PSIP device are found on the device product folder at: ti.com/product/CC2652PSIP/technicaldocuments.

**Technical Reference Manual (TRM)**

*CC13xx, CC26xx SimpleLink™ Wireless MCU TRM* — The TRM provides a detailed description of all modules and peripherals available in the device family.

## 12.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

## 12.5 Trademarks

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## 12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。


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# 13 Mechanical, Packaging, and Orderable Information

## 13.1 Packaging Information

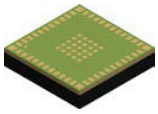
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**备注**

The total height of the module is 1.51 mm.

The weight of the CC2652PSIP module is typically 0.186 g.

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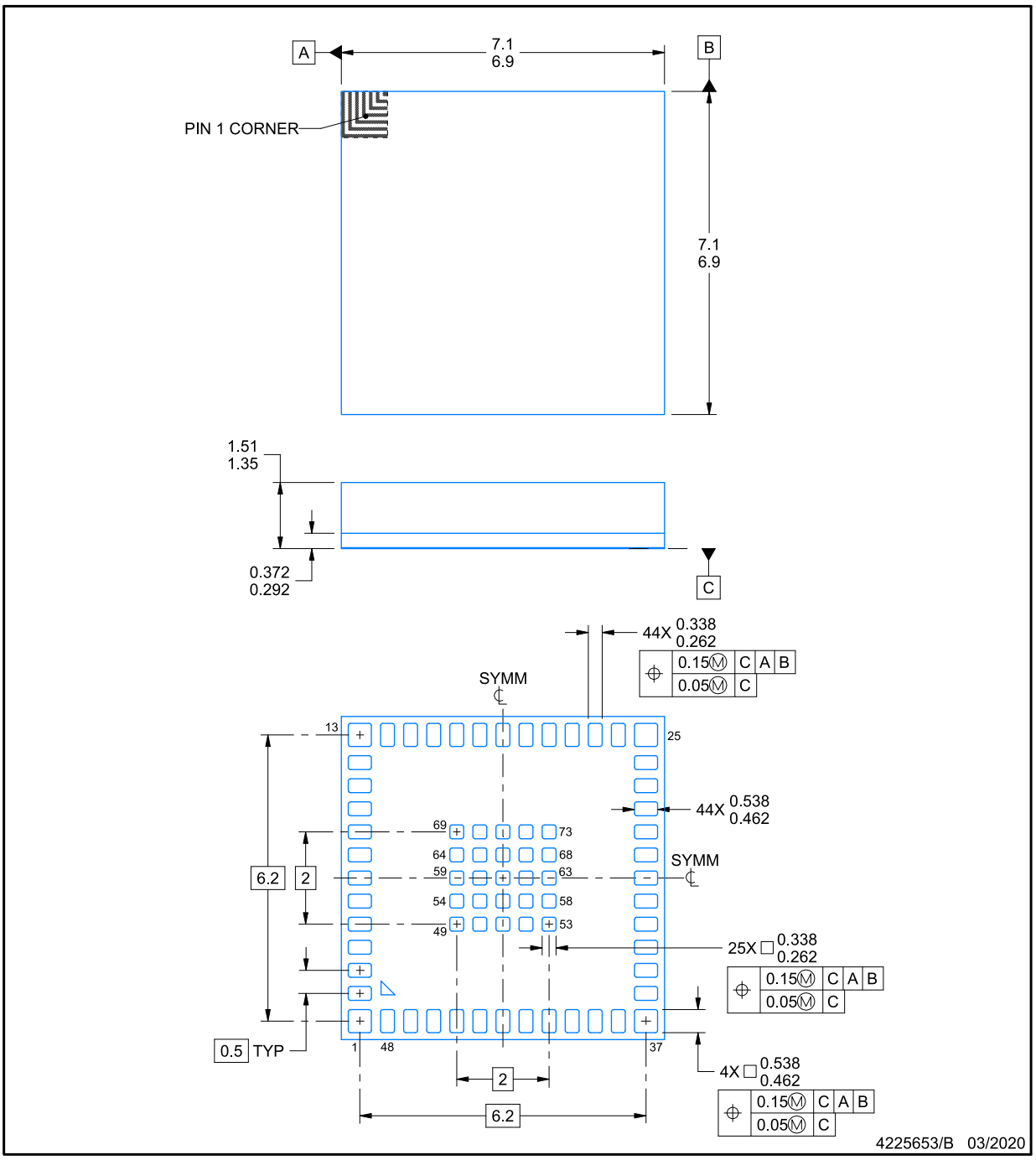


# PACKAGE OUTLINE

## MOT0048A

## QFM - 1.51 mm max height

QUAD FLAT MODULE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

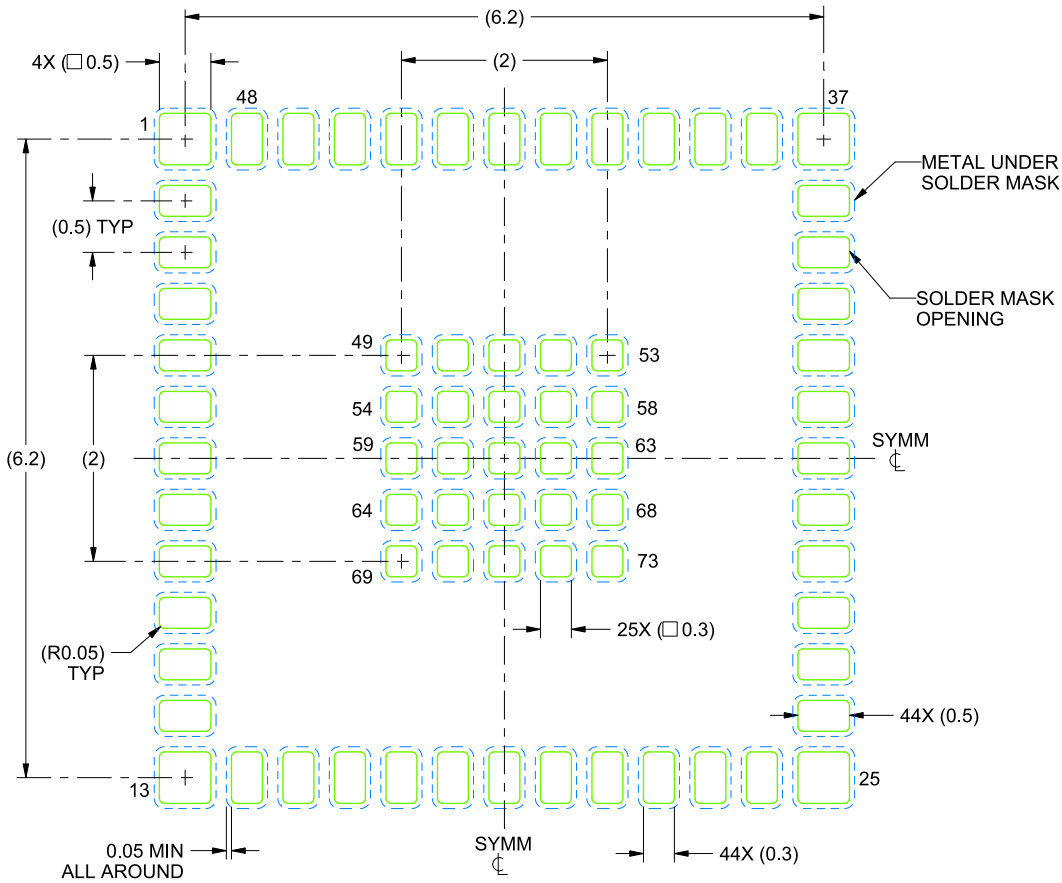

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# EXAMPLE BOARD LAYOUT

## MOT0048A

## QFM - 1.51 mm max height

QUAD FLAT MODULE




LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:15X

4225653/B 03/2020

NOTES: (continued)

3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

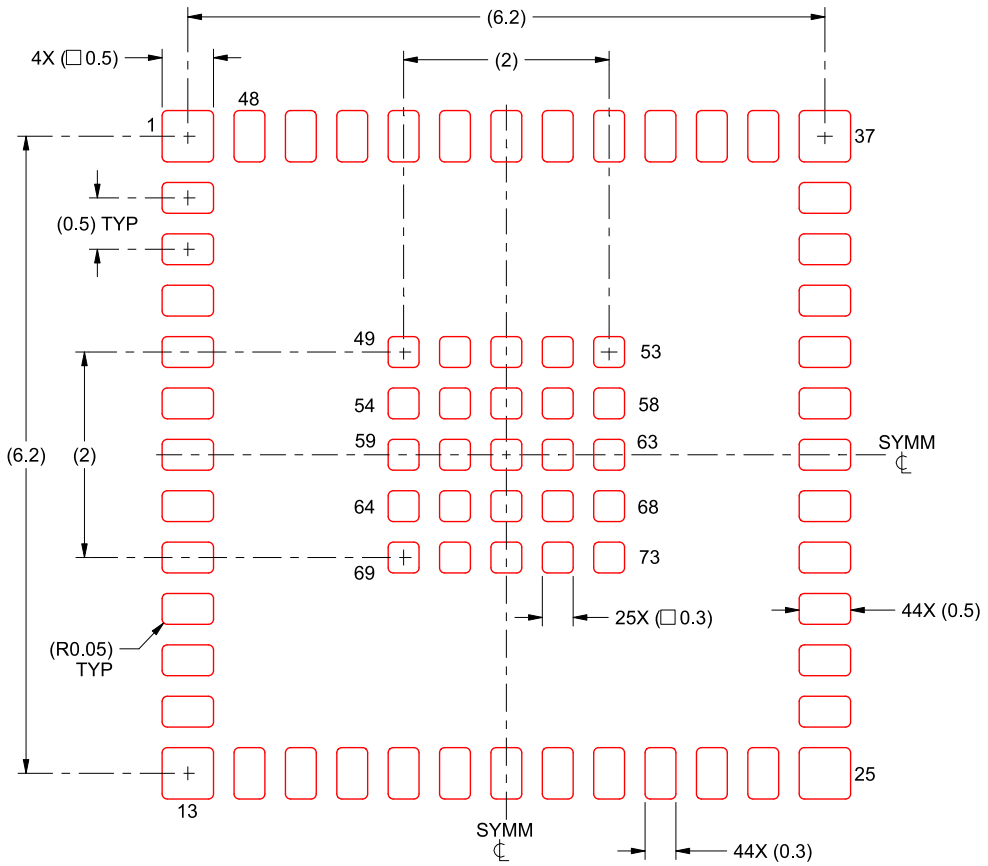
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# EXAMPLE STENCIL DESIGN

## MOT0048A

**QFM - 1.51 mm max height**

QUAD FLAT MODULE




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4225653/B 03/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| CC2652PSIPMOTR | Active | Production | QFM (MOT) \| 48 | 2000 \| LARGE T&R | Yes | ENEPIG | Level-3-260C-168 HR | -40 to 105 | CC2652 P SIP |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

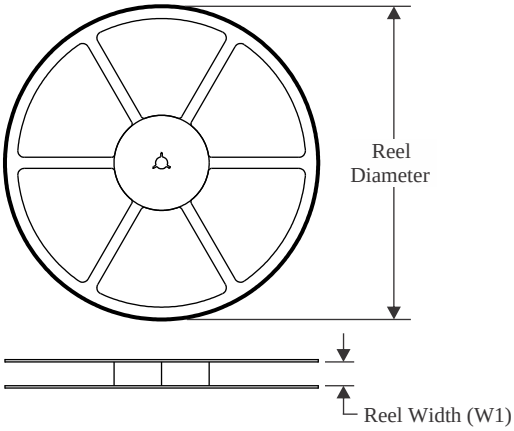
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

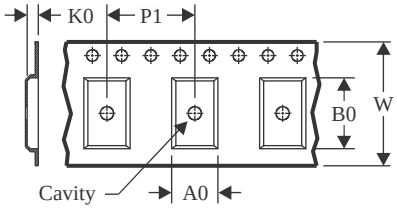
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

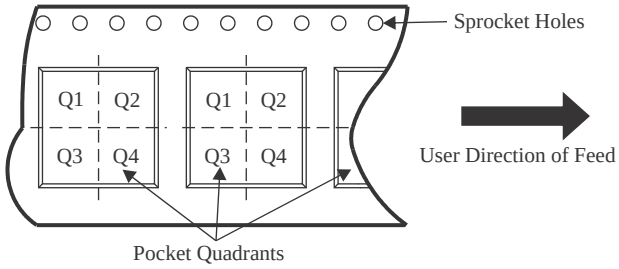



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

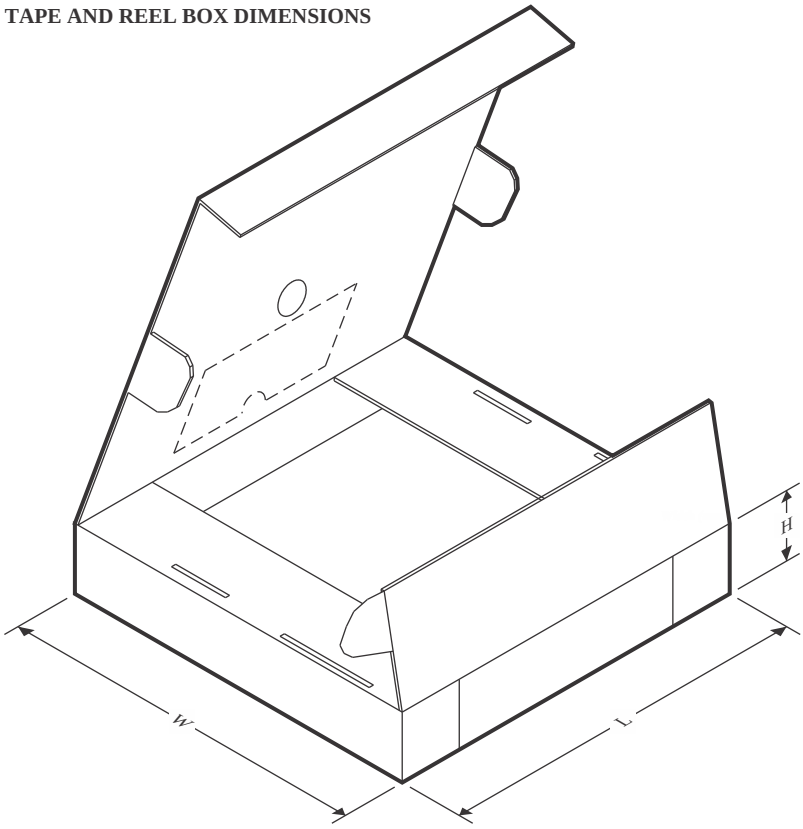
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CC2652PSIPMOTR | QFM | MOT | 48 | 2000 | 330.0 | 16.4 | 7.4 | 7.4 | 1.88 | 12.0 | 16.0 | Q1 |

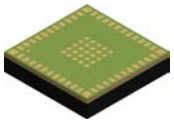
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CC2652PSIPMOTR | QFM | MOT | 48 | 2000 | 336.6 | 336.6 | 31.8 |

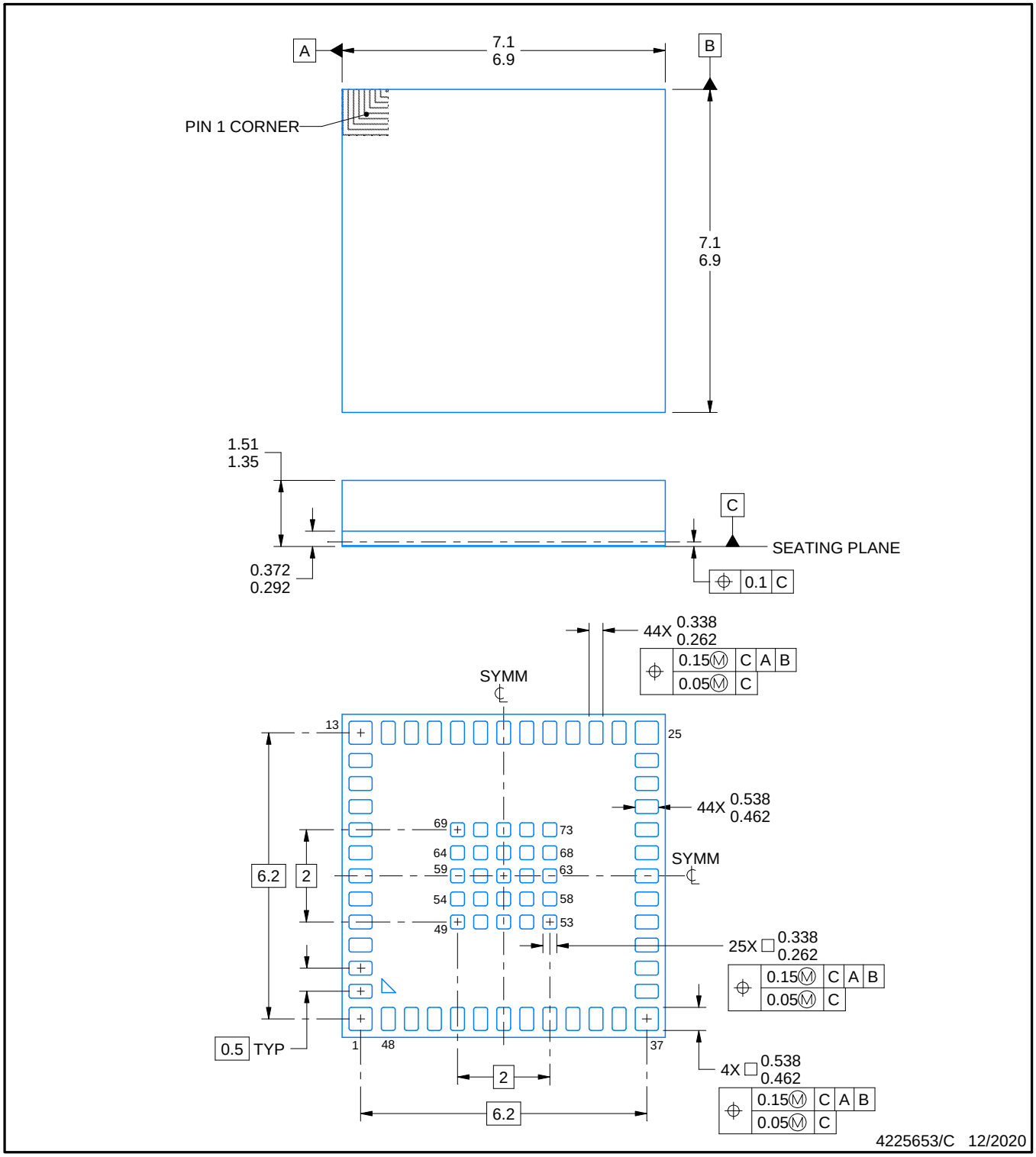
# MOT0048A



# PACKAGE OUTLINE

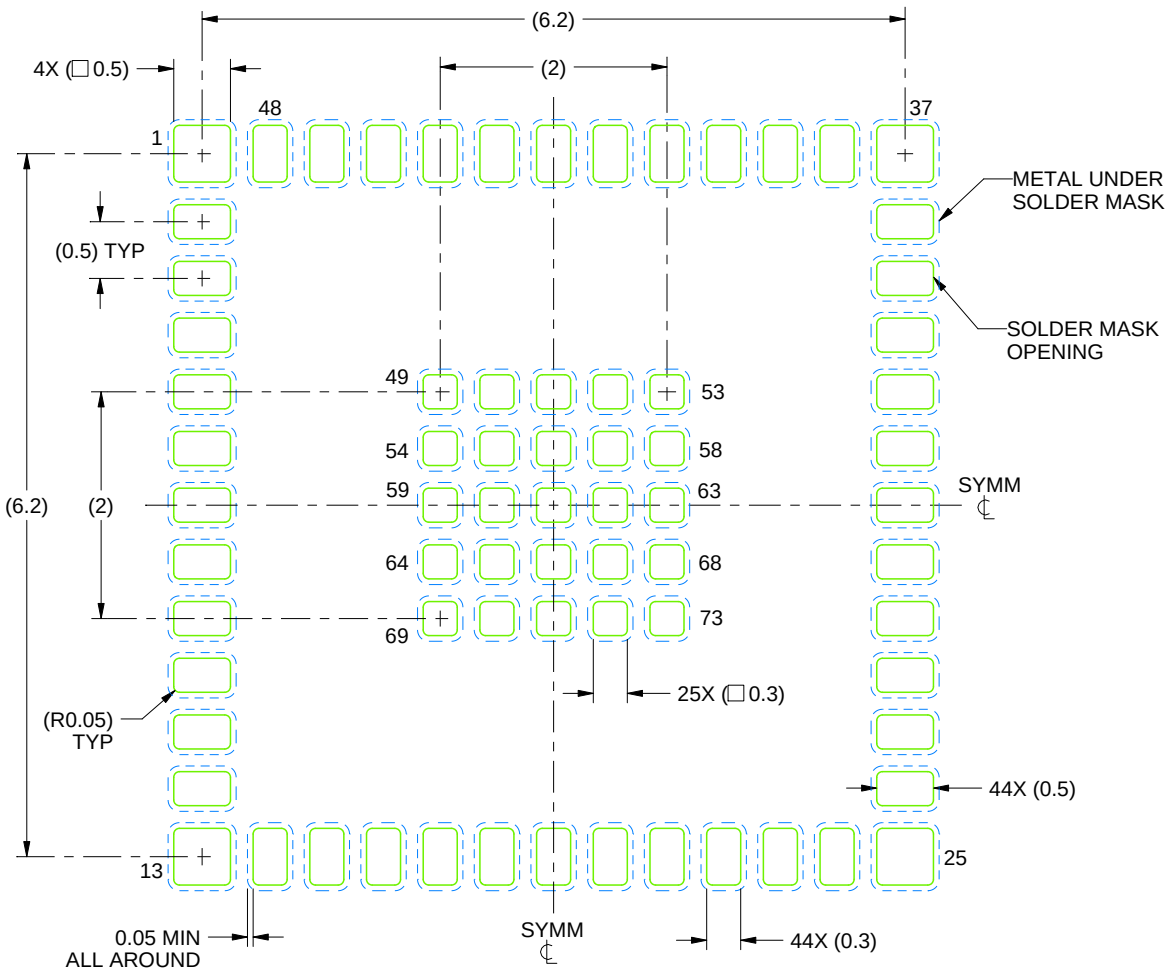
## QFM - 1.51 mm max height

QUAD FLAT MODULE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:15X

4225653/C 12/2020

NOTES: (continued)

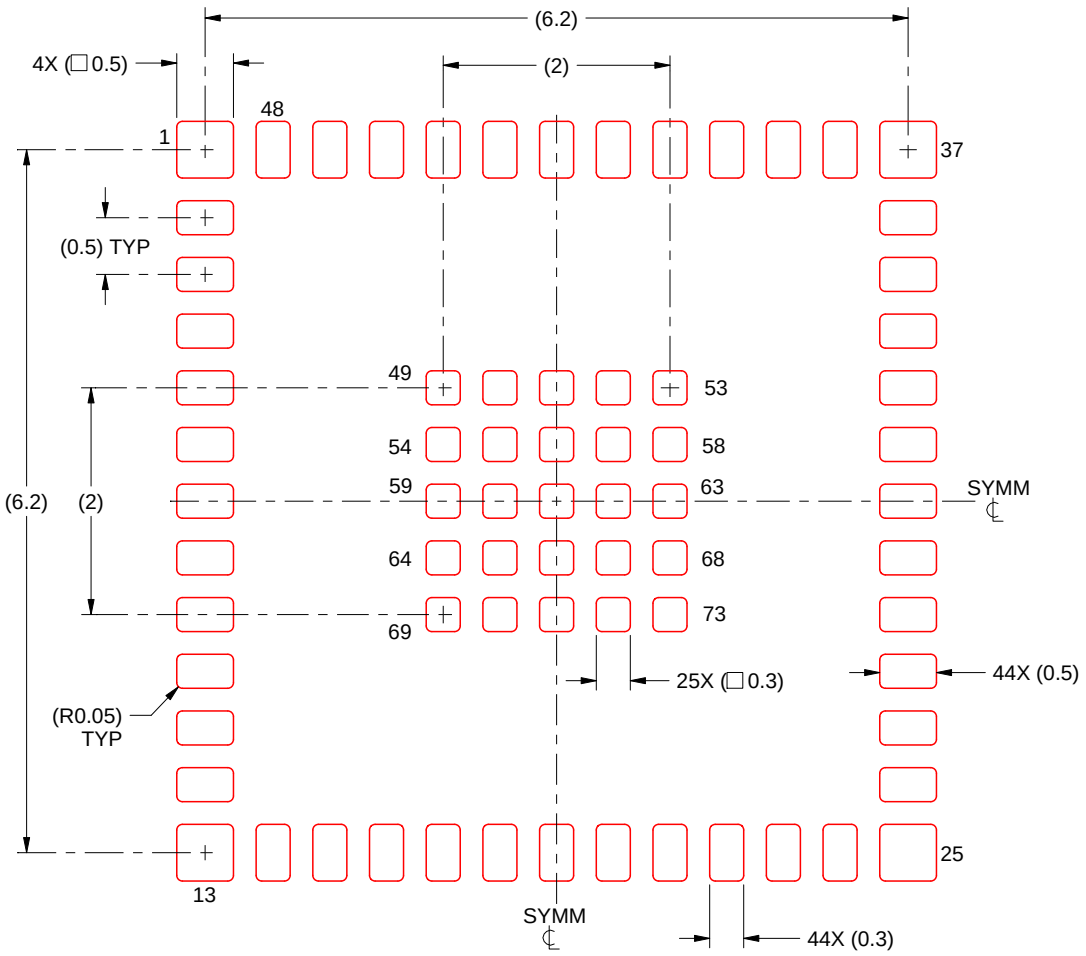
3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

# EXAMPLE STENCIL DESIGN

## MOT0048A

## QFM - 1.51 mm max height

QUAD FLAT MODULE




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4225653/C 12/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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