



CD4536 CMOS Programmable Timer

1. General Description

1.1 Description

CD4536BMS is a programmable timer consisting of 24 ripple binary counter stages. The salient feature of this device is its flexibility. The device can count from 1 to 224 or the first 8 stages can be bypassed to allow an output, selectable by a 4-bit code, from any one of the remaining 16 stages. It can be driven by an external clock or an RC oscillator that can be constructed using on-chip components. Input IN1 serves as either the external clock input or the input to the on-chip RC oscillator. OUT1 and OUT2 are connection terminals for the external RC components. In addition, an on-chip monostable circuit is provided to allow a variable pulse width output. Various timing functions can be achieved using combinations of these capabilities.

A logic 1 on the 8-BYPASS input enables a bypass of the first 8 stages and makes stage 9 the first counter stage of the last 16 stages. Selection of 1 of 16 outputs is accomplished by the decoder and the BCD inputs A, B, C and D. MONO IN is the timing input for the on-chip monostable oscillator. Grounding of the MONO IN terminal through a resistor of 10k Ω or higher, disables the one-shot circuit and connects the decoder directly to the DECODE OUT terminal. A resistor to VDD and a capacitor to ground from the MONO IN terminal enables the one-shot circuit and controls its pulse width.

A fast test mode is enabled by a logic 1 on 8-BYPASS, SET, and RESET. This mode divides the 24-stage counter into three 8-stage sections to facilitate a fast test sequence.

1.2 Features

- 24 flip-flop stages —counts from 2^0 to 2^{24}
- Last 16 stages selectable by BCD select code.
- Bypass input allows bypassing first 8 stages
- On-chip RC oscillator provision
- Clock inhibit input
- Schmitt-trigger in clock line permits operation with very long rise and fall times
- On-chip monostable output provision
- Test mode allows fast test sequence
- Set and reset inputs
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 18V
- 5V, 10V, and 15V parametric ratings

1.3 Device Information

PART NUMBER	PACKAGE
CD4536	DIP
	SOP
	TSSOP

2. Pin Description and Functional Diagram

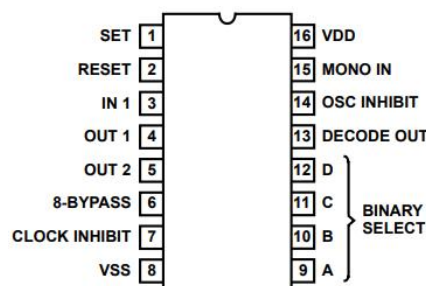


Figure 2.1 Top View

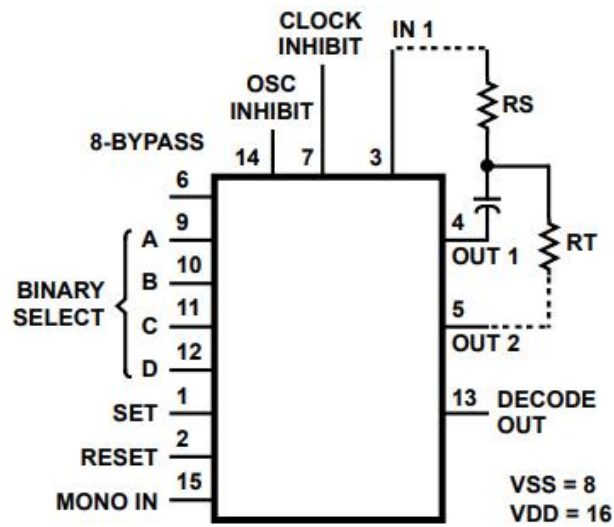


Figure 2.2 Functional Diagram

PIN No.	NAME	I/O	FUNCTION
1	SET	I	Set Input
2	RESET	I	Reset Input
3	IN1	I	Data Input
4	OUT1	O	Buffer Output
5	OUT2	O	Buffer Output
6	8-BYPASS	I	Bypass Input
7	CLOCK INHIBIT	I	Clock Inhibit Input
8	VSS		Ground
9	A	I	Binary Select Input
10	B	I	Binary Select Input
11	C	I	Binary Select Input
12	D	I	Binary Select Input
13	DECODE OUT	O	Decode output
14	OSC INHIBIT	I	OSC Inhibit Input
15	MONO IN	I	Timing Input for The On-Chip Monostable Multivibrator
16	VDD		Supply Voltage

3. System Diagram

3.1 Logic Diagram

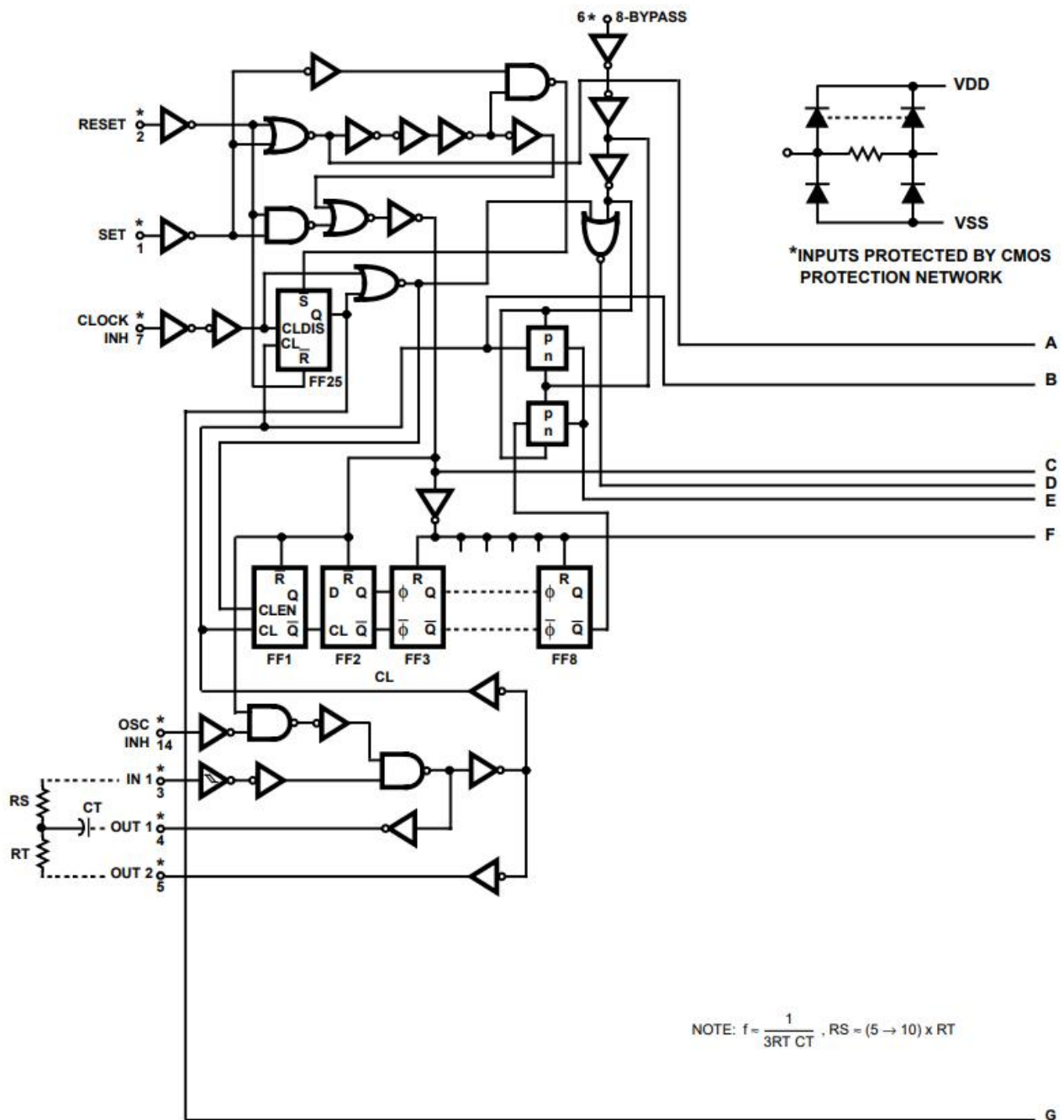
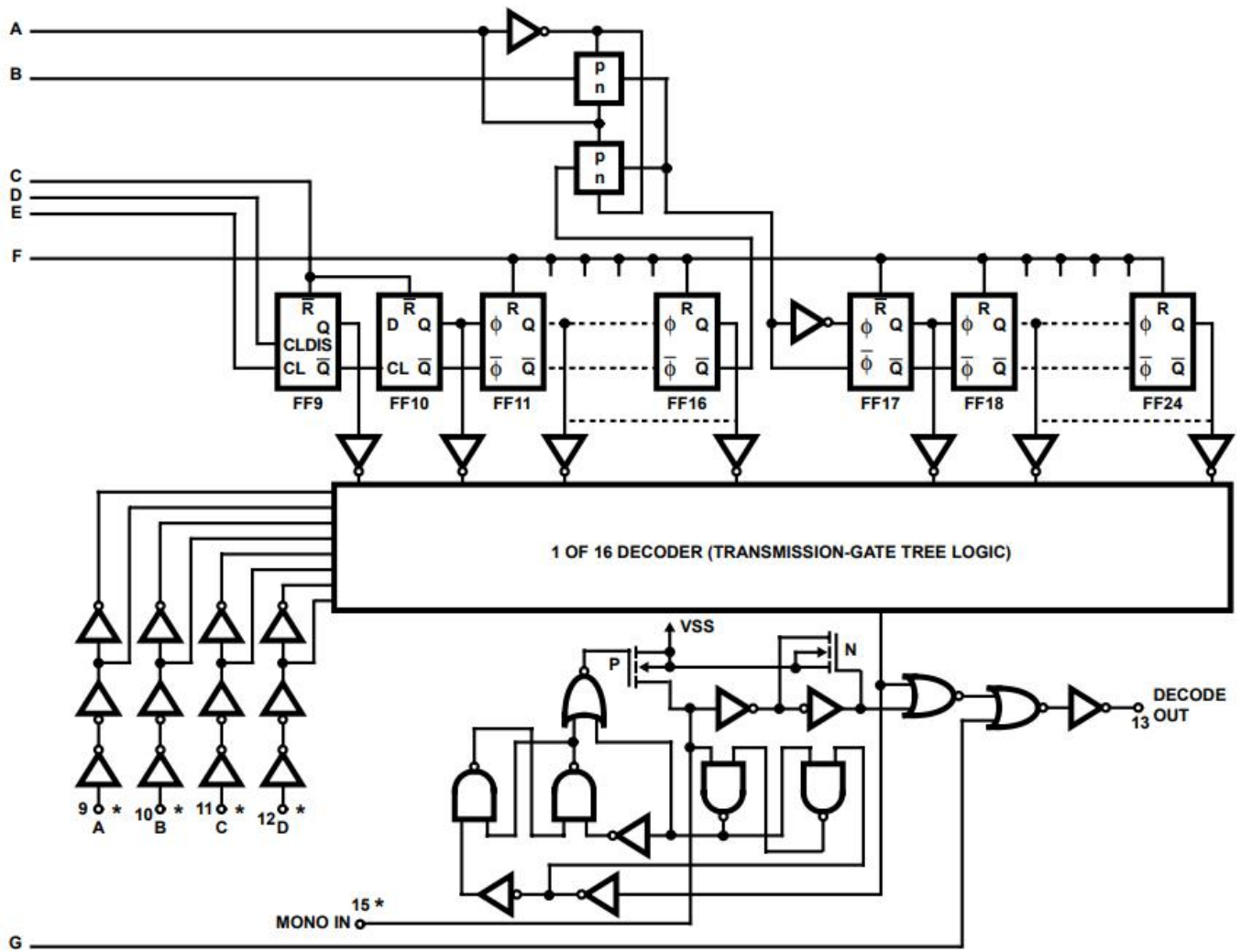
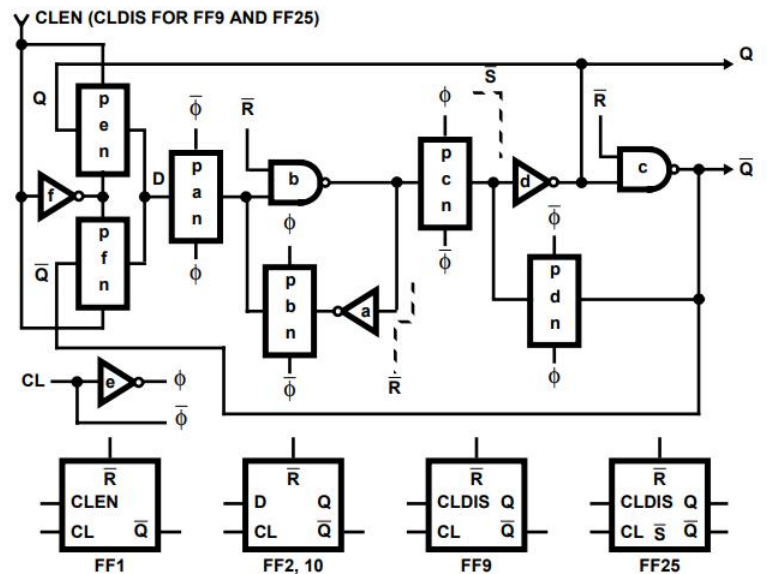
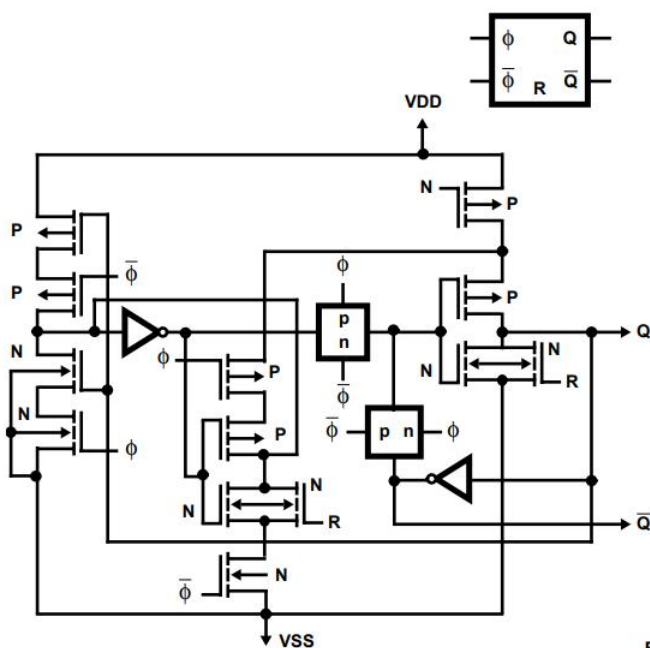


Figure 3.1: CD4536 Logic Diagram



DETAIL FOR
FF3-8, 11-16, 17-24

DETAIL FOR
FF1, FF2, FF10, FF9, FF25



FF1: AS SHOWN EXCEPT Q NOT BROUGHT OUT

FF9: SAME AS FF1 EXCEPT Q IS BROUGHT OUT AND Q, $\bar{Q}$ GO TO TgF AND TGe RESP.

FF2, FF10: DELETE TGe, TgF, AND INVf; FEED $\bar{Q}$ TO D; DELETE CLEN, CLDIS

FF25: INVa AND INVd BECOME 2-INPUT NAND GATES, WITH ADDED INPUTS $\bar{S}$; FEED Q TO TgF VSS TO TGe PREVIOUS Q INPUT; DELETE $\bar{Q}$ OUTPUT

Figure 3.1: CD4536 Logic Diagram (Continued)



3.2 Truth Table

Input					Output		
IN	SET	RESET	CLOCK INH	OSC INH	OUT1	OUT2	DECODE OUT
↑	0	0	0	0	↑	↓	No Change
↓	0	0	0	0	↓	↑	Advance to Next State
X	1	0	0	0	0	1	1
X	0	1	0	0	0	1	0
X	0	0	1	0			No Change
0	0	0	0	X	0	1	No Change
1	0	0	0	↑	↓	↑	Advance to Next State

X = Don't Care, 1 ≡ High State, 0 ≡ Low State, ↑=positive-going transition, ↓=negative-going transition

3.3 Decode Out Selection Table

D	C	B	A	Numbers of Stages in Divider Chain	
				8-BYPASS = 0	8-BYPASS = 1
0	0	0	0	9	1
0	0	0	1	10	2
0	0	1	0	11	3
0	0	1	1	12	4
0	1	0	0	13	5
0	1	0	1	14	6
0	1	1	0	15	7
0	1	1	1	16	8
1	0	0	0	17	9
1	0	0	1	18	10
1	0	1	0	19	11
1	0	1	1	20	12
1	1	0	0	21	13
1	1	0	1	22	14
1	1	1	0	23	15
1	1	1	1	24	16

1 ≡ High State, 0 ≡ Low State



4. Specifications

4.1 Absolute Maximum Ratings

Symbol	Parameter	MIN	MAX	Unit
V _{DD}	DC Supply Voltage Range (Voltage Referenced to VSS Terminals)	-0.5	20	V
V _I	Input Voltage Range, All Inputs	0.5	V _{DD} +0.5	V
P _D	Power Dissipation		500	mW
T _J	Junction Temperature		125	°C
T _{OP}	Operating Temperature	-40	85	°C

Absolute maximum ratings are those values beyond which the device could be permanently damaged. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions.

4.2 Electrical Characteristics

4.2.1 DC Specifications

(T_a=25°C, voltages are referenced to VSS (ground=0V), unless otherwise specified)

Symbol	Parameter	Test Condition			MIN	TYP	MAX	Unit
		V _O	V _{IN}	V _{DD}				
I _{DD}	Supply Current	--	0,5	5	--	0	1	uA
		--	0,10	10	--	0	1	uA
		--	0,18	18	--	0	1	uA
I _{OL}	Low Level Output Current	0.4	0,5	5	1	3	--	mA
		0.5	0,10	10	3	7	--	mA
		1.5	0,15	15	13	26	--	mA
I _{OH}	High Level Output Current	4.6	0,5	5	-0.5	-1.5	--	mA
		2.5	0,5	5	-3	-6	--	mA
		9.5	0,10	10	-1.5	-3	--	mA
		13.5	0,15	15	-6	-12	--	mA
V _{OL}	Low Level Output Voltage	--	0,5	5	--	0	0.05	V
		--	0,10	10	--	0	0.05	V
		--	0,15	15	--	0	0.05	V
V _{OH}	High Level Output Voltage	--	0,5	5	4.95	5	--	V
		--	0,10	10	9.95	10	--	V
		--	0,15	15	14.95	15	--	V
V _{IL}	Low Level Input Voltage	0.5,4.5	--	5	--	--	1.5	V
		1,9	--	10	--	--	3	V
		1.5,13.5	--	15	--	--	4	V
V _{IH}	High Level Input Voltage	0.5,4.5	--	5	3.5	--	--	V
		1,9	--	10	7	--	--	V
		1.5,13.5	--	15	11	--	--	V
I _{IN}	Input Leakage Current	--	0,18	18	--	0	±1	uA

5. Applications information

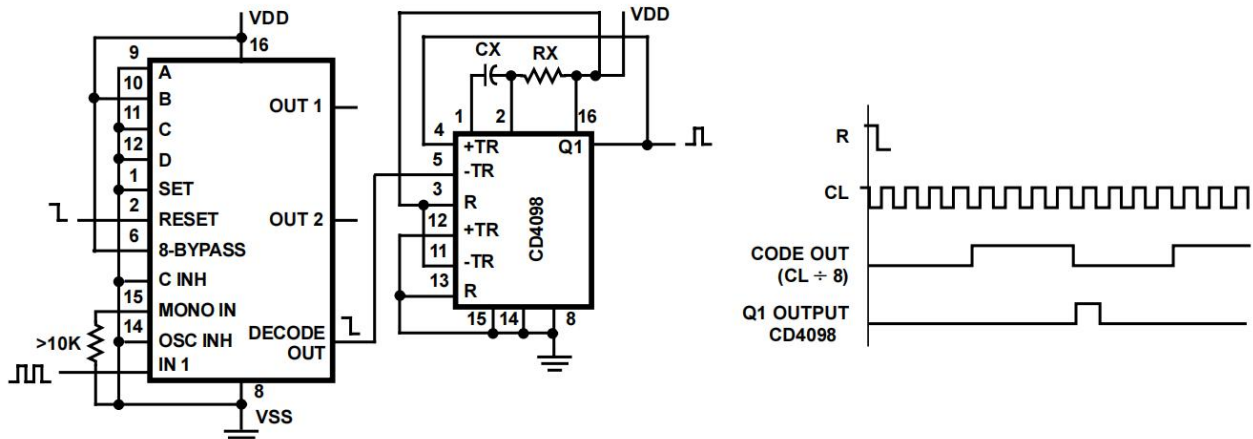


Figure 5.1: Application showing use of CD4098 and CD4536 to get decode pulse 8 clock pulses after Reset pulse.

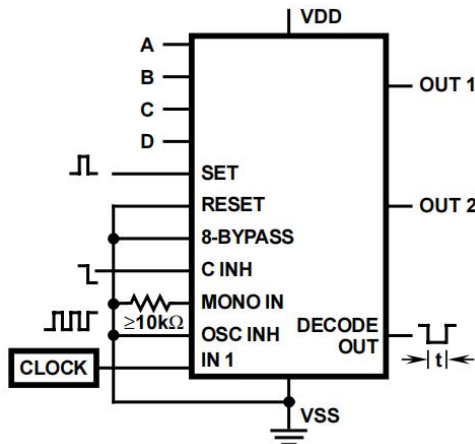


Figure 5.2: Time interval configuration using external clock; set and clock inhibit functions.

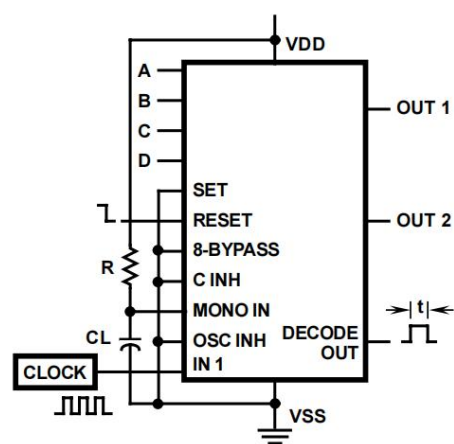


Figure 5.3: Time interval configuration using external clock; reset and output mono-stable to achieve a pulse output.

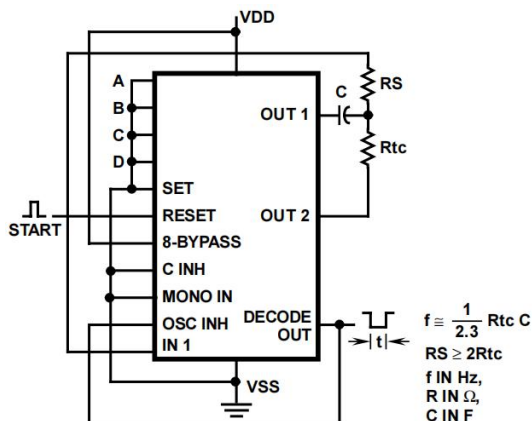


Figure 5.4: Time interval configuration using on-chip AC oscillator and reset input to initiate time interval.

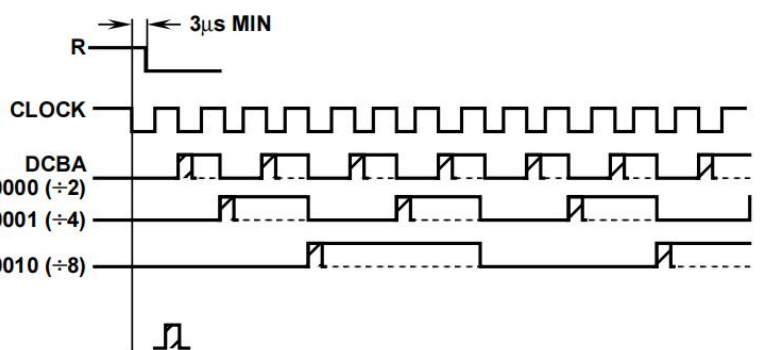


Figure 5.5: CD4536 timing diagram

NOTE:

SHADED PULSE REPRESENTS DECODE OUTPUT IN MONOSTABLE MODE. IF AN OUTPUT PULSE IS REQUIRED 1 FULL-COUNT-DOWN AFTER REMOVAL OF RESET PULSE, SEE FIGURE 5.1 FOR USE OF CD4098.



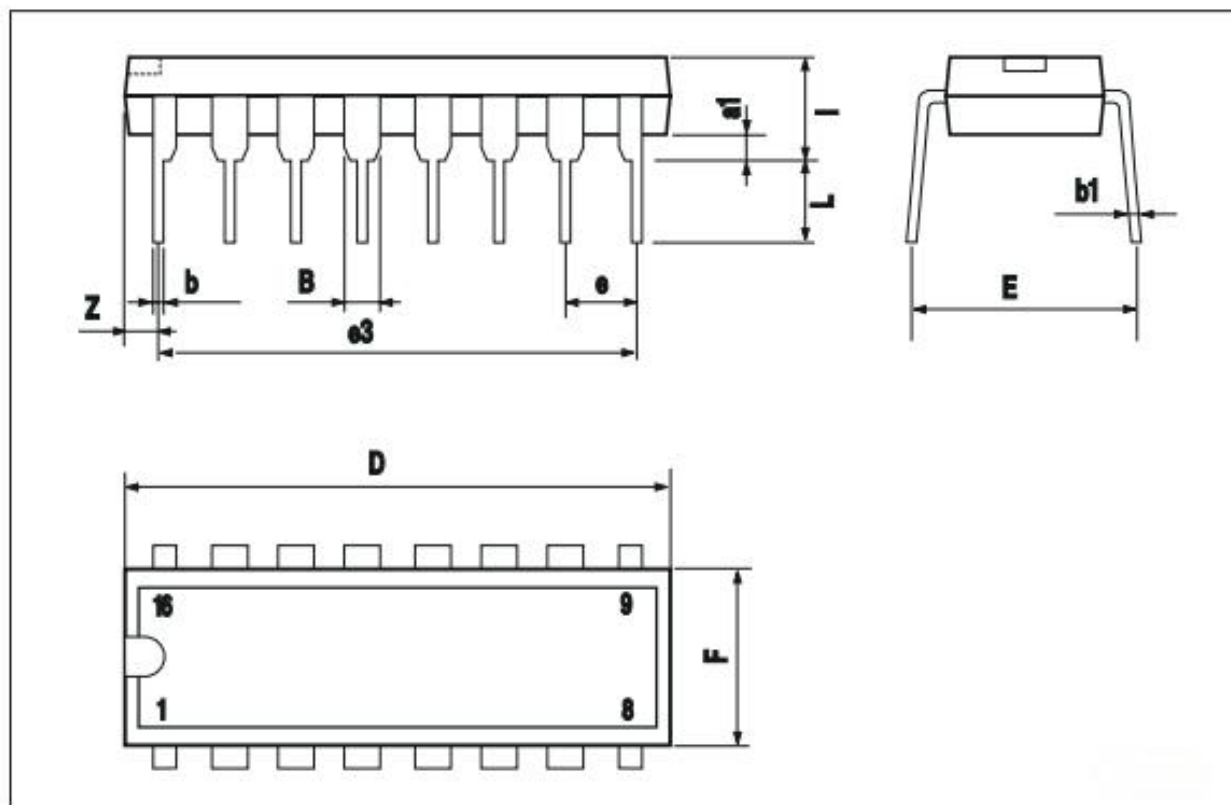
6. Ordering Information

Orderable Device	Package Type	Pins	Packing	Package Qty
CD4536ND16ATBE	DIP	16	Tube	25
CD4536NS16ARDQ	SOP	16	Tape & Reel	4000
CD4536TS16ARDQ	TSSOP	16	Tape & Reel	4000

7. Package Information

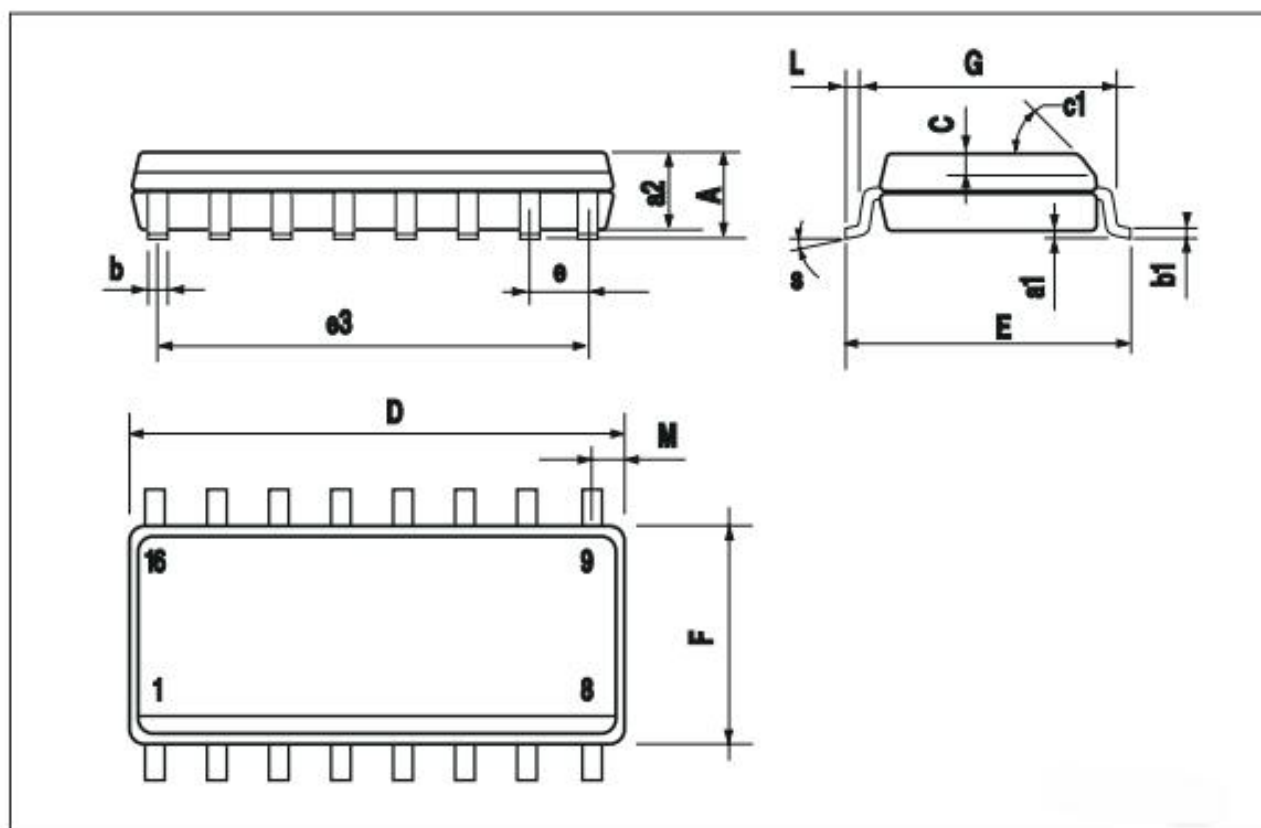
7.1 DIP16

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



7.2 SOP16

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.25	0.004		0.010
a2			1.64			0.063
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



7.3 TSSOP16

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

