

DATASHEET

N-Channel Enhancement Mode Power MOSFET

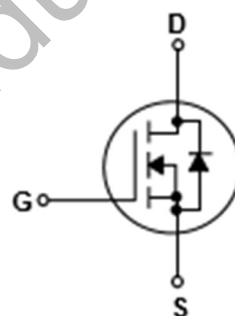
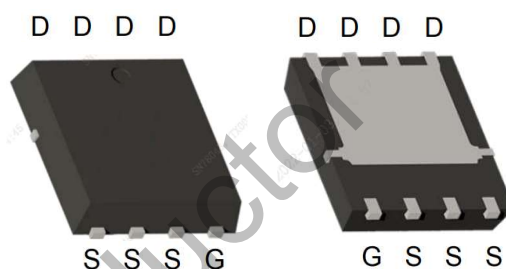
Description

This Power MOSFET is produced using advanced SGT technology. This advanced technology has been especially tailored to minimize conduction loss, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

Features

- $V_{DS}=60V$, $I_D=230A$
- $R_{DS(ON)} TYP = 1.2m\Omega @V_{GS}=10V$
- Very Low On-resistance $R_{DS(ON)}$
- Low C_{rss}
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

PDFN5*6-8L



Schematic

Applications

- PWM Application
- Load Switch
- Power Management

100% UIS TESTED!

100% ΔV_{ds} TESTED!



Package Marking and Ordering Information

Device	Marking	Package	Packing	Reel size	Reel (pcs)	Per Carton (pcs)
012N06		PDFN5*6	Reel	13inch	5000	60000

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Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C=25^{\circ}\text{C}$	I_D	230	A
	$T_C=100^{\circ}\text{C}$		160	
Pulsed Drain Current($T_C=25^{\circ}\text{C}$, T_p Limited By T_{jmax}) ^(note1)		I_{DM}	460	A
Maximum Power Dissipation($T_C=25^{\circ}\text{C}$)		P_D	166	W
Avalanche energy , single Pulse($L=0.5\text{mH}$) ^(note2)		E_{AS}	543	mJ
Thermal Resistance Junction to Case		$R_{\theta JC}$	1.2	$^{\circ}\text{C}/\text{W}$
Operating Junction And Storage Temperature		T_j, T_{stg}	-55 To 150	$^{\circ}\text{C}$
Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		T_L	300	$^{\circ}\text{C}$

* Drain current limited by maximum junction temperature.

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition: $T_J=25^{\circ}\text{C}$, $I_{AS}=45\text{A}$, $V_{GS}=10\text{V}$, $L=0.5\text{mH}$,
3. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 0.5\%$

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Electrical Characteristic (TC=25°C unless otherwise noted)

Parameter	Symbol	Value			Unit	Test Condition
		Min.	Typ.	Max.		
Off Characteristic						
Drain-source breakdown voltage	BV_{DSS}	60	-	-	V	$V_{GS}=0V, I_D=250\mu A$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=60V, V_{GS}=0V$
Gate-source leakage current	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
On Characteristics						
Gate threshold voltage	$V_{GS(th)}$	2.2	2.9	3.5	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.2	1.5	m Ω	$V_{GS}=10V, I_D=20A$
Dynamic Characteristic						
Input Capacitance	C_{iss}	-	7350	-	PF	$V_{GS}=0V, V_{DS}=30V, f=1.0MHz$
Output Capacitance	C_{oss}	-	1850	-		
Reverse Transfer Capacitance	C_{rss}	-	92	-		
Switching Characteristics						
Turn-on delay time	$t_{d(on)}$	-	31	-	nS	$V_{GS}=10V, V_{DS}=30V, I_D=30A, R_G=25\Omega$
Turn-on Rise time	t_r	-	28.1	-		
Turn-off delay time	$t_{d(off)}$	-	87	-		
Turn-off Fall time	t_f	-	27	-		
Gate Total Charge	Q_G	-	105	-	nC	$V_{GS}=10V, V_{DS}=30V, I_D=30A$
Gate-Source Charge	Q_{gS}	-	34	-		
Gate-Drain Charge	Q_{gd}	-	25	-		
Drain-Source Diode Characteristics						
Body Diode Forward Voltage	V_{SD}	-	-	1.2	V	$V_{GS}=0V, I_{SD}=20A, T_J=25^{\circ}C$
Body Diode Forward Current	I_S	-	-	160	A	-
Body Diode Reverse Recovery Time	T_{rr}	-	71	-	ns	$T_J=25^{\circ}C, I_{SD}=20A, V_{GS}=0V, di/dt=100A/\mu s$
Body Diode Reverse Recovery Charge	Q_{rr}	-	113	-	nC	

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Typical Electrical & Thermal Characteristics

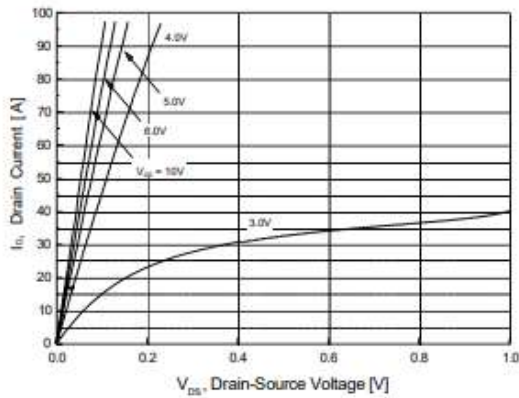


Fig.1 On-Region Characteristics

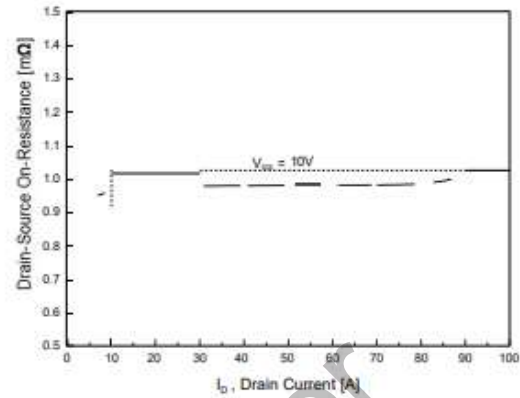


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

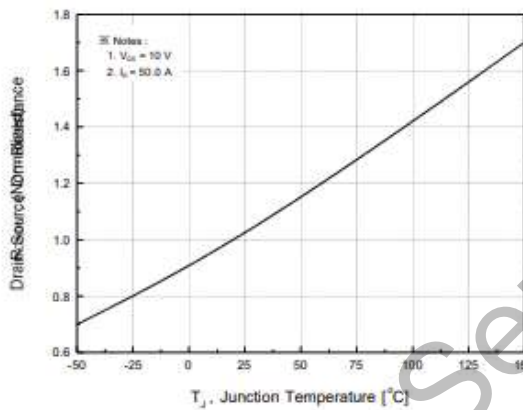


Fig.3 On-Resistance Variation with Temperature

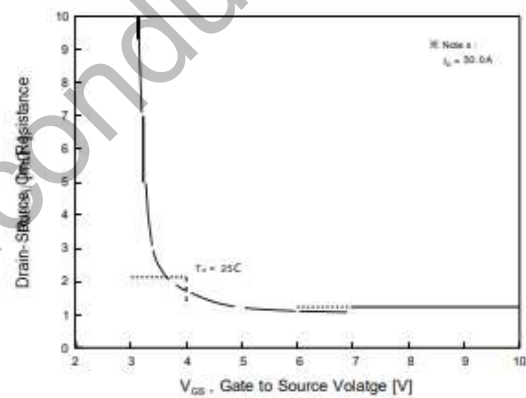
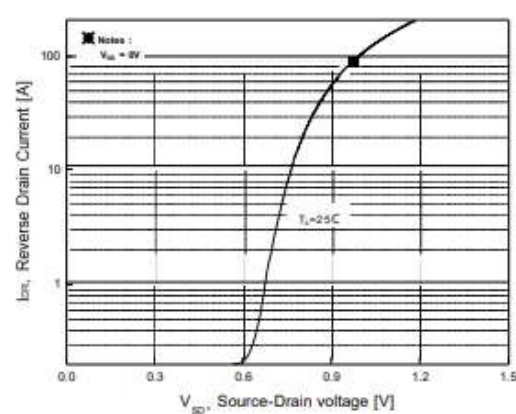
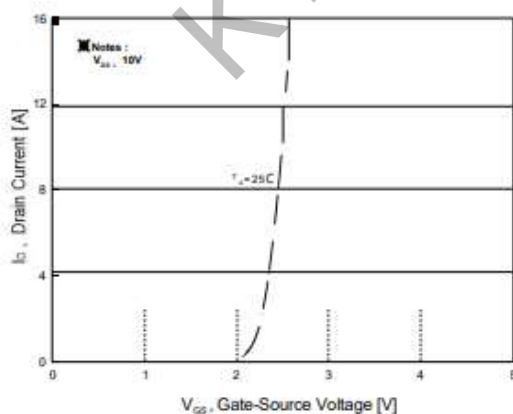


Fig.4 On-Resistance Variation with Gate to Source Voltage



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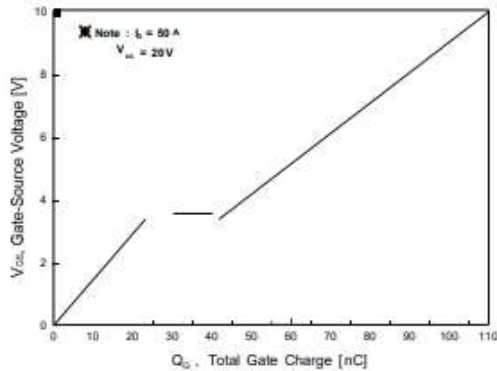


Fig.7 Gate Charge Characteristics

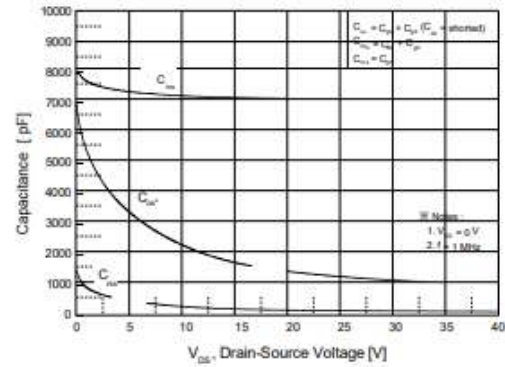


Fig.8 Capacitance Characteristics

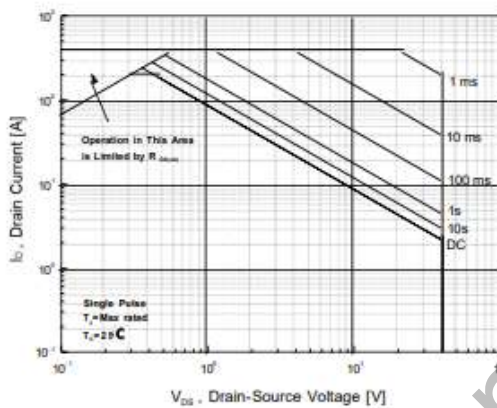


Fig.9 Maximum Safe Operating Area

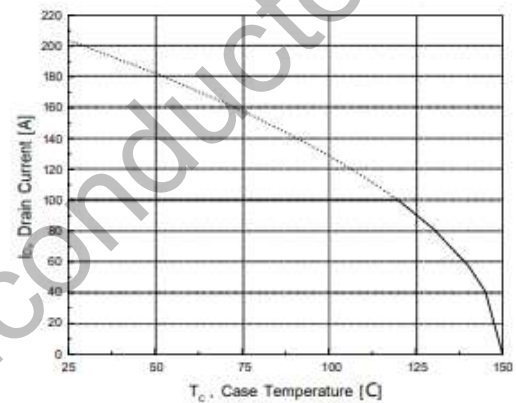


Fig.10 Maximum Drain Current vs. Case Temperature

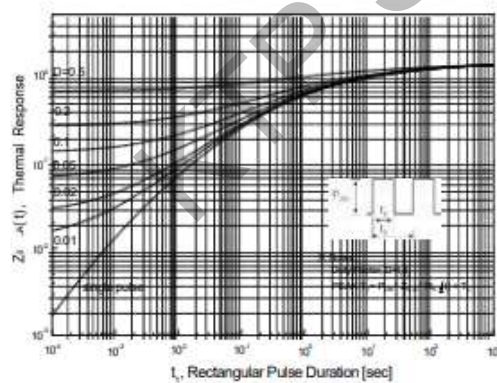
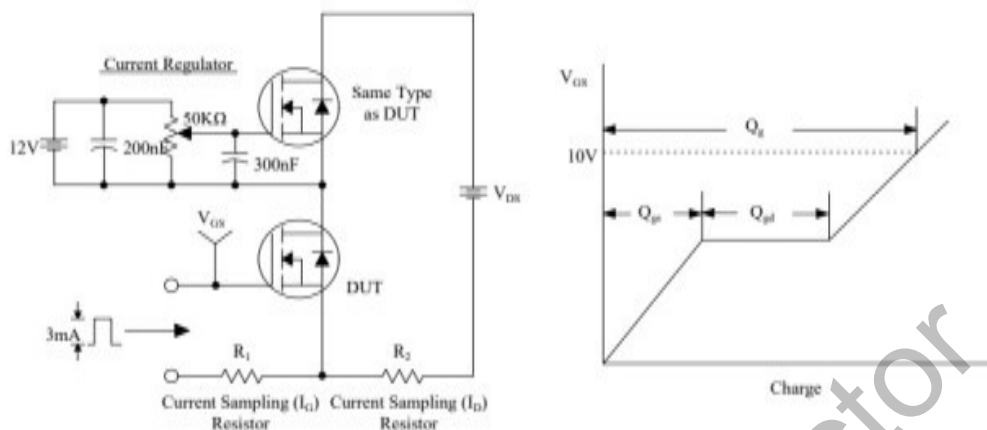


Fig.11 Transient Thermal Response Curve

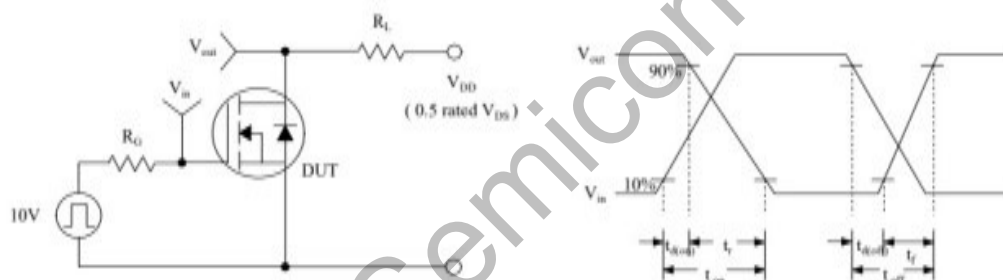
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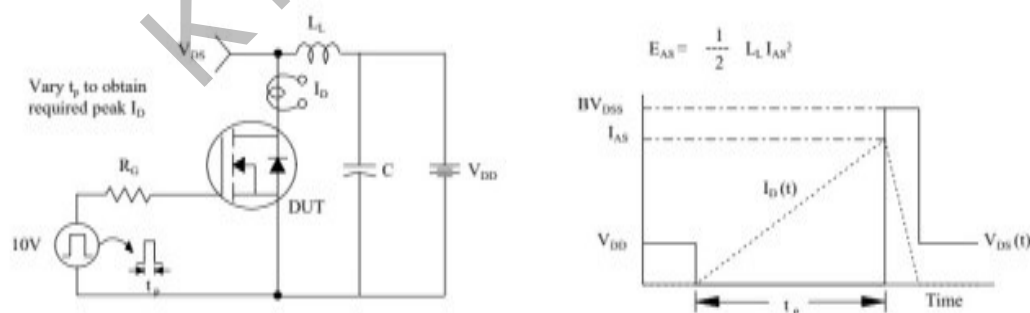
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



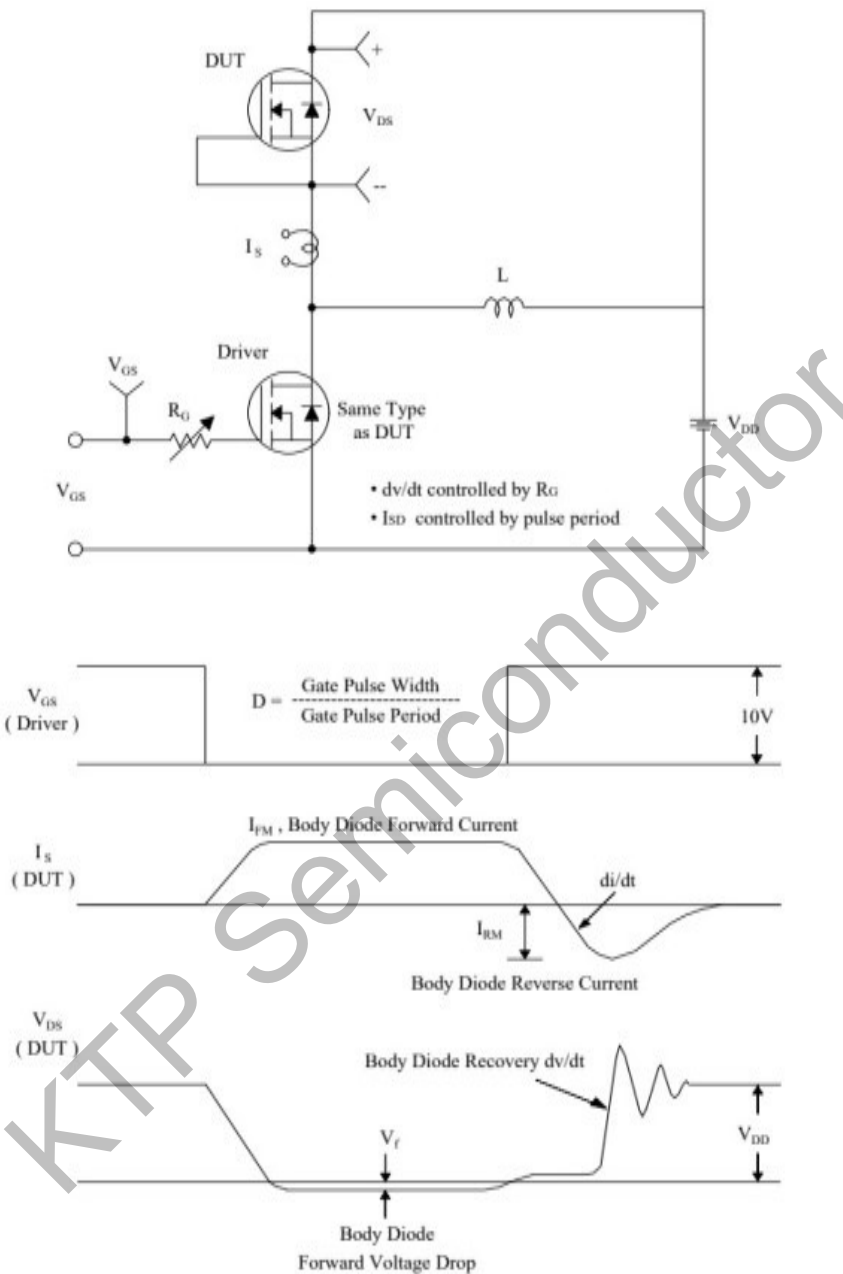
Unclamped Inductive Switching Test Circuit & Waveforms



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Peak Diode Recovery dv/dt Test Circuit & Waveforms

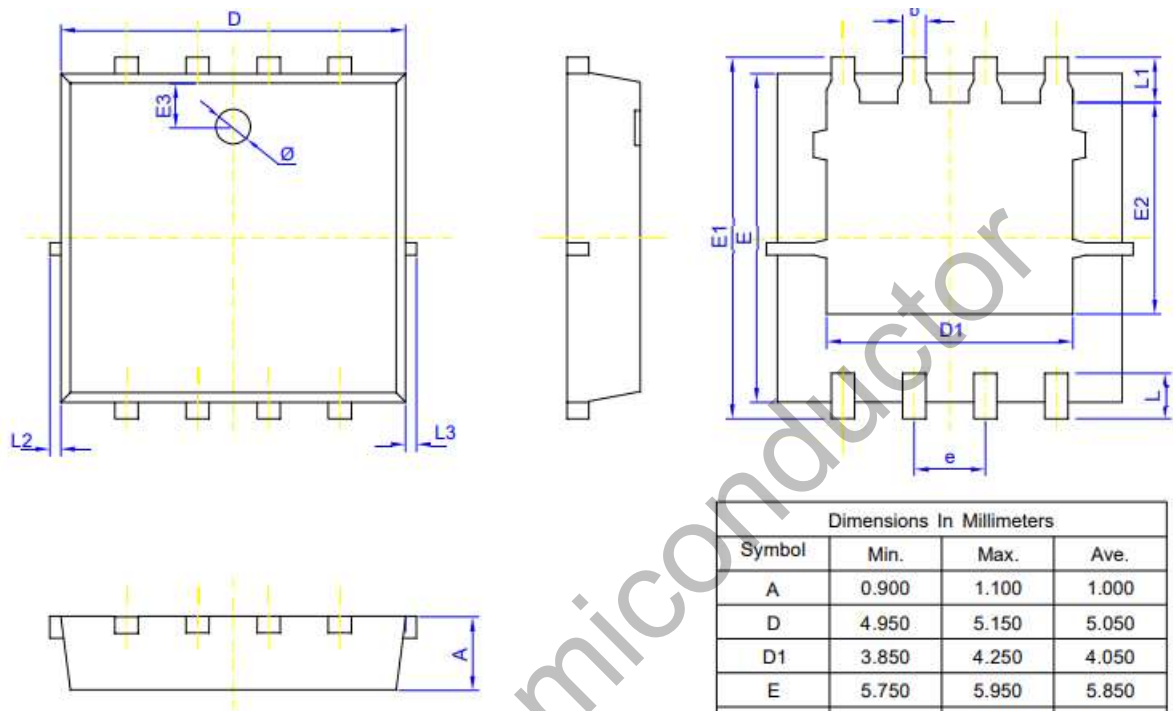


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Package Information

PDFN5*6-8L



注:

1. 未注公差±0.05, 未标注圆角R_{max}=0.25

2. 标注单位mm

Dimensions In Millimeters			
Symbol	Min.	Max.	Ave.
A	0.900	1.100	1.000
D	4.950	5.150	5.050
D1	3.850	4.250	4.050
E	5.750	5.950	5.850
E1	5.950	6.350	6.150
E2	3.300	3.700	3.500
E3	0.900	1.300	1.100
b	0.250	0.350	0.300
e	1.220	1.320	1.270
L	0.585	0.785	0.685
L1	0.525	0.725	0.625
Ø	1.000	1.400	1.200
L2	0~0.100		
L3	0~0.100		