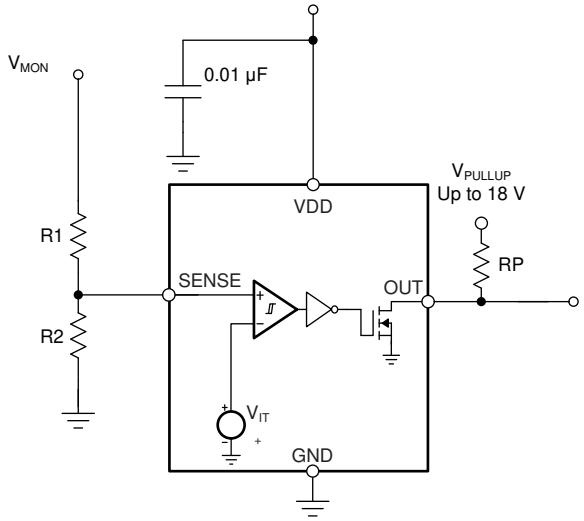
具有 400mV 基准电压的 TLV6703-Q1 汽车微功耗、18V 比较器

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：–40°C 至 125°C 环境工作温度范围
  - 器件 HBM ESD 分类等级 H2
  - 器件 CDM ESD 分类等级 C6
- 宽电源电压范围：1.8 V 至 18V
- 可调节阈值：低至 400mV
- 高阈值精度：
  - 25°C 时最高为 0.5%
  - 在工作温度范围内最大值为 1.0%
- 低静态电流：5.5µA（典型值）
- 开漏输出
- 内部迟滞：5.5mV（典型值）
- 温度范围：–40°C 至 +125°C
- 封装：无引线 WSON-6

2 应用

- 紧急呼叫 (eCall)
- 汽车音响主机
- 仪表组
- 车载充电器 (OBC) 和无线充电器



简化版方框图

3 说明

TLV6703-Q1 是一款高电压比较器，工作电压范围为 1.8V 至 18V。TLV6703-Q1 具有一个内部基准电压为 400mV 的高精度比较器和一个额定电压为 18V 的开漏输出，用于实现精确的电压检测。可以使用外部电阻设置监视电压。

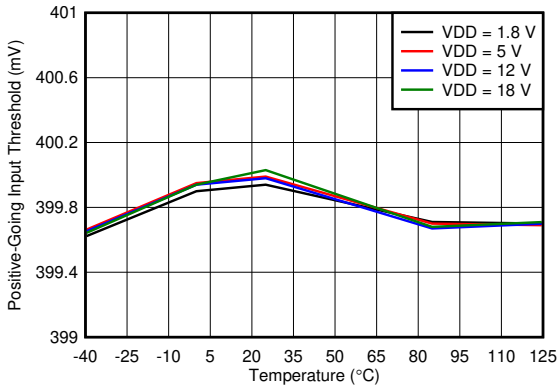
当 SENSE 引脚上的电压下降至低于 (V_{IT-}) 时，OUT 引脚被驱动至低电平，而当电压返回到对应阈值 (V_{IT+}) 之上时，OUT 引脚变为高电平。TLV6703-Q1 中的比较器具有拒绝短暂干扰的内置迟滞，确保稳定的输出运行，不会引起误触发。

TLV6703-Q1 采用无引线 WSON-6 封装，额定工作结温范围为 –40°C 至 +125°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TLV6703-Q1	WSON (6)	1.50mm × 1.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。



上升输入阈值电压 (V_{IT+}) 与温度间的关系

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

Table of Contents

1 特性 ... 1
2 应用 ... 1
3 说明 ... 1
4 Revision History ... 2
5 Device Comparison Table ... 3
6 Pin Configuration and Functions ... 4
7 Specifications ... 5
7.1 Absolute Maximum Ratings ... 5
7.2 ESD Ratings ... 5
7.3 Recommended Operating Conditions ... 5
7.4 Thermal Information ... 5
7.5 Electrical Characteristics ... 6
7.6 Timing Requirements ... 7
7.7 Switching Characteristics ... 7
7.8 Timing Diagrams ... 7
7.9 Typical Characteristics ... 8
8 Detailed Description ... 10
8.1 Overview ... 10
8.2 Functional Block Diagram ... 10
8.3 Feature Description ... 11
8.4 Device Functional Modes ... 11
9 Application and Implementation ... 12
9.1 Application Information ... 12
9.2 Typical Application ... 14
9.3 Dos and Don'ts ... 15
10 Power-Supply Recommendations ... 16
11 Layout ... 17
11.1 Layout Guidelines ... 17
11.2 Layout Example ... 17
12 Device and Documentation Support ... 18
12.1 Device Support ... 18
12.2 Receiving Notification of Documentation Updates ... 18
12.3 支持资源 ... 18
12.4 Trademarks ... 18
12.5 静电放电警告 ... 18
12.6 术语表 ... 18
13 Mechanical, Packaging, and Orderable Information ... 18

4 Revision History

DATE	REVISION	NOTES
November 2020	*	Initial release.

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5 Device Comparison Table

表 5-1. TLV67xx Integrated Comparator Family

PART NUMBER	CONFIGURATION	OPERATING VOLTAGE RANGE	THRESHOLD ACCURACY OVER TEMPERATURE
TLV6700	Window	1.8 V to 18 V	1%
TLV6700-Q1	Window	1.8 V to 18 V	1%
TLV6703	Non-Inverting Single Channel	1.8 V to 18 V	1%
TLV6703-Q1	Non-Inverting Single Channel	1.8 V to 18 V	1%
TLV6710	Window	1.8 V to 36 V	0.75%
TLV6713	Non-Inverting Single Channel	1.8 V to 36 V	0.75%

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6 Pin Configuration and Functions

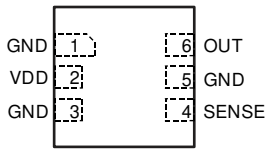


图 6-1. DSE Package, 6-Pin WSON, Top View

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	DSE		
GND	1,3,5	—	Connect all three pins to ground.
OUT	6	O	SENSE comparator open-drain output. OUT is driven low when the voltage at this comparator is below (V_{IT-}). The output goes high when the sense voltage returns above the respective threshold (V_{IT+}).
SENSE	4	I	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this pin drops below the threshold voltage (V_{IT-}), OUT is driven low.
VDD	2	I	Supply voltage input. Connect a 1.8-V to 18-V supply to VDD to power the device. Good analog design practice is to place a 0.1-µF ceramic capacitor close to this pin.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	VDD	–0.3	20	V
	OUT	–0.3	20	
	SENSE	–0.3	7	
Current	OUT (output sink current)		40	mA
Temperature	Operating junction, T_J	–40	125	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground pin.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002, all pins(1)	±2500	V
		Charged device model (CDM), per AEC Q100-002, all pins	±1000	

(1) AEC Q100-002 indicates that HBM stressing shal be in accordance with ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		1.8		18	V
V_I	Input voltage	SENSE	0		6.5	V
V_O	Output voltage	OUT	0		18	V

7.4 Thermal Information

THERMAL METRIC (1)		DSE (WSON) 6 PADS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	194.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	128.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	153.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	157.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor an IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

Over the operating temperature range of T_J = –40°C to +125°C, and 1.8 V < V_{DD} < 18 V (unless otherwise noted). Typical values are at T_J = 25°C and V_{DD} = 5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(POR)}$	Power-on reset voltage (1)	V_{OL}max = 0.2 V, output sink current = 15 µA			0.8	V
V_{IT+}	Positive-going input threshold voltage	V_{DD} = 1.8V and 18 V, T_J = 25°C	398	400	402.5	mV
		V_{DD} = 1.8V and 18 V, T_J = –40°C to 125°C	396		404	
V_{IT-}	Negative-going input threshold voltage	V_{DD} = 1.8V and 18 V, T_J = 25°C	391.6	394.5	397.5	mV
		V_{DD} = 1.8V and 18 V, T_J = –40°C to 125°C	387		400	
V_{hys}	Hysteresis voltage (hys = V_{IT+} – V_{IT-})			5.5	12	mV
$I_{(SENSE)}$	Input current (at the SENSE pin)	V_{DD} = 1.8 V and 18 V, V_I = 6.5 V	–25	1	25	nA
V_{OL}	Low-level output voltage	V_{DD} = 1.8 V, output sink current = 3 mA			250	mV
		V_{DD} = 5 V, output sink current = 5 mA			250	
$I_{lkg(OD)}$	Open-drain output leakage-current	V_{DD} = 1.8 V and 18 V, V_O = V_{DD}			300	nA
		V_{DD} = 1.8 V, V_O = 18 V			300	
I_{DD}	Supply current	V_{DD} = 1.8 V, no load		5.5	11	µA
		V_{DD} = 5 V		6	13	
		V_{DD} = 12 V		6	13	
		V_{DD} = 18 V		7	13	
UVLO	Undervoltage lockout (2)	V_{DD} falling	1.3		1.7	V

(1) The lowest supply voltage (V_{DD}) at which output is active; $t_{r(VDD)}$ > 15 µs/V. Below $V_{(POR)}$, the output cannot be determined.
(2) When V_{DD} falls below UVLO, OUT is driven low. The output cannot be determined below $V_{(POR)}$.

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7.6 Timing Requirements

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$t_{pd(HL)}$	High-to-low propagation delay (1)	V_{DD} = 5 V, 10-mV input overdrive, R_P = 10 kΩ, V_{OH} = 0.9 × V_{DD}, V_{OL} = 400 mV, see 图 7-1		18		µs
$t_{pd(LH)}$	Low-to-high propagation delay (1)	V_{DD} = 5 V, 10-mV input overdrive, R_P = 10 kΩ, V_{OH} = 0.9 × V_{DD}, V_{OL} = 400 mV, see 图 7-1		29		µs
$t_{d(start)}$	Start-up delay (2)			150		µs

(1) High-to-low and low-to-high refers to the transition at the input pin (SENSE).
(2) During power on, V_{DD} must exceed 1.8 V for at least 150 µs before the output is in a correct state.

7.7 Switching Characteristics

over operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output rise time	V_{DD} = 5 V, 10-mV input overdrive, R_P = 10 kΩ, V_O = (0.1 to 0.9) × V_{DD}		2.2		µs
t_f	Output fall time	V_{DD} = 5 V, 10-mV input overdrive, R_P = 10 kΩ, V_O = (0.1 to 0.9) × V_{DD}		0.22		µs

7.8 Timing Diagrams

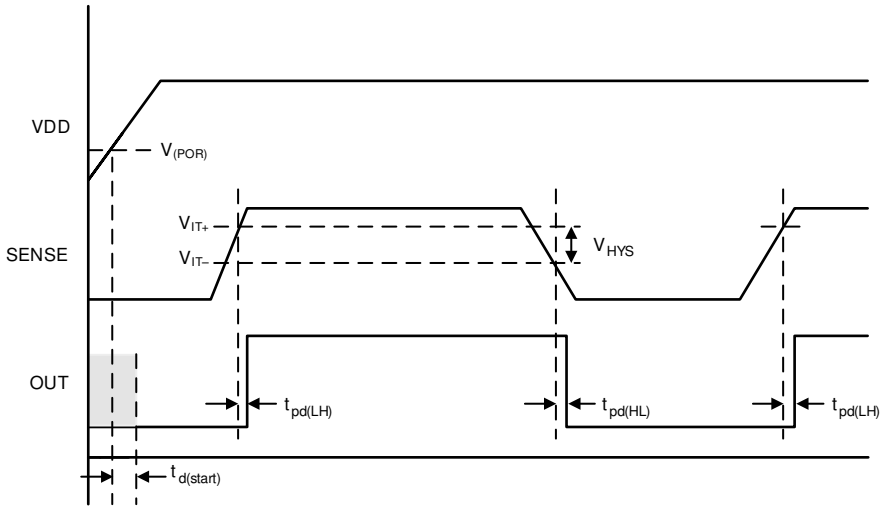


图 7-1. Timing Diagram

7.9 Typical Characteristics

at T_J = 25°C and V_{DD} = 5 V (unless otherwise noted)

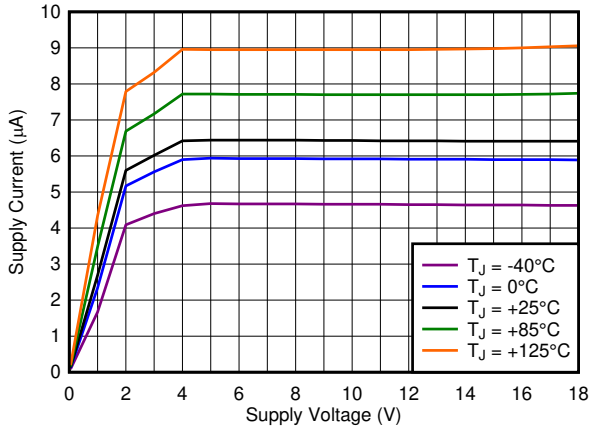


图 7-2. Supply Current (I_{DD}) vs Supply Voltage (V_{DD})

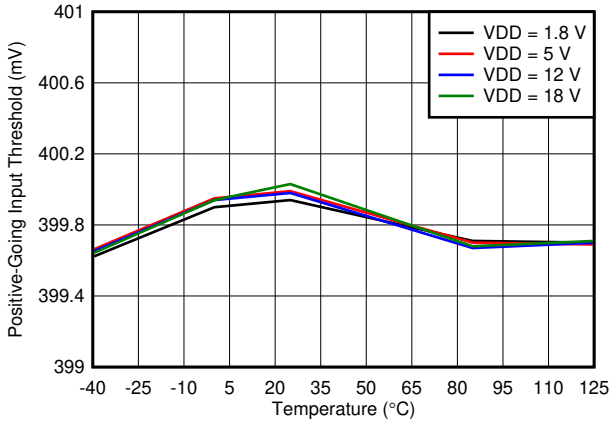


图 7-3. Rising Input Threshold Voltage (V_{IT+}) vs Temperature

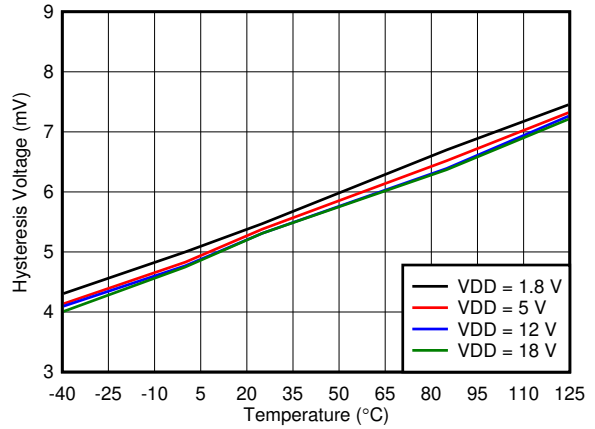


图 7-4. Hysteresis (V_{hys}) vs Temperature

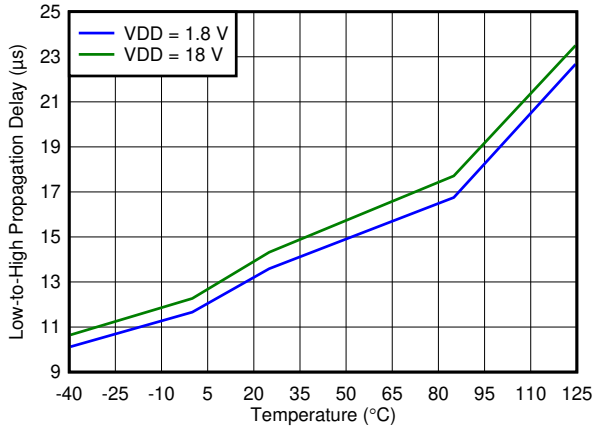


图 7-5. Propagation Delay vs Temperature (High-to-Low Transition at Sense)

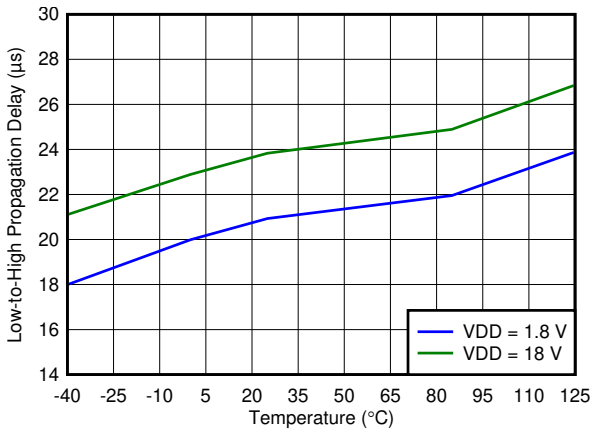
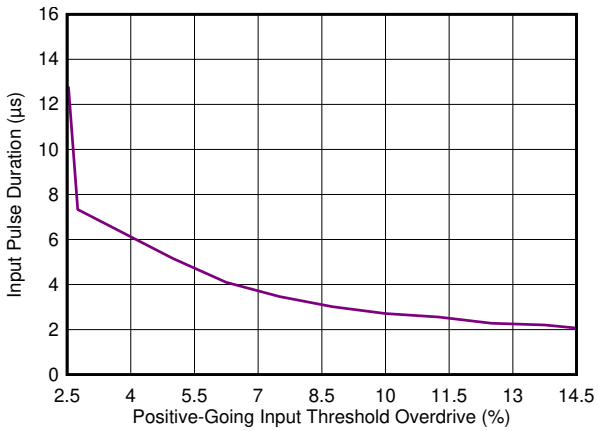


图 7-6. Propagation Delay vs Temperature (Low-to-High Transition at Sense)



SENSE = negative spike below V_{IT-}

图 7-7. Minimum Pulse Width vs Threshold Overdrive Voltage

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7.9 Typical Characteristics (continued)

at T_J = 25°C and V_{DD} = 5 V (unless otherwise noted)

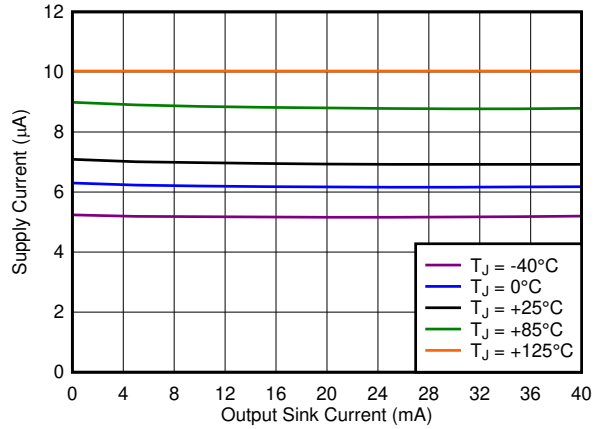


图 7-8. Supply Current (I_{DD}) vs Output Sink Current

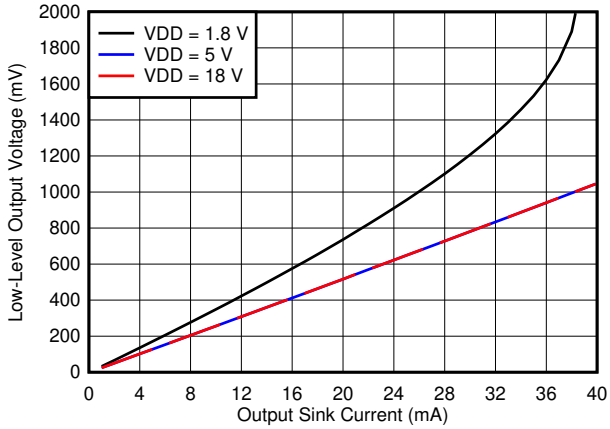


图 7-9. Output Voltage Low (V_{OL}) vs Output Sink Current (– 40°C)

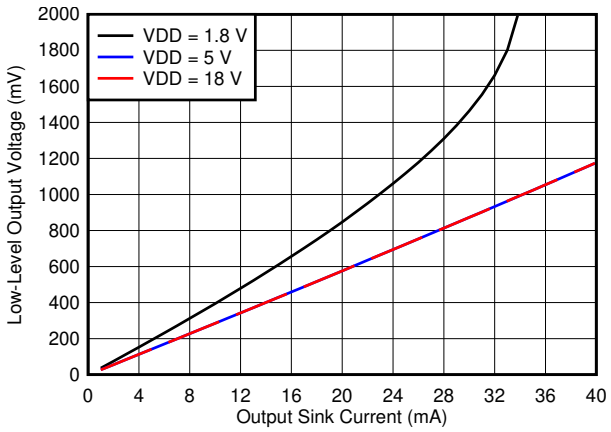


图 7-10. Output Voltage Low (V_{OL}) vs Output Sink Current (0°C)

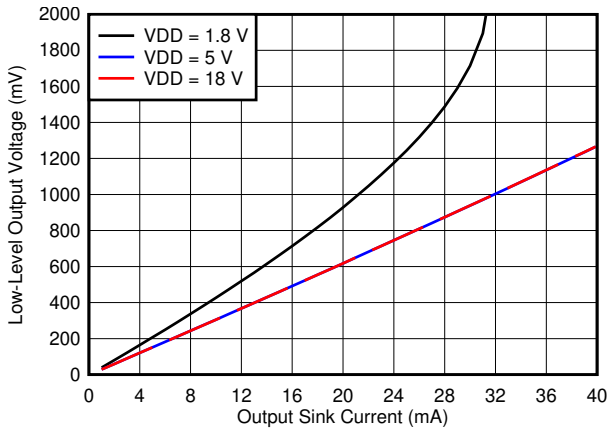


图 7-11. Output Voltage Low (V_{OL}) vs Output Sink Current (25°C)

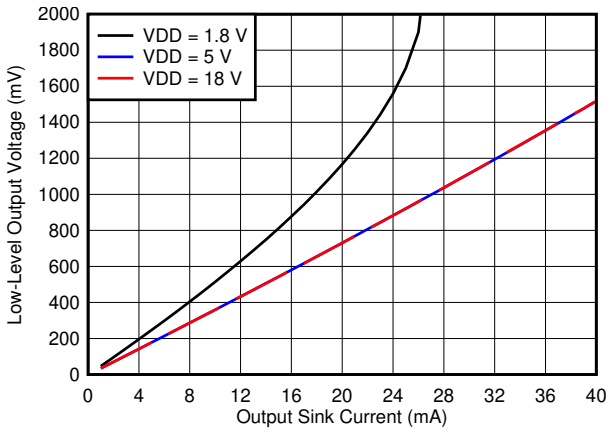


图 7-12. Output Voltage Low (V_{OL}) vs Output Sink Current (85°C)

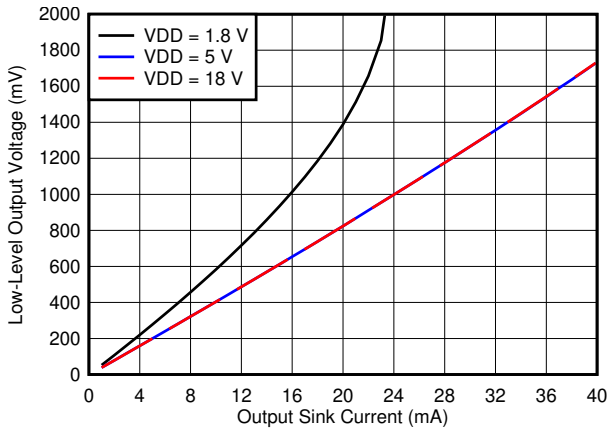


图 7-13. Output Voltage Low (V_{OL}) vs Output Sink Current (125°C)

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8 Detailed Description

8.1 Overview

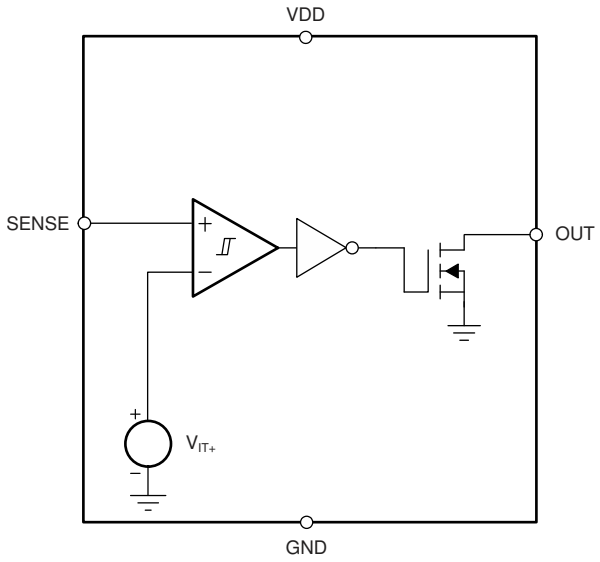
The TLV6703-Q1 provides precision voltage detection. The TLV6703-Q1 is a wide-supply voltage range (1.8 V to 18 V) comparator with a high-accuracy rising input threshold of 400 mV (1% over temperature) and built-in hysteresis. The output is also rated to 18 V, independant of supply voltage, and can sink up to 40 mA.

The TLV6703-Q1 asserts the output signal, as shown in 表 8-1. To monitor any voltage above 0.4 V, set the input using an external resistor divider network. Each input pin has very low input leakage current, allowing the use of large resistor dividers without sacrificing system accuracy. Broad voltage thresholds are supported that enable the device for use in a wide array of applications.

表 8-1. TLV6703-Q1 Truth Table

CONDITION	OUTPUT	OUTPUT STATE
SENSE > V_{IT+}	OUT high	Output high impedance
SENSE < V_{IT-}	OUT low	Output sinking

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Input Pin (SENSE)

The TLV6703-Q1 comparator has two inputs: one external input, and one input internally connected to the internal 400mV reference. The comparator rising threshold is trimmed to be equal to the reference voltage (400 mV). The comparator also has a built-in falling hysteresis that makes the device less sensitive to supply-rail noise and provides stable operation.

The comparator input (SENSE) is able to swing from ground to 6.5 V, regardless of the device supply voltage. Although not required in most cases, to reduce sensitivity to transients and layout parasitics for extremely noisy applications, place a 1-nF to 10-nF bypass capacitor at the comparator input.

OUT is driven to logic low when the input SENSE voltage drops below (V_{IT-}). When the voltage exceeds V_{IT+}, the output (OUT) goes to a high-impedance state; see 图 7-1 .

8.3.2 Output Pin (OUT)

In a typical TLV6703-Q1 application, the output is connected to a GPIO input of the processor (such as a digital signal processor [DSP], central processing unit [CPU], field-programmable gate array [FPGA], or application-specific integrated circuit [ASIC]).

The TLV6703-Q1 device provides an open-drain output (OUT). Use a pullup resistor to hold this line high when the output goes to high impedance (not asserted). To connect the output to another device at the correct interface-voltage level, connect a pullup resistor to the proper voltage rail. The TLV6703-Q1 output can be pulled up to 18 V, independent of the device supply voltage.

表 8-1 and the *节 8.3.1* section describe how the output is asserted or deasserted. See for a 图 7-1 timing diagram that describes the relationship between threshold voltage and the respective output.

8.3.3 Immunity to Input-Pin Voltage Transients

The TLV6703-Q1 is relatively immune to short voltage transient spikes on the sense pin. Sensitivity to transients depends on both transient duration and amplitude; see 图 7-7, *Minimum Pulse Width vs Threshold Overdrive Voltage*.

8.4 Device Functional Modes

8.4.1 Normal Operation (V_{DD} > UVLO)

When the voltage on V_{DD} is greater than 1.8 V for at least 150 µs, the OUT signal correspond to the voltage on SENSE as listed in 表 8-1.

8.4.2 Undervoltage Lockout ($V_{(POR)} < V_{DD} <$ UVLO)

When the voltage on V_{DD} is less than the device UVLO voltage, and greater than the power-on reset voltage, $V_{(POR)}$, the OUT signal is asserted regardless of the voltage on SENSE.

8.4.3 Power-On Reset ($V_{DD} < V_{(POR)}$)

When the voltage on V_{DD} is lower than the required voltage to internally pull the asserted output to GND ($V_{(POR)}$), SENSE is in a high-impedance state.

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9 Application and Implementation

备注

以下应用部分的信息不属于 TI 组件规范，TI 不担保其准确性和完整性。客户应负责确定 TI 组件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The TLV6703-Q1 device is a wide-supply voltage comparator that operates over a V_{DD} range of 1.8 V to 18 V. The device has a high-accuracy comparator with an internal 400-mV reference and an open-drain output rated to 18 V for precision voltage detection. The device can be used as a voltage monitor. The monitored voltage are set with the use of external resistors.

9.1.1 V_{PULLUP} to a Voltage Other Than V_{DD}

The output is often tied to V_{DD} through a resistor. However, some applications may require the output to be pulled up to a higher or lower voltage than V_{DD} to correctly interface with the reset and enable pins of other devices.

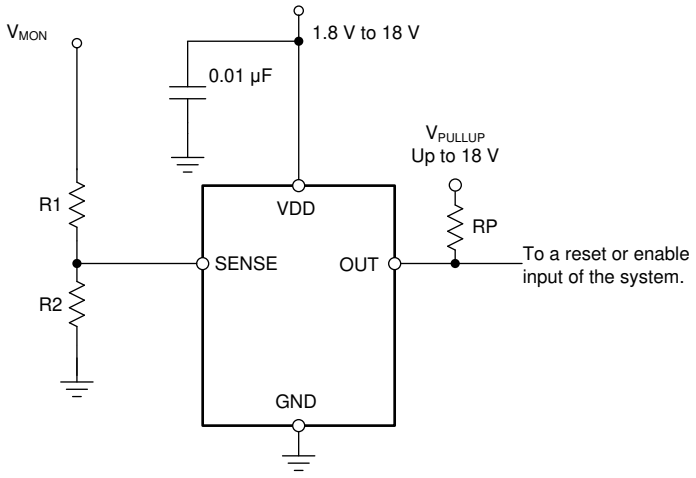


图 9-1. Interfacing to a Voltage Other Than V_{DD}

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9.1.2 Monitoring V_{DD}

Many applications monitor the same rail that is powering V_{DD}. In these applications the resistor divider is simply connected to the V_{DD} rail.

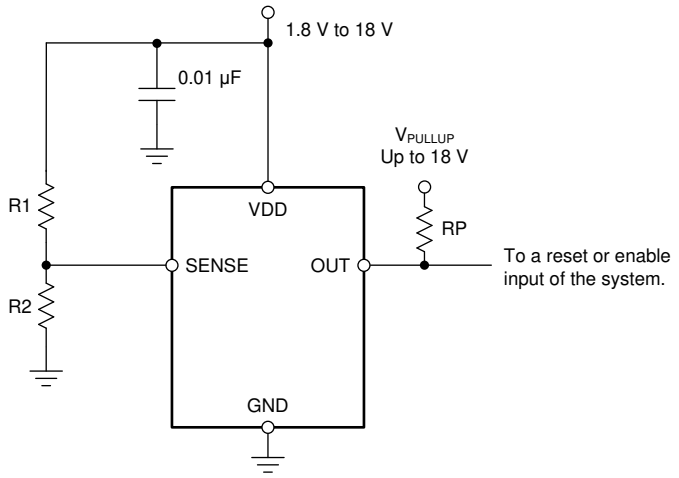
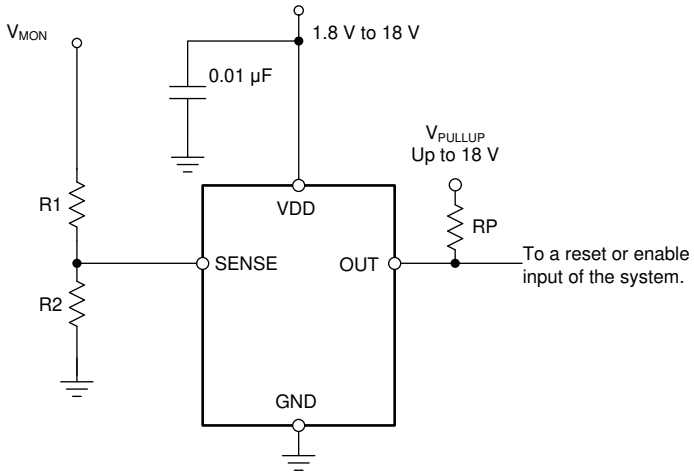


图 9-2. Monitoring the Same Voltage as V_{DD}

9.1.3 Monitoring a Voltage Other Than V_{DD}

Some applications monitor rails other than the one that is powering V_{DD}. In these types of applications the resistor divider used to set the desired threshold is connected to the rail that is being monitored.



NOTE: The input can monitor a voltage greater than maximum V_{DD} with the use of an external resistor divider network.

图 9-3. Monitoring a Voltage Other Than V_{DD}

9.2 Typical Application

The TLV6703-Q1 device is a wide-supply voltage comparator that operates over a V_{DD} range of 1.8 to 18 V. The monitored voltage is set with the use of external resistors, so the device can be used either as a precision voltage monitor.

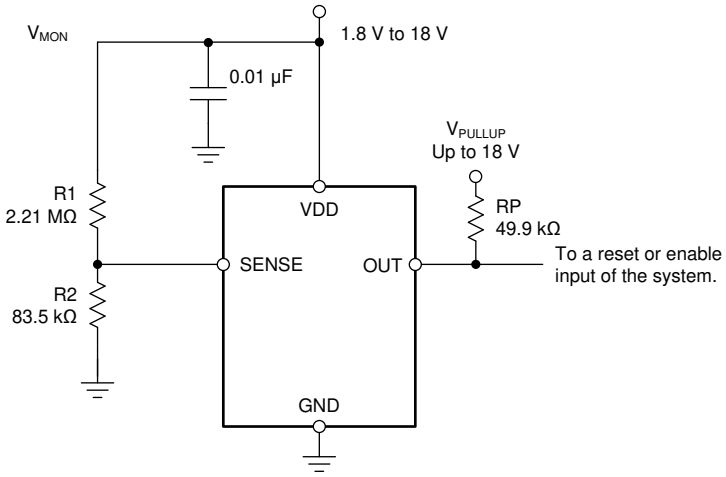


图 9-4. Wide VIN Voltage Monitor

9.2.1 Design Requirements

For this design example, use the values summarized in 表 9-1 as the input parameters.

表 9-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Monitored voltage	12-V nominal rail with maximum falling threshold of 10%	$V_{MON(UV)}$= 10.99 V (8.33%)

9.2.2 Detailed Design Procedure

9.2.2.1 Resistor Divider Selection

The resistor divider values and target threshold voltage can be calculated by using 方程式 1 to determine $V_{MON(UV)}$.

$$V_{MON(UV)} = \left(1 + \frac{R1}{R2}\right) \times V_{IT-} \quad (1)$$

where

- R1 and R2 are the resistor values for the resistor divider on the SENSEx pins
- $V_{MON(UV)}$ is the target voltage at which an undervoltage condition is detected

Choose R_{TOTAL} (= R1 + R2) so that the current through the divider is approximately 100 times higher than the input current at the SENSE pin. The resistors can have high values to minimize current consumption as a result of low input bias current without adding significant error to the resistive divider. For details on sizing input resistors, refer to application report SLVA450, *Optimizing Resistor Dividers at a Comparator Input*, available for download from www.ti.com.

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9.2.2.2 Pullup Resistor Selection

To ensure the proper voltage level, the pullup resistor value is selected by ensuring that the pullup voltage divided by the resistor does not exceed the sink-current capability of the device. This confirmation is calculated by verifying that the pullup voltage minus the output-leakage current ($I_{lkg(OD)}$) multiplied by the resistor is greater than the desired logic-high voltage. These values are specified in the 节 7.5.

Use 方程式 2 to calculate the value of the pullup resistor.

$$\frac{(V_{HI} - V_{PU})}{I_{lkg(OD)}} \geq R_{PU} \geq \frac{V_{PU}}{I_O} \quad (2)$$

9.2.2.3 Input Supply Capacitor

Although an input capacitor is not required for stability, for good analog design practice, connect a 0.1-μF low equivalent series resistance (ESR) capacitor across the VDD and GND pins. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source.

9.2.2.4 Sense Capacitor

Although not required in most cases, for extremely noisy applications, place a 1-nF to 10-nF bypass capacitor from the comparator input (SENSE) to the GND pin for good analog design practice. This capacitor placement reduces device sensitivity to transients.

9.2.3 Application Curves

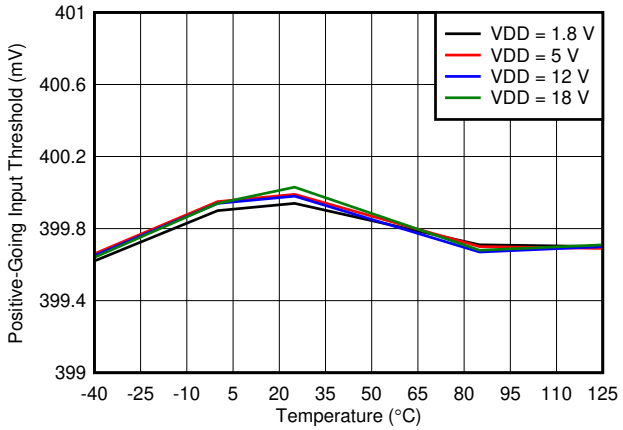


图 9-5. Rising Input Threshold Voltage (V_{IT+}) vs Temperature

9.3 Dos and Don'ts

Do connect a 0.1-μF decoupling capacitor from V_{DD} to GND for best system performance.

If the monitored rail is noisy, do connect a decoupling capacitor from the comparator input (sense) to GND.

Don't use resistors for the voltage divider that cause the current through them to be less than 100 times the input current of the comparator without also accounting for the effect to the accuracy.

Don't use a pullup resistor that is too small, because the larger current sunk by the output then exceeds the desired low-level output voltage (V_{OL}).

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10 Power-Supply Recommendations

These devices operate from an input voltage supply range between 1.8 V and 18 V.

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11 Layout

11.1 Layout Guidelines

Placing a 0.1-µF capacitor close to the VDD pin to reduce the input impedance to the device is good analog design practice.

11.2 Layout Example

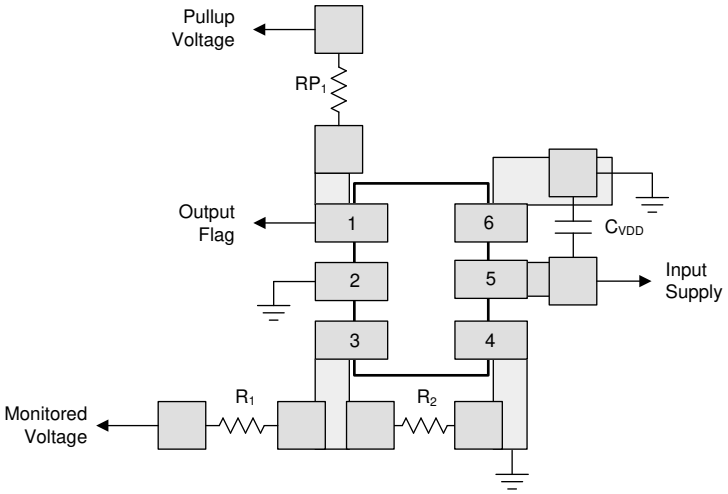


图 11-1. Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

The *DIP Adapter Evaluation Module* allows conversion of the SOT-23-6 package to a standard DIP-6 pinout for ease of prototyping and bench evaluation.

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV6703QDSERQ1	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	K7
TLV6703QDSERQ1.Z	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	K7

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TLV6703-Q1 :

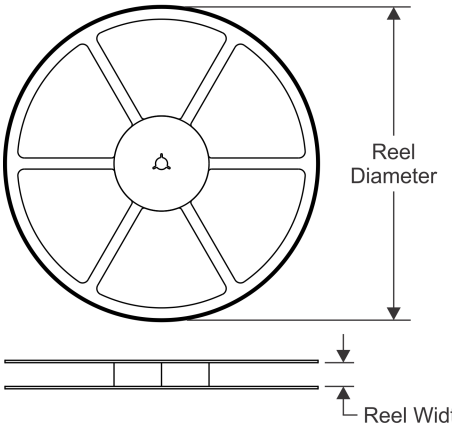
- Catalog : TLV6703

NOTE: Qualified Version Definitions:

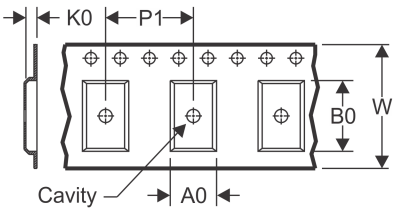
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

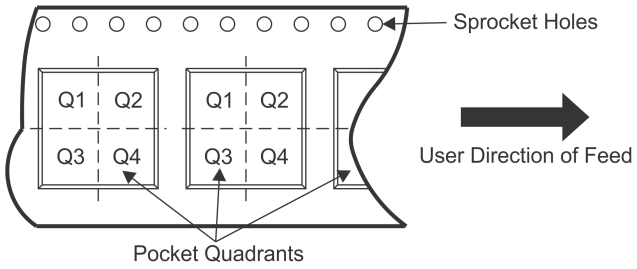


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

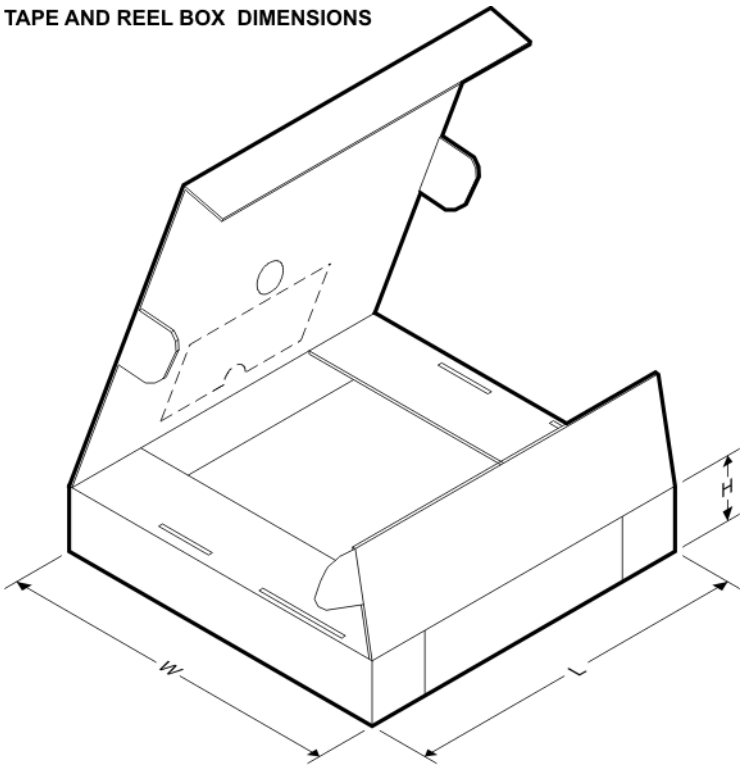
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV6703QDSERQ1	WSON	DSE	6	3000	180.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

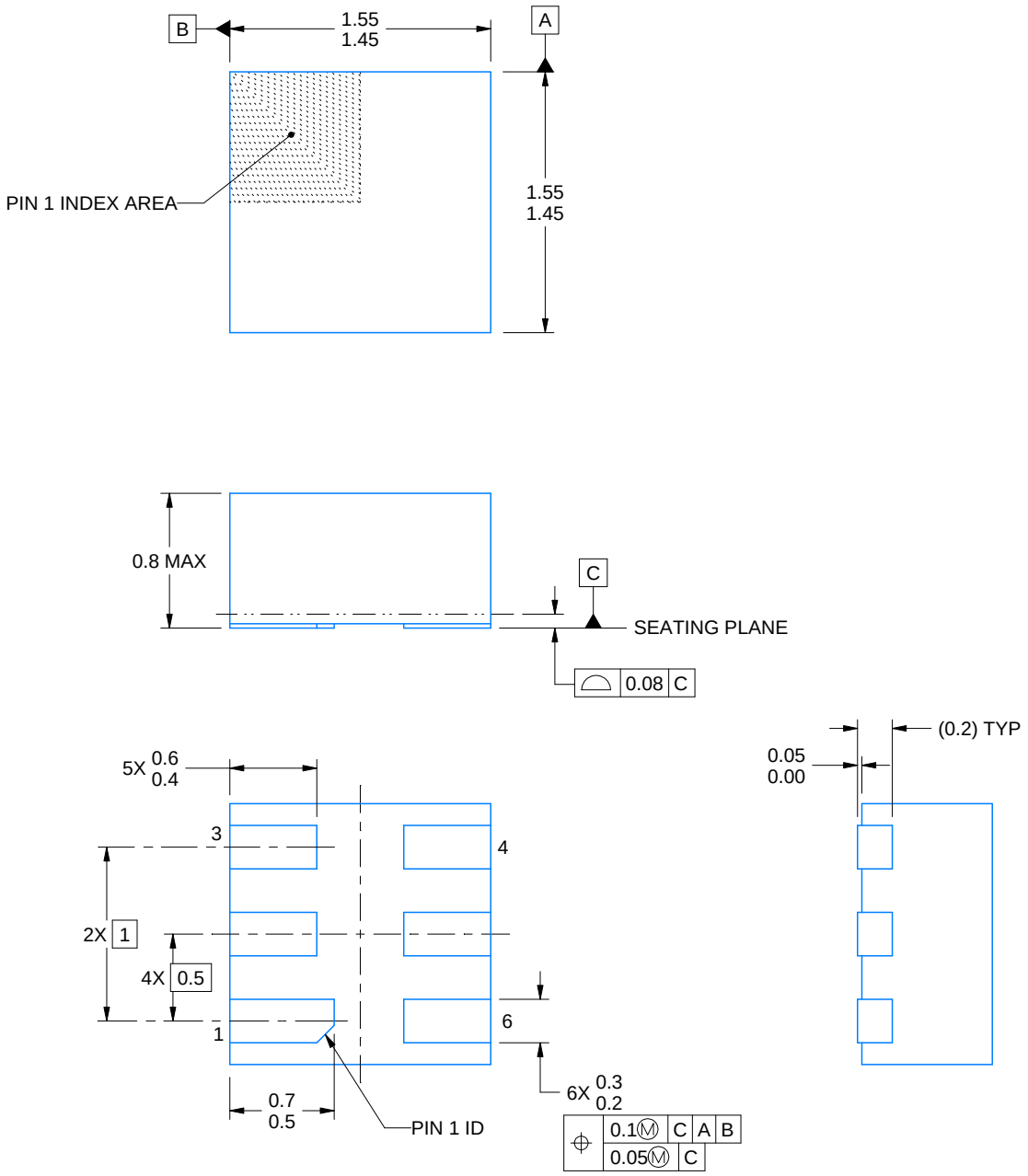
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV6703QDSERQ1	WSON	DSE	6	3000	213.0	191.0	35.0

DSE0006A

PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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NOTES:

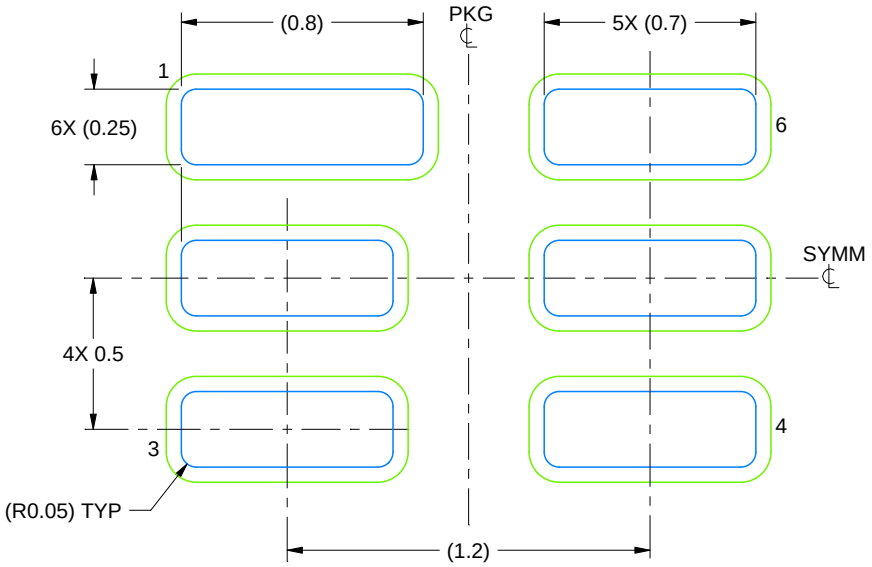
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

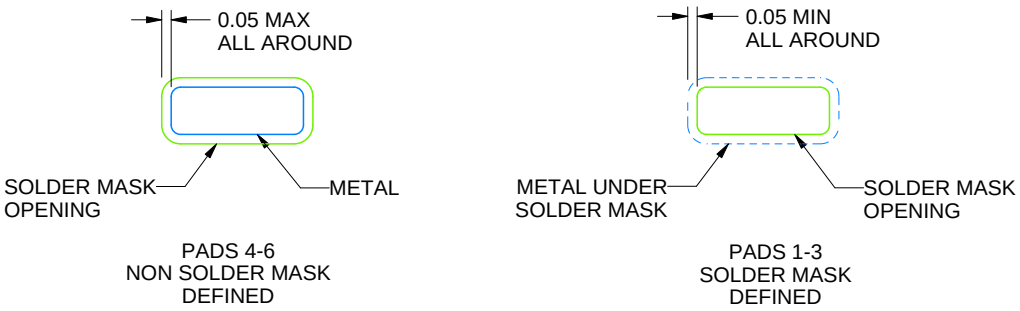
DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS

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NOTES: (continued)

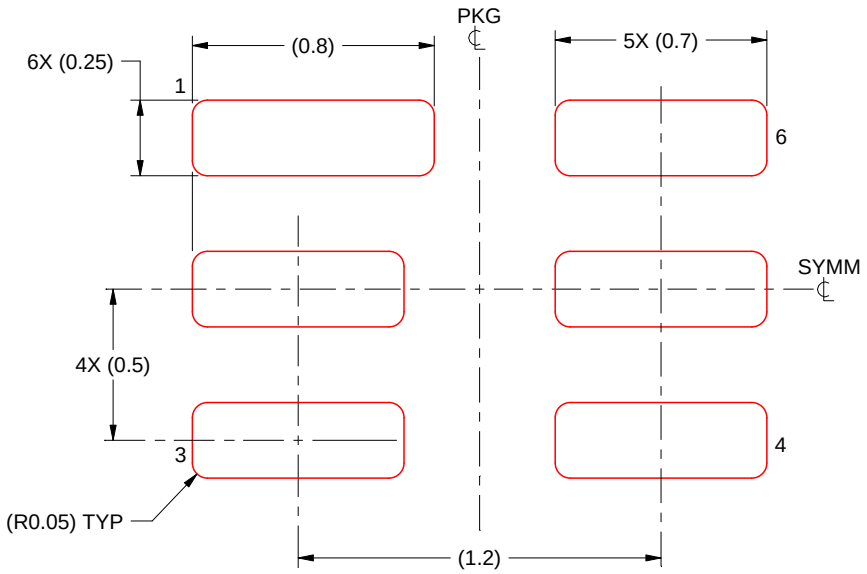
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:40X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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