



Product Specification

XBLW GT4427

Dual 2A Ultra-high-speed Power Switching Driver

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Descriptions

XBLW GT4427 is a power switching driver. It has matched rise and fall times when charging and discharging the gate. This device is highly latch-up resistant under any conditions within their power and voltage ratings. It is not subject to damage when up to 5V of noise spiking (of either polarity) occurs on the ground pin. The GT4427 can accept, without damage or logic upset, up to 500 mA of reverse current (of either polarity) being forced back into their outputs. All terminals are fully protected against Electrostatic Discharge (ESD) up to 2.0 kV.



SOP-8

Feature

- Latch-Up Protected: Withstands 0.5A Reverse Current
- Input Logic Protection Down To -10V
- Low Output Impedance
- Single Chip Integrated Two-Way Drive
- Output Peak Current: 2A
- Input Supply Voltage Operating Range: 4.5V~25V
- The Maximum Input Voltage up to 5V
- High Capacity Load Drive Capability: 1000 pF in 25ns
- Matched Rise And Fall Times
- Short Delay Times: 40ns
- Wide Temperature Range: -40°C~125°C
- Chip Turn-On/Turn-Off Delay Characteristics -- T_{on} / T_{off} = 70ns/70ns
- Compliant With RoSH Standard, Adopting SOP-8 Package
- Outputs in phase with inputs

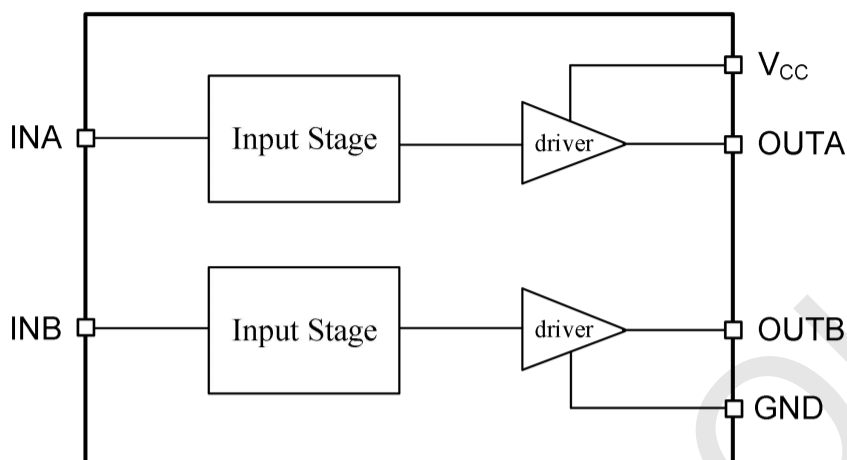
Applications

- Switch Mode Power Supplies & Switching Converters
- Line Drivers
- Pulse Transformer Drive
- Driving MOSFETs and IGBTs
- Motor Control
- Pulse Generator
- Power Switch
- DC-DC Converters
- Switching Amplifier Class D

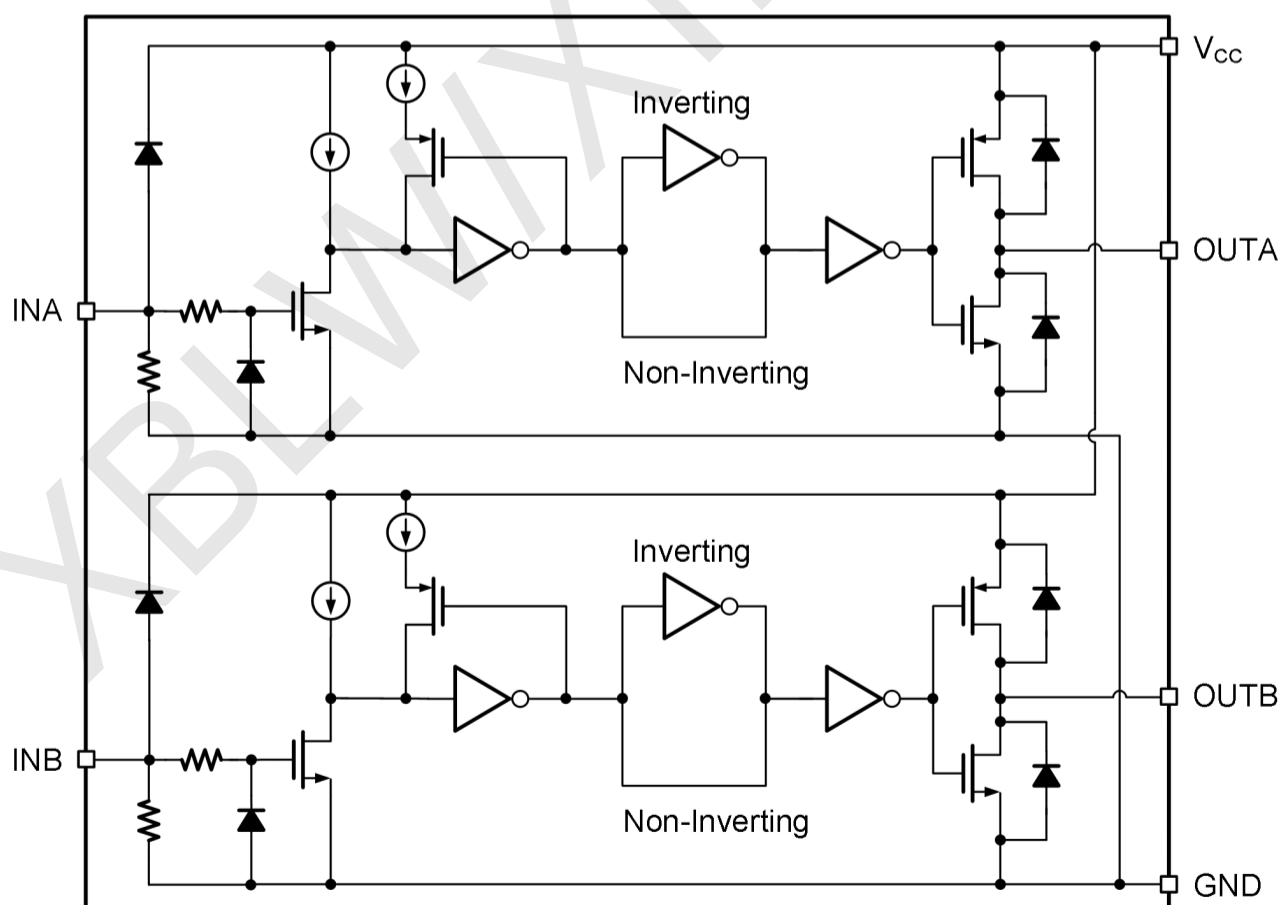
Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty	Input/Output Phase
XBLW GT4427DTR	SOP-8	GT4427	Tape	3000Pcs/Reel	In-Phase

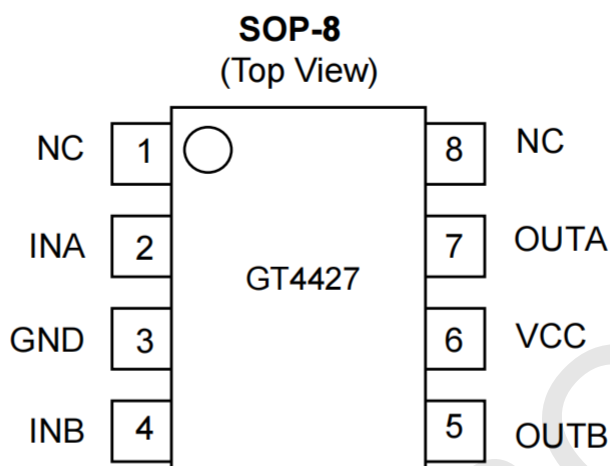
Simplified Diagram



Function Diagram



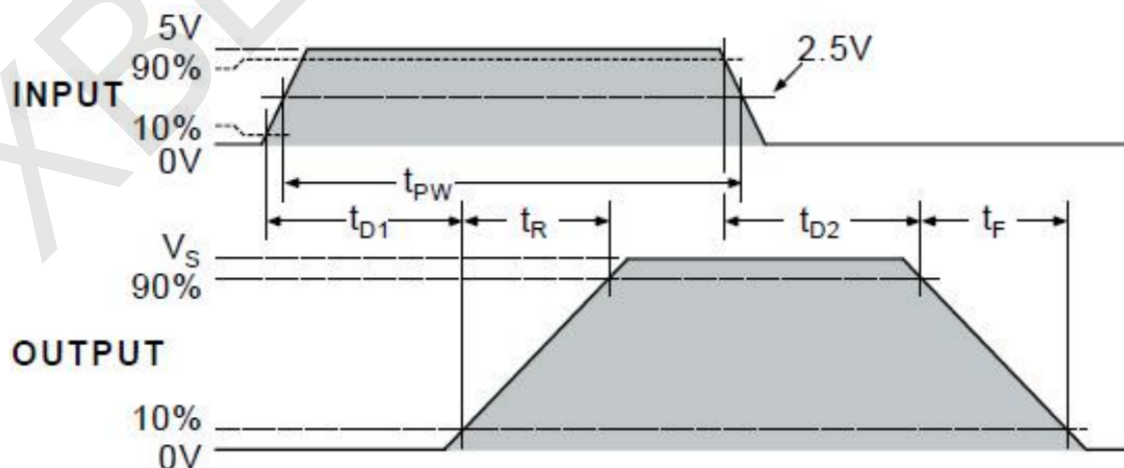
Pin Configurations



Pin Description

No.	Name	Function
1	NC	No Internal Connection
2	INA	Input A
3	GND	Ground
4	INB	Input B
5	OUTB	Output B
6	V _{CC}	Power Supply
7	OUTA	Output A
8	NC	No Internal Connection

Function Description



Input/output (In-Phase) waveform diagram

Product Specifications

Limit Operating Range

Exceeding the limit maximum rating may cause permanent damage to the device. The rated values of all voltage parameters are referenced to GND, and the current parameters are referenced to the positive input, and the ambient temperature is 25°C.

Symbol	Definition	Min.	Max.	Unit
V _{CC}	Power Supply	—	25	V
V _{IN}	Logical Input Voltage (INA/INB)	- 10	V _{CC} +0.3	

ESD Rating

Symbol	Definition	Min.	Max.	Unit
ESD	HBM	—	2000	V
	MM	—	500	V

Rated Power

Symbol	Definition	Min.	Max.	Unit
PD	SOIC Package Power (T _A ≤70°C)	—	470	mW

Thermal information

Symbol	Definition	Min.	Max.	Unit
T _J	Junction Temperature	—	+150	°C
T _S	Storage Temperature	-45	+150	

Recommended Operating Range

For proper operation, the device should be used under the following recommended conditions. The rated values of all voltage parameters are referenced to GND, and the current parameters are referenced to input positive current and the ambient temperature is 25°C.

Symbol	Definition	Min.	Max.	Unit
V _{CC}	Power Supply	4.5	20	V
T _C	Test Ambient Temperature	-40	125	°C

Electrical Characteristics

Unless otherwise specified, $T_A = 25^\circ\text{C}$, $4.5\text{V} \leq V_{CC} \leq 18\text{V}$.

Symbol	Definition	Min.	Typ.	Max.	Unit
V_{IH}	Logic '1', High Input Voltage	2.4	—	—	V
V_{IL}	Logic '0', Low Input Voltage			0.8	V
I_{IN}	Input Current ($0\text{V} \leq V_{IN} \leq V_{CC}$)	—	—	200	μA
V_{OH}	High Output Voltage	$V_{CC} - 0.025$			V
V_{OL}	Low Output Voltage	—	—	0.025	V
R_{OH}	High Voltage, Output Resistance ($V_{CC} = 18\text{V}$, $I_O = 100\text{mA}$)	—	4	8	Ω
R_{OL}	Low Voltage, Output Resistance ($V_{CC} = 18\text{V}$, $I_O = 100\text{mA}$)		2	4	Ω
I_{PK}	Peak Output Current	—	2	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current (Duty Cycle $\leq 2\%$, $t \leq 300\mu\text{s}$, $V_{CC} = 18\text{V}$)		>0.5		A
t_R	Rise Time ($V_{CC} = 18\text{V}$, $C_{LOAD} = 100\text{pF}$)	—	—	30	ns
t_F	Fall Time ($V_{CC} = 18\text{V}$, $C_{LOAD} = 100\text{pF}$)			30	ns
t_{ON}	Turn On Delay Time ($V_{CC} = 18\text{V}$, $C_{LOAD} = 100\text{pF}$)			70	ns
t_{OFF}	Turn Off Delay Time ($V_{CC} = 18\text{V}$, $C_{LOAD} = 100\text{pF}$)			70	ns
I_{Q1}	Power Supply Current ($V_{INA} = V_{INB} = \text{a Logic-High}$)	—	—	1	mA
I_{Q0}	Supply Current ($V_{INA} = V_{INB} = \text{a Logic-Low}$)	—	—	1	mA

Chip Operating Logic

The GT4427 signal input Pin (INA, INB) adopts the level trigger mode, that is, if the voltage value meets the logic requirements, the chip can work normally, as shown in the following table.

Input And Output Logic Table

INPUT		OUTPUT	
INA	INB	OUTA	OUTB
L	L	L	L
H	H	H	H
L	H	L	H
H	L	H	L

Note: H represents high level; L represents low level

Signal input port

The GT4427 includes two independent signal input pins to receive control signals from the master controller without mutual interference. These two pins are designed with a high reliability. They can accept, without damage or logic upset, up to 500 mA of reverse current (of either polarity) being forced back into their outputs. At the same time, the input port has the ability to directly process -10V voltage, which can still ensure the safe operation of the chip under the influence of large noise wave, increasing the stability of chip.

It is not recommended to adjust the output waveform by adjusting the slope or delay of the input pin waveform during designation. If the rise and fall time of power needs to be adjusted, it is recommended to add an additional resistance between the output pin and the power pin. The GT4427 signal input pin has a Pull-up resistance for Vcc, so it is recommended to short this pin to Vcc when not in use.

Output port

GT4427 can be used to drive P-type or N-type MOSFETs. Each output port can provide a peak pull-up or pull-down current of 2A, and its high-speed and high current characteristics can be used to drive MOSFETs in high-frequency application designs

Application Information

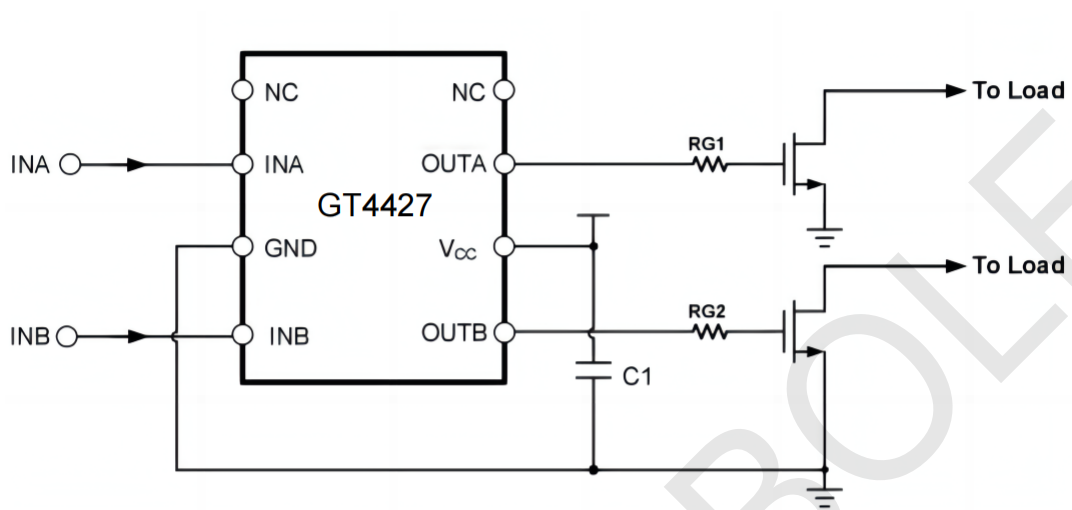
The high-speed and high-current characteristics of GT4427 can be used in high-frequency power supplies and other power supplies. Typical applications include that the power of the PWM output stage of the main control IC is often not enough to drive the MOSFET at the power end, so a high-power driver stage chip is required between the main control IC and the MOSFET to drive the Voltage gate of the MOSFET to ensure that the MOSFET works in a stable state.

Application Recommendations

In the high-frequency and high-power application environment, it is particularly important to ensure the stable operation of the chip. Therefore, the following suggestions are put forward for the application of GT4427:

- 1) During the switching process, GT4427 will output a switching current with a peak value of 2A, and with the increase of frequency, the requirements for Vcc stability are more stringent. Therefore, during design, an electrolytic capacitor with a large capacitance can be selected to stabilize the Vcc voltage, and in order to cope with the high-frequency characteristics, a low ESR/ESL capacitor (ceramic capacitor or chip capacitor) can be used in parallel. Physically, the capacitor should be as close as possible to both ends of Vcc and GND.
- 2) The output pin is also a part of the power circuit. In order to ensure the flatness of the output waveform, the output pin should be designed with the power pin and the gates of the MOSFETs are placed as close together as possible. In addition, additional resistance can be designed outside of OUT to make the operating waveform more stable.

Typical Application Circuit



Circuit diagram for in-phase application

PCB Layout Guide

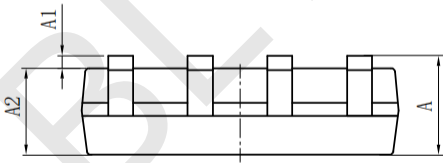
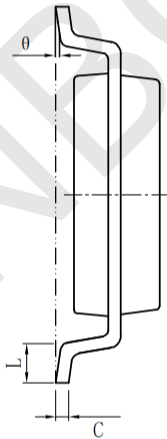
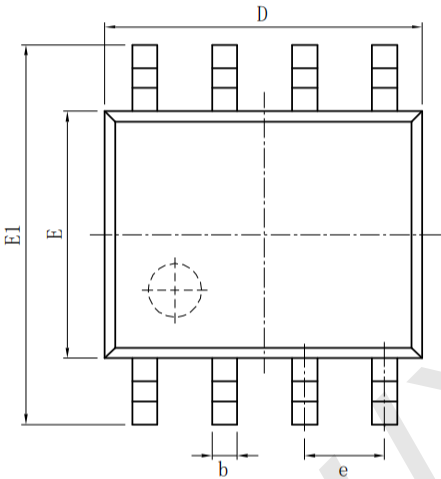
In order to achieve the best performance of the high speed low side driver. It is recommended to pay attention to the following points:

- 1) A low ESR/ESL capacitor must be tightly connected to the IC between the Vcc and GND pins to support the high peak current drawn from the VDD during MOSFET ON.
- 2) Grounding considerations:
 - The primary goal of designing the ground connection is to limit the loop of MOSFET gate charge and discharge to the smallest possible area. In this way, the loop inductance is reduced, which can effectively avoid noise problems on the MOSFET gate. At the same time, the gate driver chip should be as close as possible to the MOSFET.
 - Star point grounding is a good way to reduce noise coupling from one current loop to another. The ground single point of the driver is connected to other circuit nodes such as the source of the power MOSFET and the ground of the PWM controller. The connection path must be as short as possible to reduce inductance and as wide as possible to reduce resistance.
 - Adopting a ground plane to shield noise. Since the fast rise and fall time of OUT may destroy the input signal during the transition, the input signal can be guaranteed not to be disturbed by shielding the noise through the ground plane. The ground plane must not be a conduction path for any current loop, and the ground plane must be connected to the star point to establish ground potential. In addition to shielding against noise, the ground plane also helps to dissipate heat.
- 3) In a noisy environment, to prevent output failure caused by noise, an unused PIN can be connect to VDD or GND.
- 4) Separate power circuit and signal circuit, such as output and input signals.

Package Information

- SOP-8

Size Symbol	Dimensions In Millimeters		Size Symbol	Dimensions In Inches	
	Min (mm)	Max (mm)		Min (in)	Max (in)
A	1.350	1.750	A	0.053	0.069
A1	0.100	0.250	A1	0.004	0.010
A2	1.350	1.550	A2	0.053	0.061
b	0.330	0.510	b	0.013	0.020
c	0.170	0.250	c	0.006	0.010
D	4.700	5.100	D	0.185	0.200
E	3.800	4.000	E	0.150	0.157
E1	5.800	6.200	E1	0.228	0.224
e	1.270 (BSC)		e	0.050 (BSC)	
L	0.400	1.270	L	0.016	0.050
θ	0°	8°	θ	0°	8°



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