- **Replacements for ADI, PMI and LTC OP27 Series**

**Features of OP27A and OP27C:**

- **Maximum Equivalent Input Noise Voltage:**
  **3.8 nV/$\sqrt{\text{Hz}}$ at 1 kHz**
  **5.5 nV/$\sqrt{\text{Hz}}$ at 10 kHz**
- **Very Low Peak-to-Peak Noise Voltage at 0.1 Hz to 10 Hz . . . 80 nV Typ**
- **Low Input Offset Voltage**
  **OP27A . . . 25 μV Max**
  **OP27C . . . 100 μV Max**
- **High Voltage Amplification**
  **OP27A . . . 1 V/μV Min**
  **OP27C . . . 0.7 V/μV Min**

## description

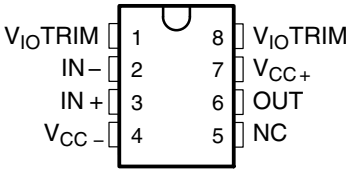
The OP27 operational amplifiers combine outstanding noise performance with excellent precision and high-speed specifications. The wideband noise is only 3 nV/$\sqrt{\text{Hz}}$ and with the 1/f noise corner at 2.7 Hz, low noise is maintained for all low-frequency applications.

The outstanding characteristics of the OP27 make these devices excellent choices for low-noise amplifier applications requiring precision performance and reliability.

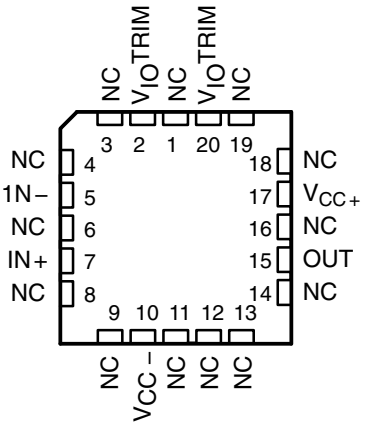
The OP27 series is compensated for unity gain.

The OP27A and OP27C are characterized for operation over the full military temperature range of −55°C to 125°C.

**JG PACKAGE**
**(TOP VIEW)**

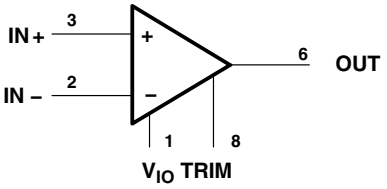



**FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## symbol




Pin numbers are for the JG packages.

**AVAILABLE OPTIONS**

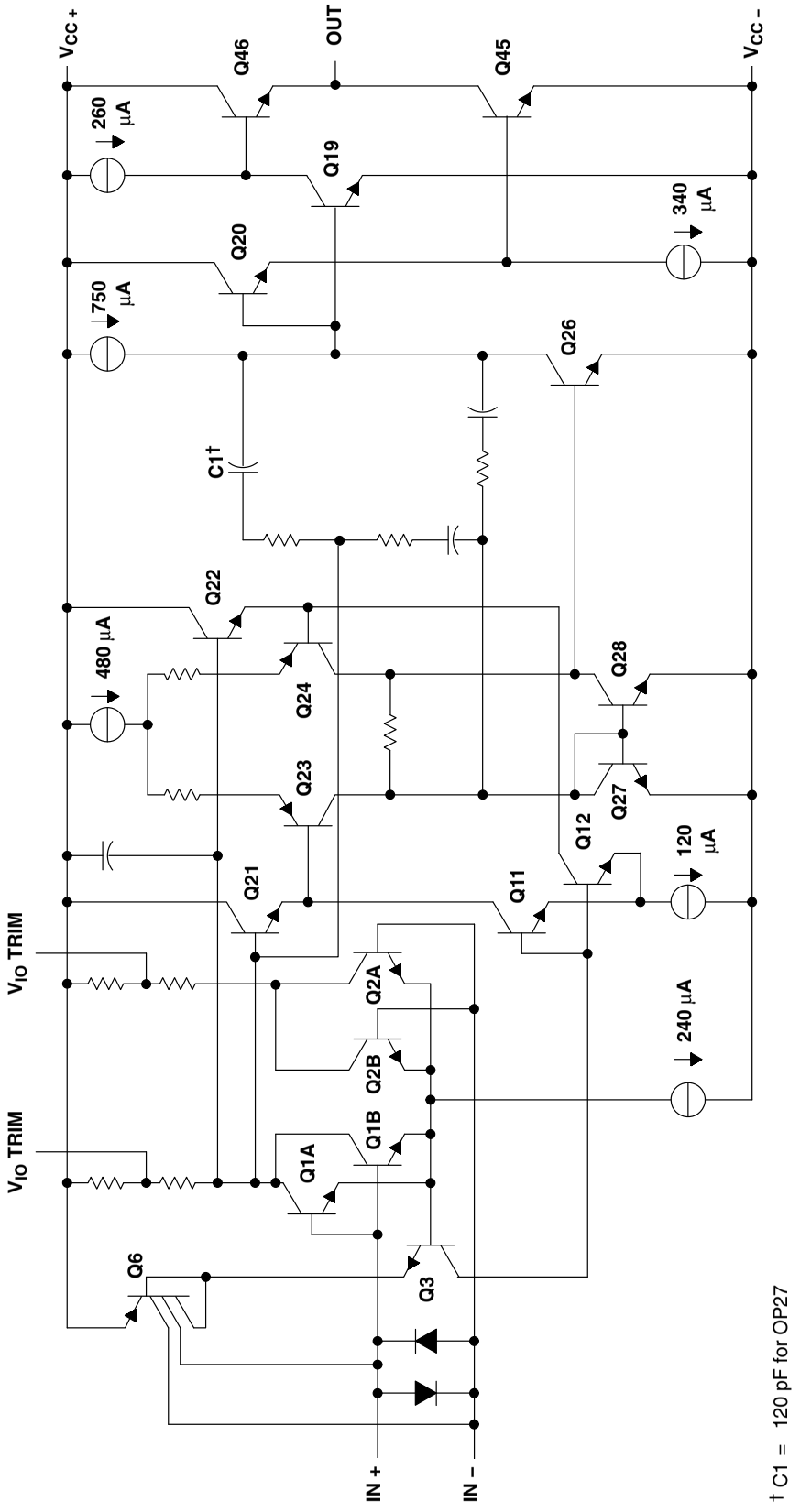
| $T_A$ | $V_{IO}$max AT 25°C | STABLE GAIN | PACKAGE | |
|---|---|---|---|---|
| | | | CERAMIC DIP (JG) | CHIP CARRIER (FK) |
| −55°C to 125°C | 25 μV | 1 | OP27AJG | OP27AFK |
| | 100 μV | 1 | OP27CJG | — |

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## schematic




† C1 = 120 pF for OP27

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC+}$ (see Note 1) . . . . . 22 V
Supply voltage, $V_{CC-}$ (see Note 1) . . . . . 22 V
Input voltage, $V_I$ . . . . . $V_{CC\pm}$
Duration of output short circuit . . . . . unlimited
Differential input current (see Note 2) . . . . . ±25 mA
Continuous power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: OP27A, OP27C . . . . . –55°C to 125°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or FK package . . . . . 300°C

NOTES: 1. All voltage values are with respect to the midpoint between $V_{CC+}$ and $V_{CC-}$ unless otherwise noted.
2. The inputs are protected by back-to-back diodes. Current-limiting resistors are not used in order to achieve low noise. Excessive input current will flow if a differential input voltage in excess of approximately ±0.7 V is applied between the inputs unless some limiting resistance is used.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \leq 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 85°C$ POWER RATING | $T_A = 125°C$ POWER RATING |
|---|---|---|---|---|
| JG | 1050 mW | 8.4 mW/°C | 546 mW | 210 mW |
| FK | 1375 mW | 11.0 mW/°C | 715 mW | 275 mW |

## recommended operating conditions

| | | OP27A | | | OP27C | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC+}$ | | 4 | 15 | 22 | 4 | 15 | 22 | V |
| Supply voltage, $V_{CC-}$ | | −4 | −15 | −22 | −4 | −15 | −22 | V |
| Common-mode input voltage, $V_{IC}$ | $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$ | ±11 | | | ±11 | | | V |
| | $V_{CC\pm} = \pm 15$ V, $T_A = -55°C$ to 125°C | ±10.3 | | | ±10.2 | | | |
| Operating free-air temperature, $T_A$ | | −55 | | 125 | −55 | | 125 | °C |

## electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$† | OP27A | | | OP27C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{IO}$ | Input offset voltage | $V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$, See Note 3 | 25°C | | 10 | 25 | | 30 | 100 | μV |
| | | | Full range | | | 60 | | | 300 | |
| $\alpha_{VIO}$ | Average temperature coefficient of input offset voltage | | Full range | | 0.2 | 0.6 | | 0.4 | 1.8 | μV/°C |
| | Long-term drift of input offset voltage | See Note 4 | | | 0.2 | 1 | | 0.4 | 2 | μV/mo |
| $I_{IO}$ | Input offset current | $V_O = 0$, $V_{IC} = 0$ | 25°C | | 7 | 35 | | 12 | 75 | nA |
| | | | Full range | | | 50 | | | 135 | |
| $I_{IB}$ | Input bias current | $V_O = 0$, $V_{IC} = 0$ | 25°C | | ±10 | ±40 | | ±15 | ±80 | nA |
| | | | Full range | | | ±60 | | | ±150 | |
| $V_{ICR}$ | Common-mode input voltage range | | 25°C | 11 to −11 | | | 11 to −11 | | | V |
| | | | Full range | 10.3 to −10.3 | | | 10.5 to −10.5 | | | |
| $V_{OM}$ | Peak output voltage swing | $R_L \geq 2$ kΩ | | ±12 | ±13.8 | | ±11.5 | ±13.5 | | V |
| | | $R_L \geq 0.6$ kΩ | | ±10 | ±11.5 | | ±10 | ±11.5 | | |
| | | $R_L \geq 2$ kΩ | Full range | ±11.5 | | | 10.5 | | | |
| $A_{VD}$ | Large-signal differential voltage amplification | $R_L \geq 2$ kΩ, $V_O = \pm 10$ V | | 1000 | 1800 | | 700 | 1500 | | V/mV |
| | | $R_L \geq 1$ kΩ, $V_O = \pm 10$ V | | 800 | 1500 | | | 1500 | | |
| | | $R_L \geq 0.6$ kΩ, $V_O = \pm 1$ V, $V_{CC\pm} = \pm 4$ V | | 250 | 700 | | 200 | 500 | | |
| | | $R_L \geq 2$ kΩ, $V_O = \pm 10$ V | Full range | 600 | | | 300 | | | |
| $r_{i(CM)}$ | Common-mode input resistance | | | | 3 | | | 2 | | GΩ |
| $r_o$ | Output resistance | $V_O = 0$, $I_O = 0$ | 25°C | | 70 | | | 70 | | Ω |
| CMRR | Common-mode rejection ratio | $V_{IC} = \pm 11$ V | 25°C | 114 | 126 | | 100 | 120 | | dB |
| | | $V_{IC} = \pm 10$ V | Full range | 110 | | | 94 | | | |
| $k_{SVR}$ | Supply voltage rejection ratio | $V_{CC\pm} = \pm 4$ V to ±18 V | 25°C | 100 | 120 | | 94 | 118 | | dB |
| | | $V_{CC\pm} = \pm 4.5$ V to ±18 V | Full range | 96 | | | 86 | | | |

† Full range is – 55°C to 125°C.

NOTES: 3. Input offset voltage measurements are performed by automatic test equipment approximately 0.5 seconds after applying power.
4. Long-term drift of input offset voltage refers to the average trend line of offset voltage versus time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in $V_{IO}$ during the first 30 days are typically 2.5 μV (see Figure 3).

## OP27 operating characteristics, $V_{CC\pm}$ = ±15 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | OP27A | | | OP27C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| SR | Slew rate | $A_{VD} \geq 1$, | $R_L \geq 2$ kΩ | 1.7 | 2.8 | | 1.7 | 2.8 | | V/μs |
| $V_{N(PP)}$ | Peak-to-peak equivalent input noise voltage | f = 0.1 Hz to 10 Hz, See Figure 26 | $R_S$ = 20 Ω, | | 0.225 | 0.375 | | 0.225 | 0.375 | μV |
| $V_n$ | Equivalent input noise voltage | f = 10 Hz, | $R_S$ = 20 Ω | | 3.5 | 8 | | 3.8 | 8 | nV/√Hz |
| | | f = 1 kHz, | $R_S$ = 20 Ω | | 3 | 4 | | 3.2 | 4 | |
| $I_n$ | Equivalent input noise current | f = 10 Hz, | See Figure 27 | | 5 | 25 | | 5 | 25 | pA/√Hz |
| | | f = 1 kHz, | See Figure 27 | | 0.7 | 2.5 | | 0.7 | 2.5 | |
| | Gain-bandwidth product | f = 100 kHz | | 5 | 8 | | 5 | 8 | | MHz |

## TYPICAL CHARACTERISTICS

### Table of Graphs

| | | | FIGURE |
|---|---|---|---|
| $V_{IO}$ | Input offset voltage | vs Temperature | 1 |
| $\Delta V_{IO}$ | Change in input offset voltage | vs Time after power on<br>vs Time (long-term drift) | 2<br>3 |
| $I_{IO}$ | Input offset current | vs Temperature | 4 |
| $I_{IB}$ | Input bias current | vs Temperature | 5 |
| $V_{ICR}$ | Common-mode input voltage range | vs Supply voltage | 6 |
| $V_{OM}$ | Maximum peak output voltage | vs Load resistance | 7 |
| $V_{O(PP)}$ | Maximum peak-to-peak output voltage | vs Frequency | 8 |
| $A_{VD}$ | Differential voltage amplification | vs Supply voltage<br>vs Load resistance<br>vs Frequency | 9<br>10<br>11, 12 |
| CMRR | Common-mode rejection ratio | vs Frequency | 13 |
| $k_{SVR}$ | Supply voltage rejection ratio | vs Frequency | 14 |
| SR | Slew rate | vs Temperature | 15 |
| $\phi_m$ | Phase margin | vs Temperature | 16 |
| $\phi$ | Phase shift | vs Frequency | 11 |
| $V_n$ | Equivalent input noise voltage | vs Bandwidth<br>vs Source resistance<br>vs Supply voltage<br>vs Temperature<br>vs Frequency | 17<br>18<br>19<br>20<br>21 |
| | Gain-bandwidth product | vs Temperature | 16 |
| $I_{OS}$ | Short-circuit output current | vs Time | 22 |
| $I_{CC}$ | Supply current | vs Supply voltage | 23 |
| | Pulse response | Small signal<br>Large signal | 24<br>25 |

## TYPICAL CHARACTERISTICS

**INPUT OFFSET VOLTAGE OF REPRESENTATIVE INDIVIDUAL UNITS vs FREE-AIR TEMPERATURE**

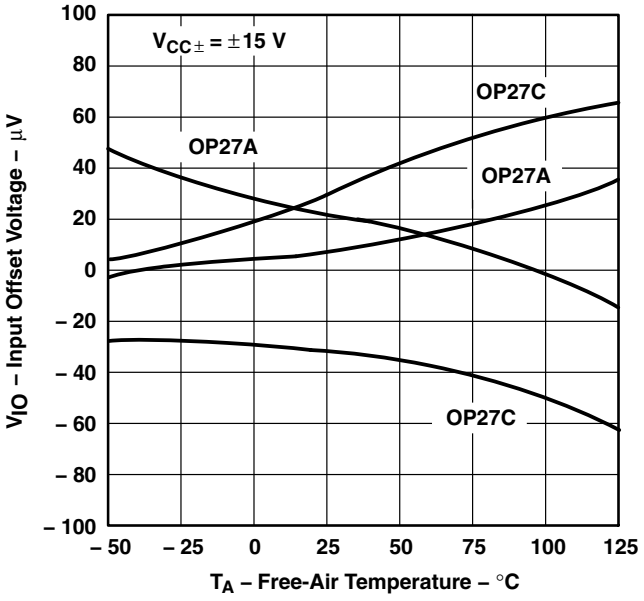



Figure 1

**WARM-UP CHANGE IN INPUT OFFSET VOLTAGE vs ELAPSED TIME**

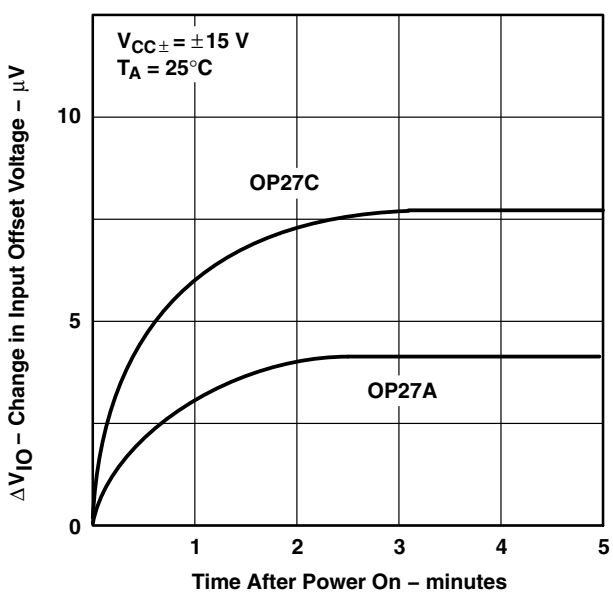



Figure 2

**LONG-TERM DRIFT OF INPUT OFFSET VOLTAGE OF REPRESENTATIVE INDIVIDUAL UNITS**

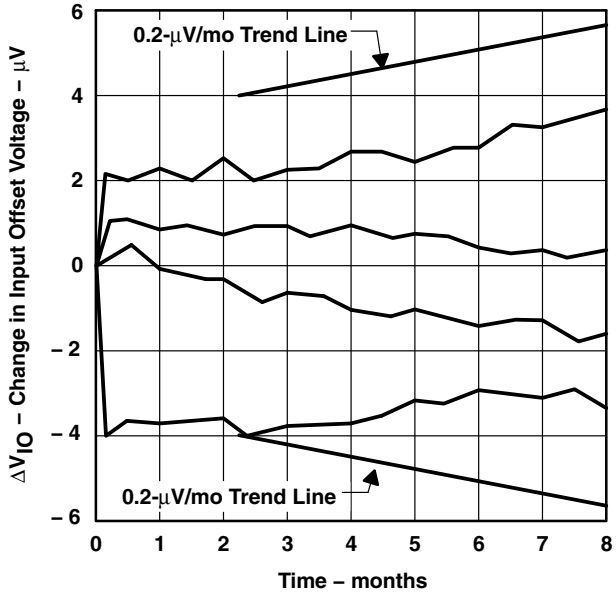



Figure 3

## TYPICAL CHARACTERISTICS

**INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE**

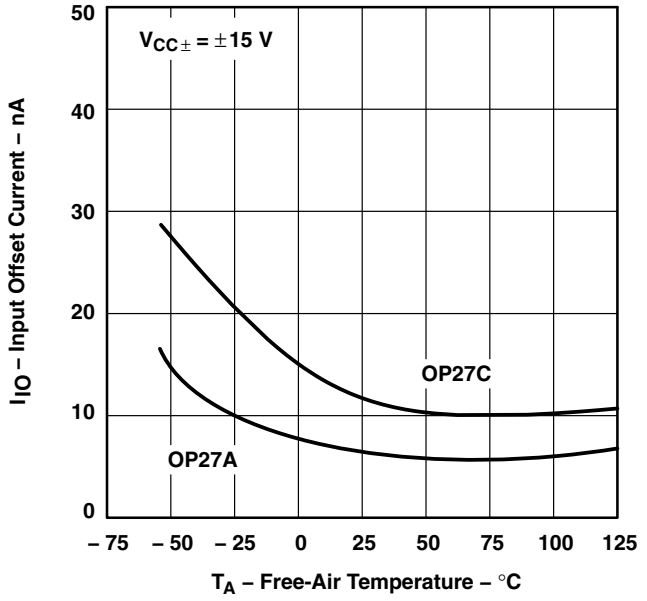



Figure 4

**INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE**

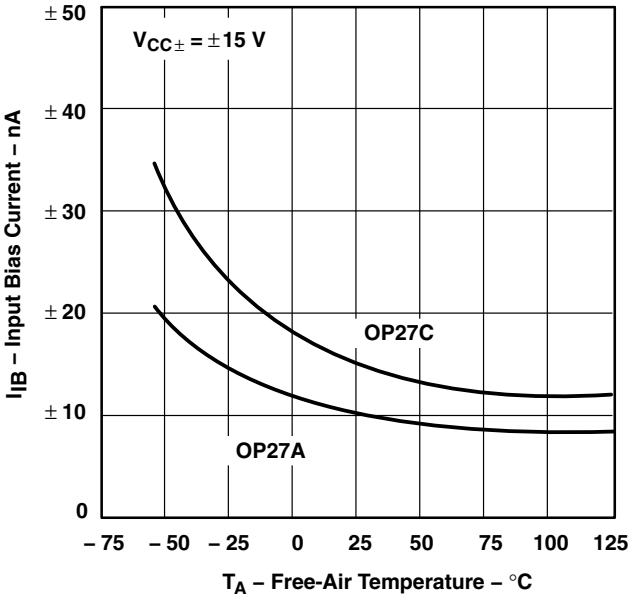



Figure 5

**COMMON-MODE INPUT VOLTAGE RANGE LIMITS vs SUPPLY VOLTAGE**

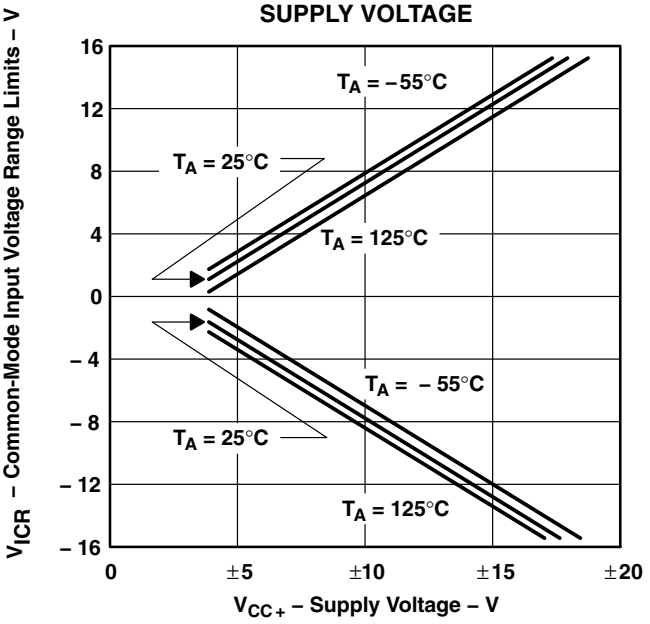



Figure 6

**MAXIMUM PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE**

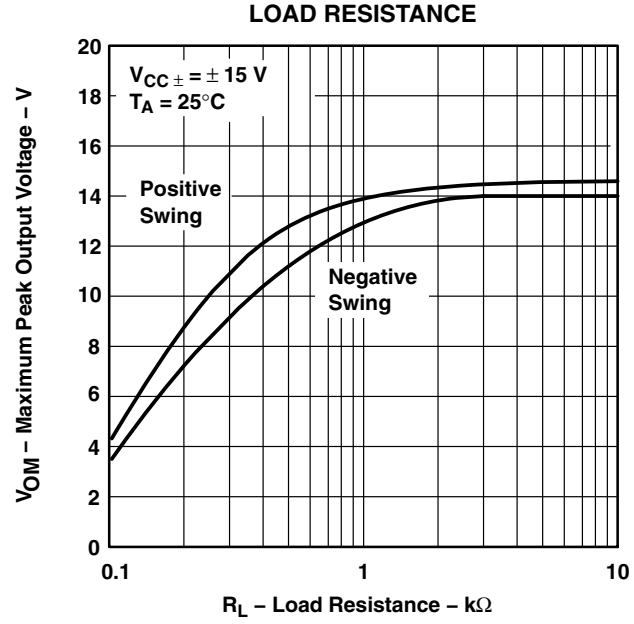



Figure 7

## TYPICAL CHARACTERISTICS

**OP27**
**MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY**

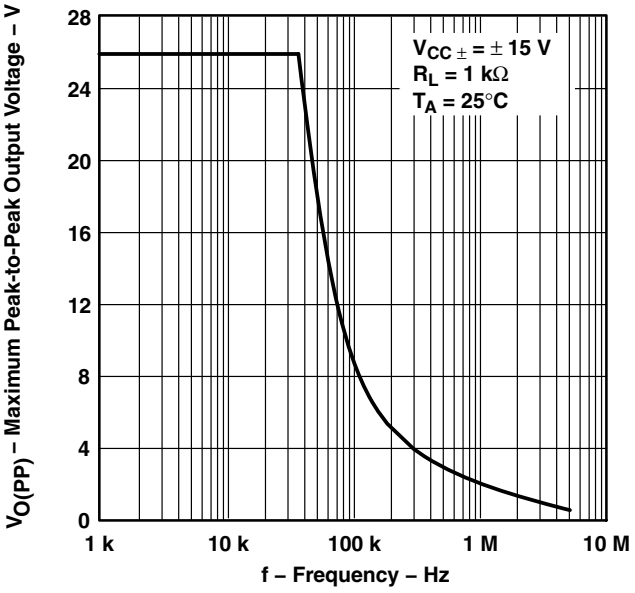



**Figure 8.**

**OP27A**
**LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs TOTAL SUPPLY VOLTAGE**

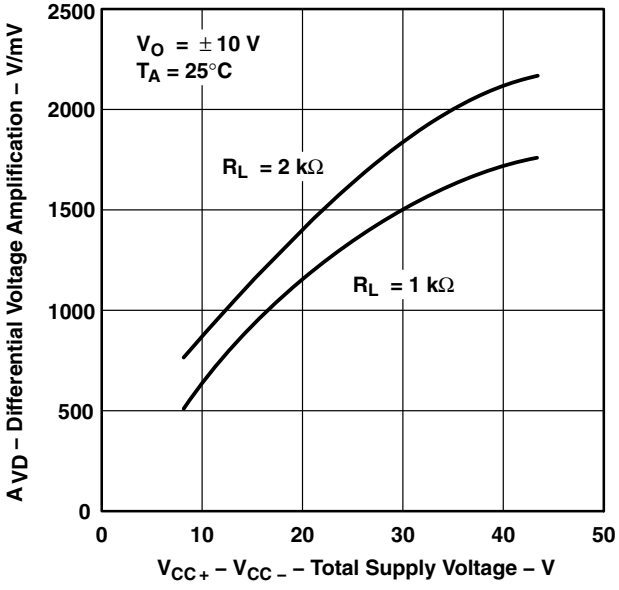



**Figure 9**

**OP27A**
**LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE**

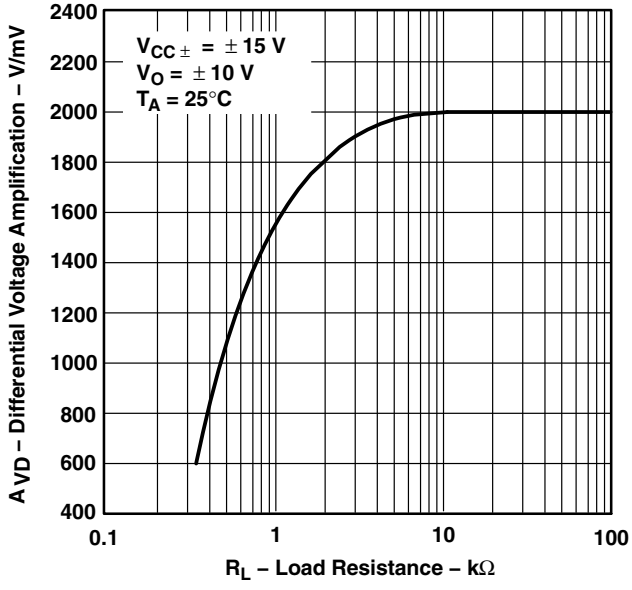



**Figure 10**

## TYPICAL CHARACTERISTICS

**OP27**
**LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY**

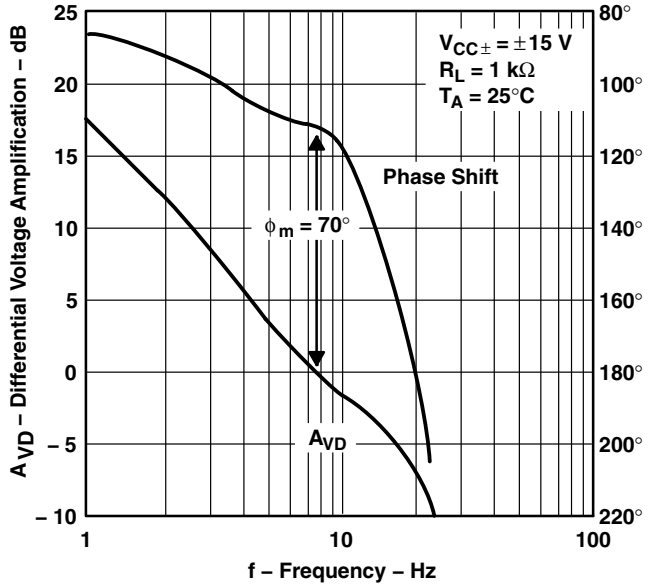



**Figure 11.**

**OP27A**
**LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY**

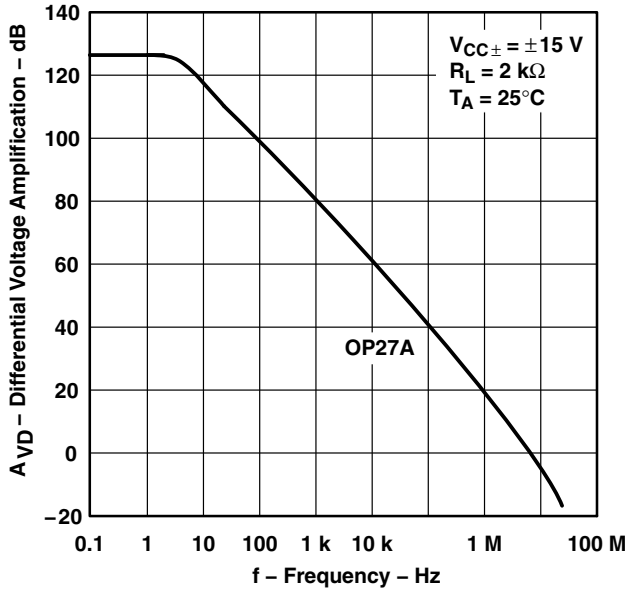



**Figure 12**

**OP27A**
**COMMON-MODE REJECTION RATIO vs FREQUENCY**

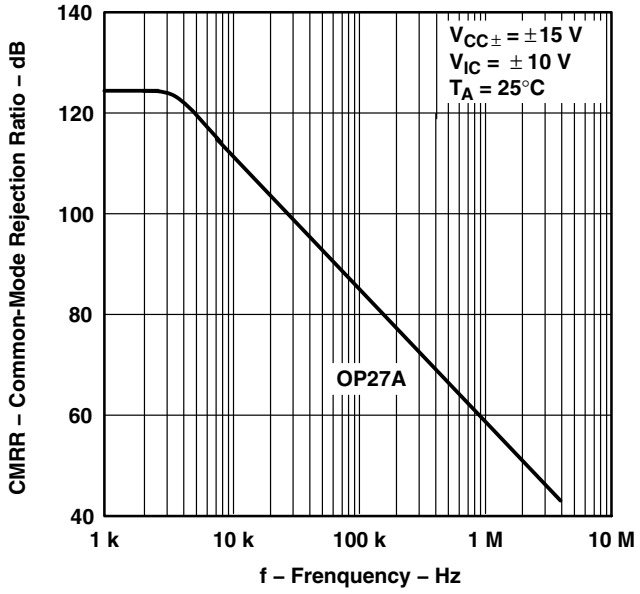



**Figure 13**

## TYPICAL CHARACTERISTICS

**SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY**

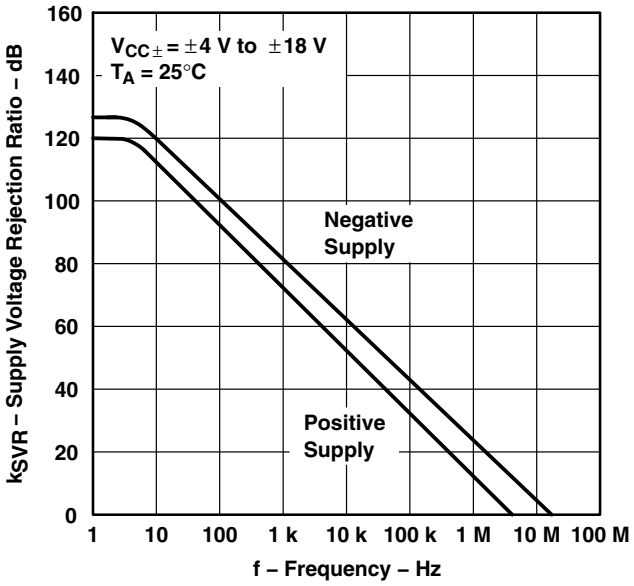



**Figure 14**

**SLEW RATE vs FREE-AIR TEMPERATURE**

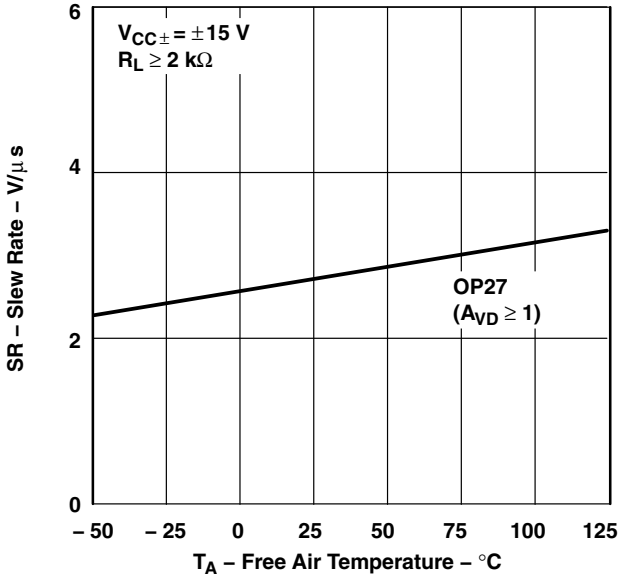



**Figure 15**

**OP27**
**PHASE MARGIN AND GAIN-BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE**

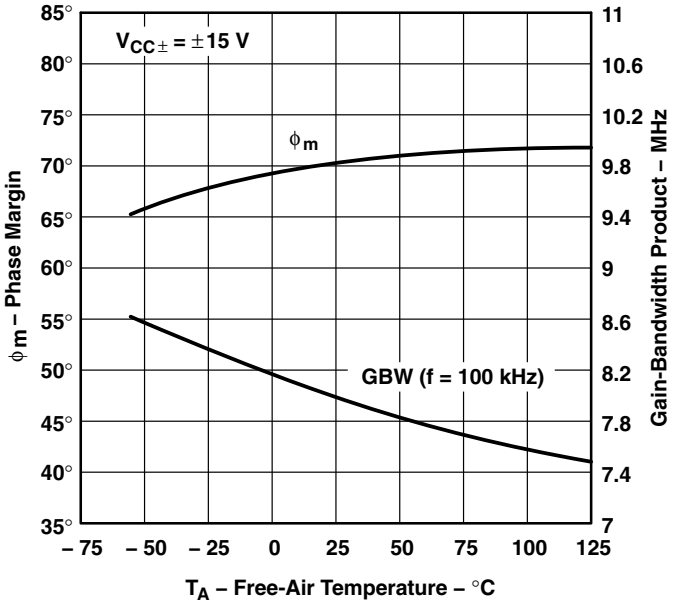



**Figure 16.**

## TYPICAL CHARACTERISTICS

**EQUIVALENT INPUT NOISE VOLTAGE vs BANDWIDTH**

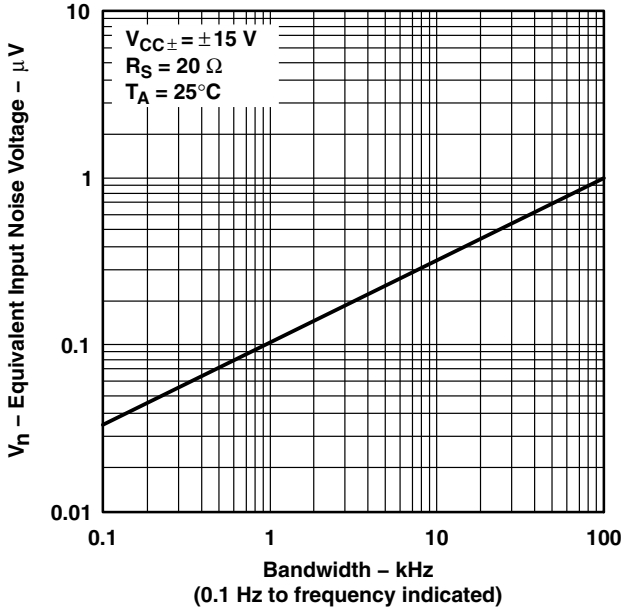



Figure 17

**TOTAL EQUIVALENT INPUT NOISE VOLTAGE vs SOURCE RESISTANCE**

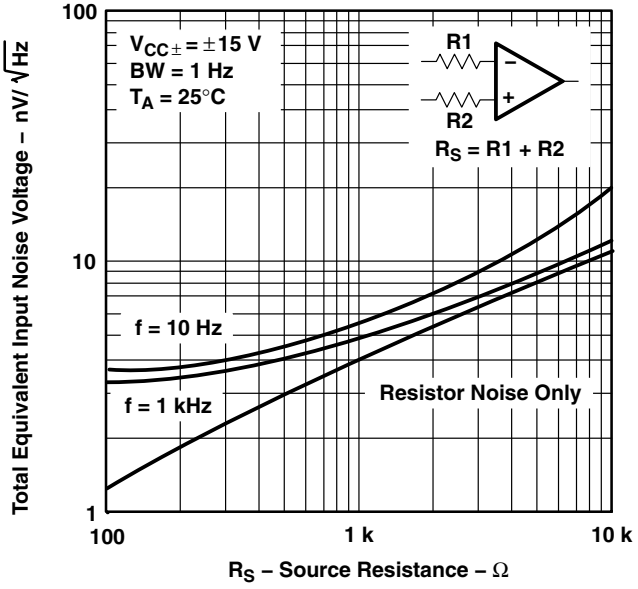



Figure 18

**OP27A EQUIVALENT INPUT NOISE VOLTAGE vs TOTAL SUPPLY VOLTAGE**

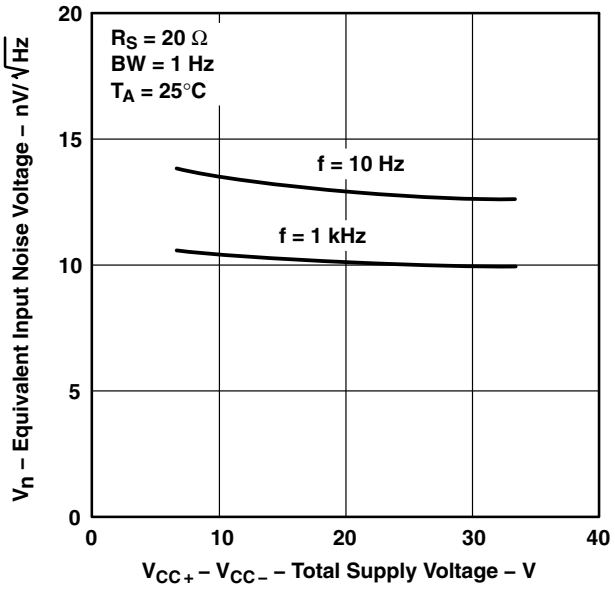



Figure 19

**OP27A EQUIVALENT INPUT NOISE VOLTAGE vs FREE-AIR TEMPERATURE**

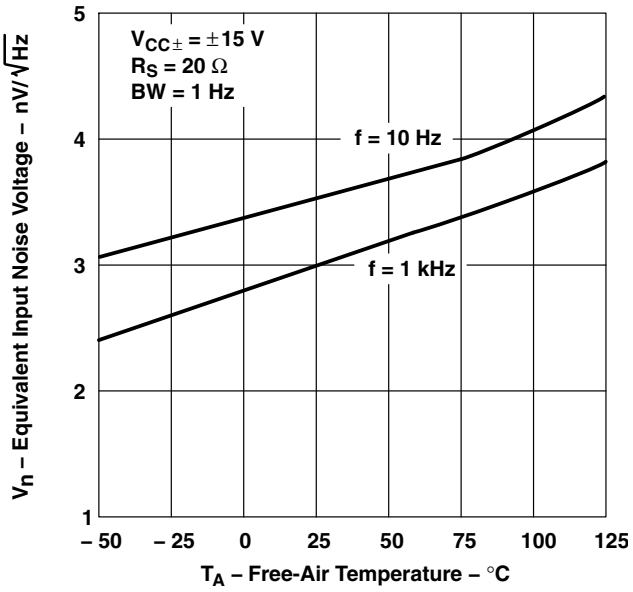



Figure 20

## TYPICAL CHARACTERISTICS

**OP27A**
**EQUIVALENT INPUT NOISE VOLTAGE**
**vs**
**FREQUENCY**

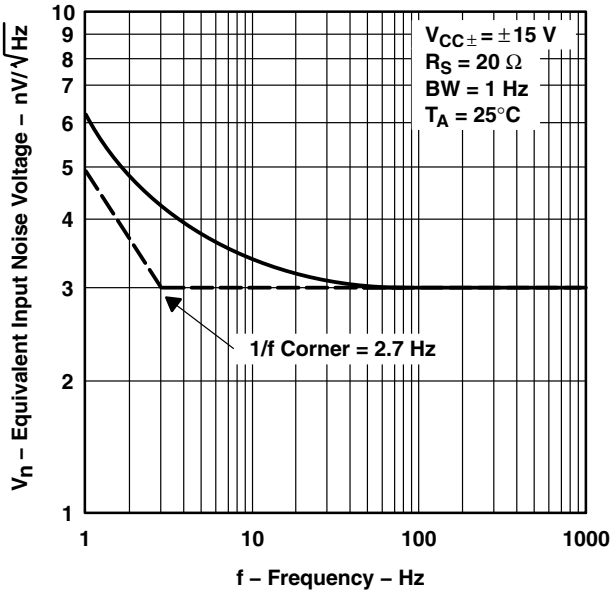



**Figure 21**

**SHORT-CIRCUIT OUTPUT CURRENT**
**vs**
**ELAPSED TIME**

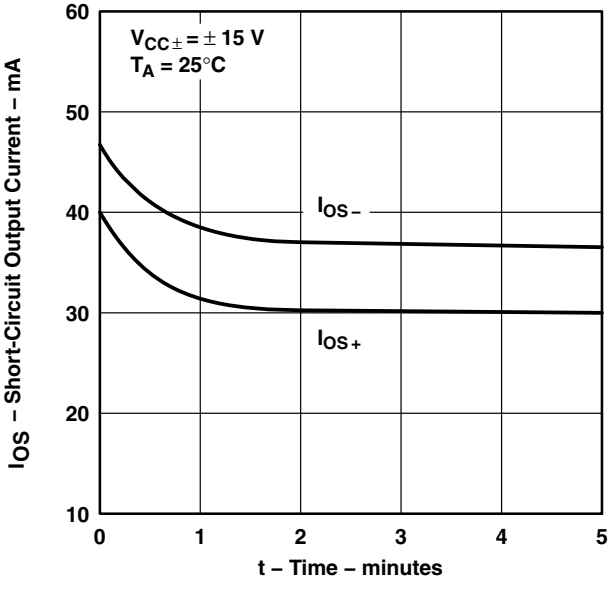



**Figure 22**

**SUPPLY CURRENT**
**vs**
**TOTAL SUPPLY VOLTAGE**

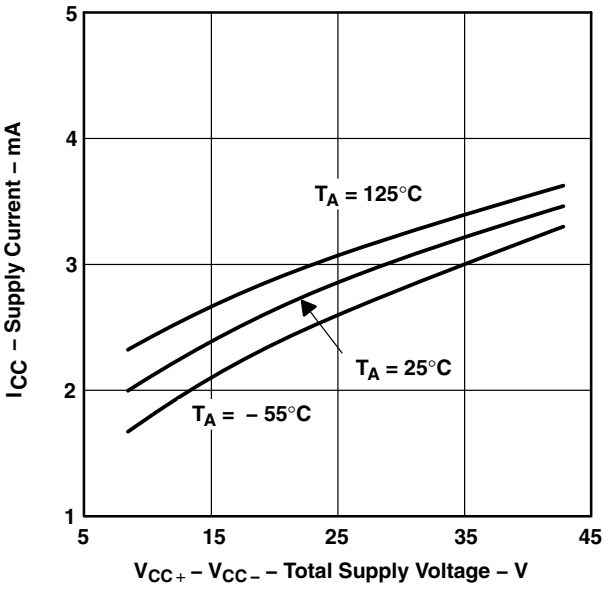



**Figure 23**

## TYPICAL CHARACTERISTICS

**OP27**
**VOLTAGE FOLLOWER**
**SMALL-SIGNAL**
**PULSE RESPONSE**

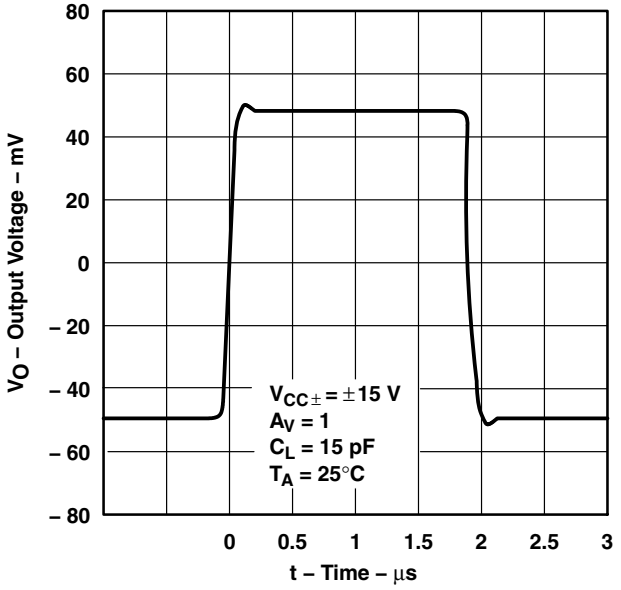



Figure 24

**OP27**
**VOLTAGE FOLLOWER**
**LARGE-SIGNAL**
**PULSE RESPONSE**

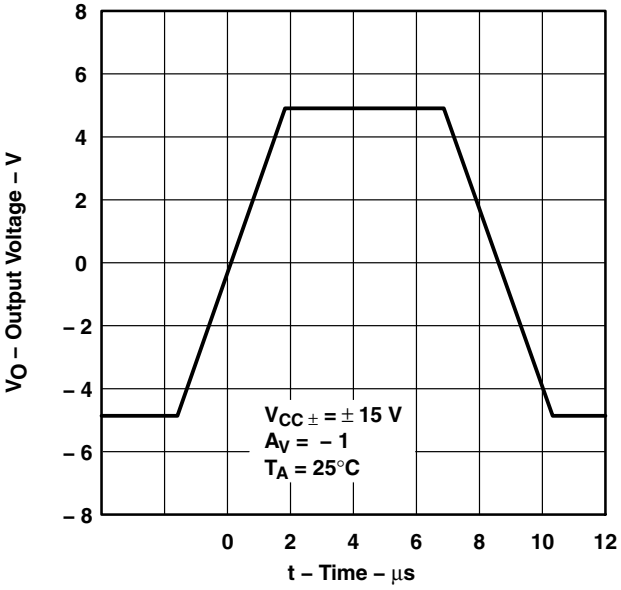



Figure 25

## APPLICATION INFORMATION

### general

The OP27 series devices can be inserted directly onto OP07, OP05, μA725, and SE5534 sockets with or without removing external compensation or nulling components. In addition, the OP27 can be fitted to μA741 sockets by removing or modifying external nulling components.

### noise testing

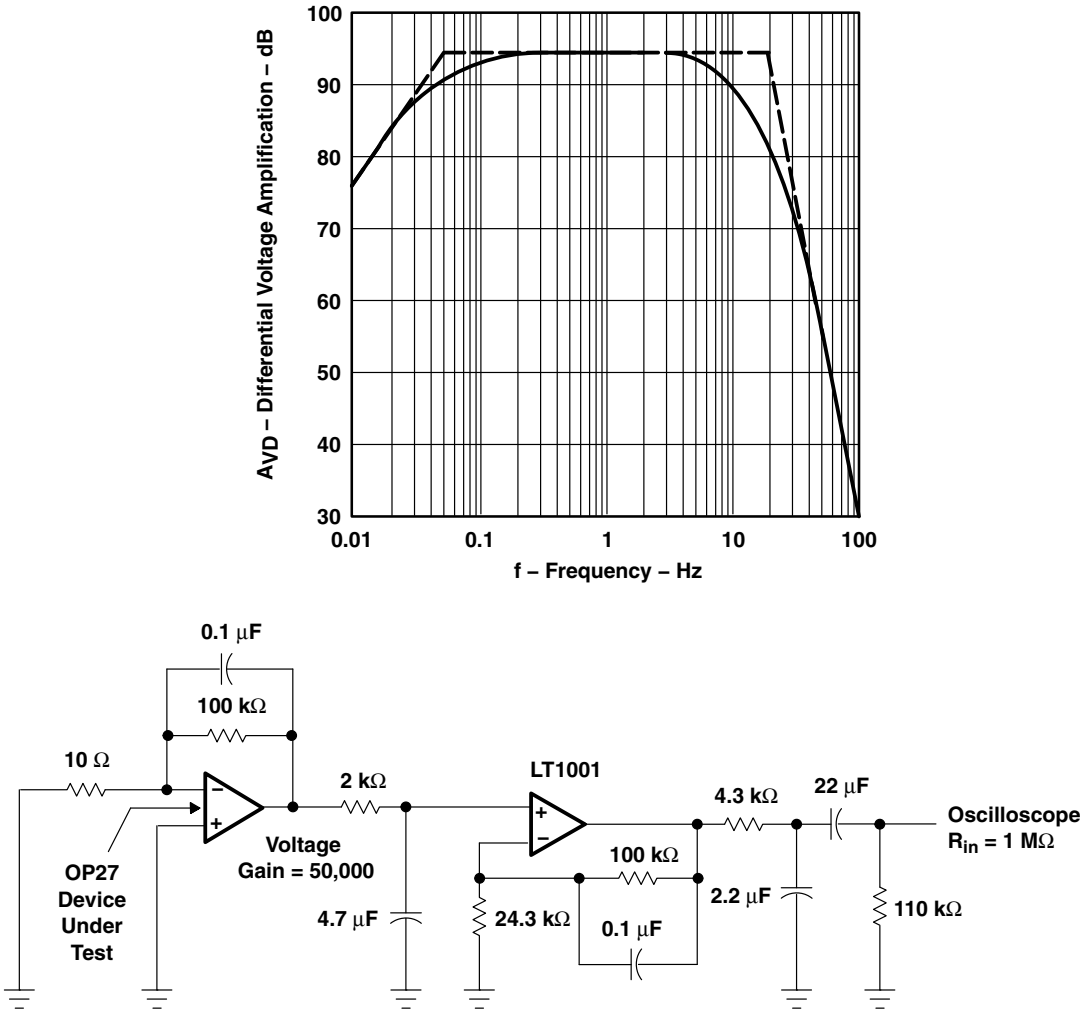
Figure 26 shows a test circuit for 0.1-Hz to 10-Hz peak-to-peak noise measurement of the OP27. The frequency response of this noise tester indicates that the 0.1-Hz corner is defined by only one zero. Because the time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1 Hz, the test time to measure 0.1-Hz to 10-Hz noise should not exceed 10 seconds.

Measuring the typical 80-nV peak-to-peak noise performance of the OP27 requires the following special test precautions:

## APPLICATION INFORMATION

### noise testing (continued)

1. The device should be warmed up for at least five minutes. As the operational amplifier warms up, the offset voltage typically changes 4 μV due to the chip temperature increasing from 10°C to 20°C starting from the moment the power supplies are turned on. In the 10-s measurement interval, these temperature-induced effects can easily exceed tens of nanovolts.
2. For similar reasons, the device should be well shielded from air currents to eliminate the possibility of thermoelectric effects in excess of a few nanovolts, which would invalidate the measurements.
3. Sudden motion in the vicinity of the device should be avoided, as it produces a feedthrough effect that increases observed noise.




NOTE: All capacitor values are for nonpolarized capacitors only.

**Figure 26. 0.1-Hz to 10-Hz Peak-to-Peak Noise Test Circuit and Frequency Response**

## APPLICATION INFORMATION

### noise testing (continued)

When measuring noise on a large number of units, a noise-voltage density test is recommended. A 10-Hz noise-voltage density measurement correlates well with a 0.1-Hz to 10-Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

Figure 27 shows a circuit measuring current noise and the formula for calculating current noise.

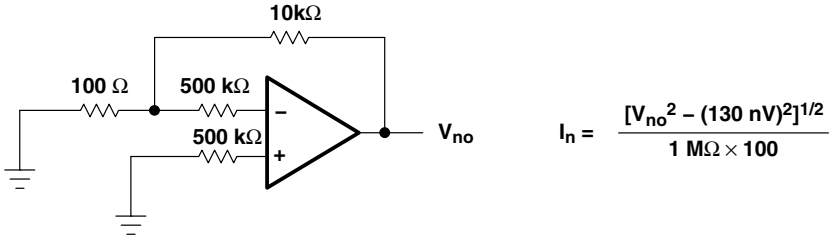



**Figure 27. Current Noise Test Circuit and Formula**

### offset voltage adjustment

The input offset voltage and temperature coefficient of the OP27 are permanently trimmed to a low level at wafer testing. However, if further adjustment of $V_{IO}$ is necessary, using a 10-kΩ nulling potentiometer as shown in Figure 28 does not degrade the temperature coefficient $\alpha_{VIO}$. Trimming to a value other than zero creates an $\alpha_{VIO}$ of $V_{IO}$/300 μV/°C. For example, if $V_{IO}$ is adjusted to 300 μV, the change in $\alpha_{VIO}$ is 1 μV/°C.

The adjustment range with a 10-kΩ potentiometer is approximately ±2.5 mV. If a smaller adjustment range is needed, the sensitivity and resolution of the nulling can be improved by using a smaller potentiometer in conjunction with fixed resistors. The example in Figure 29 has an approximate null range of ±200 μV.

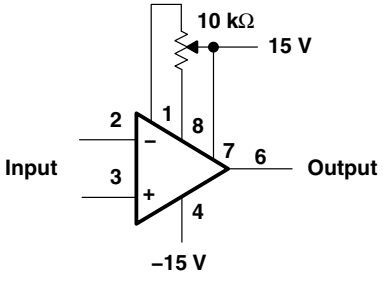



**Figure 28. Standard Input Offset Voltage Adjustment**

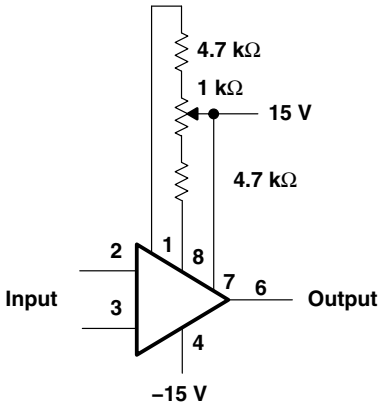



**Figure 29. Input Offset Voltage Adjustment With Improved Sensitivity**

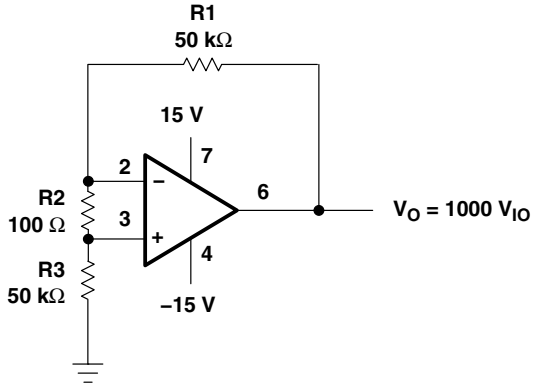
### offset voltage and drift

Unless proper care is exercised, thermoelectric effects caused by temperature gradients across dissimilar metals at the contacts to the input terminals can exceed the inherent temperature coefficient $\propto V_{IO}$ of the amplifier. Air currents should be minimized, package leads should be short, and the two input leads should be close together and at the same temperature.

## APPLICATION INFORMATION

### offset voltage and drift (continued)

The circuit shown in Figure 30 measures offset voltage. This circuit can also be used as the burn-in configuration for the OP27 with the supply voltage increased to 20 V, R1 = R3 = 10 kΩ, R2 = 200 Ω, and $A_{VD}$ = 100.




NOTE A: Resistors must have low thermoelectric potential.

**Figure 30. Test Circuit for Offset Voltage and Offset Voltage Temperature Coefficient**

### unity gain buffer applications

The resulting output waveform, when $R_f \leq 100\ \Omega$ and the input is driven with a fast large-signal pulse (>1 V), is shown in the pulsed-operation diagram in Figure 31.

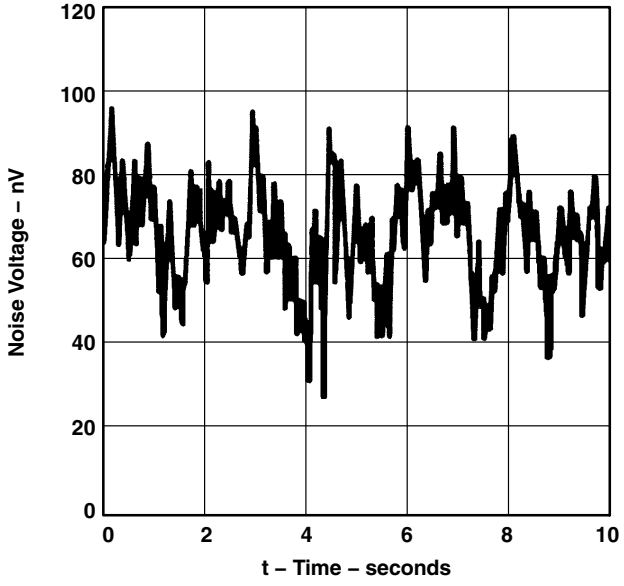


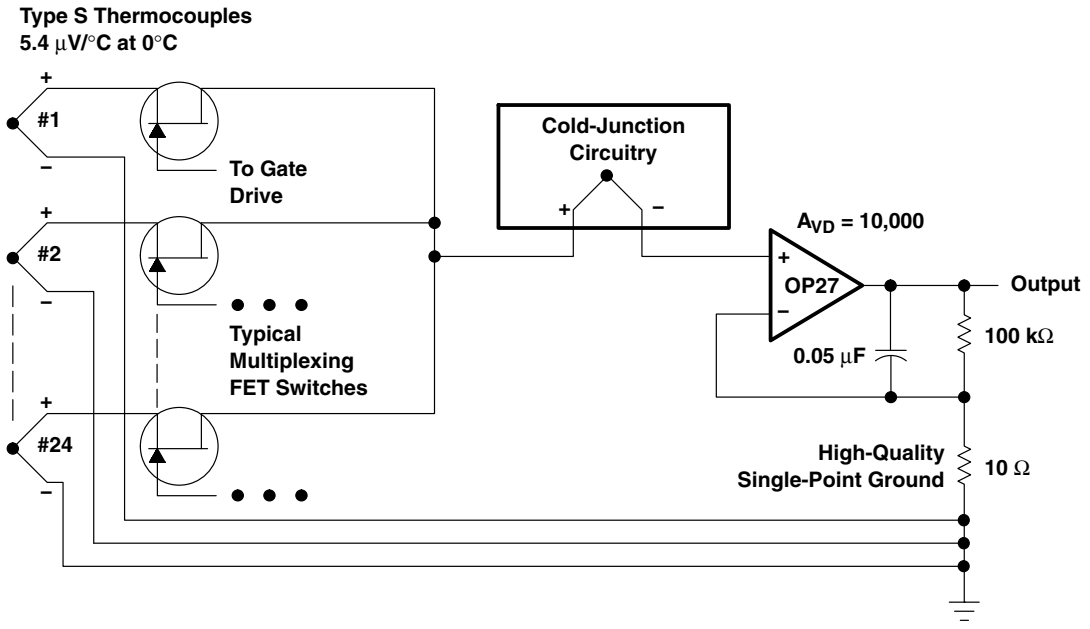

**Figure 31. Pulsed Operation**

During the initial (fast-feedthrough-like) portion of the output waveform, the input protection diodes effectively short the output to the input, and a current, limited only by the output short-circuit protection, is drawn by the signal generator. When $R_f \geq 500\ \Omega$, the output is capable of handling the current requirements (load current ≤20 mA at 10 V), the amplifier stays in its active mode, and a smooth transition occurs. When $R_f > 2$ kΩ, a pole is created with $R_f$ and the amplifier's input capacitance, creating additional phase shift and reducing the phase margin. A small capacitor (20 pF to 50 pF) in parallel with $R_f$ eliminates this problem.

## APPLICATION INFORMATION

### unity gain buffer applications (continued)




NOTE A: If 24 channels are multiplexed per second and the output is required to settle to 0.1 % accuracy, the amplifier's bandwidth cannot be limited to less than 30 Hz. The peak-to-peak noise contribution of the OP27 will still be only 0.11 μV, which is equivalent to an error of only 0.02°C.

**Figure 32. Low-Noise, Multiplexed Thermocouple Amplifier and 0.1-Hz to 10-Hz Peak-to-Peak Noise Voltage**

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| JM38510/13506BPA | Active | Production | CDIP (JG) \| 8 | 50 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510 /13506BPA |
| OP27AFKB | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | - | OP27AFKB |
| OP27AJGB | Active | Production | CDIP (JG) \| 8 | 50 \| TUBE | No | SNPB | N/A for Pkg Type | - | OP27AJGB |
| OP27CJGB | Active | Production | CDIP (JG) \| 8 | 50 \| TUBE | No | SNPB | N/A for Pkg Type | - | OP27CJGB |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

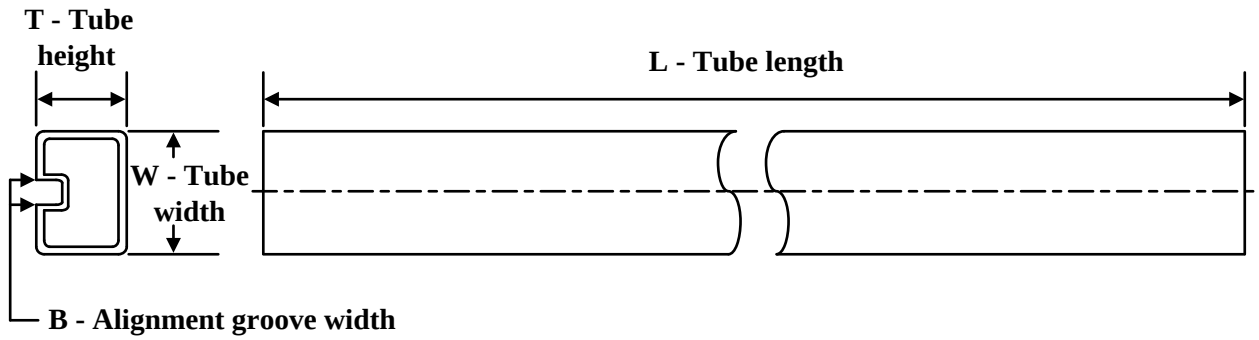
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| OP27AFKB | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |

# GENERIC PACKAGE VIEW

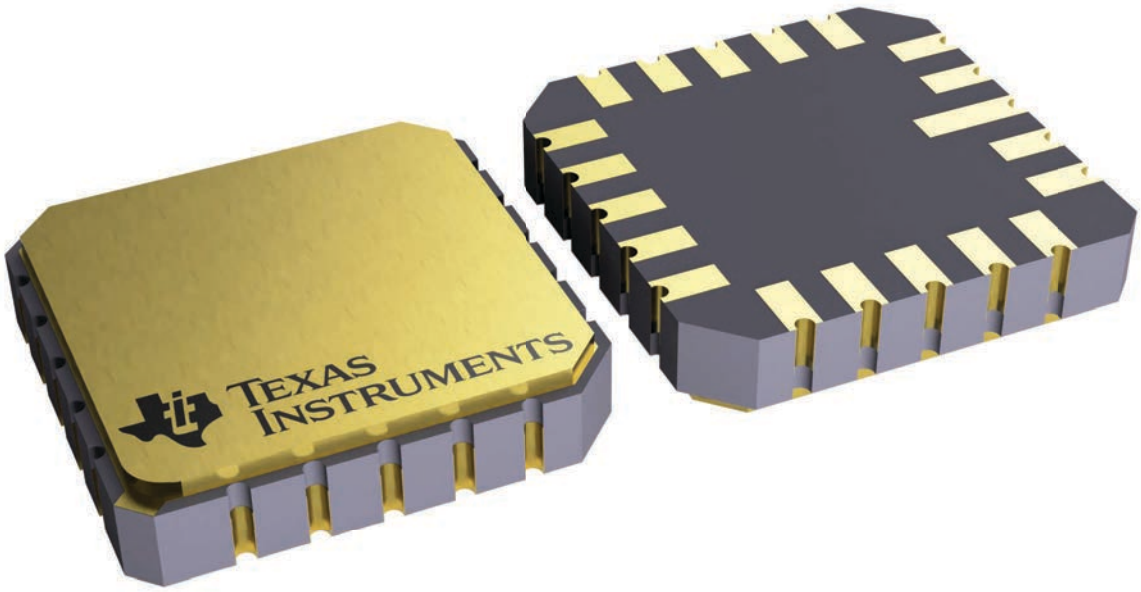
## FK 20

## LCCC - 2.03 mm max height

**8.89 x 8.89, 1.27 mm pitch**

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



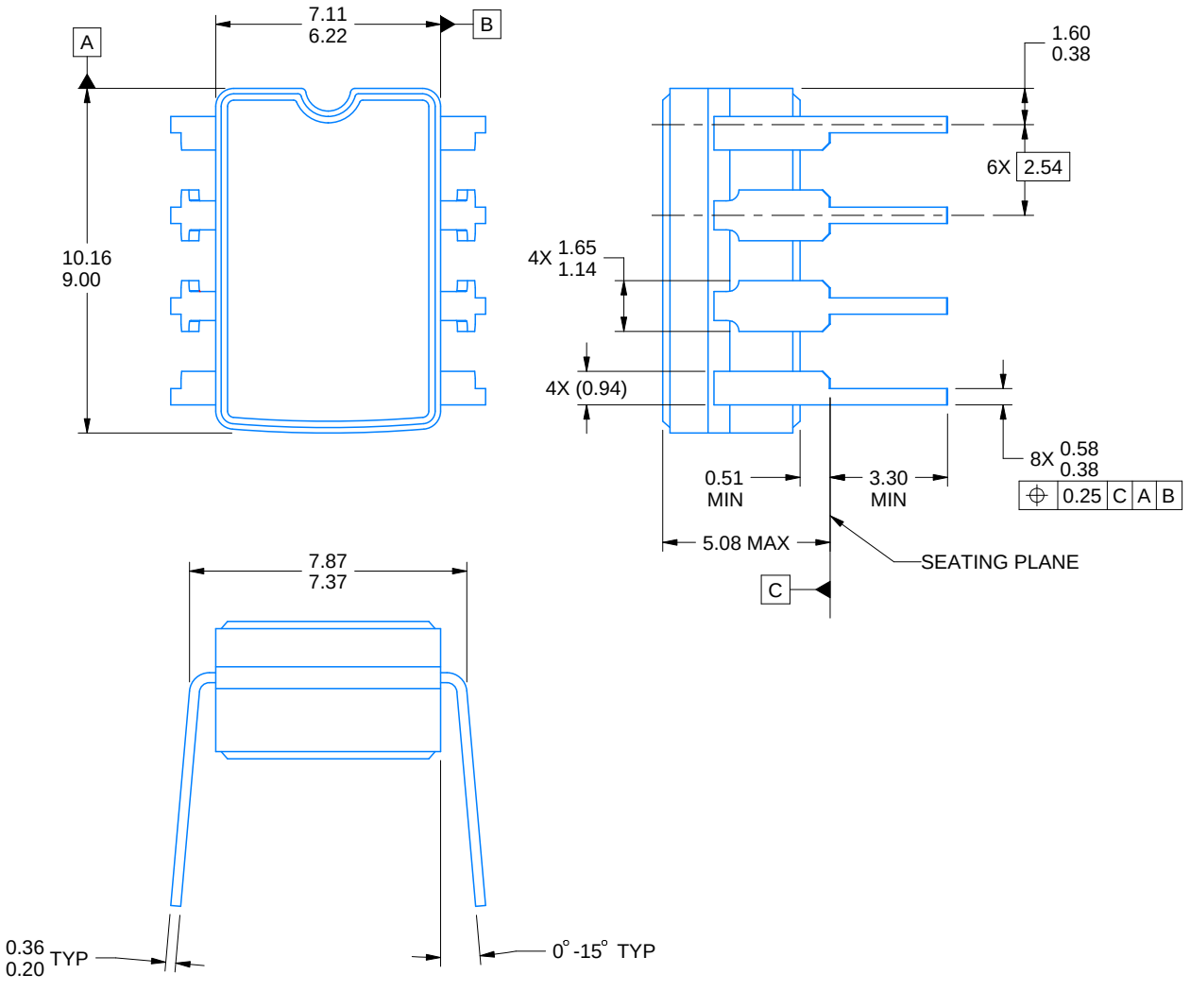

4229370VA\

# PACKAGE OUTLINE

## JG0008A

## CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE




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NOTES:

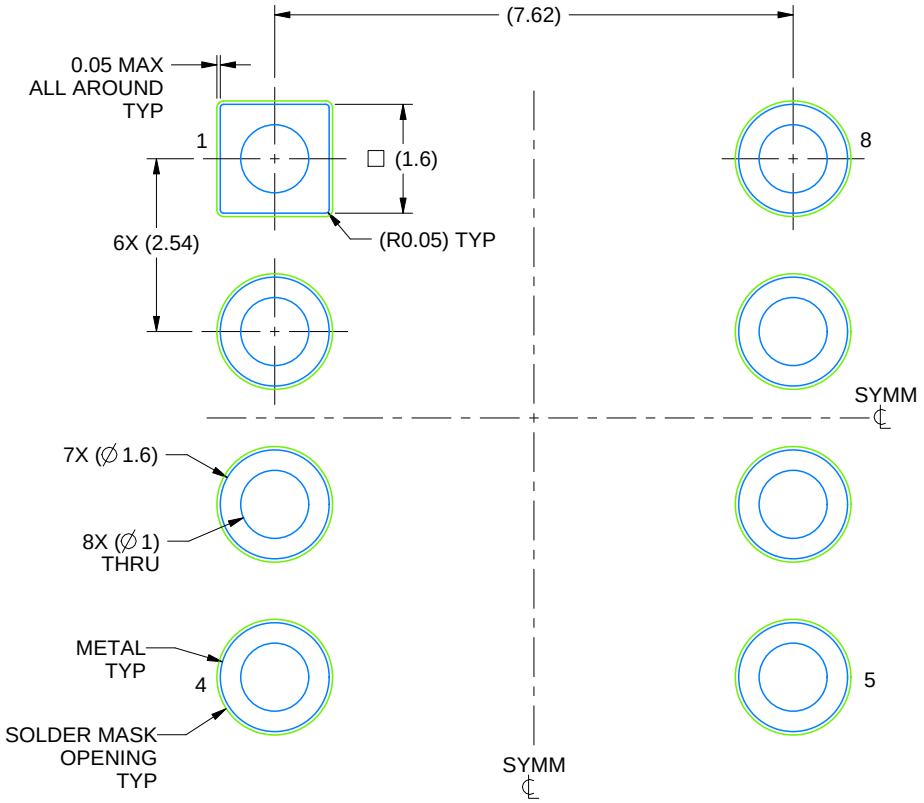
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

# EXAMPLE BOARD LAYOUT

## JG0008A

## CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE




LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

4230036/A 09/2023

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