南京扬贺扬
HeYangTek

HY SPI 1G

Serial Peripheral Interface (SPI)
NAND Flash

Parts No.	Density	Voltage	Package	MID	DID	Page Size	Pages/Block
HYF1GQ4UTACAE	1Gb/128MB	3.3V	LGA6*8	01	15	2K	64
HYF1GQ4UTDCAE	1Gb/128MB	3.3V	BGA24	01	15	2K	64
HYF1GQ4UTECAE	1Gb/128MB	3.3V	LGA5*6	01	15	2K	64

Version: 1.3.6

Features

☆ Standard Dual and Quad SPI
- Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
- Dual SPI: SCLK, CS#, SIO0, SIO1, WP#, HOLD#
- Quad SPI: SCLK, CS# ,SIO0, SIO1, SIO2, SIO3

☆ Flash Features
- Block Size : (Page size)×(64 page/block)
- Page Size : 2048 + 64 bytes
- SPI Capacity : 1Gb (1024 blocks)

☆ Performance
- Read Page Time(tR): 45 μs (Typ)
- Program time: 350 μs (Typ)
- Block Erase time: 4.0 ms (Typ)

☆ SPI power supply voltage
- Full voltage range for 3.3V：2.7 to 3.6V
- Applied Input/Output Voltage：-0.6 to 4.6V

☆ Reliability
- On-chip ECC correction Programand ECC error correction capability is Support ECC 6 bit/512B
- Operating Temperature: -40 °C to 105 °C
- Blocks 0-9 are good at the time of shipment
- 100,000 Program / Erase cycles (Typ)
- 10 Year Data Retention (Typ)

☆ Security Features
- One Time Programmable (OTP) area
- Serial number (unique ID) (Contact factory for support)
- Hardware program/erase disabled during power transition
- Volatile and Permanent Block Protection

☆ SPI Max. Clock Frequency
- 104MHz @ 3.3V

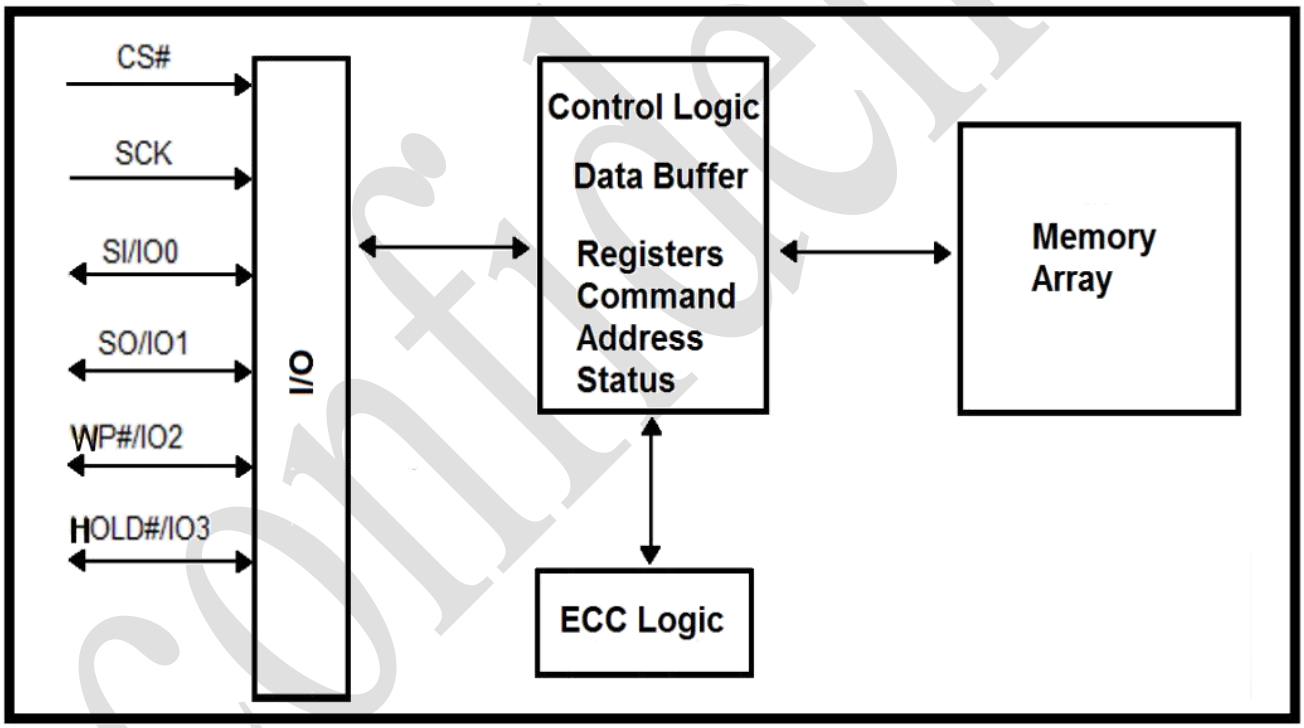
General Description

SPI (Serial Peripheral Interface) NAND Flash provides a low cost and low pin count solution to alternate SPI-NOR in high density non-volatile memory storage solution for embedded systems.

SPI NAND Flash is an SLC NAND Flash memory device based on the standard parallel NAND Flash. The serial electrical interface follows the industry-standard serial peripheral interface. The command sets is similar to the SPI-NOR command sets but with some modifications to handle NAND specific functions and new features are added to extend applications. The SPI NAND flash device has total 8 pin count, including six signal lines plus VCC and GND.

Each block of the serial NAND Flash device is subdivided into 64 programmable pages. Each page consists of a data storage region and a spare area. The data storage region is used to storage data user programmed and the spare area is typically used for memory management and error correction functions.

Functional Block Diagram



Pin Description

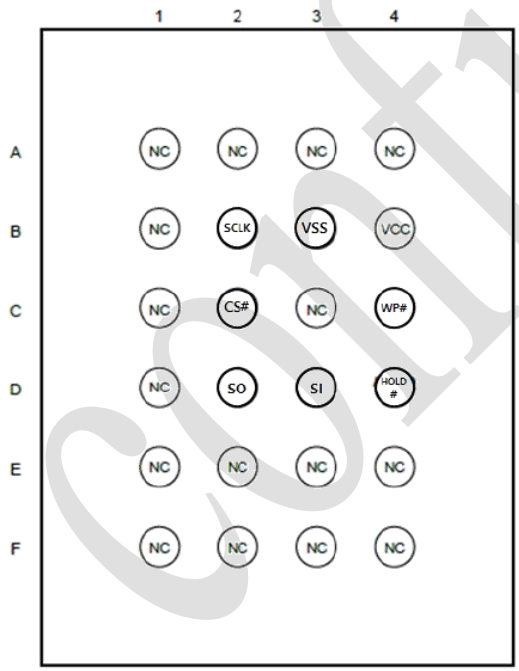
Pin Name	Type	Description
SCLK	In	Serial Clock
SI/SIO0	I/O	Serial Data Input / Serial Data I/O0
SO/SIO1	I/O	Serial Data Output / Serial Data I/O1
WP#/SIO2	I/O	Write Protect / Serial Data I/O2
Hold#/SIO3	I/O	Hold / Serial Data I/O3
CS#	In	Chip Select
VCC	Supply	Power Supply
GND	Ground	Ground

Notes:

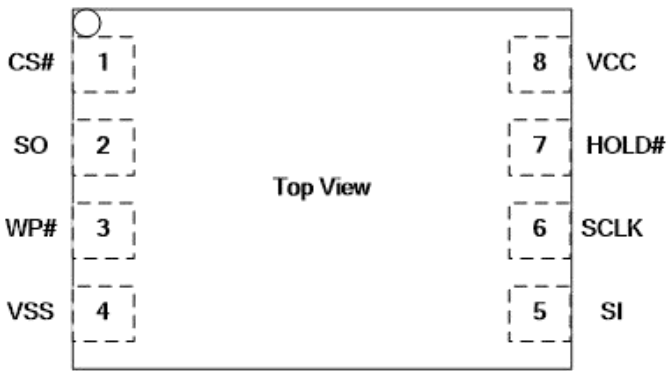
1) A 0.1 μF capacitor should be connected between the VCC Supply Voltage pin and the Vss Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

2) An internal voltage detector disables all functions whenever VCC is below 1.8V to protect the device from any involuntary program/erase during power transitions.

Connection Diagram



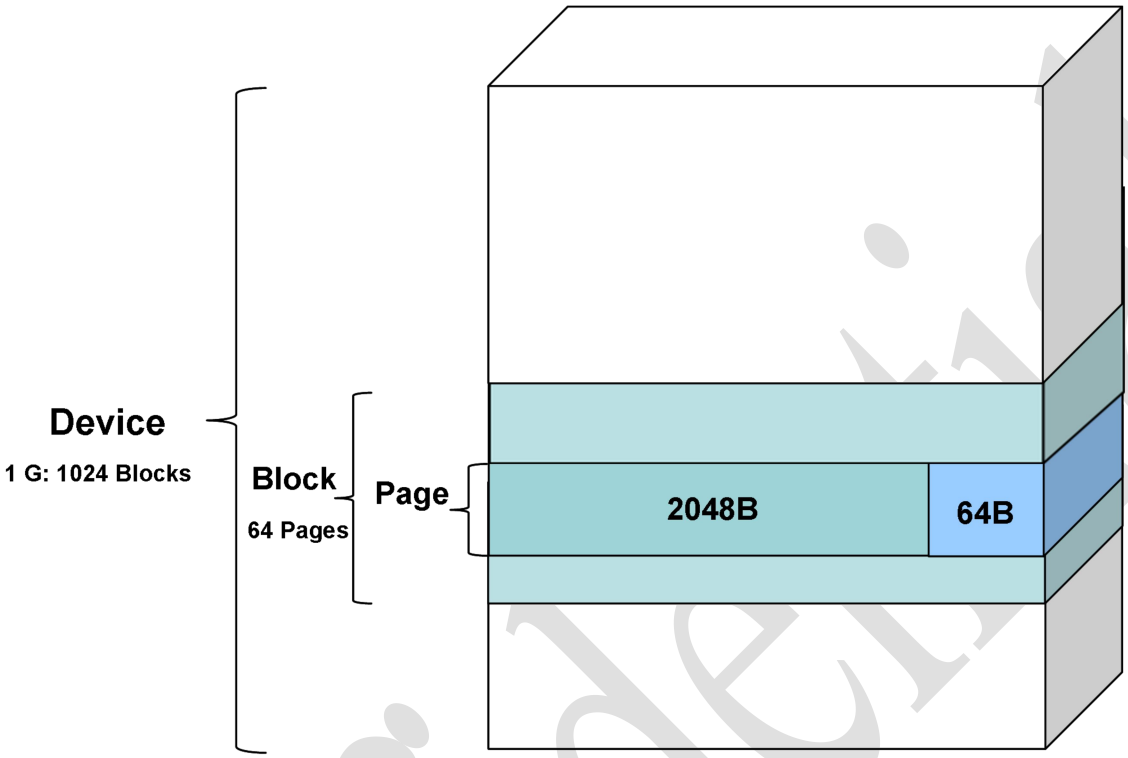
BGA24



LGA6*8 / LGA5*6

Array Organization

Device	Number of Blocks	Number of Pages	Page Size	Device Size
1G	1024	64	2K+64B	128MB+4MB

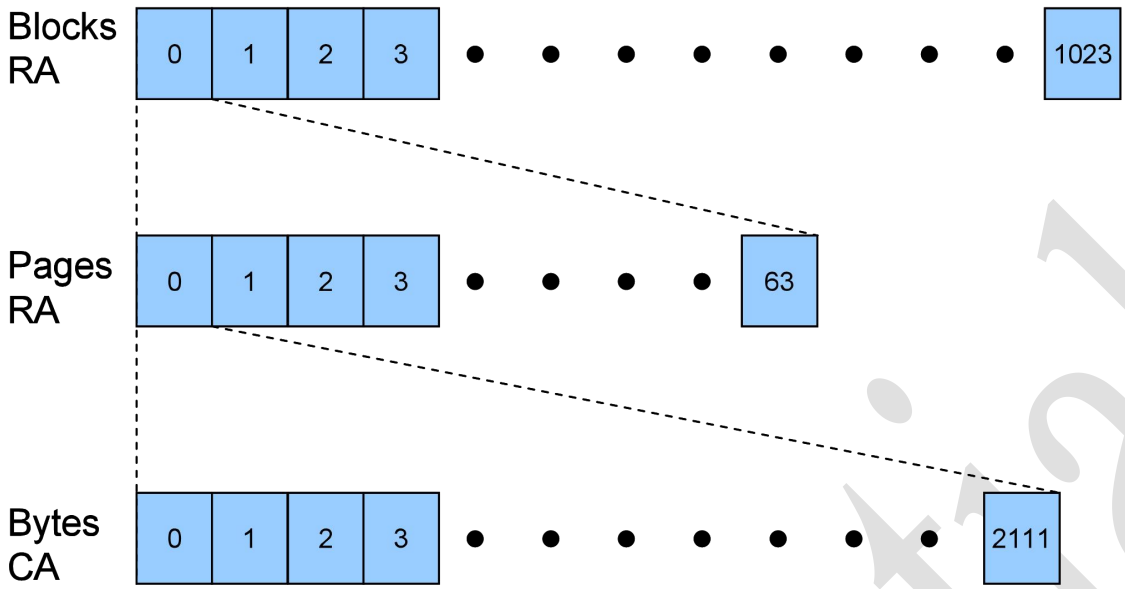


1 page (program unit) = (2K+64) bytes

1 block (Erase unit) = (2K+64)*64 pages = (128K+4K) bytes

1 G device = (128K+4K)*1024 blocks = (128MB+4MB)

Memory Mapping



Note:

1. RA: Row Address. The RA can to index and select the block.

   RA[5:0]: for Page Range 0~63.

   RA[15:6] : for 1G, have 0~1023 blocks range.

2. CA: Column Address. The CA[11:0] can only access 0~2111 bytes, include 2K(2048)bytes and 64Byte *OOB.

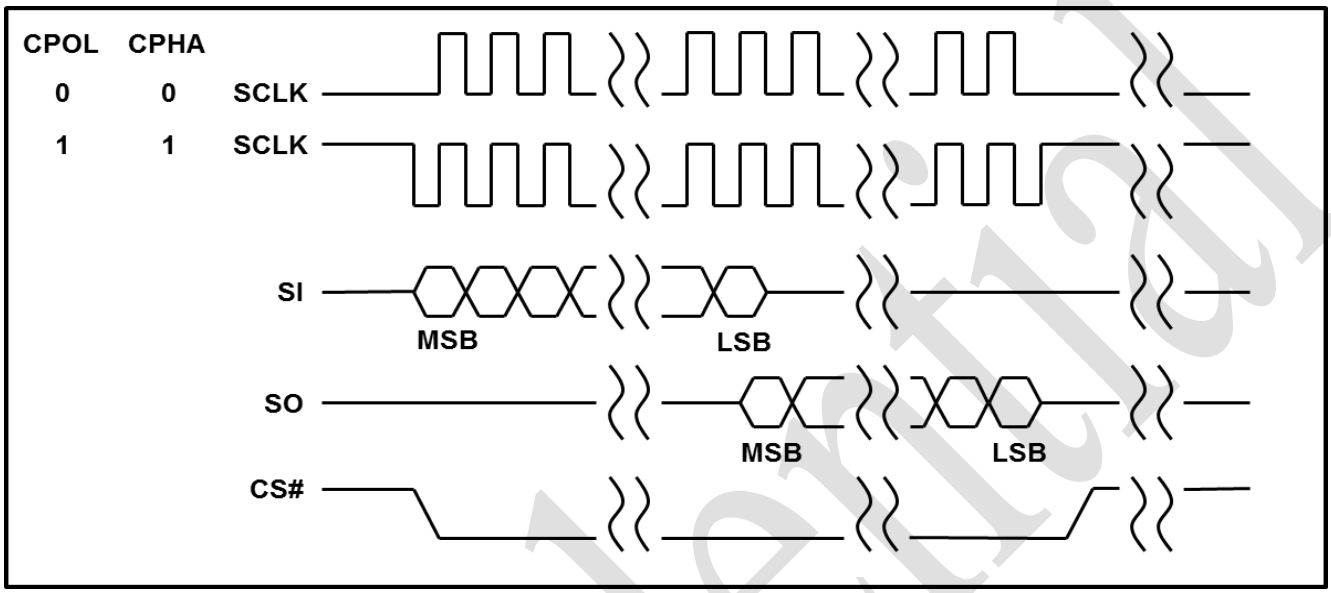
Device Operation

SPI Mode

SPI NAND supports two SPI modes:

- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched in on the rising edge of SCLK and output data is available on the falling edge of SCLK for both mode 0 and mode 3. The timing diagrams shown in this data sheet are mode 0.



SCLK	SCLK provides interface timing for SPI NAND. Address, data and commands are latched on the rising edge of SCLK. Data is placed on SO at the falling edge of SCLK.
CS#	When CS# = 0, the device is placed in active mode. When CS# = 1, the device is placed in inactive mode and SO is High-Z.

Standard SPI:

Standard serial peripheral interface on four signals bus: System Clock (SCLK), Chip Select (CS#), Serial Data In (SI) and Serial Data Out (SO).

Dual SPI:

SPI NAND supports dual SPI operation with x2 and dual IO commands. These commands allow data to be transferred to or from SPI NAND at two times of rates of Standard SPI operation. The SI and SO become bi-directional I/O pins : SIO0 and SIO1.

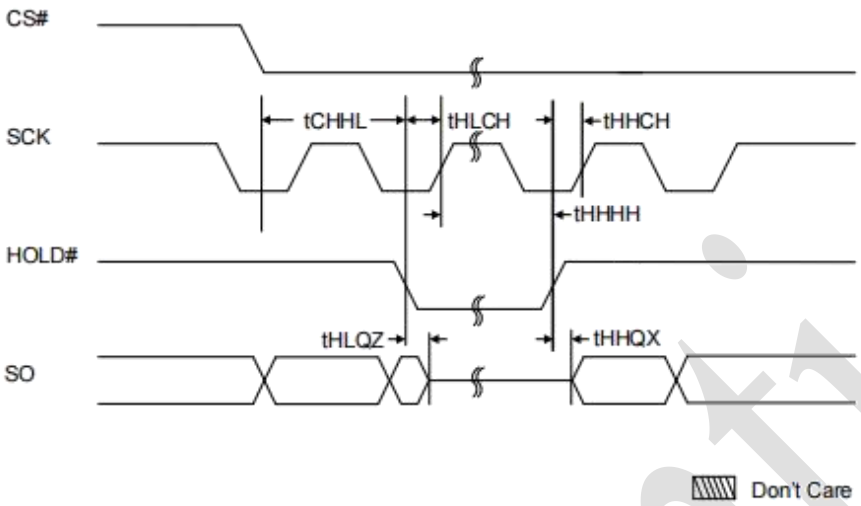
Quad SPI:

SPI NAND supports the x4 and Quad commands operation. These commands allow data to be transferred to or from SPI NAND at four times of rates of Standard SPI operation. The SI and SO become bi-directional I/O pins: SIO0 and SIO1, the WP# and HOLD# pins become SIO2 and SIO3.

Hold Mode:

The HOLD# signal goes low to stop any serial communications with the device, but doesn't stop the operation of write status register, programming or erasing in progress.

Figure 14. HOLD# Timing



HOLD	Hold mode starts at the falling edge of HOLD# provided SCLK is also LOW. If SCLK is HIGH when HOLD# goes LOW, hold mode begins after the next falling edge of SCLK.

Hardware Write Protection :

Hardware write protection prevents the block protection state from hardware modifications.

The following command sequence enables hardware write protection: The SET FEATURE command is issued on feature address A0h. Then, the Config_Protect_en bit-state is set to 0 as the default after power up.

The BRWD bit is operated in conjunction with Config_Protect_en bit. When BRWD is set to 1 and WP# is LOW, none of the other block protect register A0h bits [7:2] can be set. The block lock state cannot be changed, regardless of what is unlocked or locked. Also, when the WP#/Hold# disable bit is set to 1, the hardware protected mode is disabled. The default value of BRWD and Config_Protect_en bits = 0 after power up.

Command Set

SPI NAND Flash Command Set

Command	Op Code	2nd Byte	3rd Byte	4th Byte	5th Byte	6th Byte	Nth Byte
Write Disable	04H	-	-	-	-	-	-
Write Enable	06H	-	-	-	-	-	-
Block Erase (Block size)	D8H	A23-A16	A15-A8	A7-A0	-	-	-
Program Load	02H	A15-A8	A7-A0	D7-D0	Next data	Next data	-
Program Load x4 IO	32H	A15-A8	A7-A0	(D7-D0)x4	Next data	Next data	-
Program Execute	10H	A23-A16	A15-A8	A7-A0	-	-	-
Page Read (to Cache)	13H	A23-A16	A15-A8	A7-A0	-	-	-
Read from Cache x1 IO	03H/0BH	A15-A8	A7-A0	Dummy	D7-D0	Next data	Wrap
Read from Cache x2 IO	3BH	A15-A8	A7-A0	Dummy	(D7-D0)x2	Next data	Wrap
Read from Cache x4 IO	6BH	A15-A8	A7-A0	Dummy	(D7-D0)x4	Next data	Wrap
Read from Cache Dual IO	BBH	A15-A0	Dummy(1)	(D7-D0)x2	Next data	Next data	Wrap
Read from Cache Quad IO	EBH	A15-A0	Dummy(1)	(D7-D0)x4	Next data	Next data	Wrap
Read ID	9FH	Dummy	MID	DID	Wrap	Wrap	Wrap
Reset	FFH	-	-	-	-	-	-
Get Feature	0FH	A7-A0	D7-D0	-	-	-	-
Set Feature	1FH	A7-A0	D7-D0	-	-	-	-

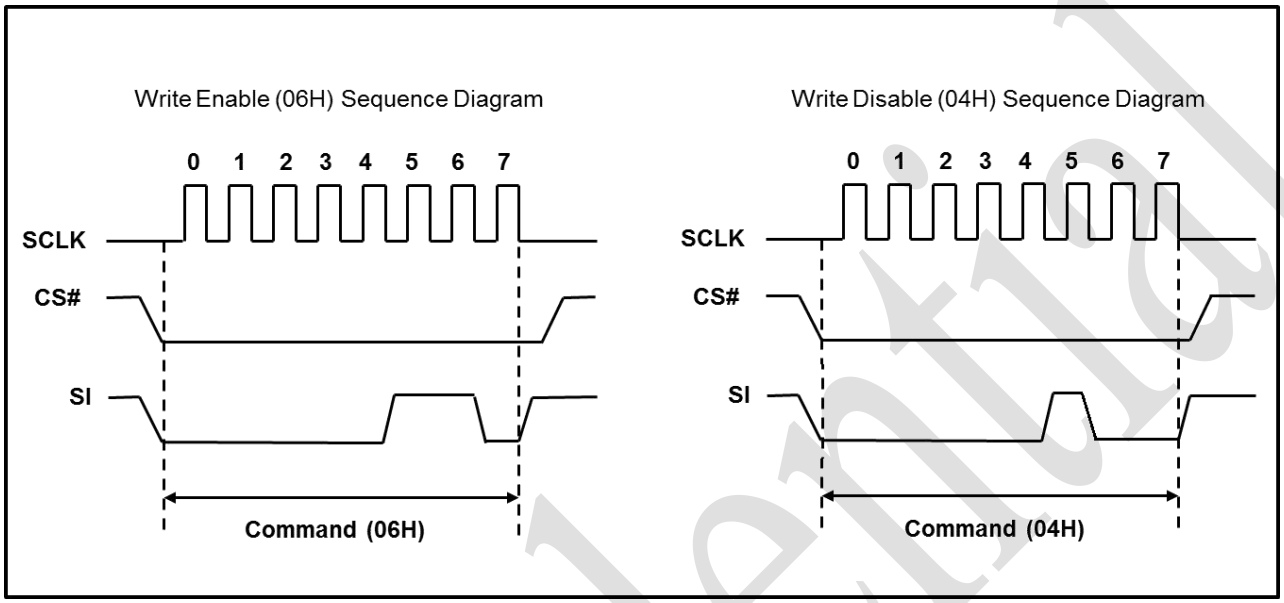
Notes:

1. The number of dummy cycles is 8 cycles

Write Enable Operations

The WRITE ENABLE (WREN, 06H) command is for setting the Write Enable Latch (WEL) bit. The WRITE DISABLE (WRDI, 04H) command is for clearing the WEL bit.

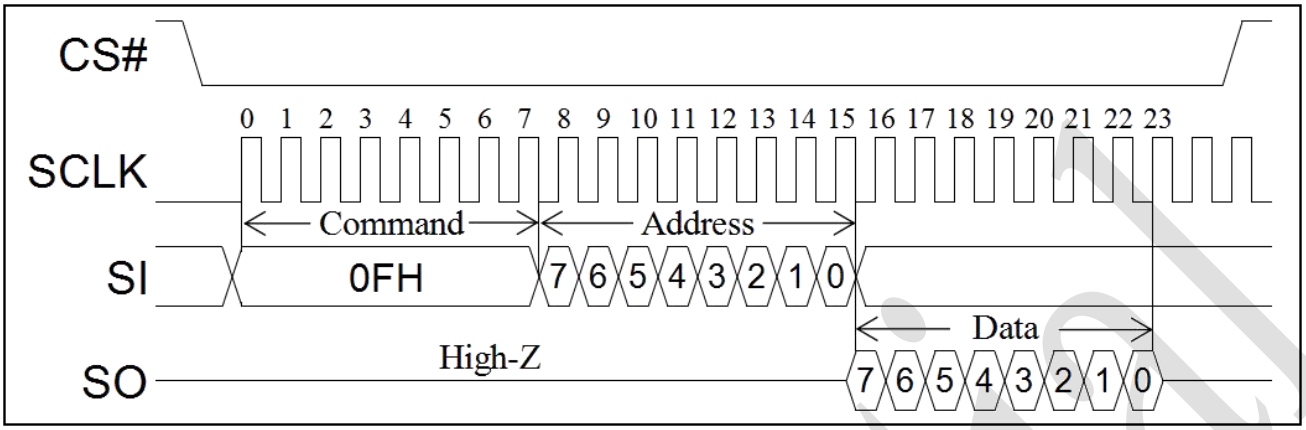
As with any command that changes the memory contents, the WRITE ENABLE command must be executed at first in order to set the WEL bit to 1. Refer to the PAGE READ operation sequence, PAGE PROGRAM operation sequence, Internal Data Move operation sequence, BLOCK ERASE operation sequence and OTP operation sequence.



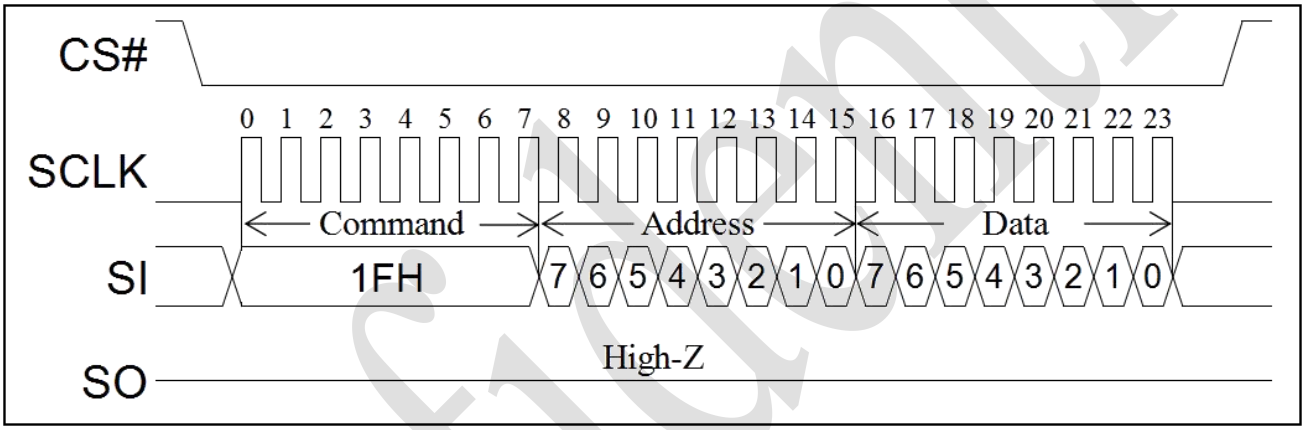
Feature Operation

The GET FEATURE (0FH) and SET FEATURE (1FH) commands are used to monitor the devices status and alter the device behavior.

Get Feature (0FH) Sequence Diagram



Set Feature (1FH) Sequence Diagram



The SET FEATURE command is valid only when WP# pin = 1.

Feature Register Table

Register	Address	Data Bits							
		7	6	5	4	3	2	1	0
Protect	A0H	BRWD1	AVBP BL[3]	AVBP BL[2]	AVBP BL[1]	AVBP BL[0]	AVBP _BL_U	Config_Protect_en(1)	Reserved
Configuration	B0H	Config[2]	Config[1]	AVBP_LD_EN(2)	ECC_Enable(3)	Reserved	Reserved	Config[0]	Reserved
Status	C0H	Reserved	Reserved	ECCS1	ECCS0	P_FAIL	E_FAIL	WEL	OIP

Notes:

1)Config_Protect_en must be enabled first before block unlock region is set

2) AVBP_LD_EN when set to 1, this bit along with the register A0H [6:0] can only be cleared during POR

3) ECC_Enable must be always set to 1

Table of Feature Address A0h (Block Protect Register R/W, protected when WP# pin = 0)

Bit	Symbol	Parameter	Default	Description
7	BRWD1	Block Register Write Disable	0	1b: Disable update of the A0[7:0]when WP# Low Ob: Enable update of the A0[7:0](Default)
6	AVBP BL[3][1]	AVBP Lock 3	1	Volatile Block protection based on addressable blocks in the device 0000b: All Blocks Unlocked 0001b:1/1024 Blocks Locked 0010b:1/512 Blocks Locked 0011b:1/256 Blocks Locked 0100b:1/128 Blocks Locked 0101b:1/64 Blocks Locked 0110b:1/32 Blocks Locked 0111b:1/16 Blocks Locked 1000b:1/8 Blocks Locked 1001b:1/4 Blocks Locked 1010b:1/2 Blocks Locked 1011b; All Blocks locked 11xx:All Blocks Locked 1111b:All Blocks Locked (default)
5	AVBP BL[2][1]	AVBP Lock 2	1	
4	AVBP BL[1][1]	AVBP Lock 1	1	
3	AVBP BL[0][1]	AVBP Lock 0	1	
2	AVBP _BL_ U[1]	AVBP LockUpper/Lower range	1	1: Protect Upper blocks 0: Protect Lower blocks
1	Config_Protect_en[1]	WP#/Config Protect enable	0	
	Reserved	Reserved	0	

State	WP#pin	0	1	1	1	1
	A0h[7]=BRWD	x	0	0	1	1
	A0h[1]	x	0	1	1	0
Effect	A0h[1]	R	W/R	W/R	W/R	W/R
	A0h[7:2]	R	A0h[7:2]=R Protected By A0h[1]	A0h[7:2]=W/R	A0h[7:2]=R Protected By A0h[7]=1	A0h[7:2]=R Protected By A0h[1]=0

Note：

1)Before setting “1F A0 00”, you need to add the “1F A0 02” command, When setting the value of A0H, keep WP# always at 1.

2) A0h[1]= 0 ; A0h[7:2] R/W :Write operation depends on WP#, A0h[1], and A0h[7] values

3) Feature address A0h command is allowed to be issued in OIP Ready status

Table of Feature Address B0h (Configuration Register R/W, protected when WP# pin = 0)

Bit	Symbo	Parameter	Default	Description
7	Config[2]	Configuration bit 2	0	Config[2:0] 000:(default) Normal Operation 010: Access OTP Area/parameter page / Unique ID (Note 1) 110: **Access to OTP data protection bit to lock OTP area**
6	Config[1]	Configuration bit 1	0	
5	AVBP_LD_EN	Advance Lock down enable	0	1:AVBP Lock down is enabled A0[7:0] and B0[5] are locked until power down. O:AVB Lock down is disabled
4	ECC_Enable	ECC_Enable	1	Must be always set to 1
3	Reserved	Reserved	0	
2	Reserved	Reserved	0	
1	Config[0]	Configuration bit 0	0	See Config[2:1] description
0	Reserved	Reserved	0	

1) AVBP_LD_EN when set to 1, this bit along with the Block Protection register [6:0] can only be cleared during POR

2) Feature address B0h command is allowed to be issued in OIP Ready status

Table of Feature Address C0h (Status Register R Only)

The content of status register can be read by issuing the GET FEATURE (0FH) command, followed by the status register address C0H.

The meaning of each Bit in status register is as the table below

Bit	Symbol	Parameter	Default	Description
7	Reserved	Reserved	0	
6	Reserved	Reserved	0	
5	ECCS1	ECC status register[1:0][1,2]	0	11=uncorrectable 10=3-6 errors corrected 01=1-2 errors corrected 00=Normal
4	ECCSO		0	
3	P_Fail	Program fail	0	1:Program failure occurred 0: Operation passed
2	E_Fail	Erase fail	0	1: Erase Failure occurred 0: Operation passed
1	WEL[3]	Write enable latch	0	1:Write Enabled 0:Write Disabled
0	OIP	Operation in progress	0	1:Device is busy with executing commands: Reset, Program Execute, Page Read, Block Erase 0: Device is ready

1: SR [5:4] defines the number of corrections.

2: A Program and Erase fails include a block being protected (Array blocks + OTP)

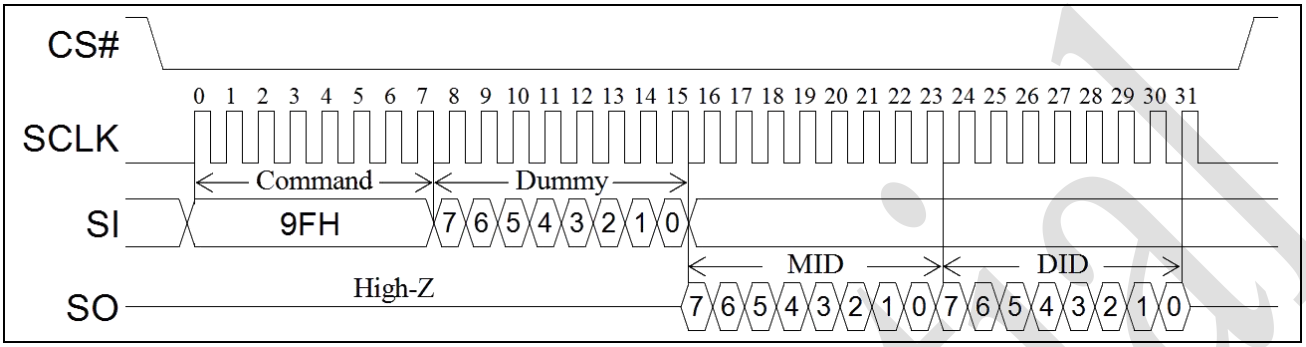
3.The WEL signal will be ignored due to the low WP state during erase/program command writing

Read ID Operations

Read ID (9FH)

The READ ID command is used to identify the SPI NAND Flash memory device. The Read ID command outputs the manufacture ID with address byte 00H and outputs the device ID when address byte is 01H.

Read ID (9FH) Sequence Diagram



ID Definition Table

Address	Value	R/W	Description
00H	01h	R	Manufacture ID
01H	15h	R	Device ID

Read Unique ID

Read Unique ID located in OTP page 0

1, Use SET FEATURES command (1Fh) with feature address B0h and data value of 0x50 for ECC enabled

2, Page Read command (13h) with Block/Pageaddress:

- 0x180 for unique ID (OTP page 0)

-GET FEATURE command (0Fh) with feature address C0h to check OIP bit ready

3, Read Buffer (03h) command to read the data out

4, Use SET FEATURES command (1Fh) with feature address B0h and data value with Config[2:0] = 000b to exit.

5, Or use RESET (FFh) command to clear the configuration bits and return to normal mode.

One-Time Programmable (OTP) function

OTP States

CFG2	CFG1	CFG0	Description
0	0	0	Normal Operation (default)
0	1	0	Access OTP Area / Unique ID
1	1	0	Access to OTP data protection bit to lock OTP area

The device contains a one-time programmable (OTP) area, that consists of (62 pages), accessed by SET/GET FEATURES commands.

OTP Read

OTP Read: 62 pages accessible for user data located in Block #6 from page 2 to page 63

1, Use SET FEATURES command (1Fh) with feature address B0h and data value of 0x50.

2, Page Read command (13h) with Block/Page address (0x0182-0x01BF)

GET FEATURE command (0Fh) with feature address C0h to check OIP bit ready

3, Read Buffer (03h) command to read the dataout

4, Use SET FEATURES command (1Fh) with feature address B0h and data value of 0x10 to exit

5, Or use RESET (FFh) command to clear the configuration bits and return to normal mode.

OTP Program

OTP Program: 62 pages accessible for user data located in Block 6 from page 2 to page 63

1, Use SET FEATURES command (1Fh) with feature address B0h and data value of 0x50 for ECC enabled

2, Use Write Enable command 06h

3, Program using Load command x1 (02h), Quad Program Data Load (32h) with data

4, Program Execute command x1 (10h) with Block/Page address(0x0182-0x01BF)

5, Use GET FEATURE command (0Fh) with feature address C0h to check OIP bitready

6, Use SET FEATURES command (1Fh) with feature address B0h and value of 0x10 to exit

7, After tPROG time, use GET FEATURE command (0Fh) with feature address C0h to verifyP_Fail bit is not set.

OTP Data Protection and Program Prevention

This mode is used to prevent further programming of the pages in the OTP area. The following sequence is used to protect and prevent further programming of the OTP area:

1, Use SET FEATURES command (1Fh) with feature address B0h and data value of 0xD0

2, Use Write Enable command 06h

3, Program execute command (10h) with row address 00h

4, Verify until OIP bit not busy and P_FAIL bit 0 using GET FEATURE command (0Fh) with status register address (C0h)

Volatile Block Protection (VBP) Overview

The AVBP feature can protect all blocks, or one selected range of contiguous blocks, from erase and program operations. After a power-cycle, all blocks are protected as the AVBP_BL[3:0] bits are high (see Block protection feature register(A0h).)The SET FEATURE command must be issued to alter the state of block protection. A Reset command will not reset the A0h register and therefore will not modify the block protection state. When a PROGRAM/ERASE command is issued to a locked block, a status register P_Fail bit or E_Fail bit will beset to indicate the operation failure.

Block Protect Bits Table (A0H [6:2])

1Gb,2KB page devices

AVB Block Selection	Description	01Gb_2KB	
AVBP_BL_U,AVBP_BL[3:0]		MIN	MAX
10000	All Blocks unlocked	-	-
10001	Upper 1/1024 Blocks locked	1023	1023
10010	Upper 1/512 Blocks locked	1022	1023
10011	Upper 1/256 Blocks locked	1020	1023
10100	Upper 1/128 Blocks locked	1016	1023
10101	Upper 1/64 Blocks locked	1008	1023
10110	Upper 1/32 Blocks locked	992	1023
10111	Upper 1/16 Blocks locked	960	1023
11000	Upper 1/8 Blocks locked	896	1023
11001	Upper 1/4 Blocks locked	768	1023
11010	Upper 1/2 Blocks locked	512	1023
All others	All Blocks locked	0	1023
00000	All Blocks unlocked	-	-
00001	Lower 1/1024 Blocks locked	0	0
00010	Lower 1/512 Blocks locked	0	1
00011	Lower 1/256 Blocks locked	0	3

00100	Lower 1/128 Blocks locked	0	7
00101	Lower 1/64 Blocks locked	0	15
00110	Lower 1/32 Blocks locked	0	31
00111	Lower 1/16 Blocks locked	0	63
01000	Lower 1/8 Blocks locked	0	127
01001	Lower 1/4 Blocks locked	0	255
01010	Lower 1/2 Blocks locked	0	511
all others	All Blocks locked	0	1023
11111(default)		0	1023

Block Lock Status Register

The Block Lock Status (BLS) register indicates whether a block is locked-down, locked or unlocked using the VBP protection methods.

The following table provides the BLS register definition:

Bits	Field Name	Function	Default	Description
7	RSVD	Reserved	0	
6	RSVD	Reserved	0	
5	RSVD	Reserved	0	
4	RSVD	Reserved	0	
3	RSVD	Reserved	1	
2	VBP Lock/Unlock Status	Volatile Block Protection Status	0	001: Block is locked down by AVBP 010: Block is locked by AVBP (**Default**) 101: Block is unlocked, Device is locked-down by AVBP 110: Block is unlocked, Device is not locked-down by AVBP (Register B0h BIT[5])
1			1	
0			0	

Read Operations

The PAGE READ (13H) command transfers the data from the NAND Flash array to the cache memory. The command sequence is follows:

I. 13H (PAGE READ to Cache)

II. 0FH (GET FEATURE command to read the status)

III. Read from Cache memory

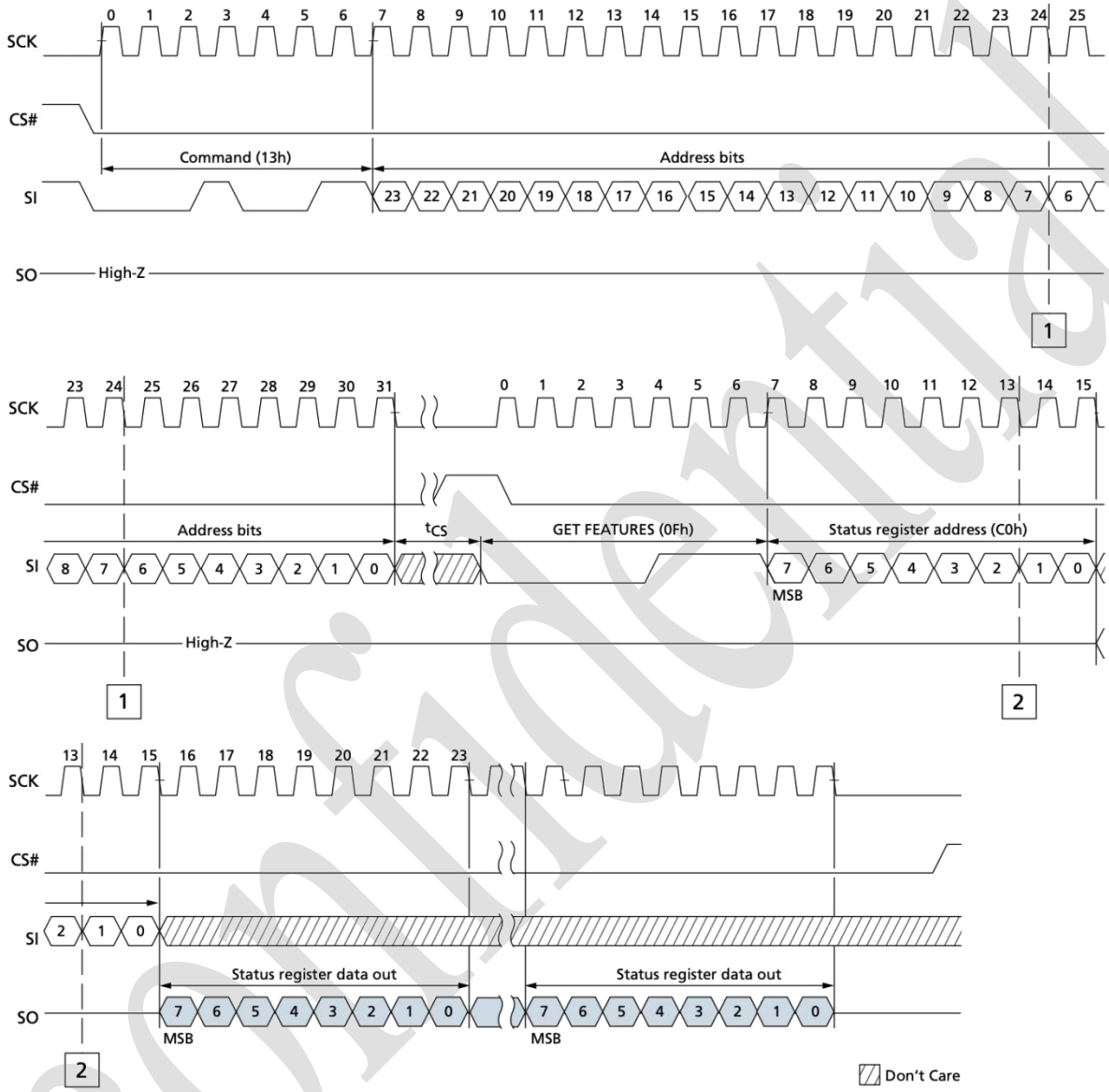
- 03H or 0BH (Read from Cache x1 IO)/3BH (Read from Cache x2 IO)/6BH (Read from Cache x4 IO)
- BBH (Read from Cache Dual IO)/EBH (Read from Cache Quad IO)

The PAGE READ command requires a 24-bit address consisting of dummy bits and block/page address bits. After the block/page addresses are registered, the device starts the transfer from the main array to the cache register, and is busy for tRD time. During the busy time, the GET FEATURE command needs to be issued to monitor the status of PAGE READ. After finishing the PAGE READ successfully, the Read from Cache command can be issued in order to read the data out of the cache. The Read from Cache command requires 16 bits of column address which is consisting of wrap bits and column address bits. The number of bits of column address is depends on the page size in different flash. Refer to figures below to view the entire READ operation.

PAGE READ to Cache (13H)

The waveform of PAGE READ to Cache (13H) is as follows,Do not toggle the CS# until the "Status Register" check is completed.

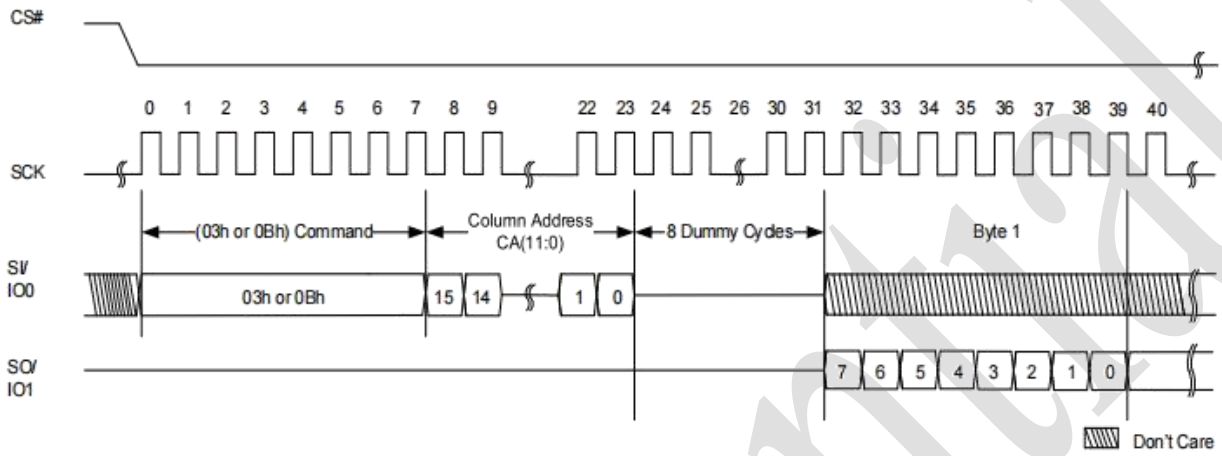
PAGE READ to Cache (13H) Sequence Diagram



Read from Cache x1 IO (03H/0BH)

The Read from Cache x1 IO (03H/0BH) consists of an OP code followed by 16-bit column address. The column address is composed of wrap bits and column address bits. Refer the Read from Cache x1 IO sequence diagram as follows,

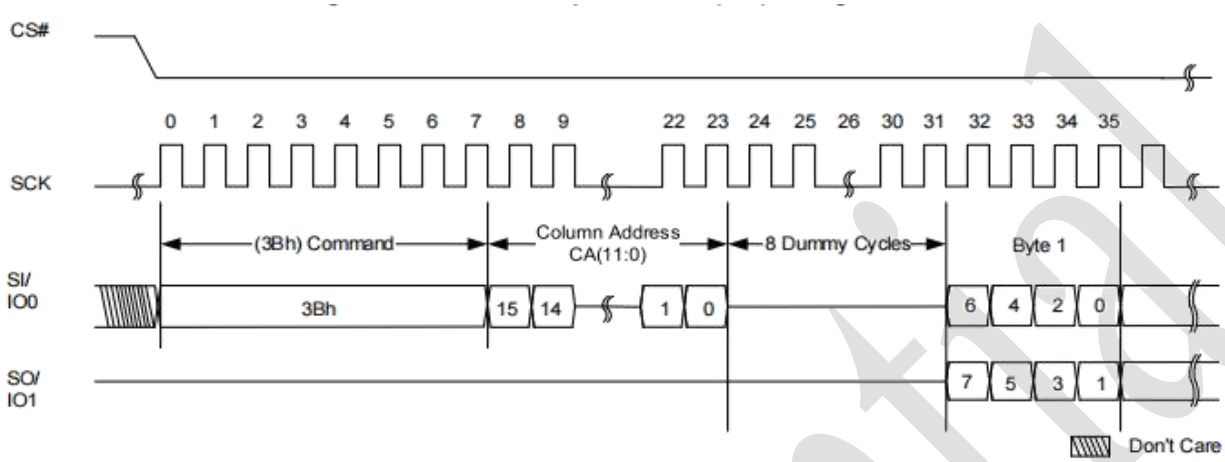
Read from Cache x1 IO (03H/0BH) Sequence Diagram



Read from Cache x2 IO (3BH)

The Read from Cache x2 IO (3BH) command is similar to the Read from Cache x1 IO (03H/0BH) but the command uses two pins to output data. The data output pins include the SI (SIO0) and SO (SIO1). Refer the Read from Cache x2 IO (3BH) sequence diagram bellowed.

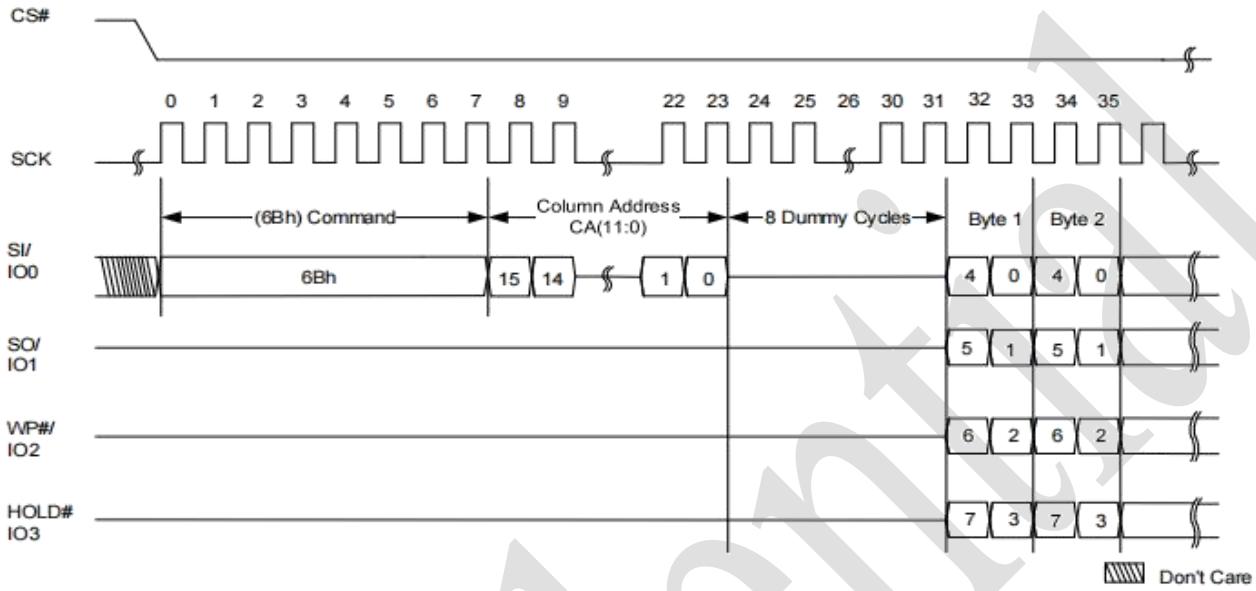
Read from Cache x2 IO (3BH) Sequence Diagram



Read from Cache x4 IO (6BH)

The Read from Cache x4 IO (6BH) command is similar to the Read from Cache x1 IO (03H/0BH) and the Read from Cache x2 IO (3BH) but the command uses four pins to output data. The four pins include the SI (SIO0), SO (SIO1), WP# (SIO2) and HOLD# (SIO3).

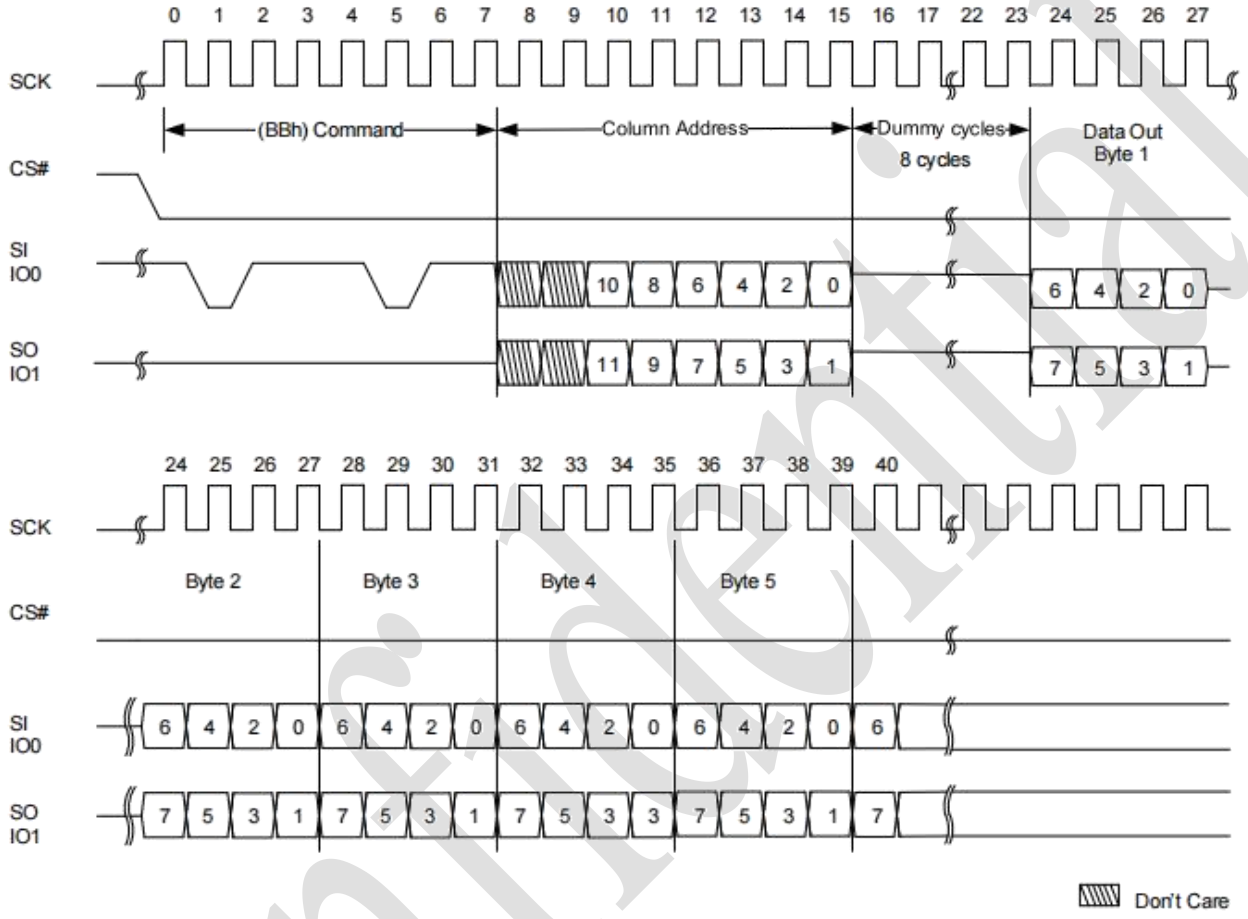
Read from Cache x4 IO (6BH) Sequence Diagram



Read from Cache Dual IO (BBH)

The Read from Cache Dual IO command (BBH) is similar to the Read from Cache x2 IO command (3BH) but using both of SI (SIO0) and SO (SIO1) as input bin. Each bit in 16-bit column address and the followed dummy byte will be latched in during the falling edge of SCLK, then the cache contents will be shifted out 8-bit in a clock cycle through the SI (SIO0) and SO (SIO1).

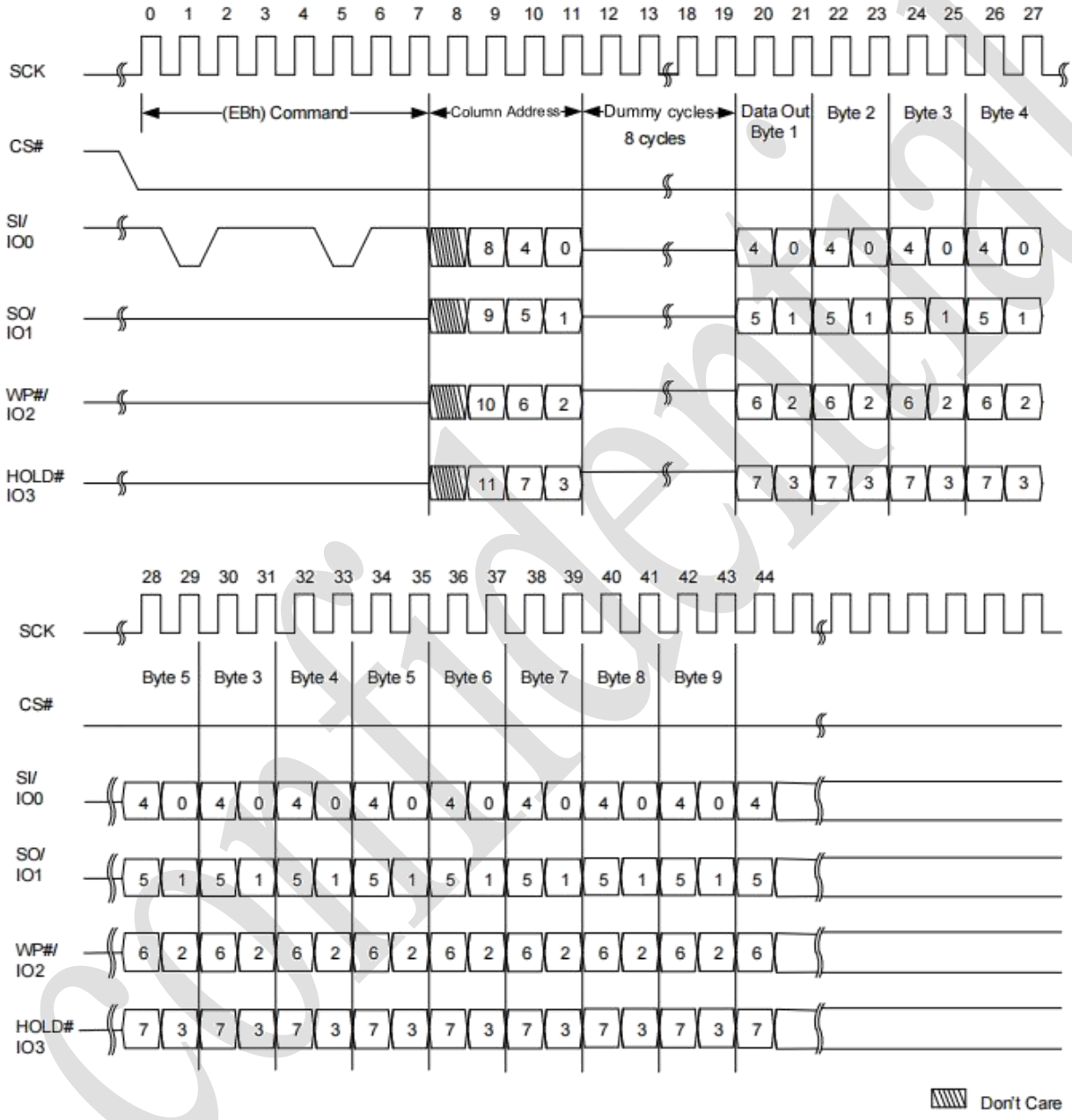
Read from Cache Dual IO (BBH) Sequence Diagram



Read from Cache Quad IO (EBH)

The Read from Cache Quad IO (EBH) command is similar to the Read from Cache x4 IO (6BH) command but with 4 input pins which include SI (SIO0), SO (SIO1), WP# (SIO2) and HOLD# (SIO3). Each bit in 16-bit column address and the followed dummy byte will be latched in during the raising edge of SCLK through these four input pins, and then the cache contents will be shifted out 8-bit in a clock cycle through the SI (SIO0), SO (SIO1), WP# (SIO2) and HOLD# (SIO3).

Read from Cache Quad (EBH) Sequence Diagram



Program Operations

The PAGE PROGRAM sequence is transfer the data from the host to NAND Flash array through cache memory. The operation sequence programs the first byte to last byte of data within a page. If more than page size, then those additional bytes are ignored by the cache memory. The PAGE PROGRAM sequence is as follows:

I. 06H (WRITE ENABLE when WEL bit is 0)

II. PROGRAM LOAD

- 02H(PROGRAM LOAD) / 32H(PROGRAM LOAD x4)

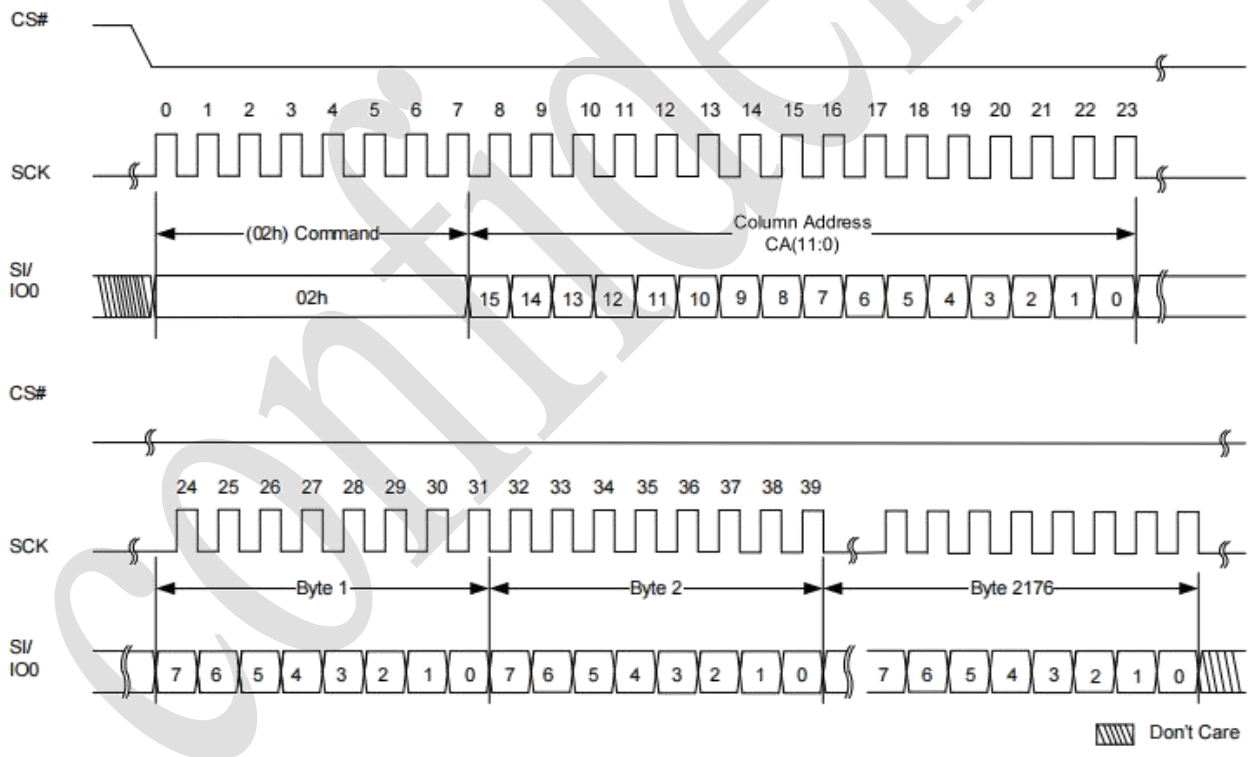
III. 10H (PROGRAM EXECUTE)

IV. 0FH (GET FEATURE command to read the status)

At first, the WRITE ENABLE (06H) command is used to set the Write Enable Latch (WEL) bit The Write Enable Latch (WEL) bit must be set prior to program execute (10h). The PROGRAM LOAD (02H/32H) command is issued then and the PROGRAM LOAD command can only be issued one time in a PAGE PROGRAM sequence. Secondly, the PROGRAM EXECUTE (10H) command is issued to program the data into the page. During the busy time, the GET FEATURE command needs to be issued to monitor the status of PAGE PROGRAM. After finishing the PAGE PROGRAM successfully, the OIP and WEL bit in status register (C0H) will be set to 0.

Program Load (02H)

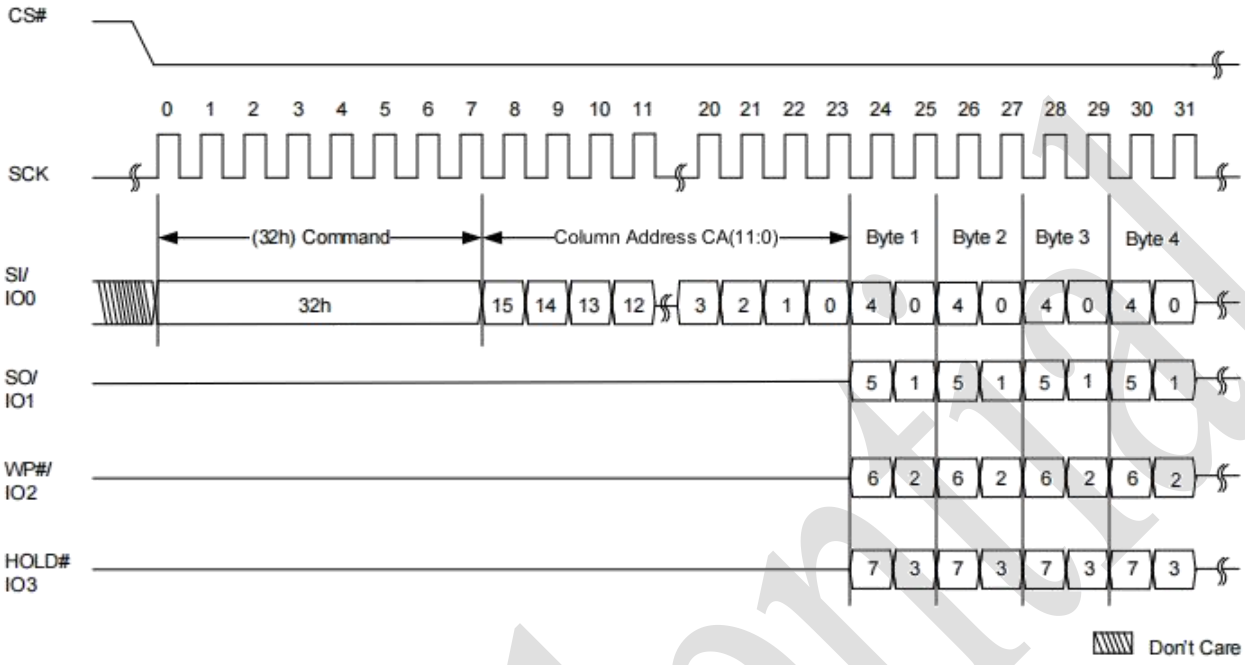
Program Load (02H) Sequence Diagram



Program Load x4 IO (PL x4) (32H)

The PROGRAM LOAD x4 IO (32H) command is similar to the PROGRAM LOAD (02H) command but with four input pins to transfer data in. The four input pins are SI (SIO0), SO (SIO1), WP# (SIO2) and HOLD# (SIO3).

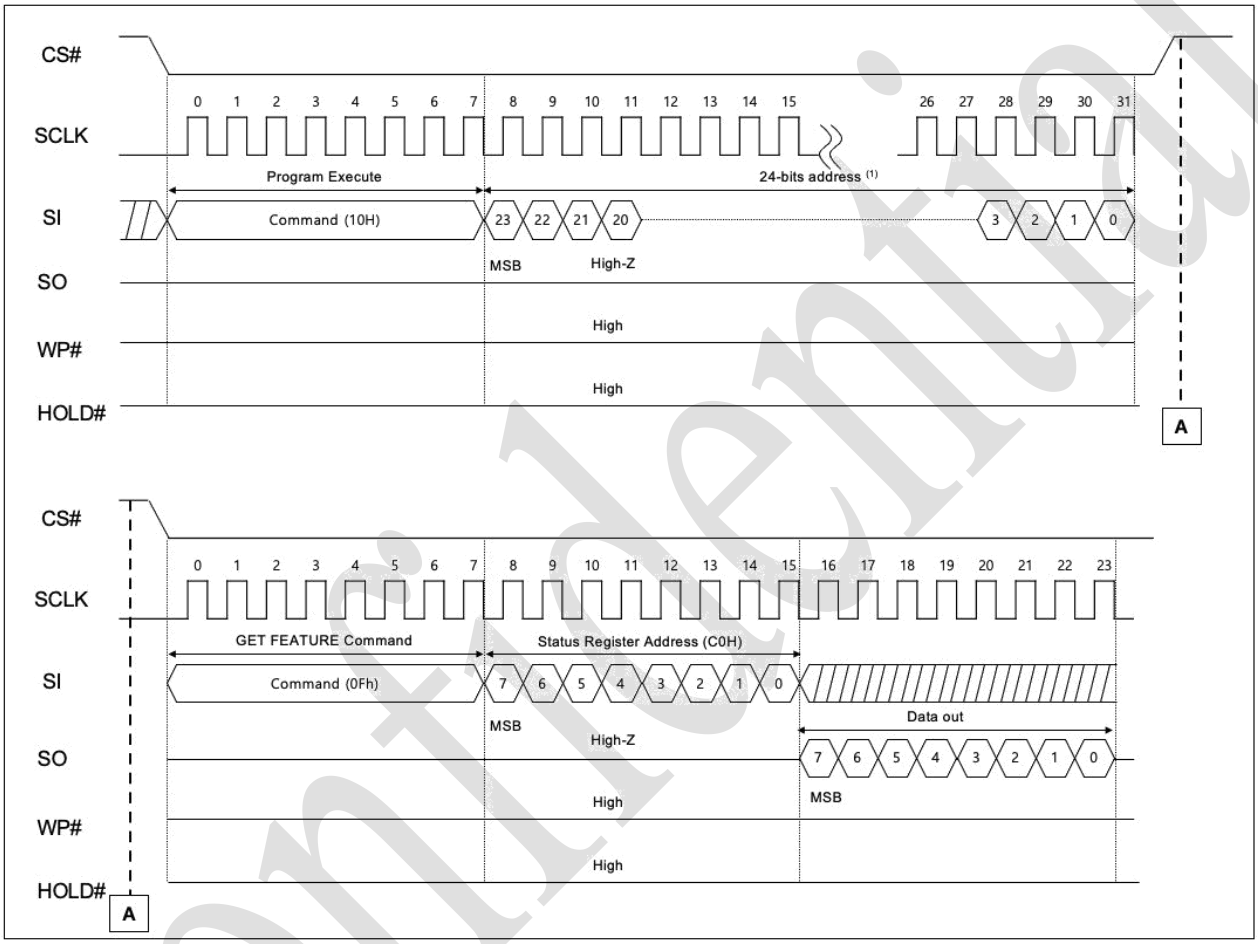
Program Load x4 IO (32H) Sequence Diagram



Program Execute (10H)

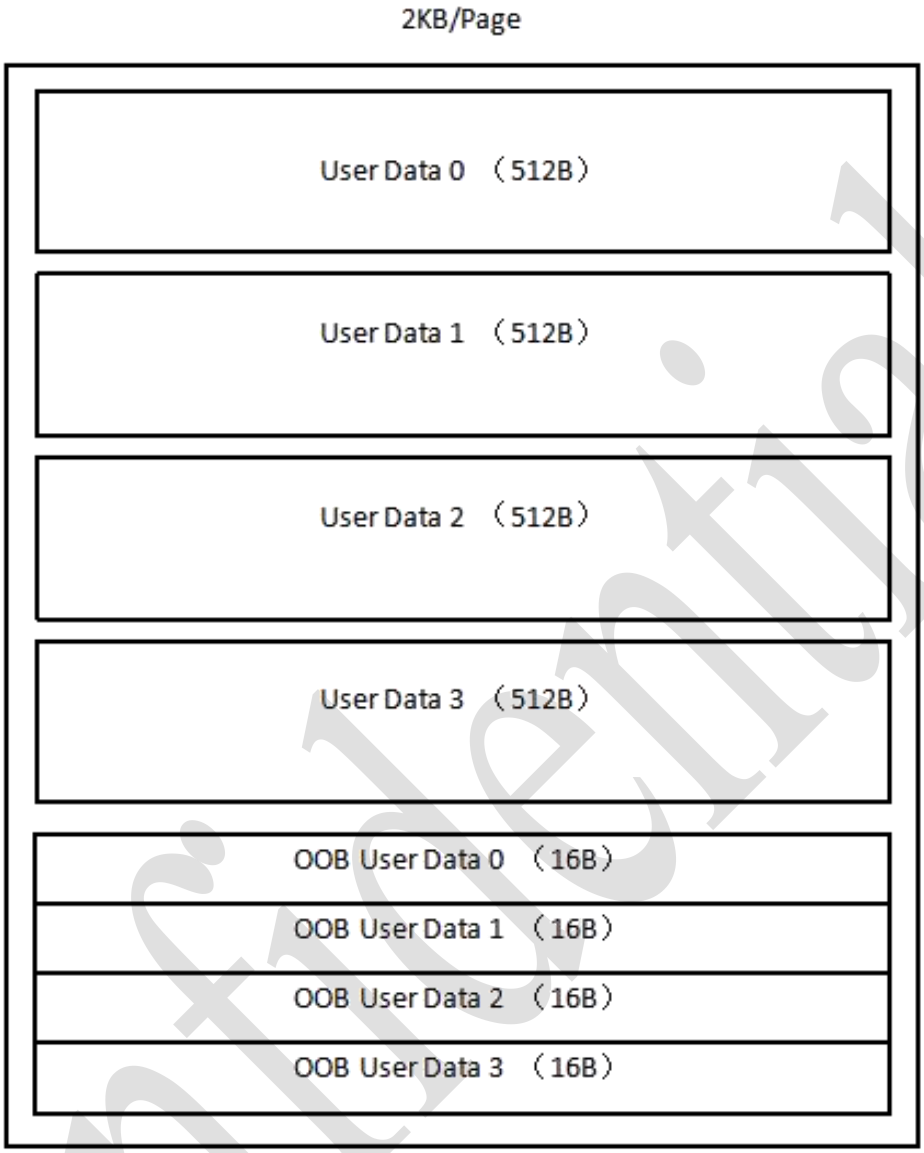
PROGRAM EXECUTE (10H) command must be issued after the data is loaded and the WEL bit be set to HIGH. The PROGRAM EXECUTE (10H) command will transfer data from the cache to the main array. The PROGRAM EXECUTE (10H) consists of an 8-bit Op code, followed by a 24-bit address which including dummy bits and page/block address. This operation needs to wait the busy time. The OIP bit in status register (C0H) will be HIGH until controller finishes the program. The P_FAIL bit in status register (C0H) will be set HIGH if program fail.

Program Execute (10H) Sequence Diagram



Description of OOB area

This Flash's OOB area is fully open for customers to use



Erase Operation

Block Erase (D8H)

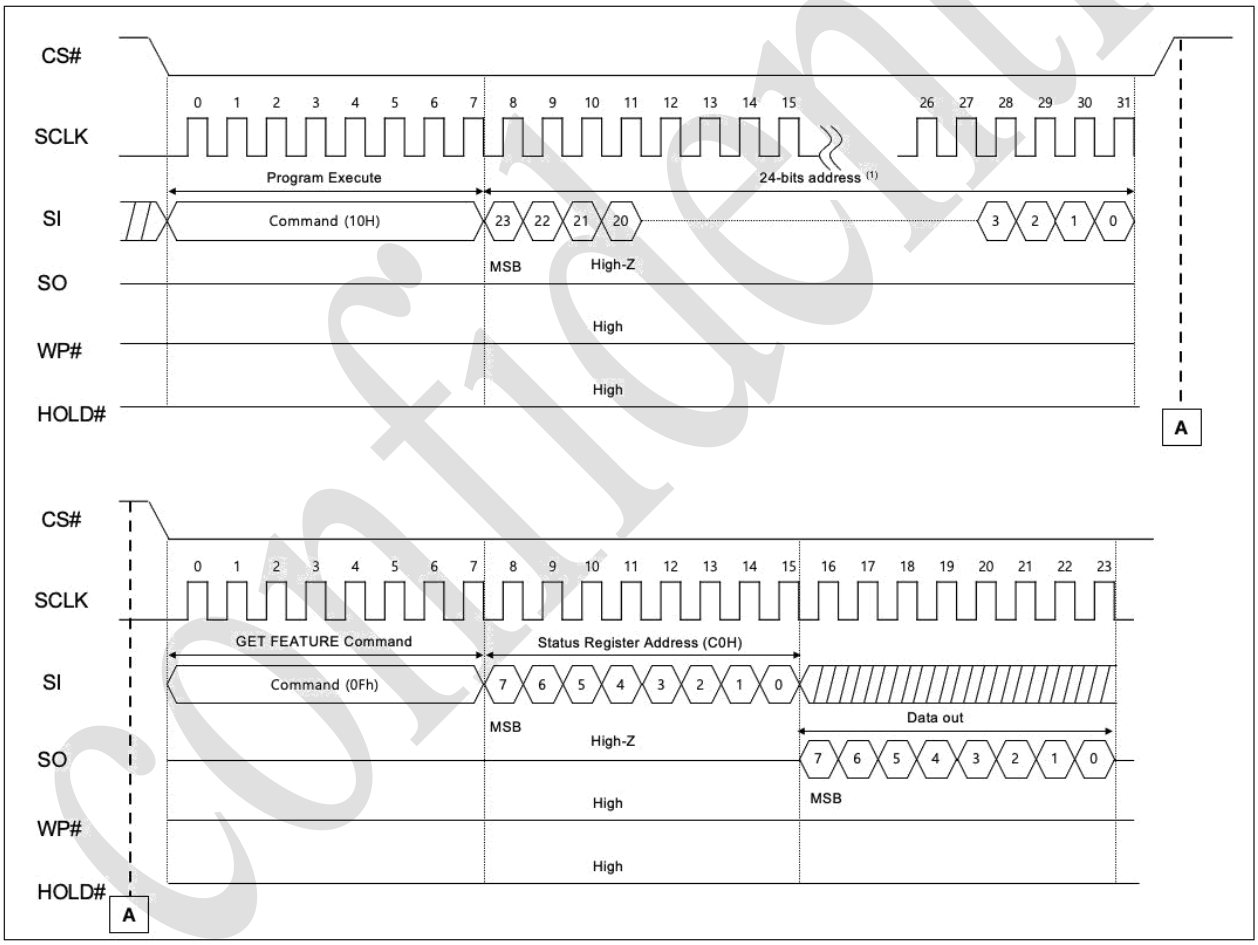
The BLOCK ERASE (D8H) command is used to erase at block level. The command sequence for BLOCK ERASE operation is as follows,

- 06H (WRITE ENABLE command)
- D8H (BLOCK ERASE command)
- 0FH (GET FEATURE command to read the status register)

Erase Operation sequence starts from a WRITE ENABLE (06H) command to set WEL bit to 1. After executing the WRITE ENABLE command, BLOCK ERASE (D8H) command can be issued. BLOCK ERASE (D8H) requires a 24-bit address which consists of dummy bits and row address (page address in row address will be ignored automatically).

Issue the GET FEATURE (0FH) command to monitor the erase operation after issuing the BLOCK ERASE. The E_FAIL bit in status register can reflect whether the block be erased successfully or not.

Block Erase (D8H) Sequence Diagram

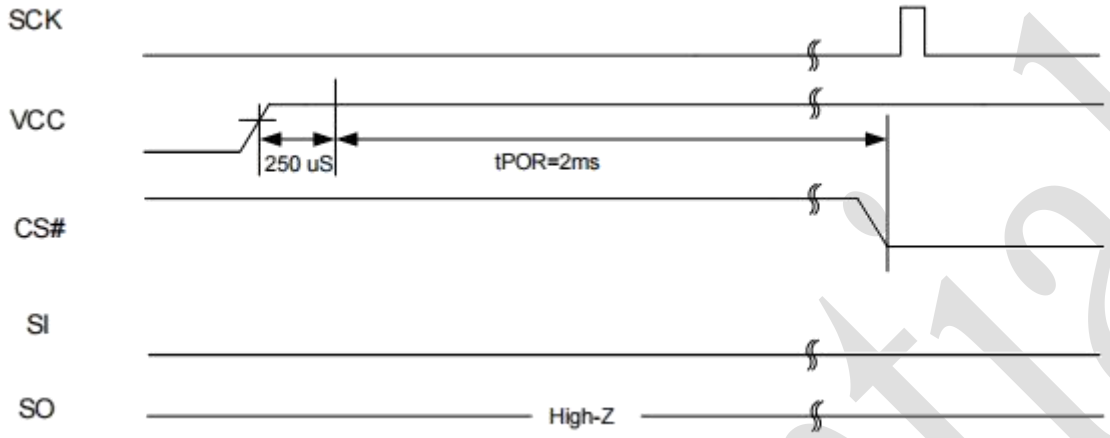


Power-On Process and Reset Operation

During Power on Reset, the first page data of page 0 is auto-loaded to the buffer register.

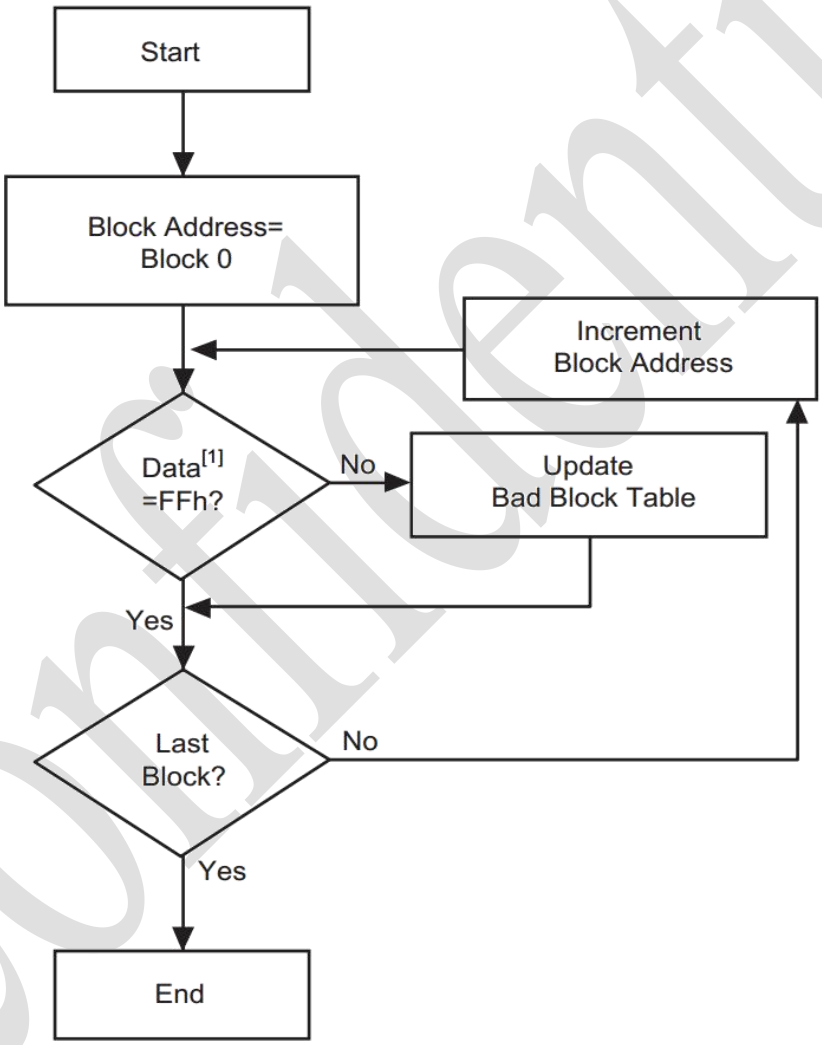
The reset command FFh, does not clear the feature registers but does clear the configuration register bits CFG[2:0] placing the device in normal operation.

Power Up Timing Diagram



Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased (FFh). The Bad Block Information is written before shipping. Any block where the 1st byte in the spare area of the 1st or 2nd or last page does not contain FFh is a Bad Block. That is, if the first page has an FF value and should have been a non-FF value, then the non-FF value in the second page or the last page will indicate a bad block. The Bad Block Information must be read before any erase is attempted, as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information, it is recommended to create a Bad Block table following the flowchart. The host is responsible to detect and track bad blocks, both factory bad blocks and blocks that may go bad during operation. Once a block is found to be bad, data should not be written to that block. Blocks 0-9 are guaranteed good at the time of shipment.



Note:

1) Check for FFh at the 1st byte in the spare area of the 1st,2nd, and last pages.

Valid Blocks

	Symbol	Min	Typ	Max	Unit
Valid Block Number	N_{VB}	1004		1024	Blocks

Opreation Characteristics

Parameters	Min	Typical	Max	Unit
Erase one block		4	10	ms
Program from cache to flash		350	600	us
Read from flash into cache		45	250	us
Reset Time (Ready /Read /Program /Erase)			5 /6 /10 /500	us

DC Characteristics

Parameters	Symbol	Test Conditions	Min	Typical	Max	Unit
Array program current	ICC3			20	25	mA
Standby current	ICC1	CS#=VIH,Vin = 0V or VCC		20	100	uA
Array erase current	ICC4			20	25	mA
Input leakage current	ILI				±10	uA
Read current	ICC2			25	35	mA
Output leakage current ILO t	ILO				±10	uA
DC Input high voltage	VIH		VCC * 0.8		VCC + 0.3	V
DC Input low voltage	VIL		-0.3		VCC * 0.2	V
Output high voltage	VOH	IOH=-400 µA	2.4			V
Output low voltage	VOL	IOL=2.1mA			0.4	V
Erase and program lockout voltage	VLKO			1.8		V

AC Time haracteristics

(T = -40 ~ 85°C,V = 2.7~ 3.6V, C_L = 30pF)

Parameters	Symbol	Min	Typical	Max	Unit
Serial Clock Frequency	FC			104	MHz
Serial Clock High Time	T_CH	4.316			ns
Serial Clock Low Time	T_CL	4.316			ns
Serial Clock Rise Time	tCLCH	1.3			V/ns
Serial Clock Fall Time	tCHCL	1.3			V/ns
CS# Active Setup Time	tSLCH	4.316			ns
CS# Active Hold Time	tCHSH	4.316			ns
CS# Not Active Setup Time	tSHCH	2.877			ns
CS# Not Active Hold Time	tCHSL	2.877			ns
CS# High Time	tSHSL / tCS	30			ns
Output Disable Time	T_WPS	20			ns
WP# Hold Time After CS# High	tSHQZ			10	ns
Output Hold Time	tCLQX	2			ns
Data In Setup Time	tDVCH	2.5			ns
Data In Hold Time	tCHDX	1.75			ns

Hold# Low Setup Time relative to Clock	tHLCH	5			ns
Hold# High Setup Time relative to Clock	tHHCH	5			ns
Hold# High Hold Time relative to Clock	tCHHL	5			ns
Hold# Low Hold Time relative to Clock	tCHHH	5			ns
Hold# Low To High-Z Output	tHLQZ			12	ns
Hold# High To Output	tHHQX			9	ns
Clock Low To Output Valid	tCLQV			7(NOTE1)	ns
WP# Setup Time Before CS# Low	tWHSL	20			ns
WP# Hold Time After CS# High	tSHWL	100			ns
Device Reset Time (Ready/Read/Program/Erase)	tRST			5/6/10/500	µs
Data transfer from cell to register tR with internal ECC on	tR		45	250	µs

Note1: The maximum value for tCLQV at 105°C = 7.5ns

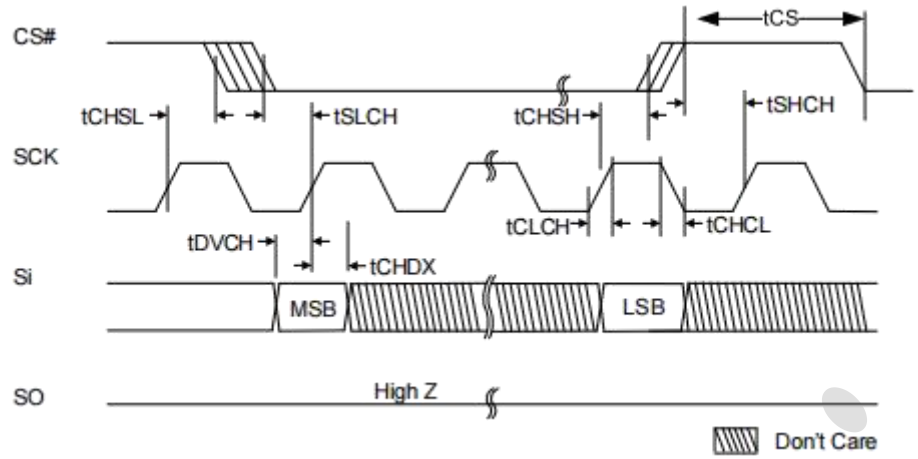
Absolute Maximum Ratings

Parameter	Symbol	Test conditions	Min	Typ	Max	Units	Comments
Temperature under Bias	TBIAS		-40		105	℃	
Storage Temperature	TSTG		-55		125	℃	
Input or Output Voltage(3.3V)	VIO		-0.6		4.6	V	
Supply Voltage(3.3V)	VCC		-0.6		4.6	V	

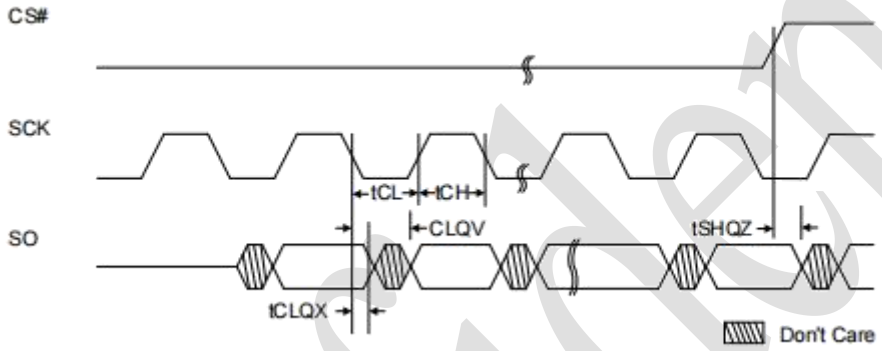
Notes:

1. Except for the rating “Operating Temperature Range”, stresses above those listed in the table Absolute Maximum Ratings “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.
2. Minimum Voltage may undershoot to -2V during transition and for less than 20 ns during transitions.
3. Maximum Voltage may overshoot to VCC +2.0V during transition and for less than 20 ns during transitions.

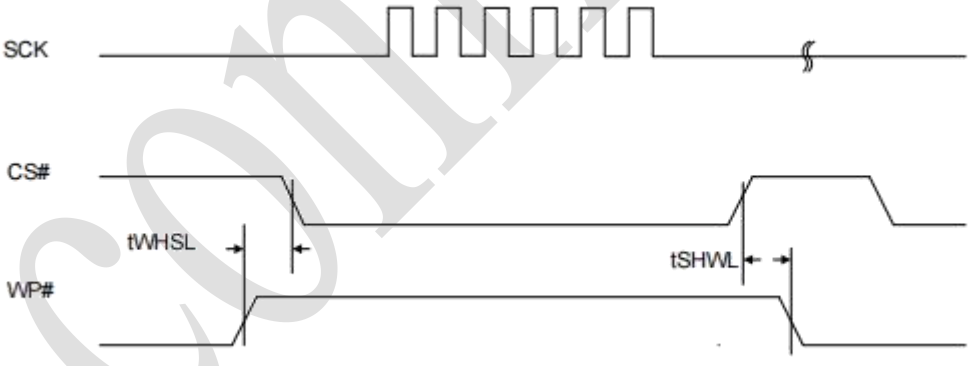
Serial Input Timing



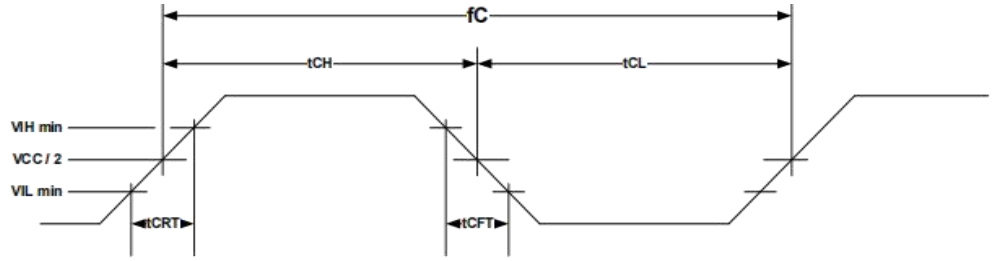
Serial Output Timing



WP# Timing



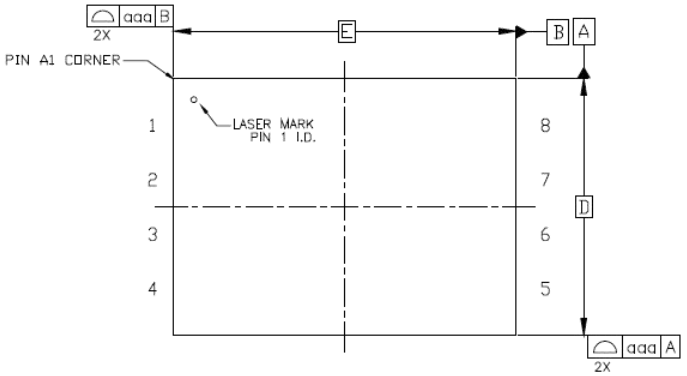
SPI Clock Timing



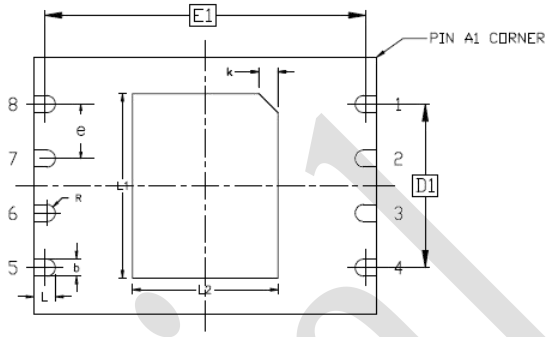
Package Outline

LGA6*8

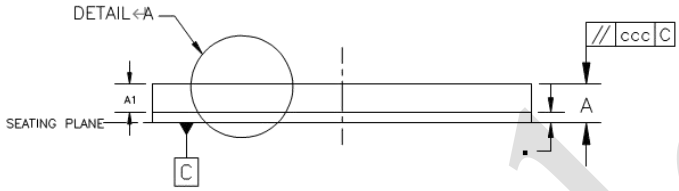
LCC (Leadless Chip Carrier) :



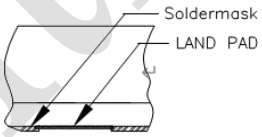
TOP VIEW



BOTTOM VIEW



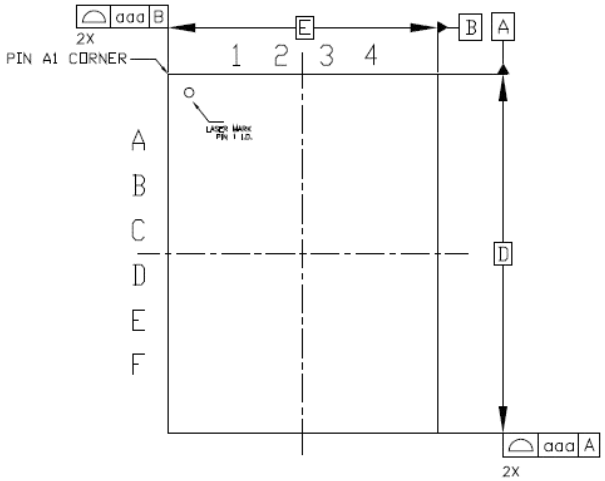
SIDE VIEW

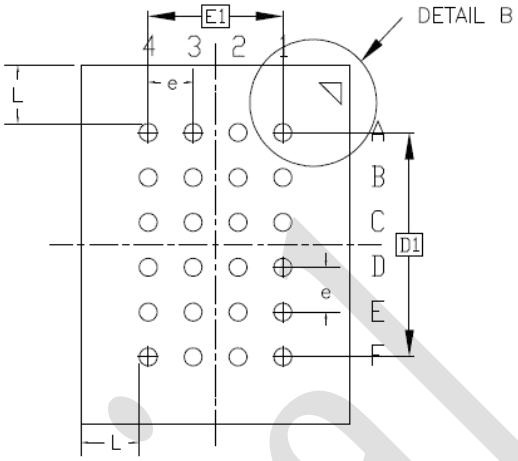


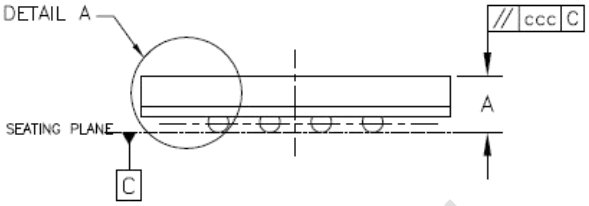
DETAIL A

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1		0.53 BASIC	
c	0.19	0.22	0.25
D	5.90	6.00	6.10
D1		3.81BASIC	
E	7.90	8.00	8.10
E1		7.50 BASIC	
e		1.27 BASIC	
b	0.35	0.40	0.45
L	0.45	0.50	0.55
L1	4.25	4.30	4.35
L2	3.35	3.40	3.45
R		0.20 REF	
k		0.45 REF	
aaa		0.10	
ccc		0.10	

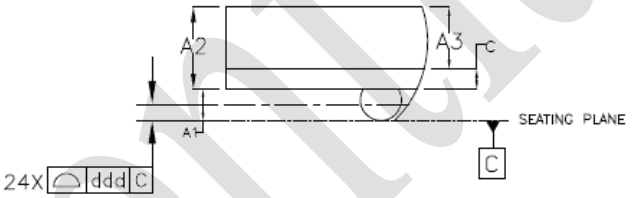
BGA24



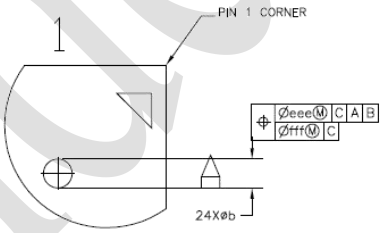




SIDE VIEW



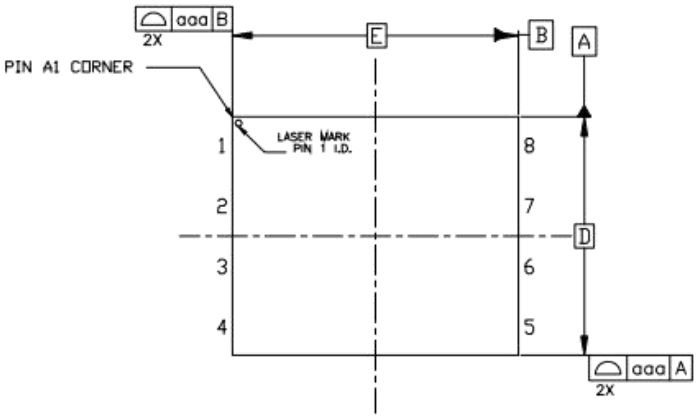
DETAIL A(2:1)



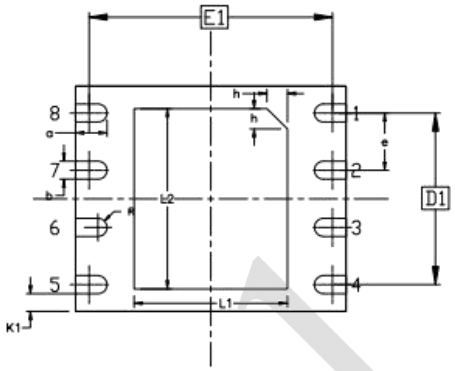
DETAIL B(2:1)

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.02	1.10	1.20
A1	0.25	0.30	0.35
A2	0.75	0.80	0.85
A3	0.55	0.60	0.65
c	0.17	0.20	0.23
D	7.90	8.00	8.10
D1	4.90	5.00	5.10
E	5.90	6.00	6.10
E1	2.90	3.00	3.10
e	0.95	1.00	1.05
b	0.35	0.40	0.45
L	1.30 REF		
aaa	0.10		
ccc	0.20		
ddd	0.12		
eee	0.15		
fff	0.08		

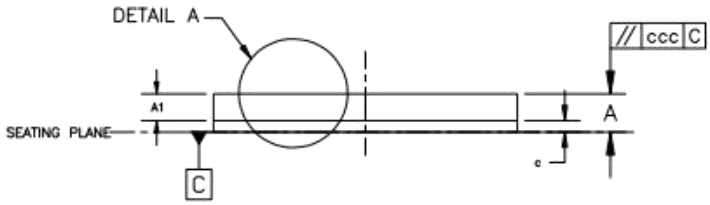
LGA5*6



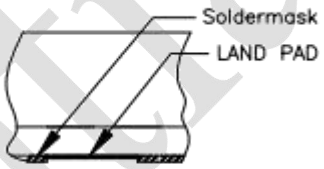
TOP VIEW



BOTTOM VIEW



SIDE VIEW



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A1	0.53 BASIC		
c	0.19	0.22	0.25
D	4.90	5.00	5.10
D1	3.81 BASIC		
E	5.90	6.00	6.10
E1	5.40 BASIC		
e	1.27 BASIC		
a	0.65	0.70	0.75
b	0.35	0.40	0.45
L1	3.35	3.40	3.45
L2	3.95	4.00	4.05
h	0.40	0.45	0.50
K1	0.395 REF		
aaa	0.10		
ccc	0.20		

Revision History

Publication Version:	Note
V1.0 06/17/2022	Initial release
V1.1 11/07/2022	Add BGA24 package information/ update LCC type2
V1.2 11/07/2022	Delete WSON8 package
V1.3 10/03/2023	Correct “ECC Status”
V1.3.1 26/04/2023	Update Page Read to Cache(13H) Sequence Diagram
V1.3.2 02/07/2023	Modify some command
V1.3.3 31/08/2023	Modify some command
V1.3.4 04/09/2023	Add description of ECC and OOB areas and AVBP setting
V 1.3.5 09/25/2023	Modify the scope of the SPI power supply Voltage
V 1.3.6 02/22/2024	Add package LGA5*6 product