N and P Channel Enhancement Mode Power MOSFET

Description

The G100C04D52 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

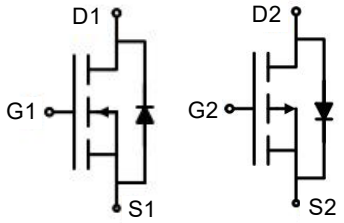
General Features

- NMOS
- V_{DS} 40V
- I_D (at V_{GS} = 10V) 40A
- $R_{DS(ON)}$ (at V_{GS} = 10V) < 9mΩ
- $R_{DS(ON)}$ (at V_{GS} = 4.5V) < 12mΩ
- 100% Avalanche Tested
- RoHS Compliant

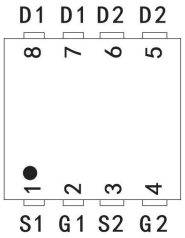
- PMOS
- V_{DS} -40V
- I_D (at V_{GS} = -10V) -24A
- $R_{DS(ON)}$ (at V_{GS} = -10V) < 16mΩ
- $R_{DS(ON)}$ (at V_{GS} = -4.5V) < 20mΩ
- 100% Avalanche Tested
- RoHS Compliant

Application

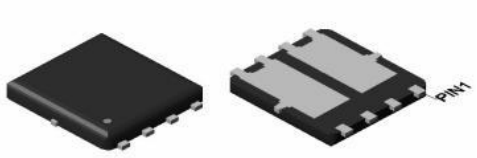
- Power switch
- DC/DC converters



Schematic diagram



pin assignment



DFN5X6-8L Dual

Ordering Information

Device	Package	Marking	Packaging
G100C04D52	DFN5*6-8L Dual	G100C04	5000pcs/Reel

Absolute Maximum Ratings T_C = 25ºC, unless otherwise noted

Parameter	Symbol	NMOS	PMOS	Unit
Drain-Source Voltage	V_{DS}	40	-40	V
Continuous Drain Current	I_D	40	-24	A
Pulsed Drain Current (note1)	I_{DM}	200	-96	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Power Dissipation	P_D	65	50	W
Single pulse avalanche energy （note2）	E_{AS}	81	81	mJ
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	-55 To 150	ºC

Thermal Resistance

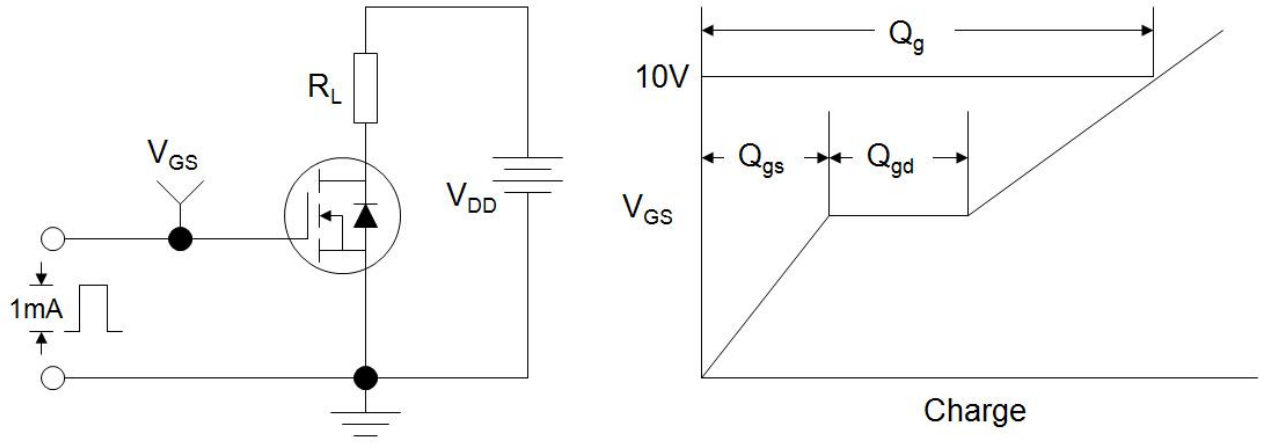
Parameter	Symbol	NMOS	PMOS	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	**40**	50	ºC/W
Maximum Junction-to-Case	R_{thJC}	**1.9**	2.5	ºC/W

NMOS Specifications T_J = 25ºC, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Value**			**Unit**
			Min.	**Typ.**	**Max.**	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	40	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40V, V_{GS} = 0V	--	--	1	μA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1	1.8	2.5	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 30A	--	7	9	mΩ
		V_{GS} = 4.5V, I_D = 20A	--	9	12	
Forward Transconductance	g_{FS}	V_{GS} = 5V, I_D = 12A	--	22	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 20V, f = 1.0MHz	--	2213	--	pF
Output Capacitance	C_{oss}		--	173	--	
Reverse Transfer Capacitance	C_{rss}		--	156	--	
Total Gate Charge	Q_g	V_{DD} = 20V, I_D = 30A, V_{GS} = 10V	--	29	--	nC
Gate-Source Charge	Q_{gs}		--	4.5	--	
Gate-Drain Charge	Q_{gd}		--	6.5	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 20V, I_D = 30A, R_G = 3Ω	--	17	--	ns
Turn-on Rise Time	t_r		--	6.5	--	
Turn-off Delay Time	$t_{d(off)}$		--	30	--	
Turn-off Fall Time	t_f		--	17	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	T_C = 25ºC	--	--	40	A
Body Diode Voltage	V_{SD}	T_J = 25ºC, I_{SD} =30A, V_{GS} = 0V	--	--	1.2	V
Reverse Recovery Charge	Qrr	I_F = 30A, V_{GS} = 0V di/dt=100A/us	--	26	--	nC
Reverse Recovery Time	Trr		--	29	--	ns

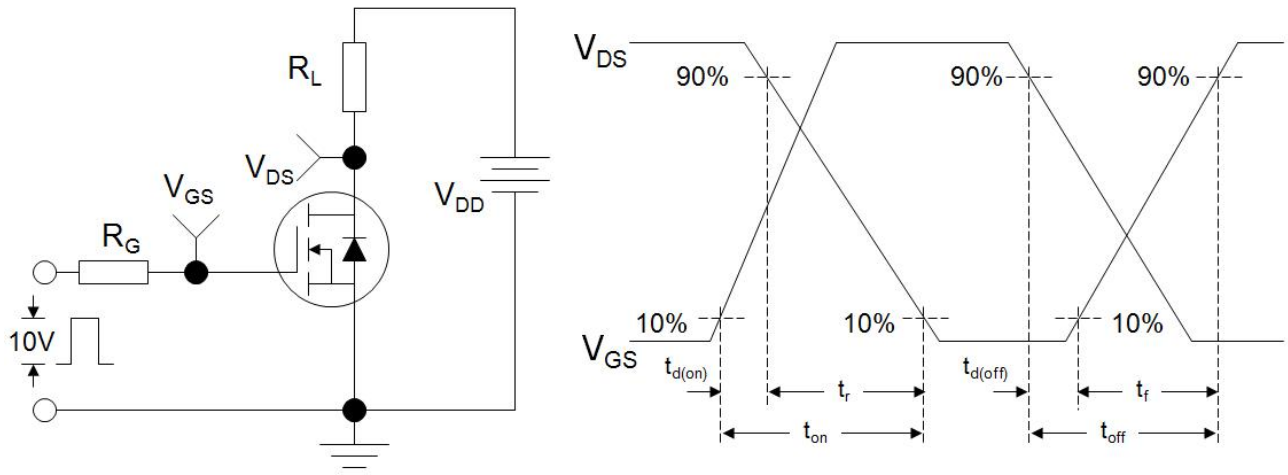
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. EAS condition : Tj=25℃ ,VDD=40V,VGS=10V,L=0.5mH,Rg=25Ω
3. Identical low side and high side switch with identical R_G

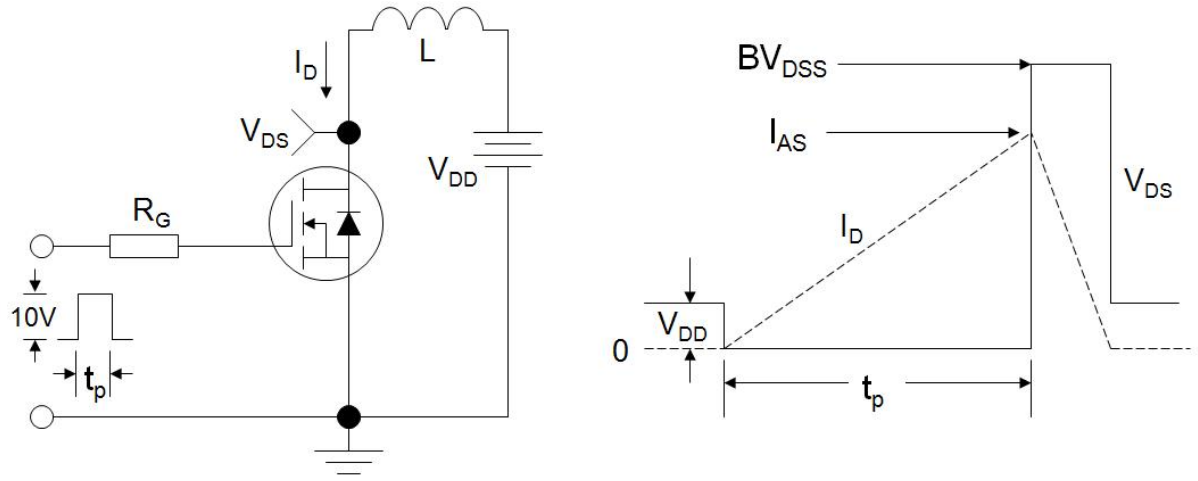
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



NMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 1. Output Characteristics

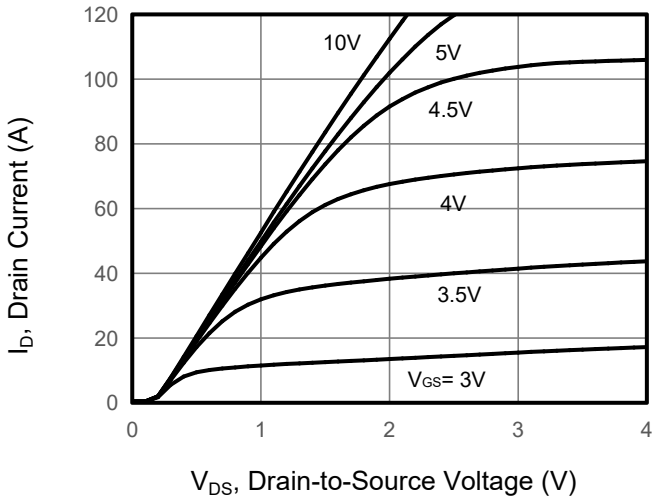


Figure 2. Transfer Characteristics

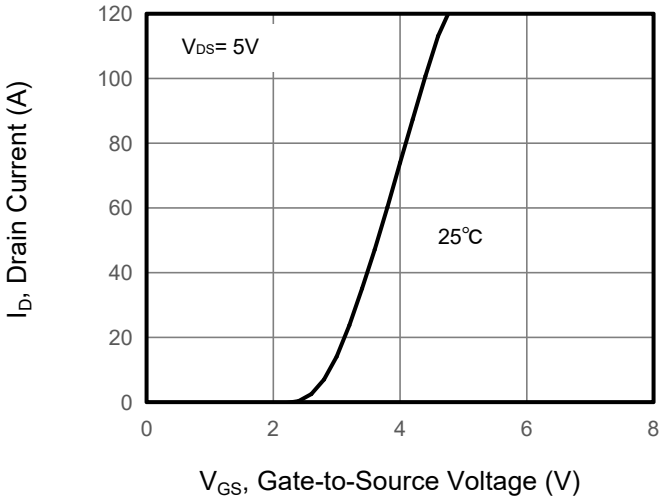


Figure 3. Drain Source On Resistance

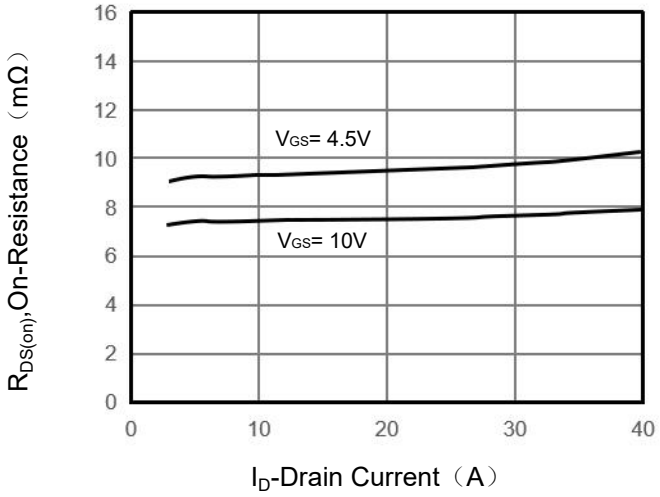


Figure 4. Gate Charge

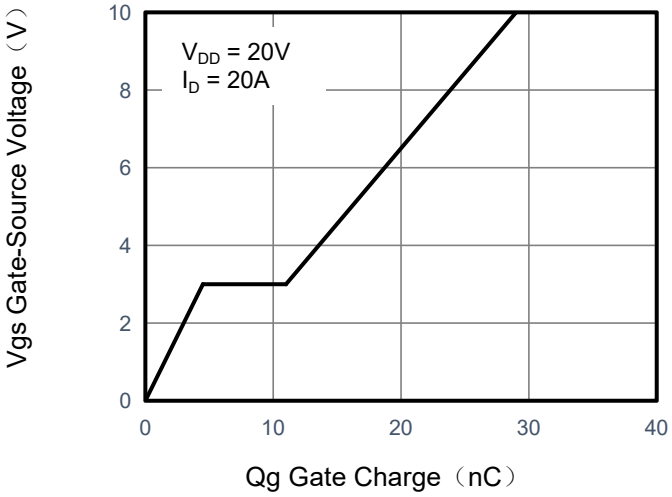


Figure 5. Capacitance

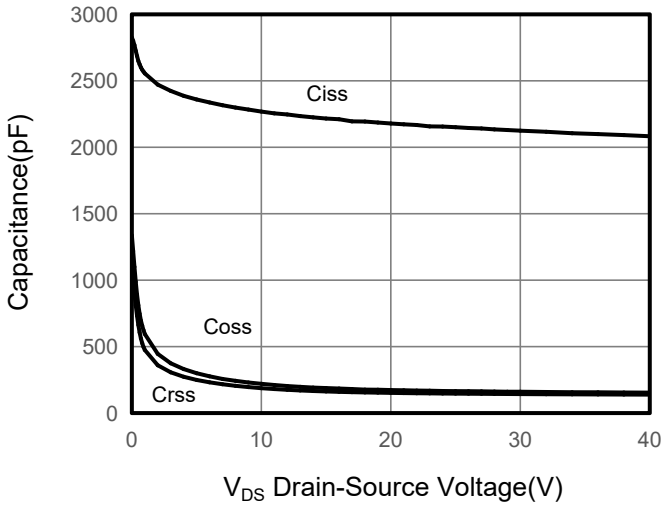
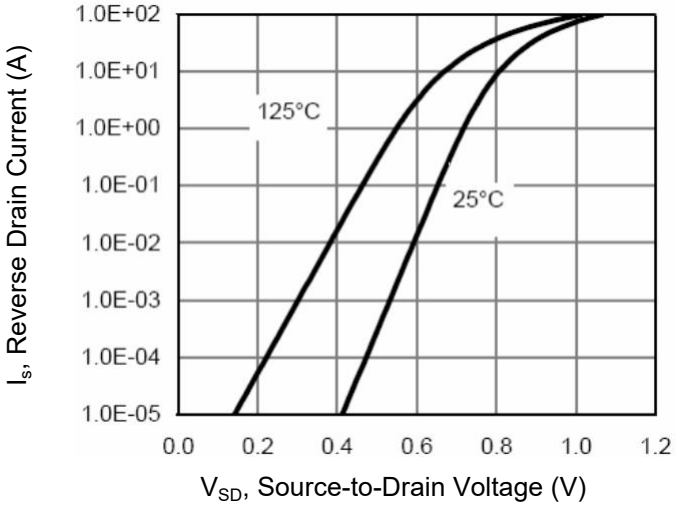


Figure 6. Source-Drain Diode Forward



NMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 7. Drain-Source On-Resistance

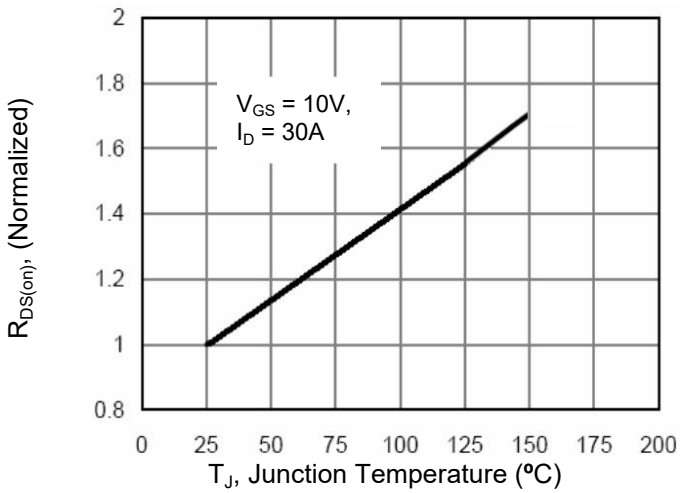


Figure 8. Safe Operation Area

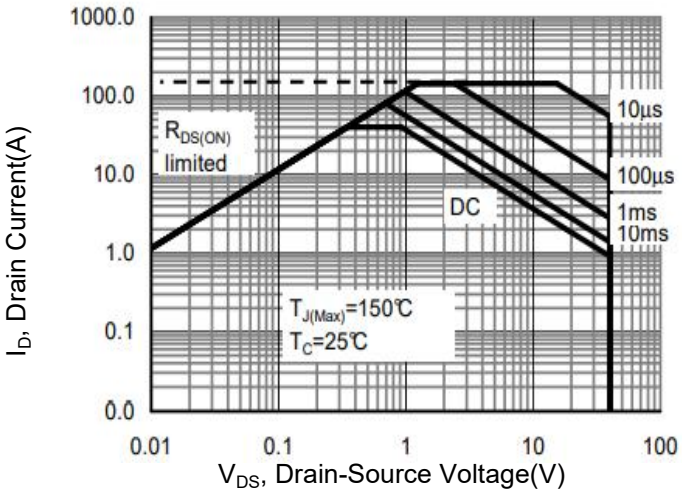
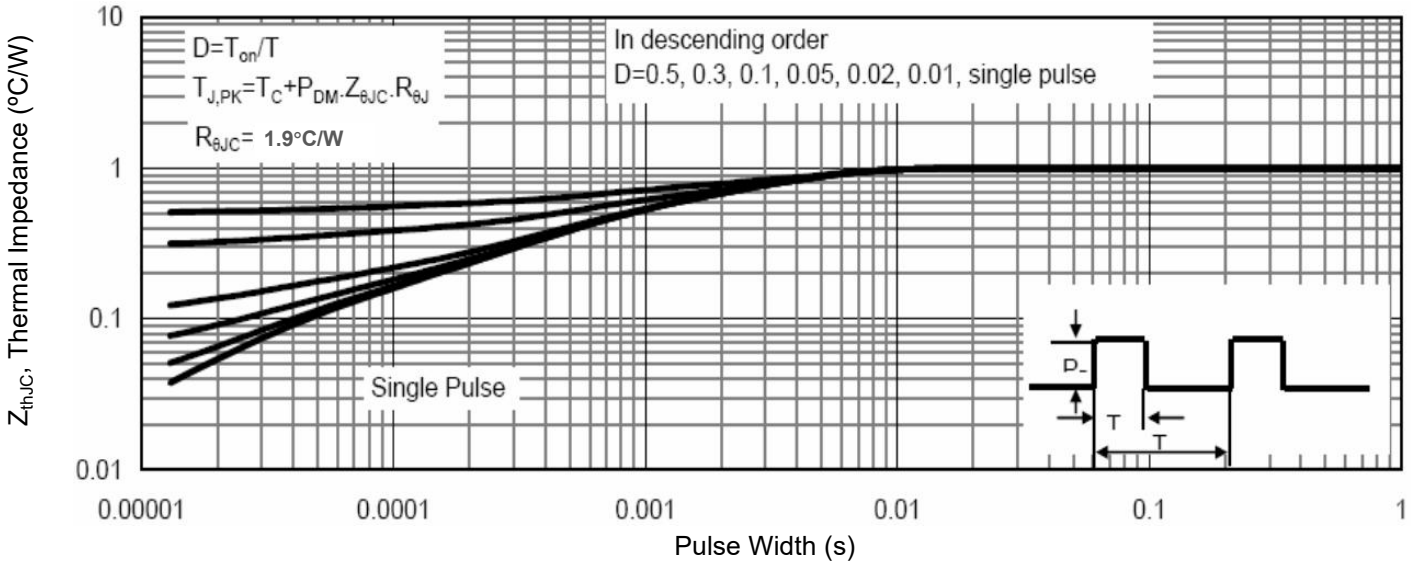


Figure 9. Normalized Maximum Transient Thermal Impedance

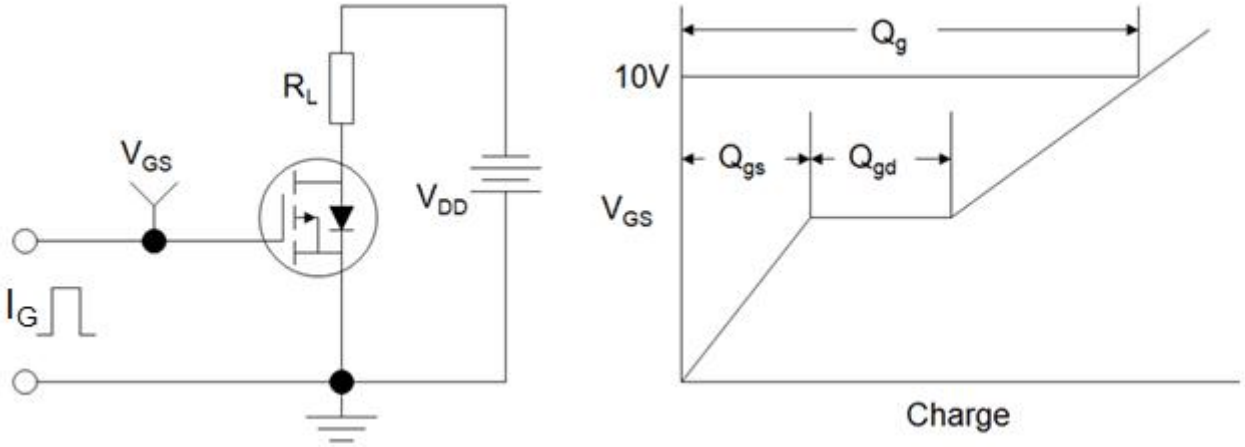


PMOS Specifications T_J = 25ºC, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Value**			**Unit**
			Min.	**Typ.**	**Max.**	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-40	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -40V, V_{GS} = 0V	--	--	-1	μA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±10V	--	--	±100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1	-1.6	-2.5	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D = -10A	--	13	16	mΩ
		V_{GS} = -4.5V, I_D = -8A	--	18	20	
Forward Transconductance	g_{FS}	V_{DS} = -5V,I_D = -12A	--	22	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -20V, f = 1.0MHz	--	2451	--	pF
Output Capacitance	C_{oss}		--	224	--	
Reverse Transfer Capacitance	C_{rss}		--	213	--	
Total Gate Charge	Q_g	V_{DD} = -20V, I_D = -20A, V_{GS} = -10V	--	45	--	nC
Gate-Source Charge	Q_{gs}		--	6.1	--	
Gate-Drain Charge	Q_{gd}		--	10.1	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = -20V, I_D = -10A, R_G = 3Ω	--	9	--	ns
Turn-on Rise Time	t_r		--	7	--	
Turn-off Delay Time	$t_{d(off)}$		--	78	--	
Turn-off Fall Time	t_f		--	39	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	T_C = 25ºC	--	--	-24	A
Body Diode Voltage	V_{SD}	T_J = 25ºC, I_{SD} = -10A, V_{GS} = 0V	--	--	-1.2	V
Reverse Recovery Charge	Q_{rr}	I_F = -20A, V_{GS} = 0V di/dt=-100A/us	--	26	--	nC
Reverse Recovery Time	T_{rr}		--	29	--	ns

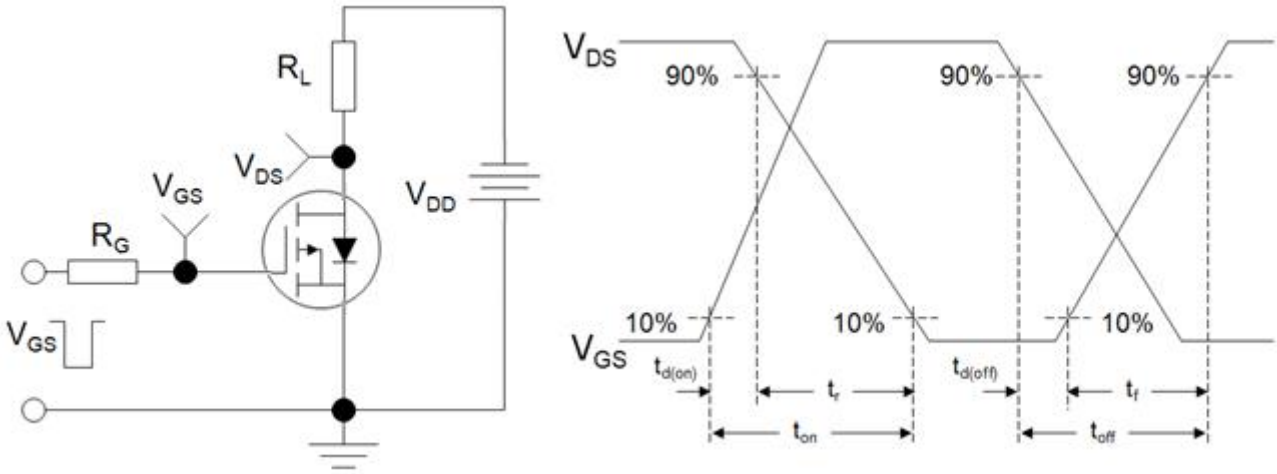
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. EAS condition : Tj=25℃ ,VDD=-40V,VGS=-10V,L=0.5mH,Rg=25Ω
3. Identical low side and high side switch with identical R_G

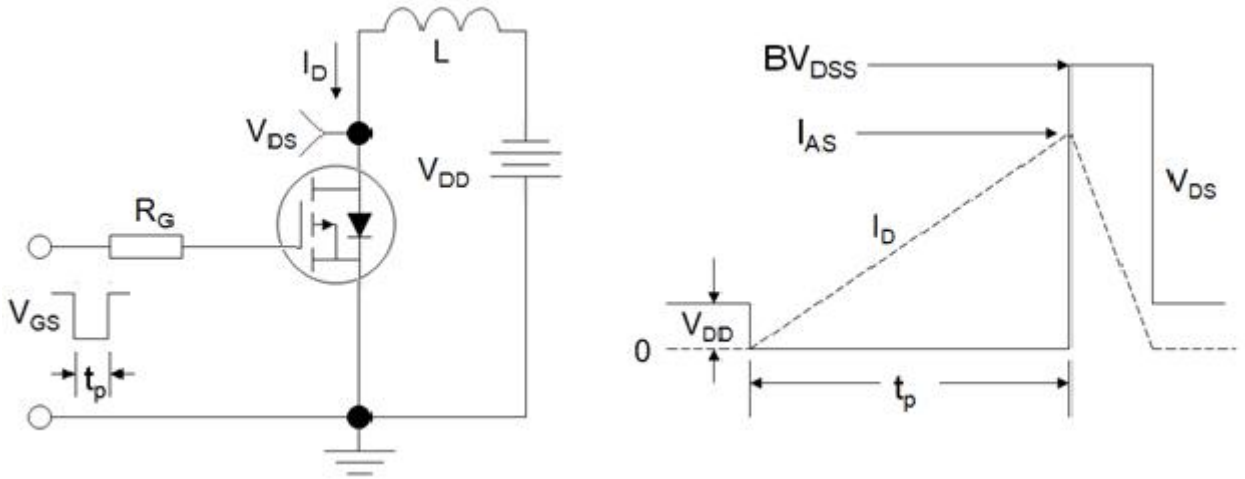
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



PMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 1. Output Characteristics

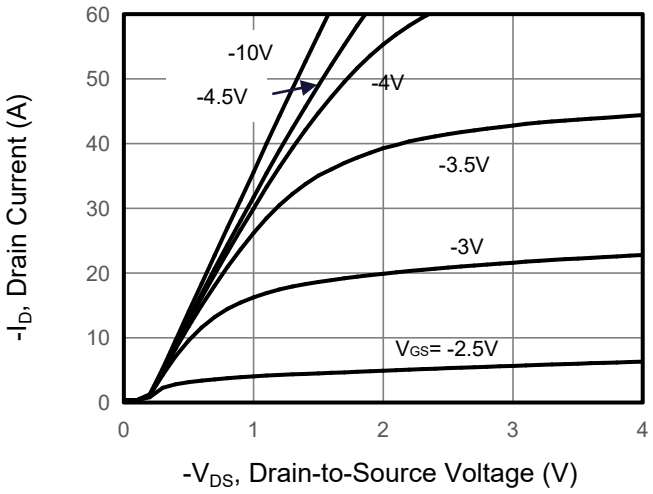


Figure 2. Transfer Characteristics

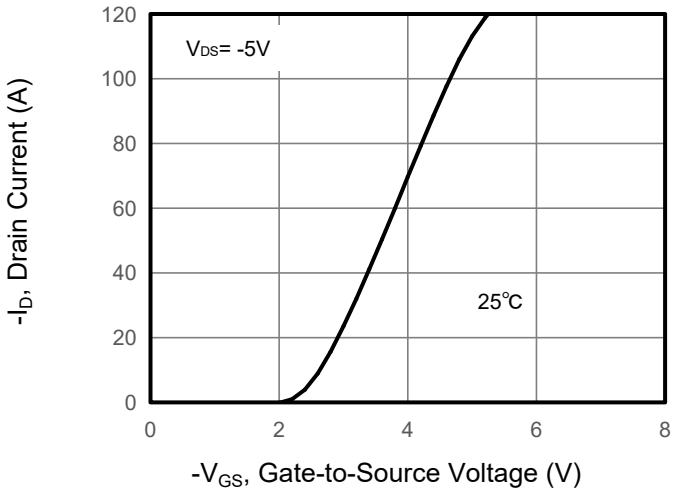


Figure 3.Drain Source On Resistance

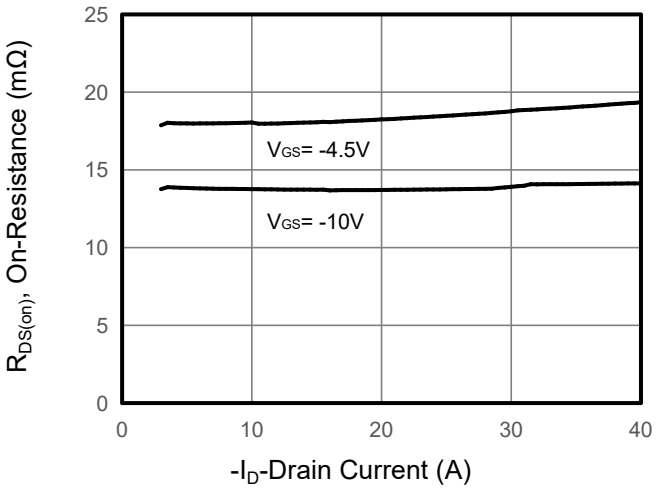


Figure 4. Gate Charge

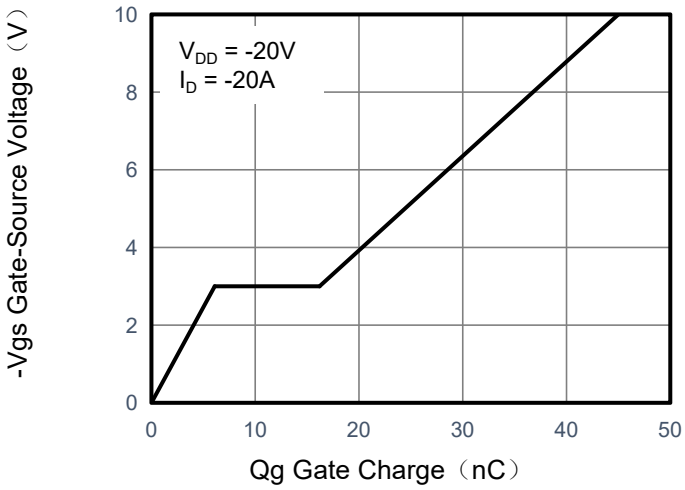


Figure 5. Capacitance

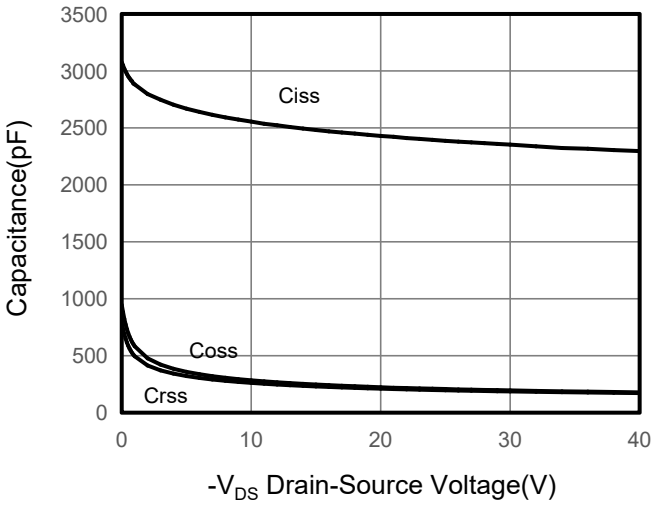
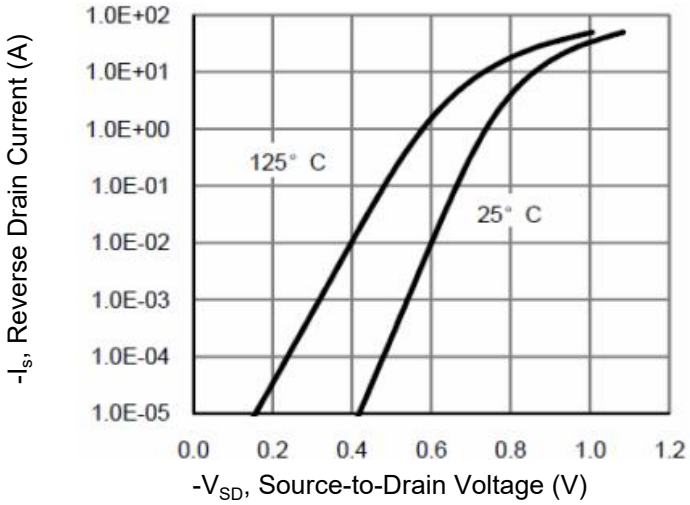


Figure 6. Source-Drain Diode Forward



PMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 7. Drain-Source On-Resistance

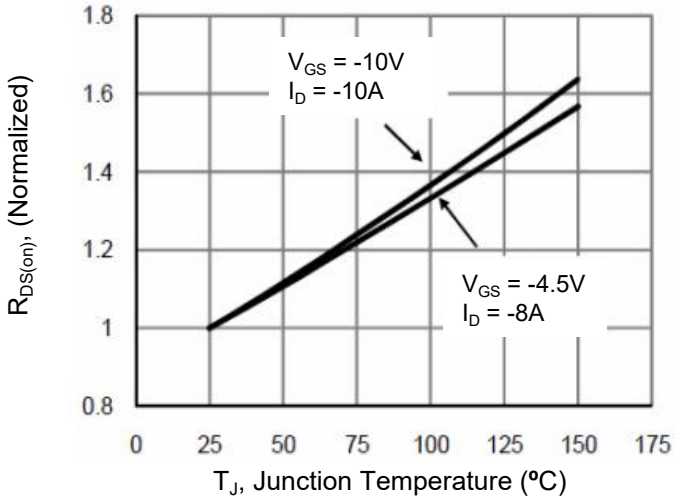


Figure 10. Safe Operation Area

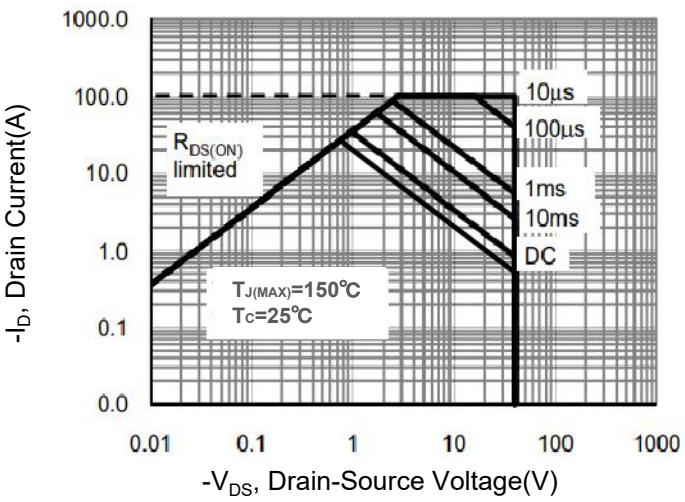
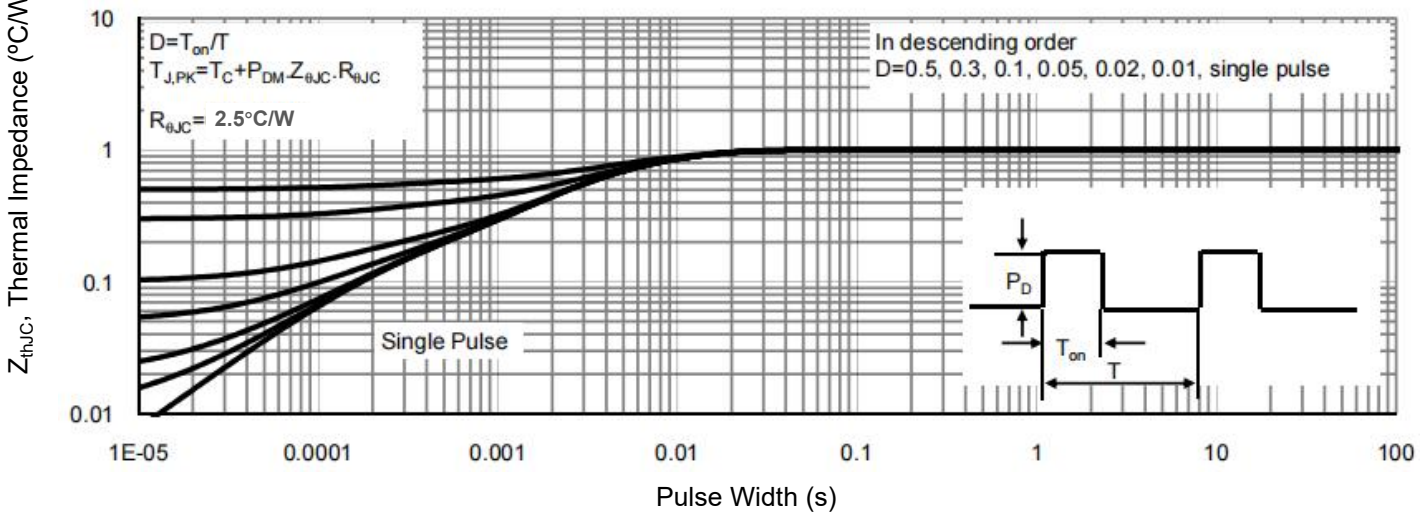
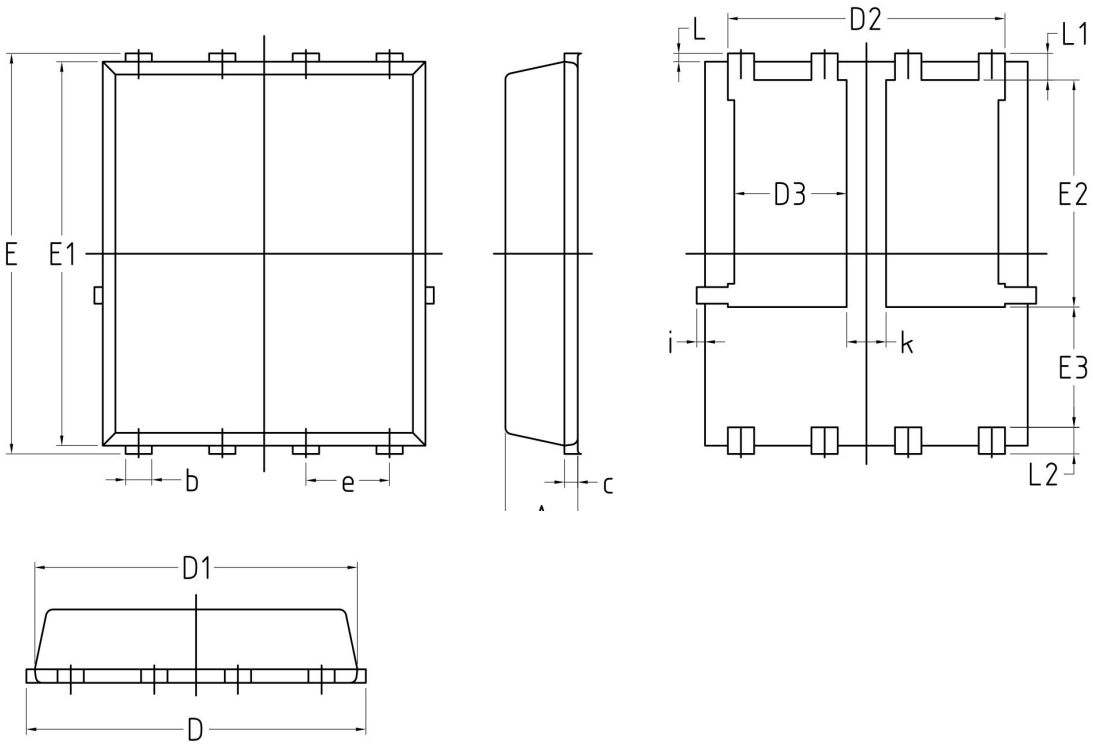


Figure 9. Normalized Maximum Transient Thermal Impedance



DFN5X6-8L Dual Package Information



SYMBOL	COMMON			
	MM		INCH	
	MIN.	MAX.	MIN.	MAX.
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.203 BSC		0.0080 BSC	
D	4.80	5.40	0.1890	0.2126
D1	4.80	5.00	0.1890	0.1969
D2	4.11	4.31	0.1620	0.1700
D3	1.60	1.80	0.0629	0.0708
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	3.30	3.50	0.1300	0.1378
E3	1.70	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0019	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
i	/	0.18	/	0.0070
k	0.5	0.7	0.0197	0.0276