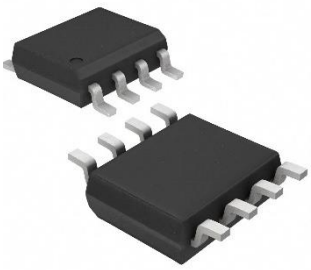
HX65LBC184-S Bus Ransceiver Circuit

The HX65LBC184-S is an RS485/RS-422 transceiver circuit equipped with a 3 .3V/5V voltage supply, half-duplex communication, and ±15KV ESD protection. This circuitencompasses a driver and a receiver.

The HX65LBC184-S showcases enhanced swing rate limits, which assist in minimizing output electromagnetic interference (EMI) and alleviating reflections caused by mismatched terminal connections, facilitating error-free data transfer rates of up to 15Mbps.

The receiver input impedance of the HX65LBC184-S chip is 1/8 unit load, enabling the attachment of up to 256 transceivers for half-duplex communication on the bus. All driver outputs provide ±15kV human mode ESD protection. The chip is packaged in SOP8 and is capable of operating within a temperature range from -40 ° C to +125 ° C.



SOP-8

Peculiarity

- 3.3V/5V supply voltage
- Electrostatic protection (ESD) : A/B±15KV, in line with the human body mode (HBM) standard
- With 1/8 unit load, the bus allows up to 256 transceivers to be attached
- Supports error-free data transmission up to 15Mbps
- With Fail-safe function
- Adopt SOP8 packaging.

Apply

- Industrial control
- ammeter
- Industrial motor drive
- Isolated RS485 interface
- Automated heating, ventilation and air conditioning (HVAC) systems

Chip Pin Description

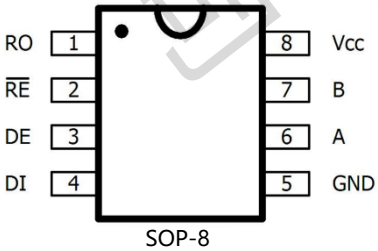
ID	NAME	FEATURE	INSTRUCTIONS
1	RO	Receiver data output	When the receiver is enabled, after polarity judgment, the following conditions apply: - If V(A) - V(B) > -50mV, then the RO output is high. - If V(A) - V(B) < -200mV, then the RO output is low. Here, A and B represent the in-phase terminals of the chip post-polarity judgment.
2	R E	Receiver output enable	When the receiver output is enabled, the RO output is effective if RE is connected to a low level.If RE is on a high level, the receiver will be turned off.At the same time, when RE is high and DE is low, the whole chip is turned off.
3	DE	Driver output enable	**When DE is high, the driver output is enabled. When DE is low, the driver turns off and the output enters a high resistance state. Additionally, when RE is high and DE is low, the entire chip is in an off state.**
4	DI	Drive driver data input	When the driver input DI is low level, the forced in-phase output is low level, and the reverse phase output is high level. When DI is high, the mandatory in-phase output is high, and the inverter output is low.
5	GND	Ground	Ground
6	A	Driver data output receiver data input	In the bus interface, the in-phase output of the driver is connected to the in-phase input of the receiver.
7	B	Driver data output receiver data input	In the bus interface, the inverting output of the driver is connected to the inverting input of the receiver.
8	Vcc	Power source	Power source

Drive truth table

Input			Exportation	
RE	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	Z	Z
1	0	X	Shutoff	

Receiver truth table

Input			Exportation
RE	DE	A-B	RO
0	X	≥-50mV	1
0	X	≤-200mV	0
0	X	Open/Short circuit	1
1	1	X	Z
1	0	X	Shutoff



SOP-8

DC electrical parameters

limit Parameter

SYMBOL	PARAMETRR	MIN	MAX	UNIT
VCC	supply voltage	3.0	+6.0	V
DE，RE	Control input voltage	-0.3	+6.0	V
DI	Drive input voltage	-0.3	+6.0	V
A,B	Drv Out/Rcv In	-8.0	+13.0	V
TSTG	Storage Temperature Range	-65	+150	℃
TOP	Working temperature range	-40	+125	℃
P_D	SOP-8 （+Above 70 ℃）		471	mW
T_L	Soldering temperature (10 seconds)		+300	℃

DC characteristics（Vcc=+3.3V±5%，TA=25℃）

PARAMETER	SYMBOL	Test conditions	MIN	TYP	MAX	UNIT
Driver						
Differential Drive Output (No Load)	VOD1	Figure 1	2			V
Differential drive output	VOD2	R=50Ω(RS-422) Figure 1	1.2			V
		R=27Ω(RS-485) Figure 1	1.2			V
Differential output amplitude variation [1]	ΔVOD	R=50Ω or R=27Ω Figure1			0.2	V
Driver output common mode level	VOC	R=50Ω or R=27Ω Figure 1	0		3	V
Driver output common mode level variatio	ΔVOC	R=50Ω or R=27Ω Figure 1	-		0.2	V
Input High Level	VIH1	DE,DI, RE	2.0			V
Input low level	VIL1	DE,DI, RE			0.8	V
Input lag	VHYS	DE,DI, RE		100		mV
Input Current	IIN1	DE,DI, RE [2]			±2	uA
Input current (A and B)	IIN4	DE=GND, VCC=GNDor5.25V, VIN=12V			125	uA
		DE=GND, VCC=GNDor5.25V, VIN=-7V	-75			uA
Driver output short-circuit current	IOD1	-7V≤VOUT≤VCC	-100			mA
		0V≤VOUT≤12V			100	mA
		0V≤VOUT≤VCC	±25			mA
Receiver						
Receiver differential input threshold voltage	VTH	-7V<VCM<+12V	-200	-	-50	mV
Receiver differential input threshold voltage hysteresis	ΔVTH		-	40	-	mV
Receiver output high level	VOH	IO=-4mA,VID=1V	Vcc-0.4	-	-0	V
Receiver output low level	VOL	IO=4mA,VID=-1V	0	-	.4 ±	V
"Receiver high impedance leakage current"	IOZR	0.4V≤VO≤2.4V	-	-	1 ±	uA
Receiver input impedance	RIN	-7V≤VCM≤+12V	96	-		KΩ
Receiver output short-circuit current	IOSR	0V≤VRO≤VCC	±7	-	95 6	mA
Power supply current		DE=VCC				
Static power supply current	ICC	No load, RE=DI=GNDorVcc, DE=GND		450	006	uA
				450	00	
turn-off current	SHDN	DE=GND, RE=Vcc	0.1		10	uA
Static protection characteristics						
Electrostatic protection (Pin A, Pin B)		Contact discharge model	±12			KV
		manikin	±15			
Electrostatic protection		manikin	±4			KV

Communication char acter istics (Vcc=3.3V ± 5%, TA=25 ℃)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Driver input/output delay	tDPLH	RDIFF=54Ω,	25	72	10	ns
	tDPHL	CL=54pF Figure 3，5	25	72	10	
Difference in Input and Output Delay of Drivers	tDSKEW	RDIFF=54ΩCL1=CL2=100pFigure 3，5		-3	±1	ns
Drive up and down time	tDR,tDF	RDIFF=54ΩCL1=CL2=100pFigure 3，5	40	70	12	ns
maximum rate	fMAX	CL=100pF,S2 Turn off Figure4,6	-	50		kb
Enable the driver to output at a high level	tDZH	CL=100pF,S1 Turn off Figure4,6			25	ns
Enable the driver to output at a low level	tDZL	CL=15pF,S1 Turn off Figure4,6			25	ns
Drive from low output to shutdown time	tDLZ	CL=15pF,S2 Turn off Figure4,6			500	ns
Drive from high output to shutdown time	tDHZ				500	ns
Receiver input/output delay	tRPLH	|VID|≥2.0V；		125	250	ns
	tRPHL	The VID's rise and fall time, as				
|TRPLH tRPHL | Receiver Input Output Delay Difference	tRSKD	depictedn Figures 7，9, is under 15ns.		10	±50	ns
Receiver enabled to output low	tRZL	CL=100pF,S1 Turn off Figure2,8		20	120	ns
Receiver enables high output	tRZH	CL=100pF,S2 Turn off Figure2,8		20	120	ns
Receiver switches from high output to off	tRHZ	CL=100pF,S1 Turn off Figure2,8		20	120	ns
Receiver switches from low output to off	tRLZ	CL=100pF,S2 Turn off Figure2,8		20	120	ns
Chip shutdown time	tSHDN	[3]	50	200	600	ns
From chip off to driver enabled to output high	tDZH(SH DN)	CL=15pF,S2 Turn off Figure4,6			4500	ns
From chip off to driver enabled to output low	Tdzl(SH DN)	CL=15pF,S1 Turn off Figure4,6			4500	ns
From chip off to driver enabled to output high	tRZH(SH DN)	CL=100pF,S2 Turn off Figure2,8			3500	ns
From chip off to driver enabled to output low	tRZL(SH DN)	CL=100pF,S1 Turn off Figure2,8			3500	ns

Notes: 1 Δ VOD and Δ VOC respectively represent the changes in VOD and VOC when DI changes.
2 The current is positive when flowing in and negative when flowing out. Unless noted, all voltages are referenced to ground.
3 WhenR⓪⓪E⓪=1 and DE=0 ， SN3485 enters the OFF state. If the duration of the off state is less than 50ns, the chip will n ot enter the off state. If the duration of the off state exceeds 600ns, the chip must enter the off state.

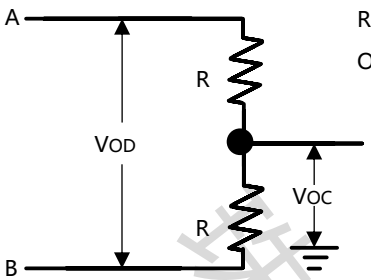


Figure 1 Driver DC characteristic test load

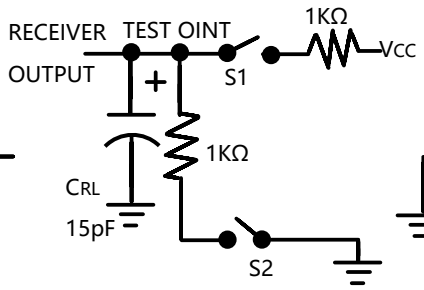


Figure 2 Receiver enable/Off switch characteristic test load

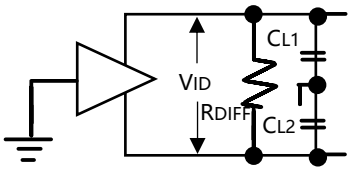


Figure 3. Actuator switch characteristic test circuit

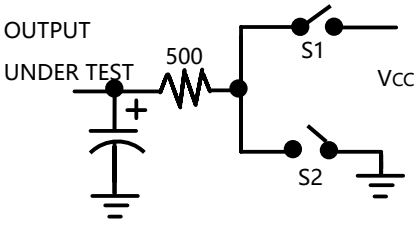


Figure 4 Driver enable/Off switch characteristic test load

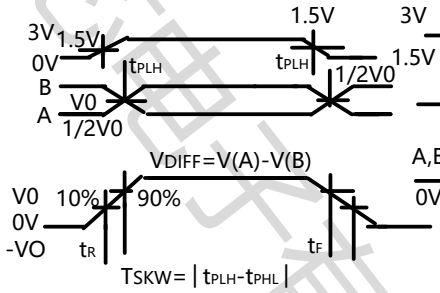


Figure 5 Driver transmission delay

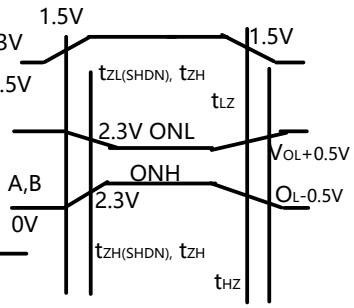


Figure 6 Drive enable/disable sequence

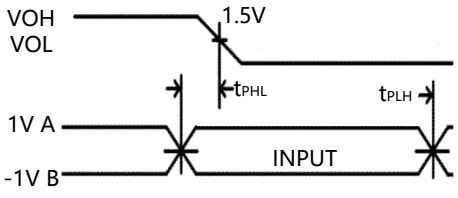


Figure 7 Receiver transmission delay

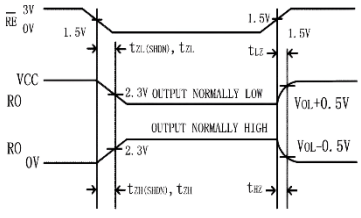


Figure 8 Receiver on/Off sequence

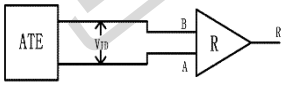


Figure 9 Receiver transmission delay test electrical

Function Description

Bus Loading

The HX65LBC184-S chip supports up to 256 transceivers on the same bus. A standard RS-485 receiver has an input impedance of 12KΩ (1 unit load), while the HX65LBC184-S features an input impedance of 96KΩ (1/8 unit load). This allows for a total of 256 transceivers on the same bus. These devices can be used in any combination, including with other RS-485 transceivers, as long as the total load does not exceed 32 unit loads on the same bus.

Low power off mode

When RE is at high level and DE is at low level, the chip enters low-power shutdown mode. The typical value of turn off current is 1.8uA. RE and DE can be driven simultaneously. If RE is at a high level and DE is at a low level for less than 50ns, the chip will not enter shutdown mode; If the holding time exceeds 600ns, the chip will ensure to enter the shutdown mode.

Reduce EMI and reflection

The limited swing rate driver of HX65LBC184-S can reduce electromagnetic interference (EMI) and minimize reflections caused by improper terminal matching cables, achieving error free data transmission of up to 15Mbps.

Driver output protection

HX65LBC184-S includes overcurrent and overpower protection mechanisms. The overcurrent protection circuit activates when excessive current occurs due to bus abnormalities, preventing the driving current from exceeding a preset limit. Additionally, the overtemperature protection circuit safeguards the chip by ensuring it remains undamaged during high power consumption and rising temperatures. If activated, this mode transitions the driver output to a high-resistance state.

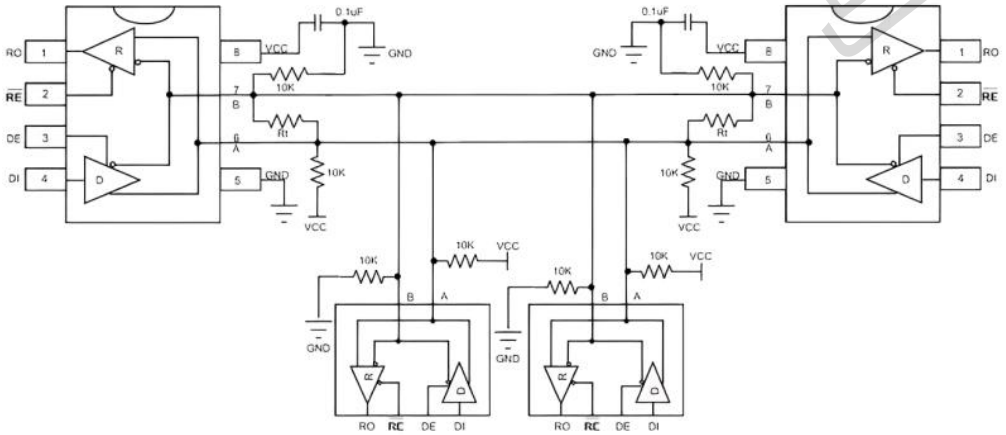
Typical applications

The HX65LBC184-S is often used in multipoint networks for two-way communication. To minimize reflection, it's crucial to match its characteristic impedance at both ends of the transmission line, and keep the branch line length outside the main trunk as short as possible.

Electrostatic protection

All pins of the HX65LBC184S feature electrostatic discharge (ESD) protection circuits to safeguard the chip from damage due to human contact or ESD events during assembly. The driver output and receiver input pin RZ have a characteristic matched impedance of 120Ω, utilizing an enhanced ESD protection circuit that can endure ±15kV human mode ESD shocks without sustaining damage. During normal operation, all ESD protection circuits remain off and do not consume current. After an ESD event, the HX65LBC184S is guaranteed to function without latching or damage. ESD protection performance testing methods include ±15kV human body model and ±12kV IEC61000-4-2 contact discharge.

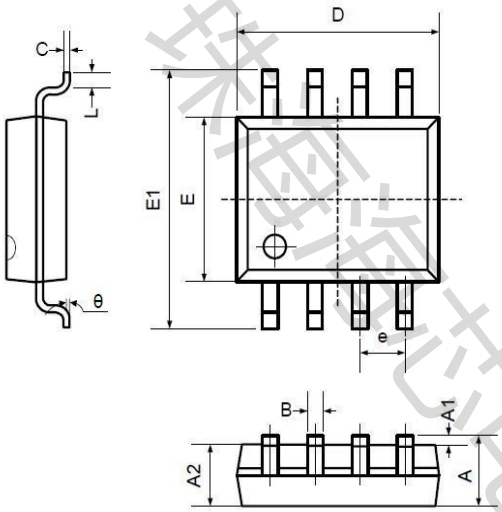
Typical Application Diagram



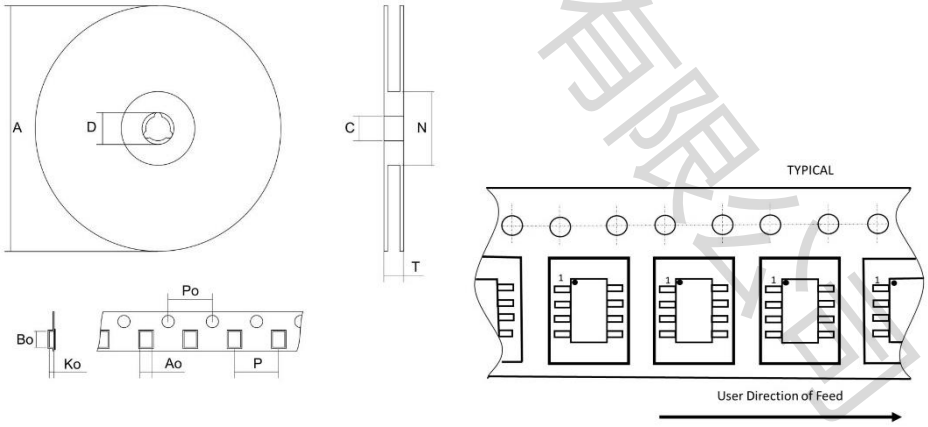
Rt is the feature matching impedance with a typical value of 120Ω

Packaging and packaging

SOP8 (Package Outline Dimensions)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Packaging method	Number
Braid	2500PCS/disk