GBI5130 4A High Accuracy Low Noise LDO Regulator

1 FEATURES

- Low dropout: 160mV (maximum) at 4A
- 1% (maximum) accuracy over line, load, and temperature with BIAS
- Output voltage noise: 7μVRMS
- Input voltage range:
  - Without BIAS: 1.4V to 6.5V
  - With BIAS: 1.1V to 6.5V
- GBI5130 output voltage range:
  - Adjustable operation: 0.5V to 5.15V
  - Fixed operation: 0.5V to 2.075V
- Power-supply ripple rejection:
  - 40dB at 500kHz
- Excellent load transient response
- Adjustable soft-start in-rush control
- Open-drain power-good (PG) output
- Thermal Shutdown and Over Current Protection

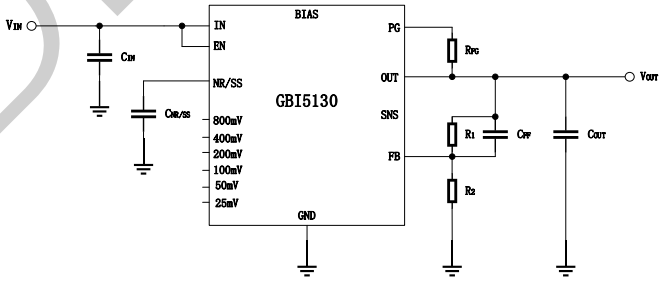
2 APPLICATIONS

- Macro remote radio units (RRU)
- Outdoor backhaul units
- Active antenna system mMIMO (AAS)
- Ultrasound scanners
- Lab and field instrumentation
- Sensor, imaging and radar

3 ORDERING INFORMATION

TYPE	MARKING	PACKAGE	Body Size
GBI5130QYAR	5130	QFN20	3.5mm x 3.5mm

4 Typical Application



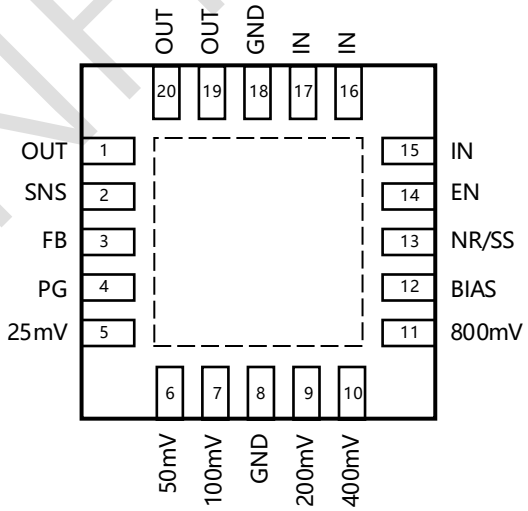
5 DESCRIPTION

The GBI5130 is a low-noise, low-dropout linear regulator (LDO) capable of sourcing 4A with only 160mV maximum dropout. The device is offered in two output voltage ranges. The GBI5130 output voltage is pin-programmable from 0.5V to 2.075V, with a 25mV resolution, and adjustable from 0.5V to 5.15V using an external resistor divider.

The combination of low-noise, high-PSRR, and high output-current capability makes the GBI5130 ideal to power noise-sensitive components such as those found in high-speed communications, video, medical, or test and measurement applications. The high performance of the GBI5130 limits power supply generated phase noise and clock jitter, making this device ideal for powering high-performance serializer and de-serializer (SerDes), analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and RF components. Specifically, RF amplifiers benefit from the high-performance and >5V output capability of the device.

For digital loads [such as application-specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs), and digital signal processors (DSPs)] requiring low-input voltage, low-output (LILO) voltage operation, the exceptional accuracy (1% over line, load, and temperature), remote sensing, excellent transient performance, and soft-start capabilities of the GBI5130 ensure optimal system performance.

6 PIN CONFIGURATION



GBI5130

Top View

Table 1. PIN CONFIGURATION

PIN OUT		I/O	PIN FUNCTION
NAME	**GBI5130**		
25mV	5	I	Voltage setting pins. These pins connect to an internal feedback network. Connect these pins to ground, SNS, or leave floating. Connecting these pins to ground increases the output voltage, whereas connecting these pins to SNS increases the resolution of the feedback network but decreases the range of the feedback network; multiple pins may be simultaneously connected to GND or SNS to select the desired output voltage. Leave these pins floating (open) when not in use.
50mV	6	I	
100mV	7	I	
200mV	9	I	
400mV	10	I	
800mV	11	I	
BIAS	12	I	BIAS supply voltage. This pin enables the use of low-input voltage, low-output (LILO) voltage conditions (that is, V_{IN}=1.2V, V_{OUT}=1V) to reduce power dissipation across the die. A 1µF capacitor (0.47µF capacitance) or larger must be connected between this pin and ground. If not used, this pin must be left floating or tied to ground.
EN	14	I	Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device. If enable functionality is not required, this pin must be connected to IN or BIAS
FB	3	I	Feedback pin connected to the error amplifier. Although not required, a 10nF feed-forward capacitor is recommended between FB and OUT (as close to the device as possible) to maximize ac performance. The use of a feed-forward capacitor may disrupt Power-Good (PG) functionality
GND	8,18		Ground pin. These pins must be connected to ground, the thermal pad, and each other with a low-impedance connection
IN	15-17	P	Input supply voltage pin. A 10µF or larger ceramic capacitor (5µF of capacitance or greater) from IN to ground is required to reduce the impedance of the input supply. Place the input capacitor as close as possible to the input.

NR/SS	13	I/O	Noise-reduction and soft-start pin. Connecting an external capacitor between this pin and ground reduces reference voltage noise and also enables the soft-start function. Although not required, GOSEMICON recommends a 10nF or larger capacitor be connected from NR/SS to GND (as close as possible to the pin) to maximize ac performance.
OUT	1,19,20	O	Regulated output pin. A 22uF or larger (10uF or greater of effective capacitance) is required for stability. Place the capacitor as close to the device as possible and minimize the distance between OUT and load.
PG	4	O	Power good indication. It is an open-drain output and is active high when output voltage is higher than 91% of the target value. The pin voltage is pulled low when the output voltage is lower than 85% of the target value, EN shutdown, OTP and OCP.
SNS	2	I	Output voltage sense pin. Connect this pin only when setting the OUT voltage by using PCB layout (no external resistor is needed). Keep SNS pin floating if the OUT voltage is set by external resistor.
THERMAL PAD		-	Connect the thermal pad to ground plane solidly.

7 SPECIFICATIONS

7.1 ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
Voltage	IN, BIAS, PG, EN	-0.3	7	V
	SNS, OUT	-0.3	IN+0.3	V
	NR/SS, FB	-0.3	3.6	V
	25mV, 50mV, 100mV, 200mV, 400mV, 800mV	-0.3	OUT+0.3	V
Current	OUT	Internal Limited	Internal Limited	
	PG		5	mA
Operating junction temperature	T_J	-40	125	°C
Storage temperature	T_{STG}	-65	150	°C

7.2 ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)	-2	+2	kV
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins (1)	-500	+500	V

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

7.3 RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range	1.1		6.5	V
V_{BIAS}	Bias supply voltage range	3		6.5	V
V_{OUT}	Output voltage range	0.5		5.15	V
V_{EN}	Enable voltage range	0		V_{IN}	V
I_{OUT}	Output current	0		4	A
C_{IN}	Input capacitor	10	47		μF

C_{OUT}	Output capacitor		47	100	μF
C_{BIAS}	Bias pin capacitor		10		μF
R_{PG}	Power-good pullup resistance	10		100	kΩ
$C_{NR/SS}$	NR/SS capacitor		10		nF
C_{FF}	Feed-forward capacitor		10		nF
R_1	Top resistor value in feedback divider		10		kΩ
R_2	Bottom resistor value in feedback divider			160	kΩ
T_J	Operating junction temperature	-40		125	℃

7.4 THERMAL INFORMATION

PARAMETER	THERMAL METRIC	QFN20	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance	43	°C/W
$R_{\theta JC(top)}$	Junction to case(top) thermal resistance	38	°C/W
ψ_{JT}	Junction to top characterization parameter	0.8	°C/W
ψ_{JB}	Junction to board characterization parameter	17.5	°C/W

7.5 ELECTRICAL CHARACTERISTICS

T_J=-40°C~125°C, typical values are tested under 25°C.

V_{IN} =1.4V or V_{IN} = $V_{OUT(nom)}$ + 0.4V(whichever is greater), V_{BIAS} = open, $V_{OUT(nom)}$=0.5V, OUT connected to 50Ω to GND, V_{EN} = 1.1V, C_{IN} = 10uF, C_{OUT}=47μF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, and PG pin pulled to VIN with 100kΩ (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Input supply voltage range		1.1		6.5	V
V_{BIAS}	Input supply voltage range	V_{IN} = 1.1V	3.0		6.5	V
$V_{UVLO1(IN)}$	Input supply UVLO with BIAS	V_{IN} rising with V_{BIAS} = 3V		1.02	1.085	V
$V_{HYS1(IN)}$	$V_{UVLO1(IN)}$ hysteresis	V_{BIAS} = 3V		200		mV
$V_{UVLO2(IN)}$	Input supply UVLO without BIAS	V_{IN} rising		1.28	1.39	V
$V_{HYS2(IN)}$	$V_{UVLO2(IN)}$ hysteresis			220		mV
$V_{UVLO(BIAS)}$	Bias supply UVLO	V_{IN} rising, V_{IN} = 1.1V		2.80		V

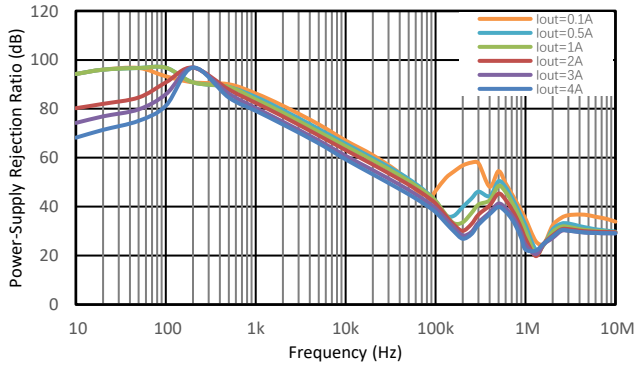
SYMBOL	PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{HYS(BIAS)}$	$V_{UVLO2(BIAS)}$ hysteresis				140		mV
$V_{IL(EN)}$	EN pin low-level output voltage					0.5	V
$V_{IH(EN)}$	EN pin high-level output voltage			1.1			V
$V_{OL(PG)}$	PG pin low-level output voltage		I_{PG} =1mA			0.4	V
V_{FB}	Feedback voltage				0.5		V
I_{FB}	FB pin leakage current		V_{IN} =6.5V	-100		100	nA
$V_{NR/SS}$	NR/SS pin voltage				0.5		V
$I_{NR/SS}$	NR/SS pin charging current		$V_{NR/SS}$ = 0V, V_{IN} =6.5V	4.5	6	7.5	μA
V_{DO}	Dropout voltage		V_{IN} =1.4V, I_{OUT} = 4A V_{FB} = 0.5V -3%		80	160	mV
			V_{IN} =5.4V, I_{OUT} = 4A V_{FB} = 0.5V -3%		80	160	mV
			V_{IN} =1.4V 3.0V≤VBIAS≤6.5V I_{OUT} = 4A V_{FB} = 0.5V -3%		80	160	mV
V_{OUT}	Output voltage	Range	Using programming pin	0.5		2.075	V
		Range	Using external resistors	0.5		5.15	V
		Accuracy	0.5V ≤ V_{OUT} ≤ 5.15V 5mA ≤ I_{OUT} ≤ 4A, over V_{IN} -40~85℃	-1%		+1%	
		Accuracy	0.5V ≤ V_{OUT} ≤ 5.15V 5mA ≤ I_{OUT} ≤ 4A 3V ≤ V_{BIAS} ≤ 6.5V -40~125℃	-1.5%		+1.5%	
		Accuracy with BIAS	0.5V ≤ V_{OUT} ≤ 5.15V 5mA ≤ I_{OUT} ≤ 4A 3V ≤ V_{BIAS} ≤ 6.5V -40~85℃	-1%		+1%	
		Accuracy with BIAS	0.5V ≤ V_{OUT} ≤ 5.15V 5mA ≤ I_{OUT} ≤ 4A	-1.5%		+1.5%	

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
		3V ≤ V_{BIAS} ≤ 6.5V -40~125℃					
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	I_{OUT} = 5mA 1.4V ≤ V_{IN} ≤ 6.5V			0.03		mV/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	5mA ≤ I_{OUT} ≤ 4A 3V ≤ V_{BIAS} ≤ 6.5V V_{IN} = 1.1V			0.07		mV/A
		5mA ≤ I_{OUT} ≤ 4A			0.08		mV/A
		5mA ≤ I_{OUT} ≤ 4A V_{OUT} = 5.15V			0.04		mV/A
I_{lim}	Output current limit			4.5	5.2	6.3	A
I_{sc}	Short circuit current limit				2.4		A
PSRR	Power Supply Ripple Rejection	V_{IN} - V_{OUT}= 0.4V V_{IN} = 1.1V/5.5V I_{OUT} = 4A $C_{NR/SS}$ = 10nF C_{FF} = 10nF C_{OUT} = 47uF||10uF||10uF	f =10kHz V_{OUT} = 0.5V V_{BIAS} = 5V		60		dB
			f = 500kHz V_{OUT} = 0.5V V_{BIAS} = 5V		40		dB
			f = 10kHz V_{OUT} = 5V		50		dB
			f = 500kHz V_{OUT} = 5V		32		dB
Vn	Output noise voltage	BW = 10Hz TO 100kHz V_{IN} = 1.1V, V_{OUT} = 0.5V V_{BIAS} = 5V, I_{OUT} = 3A $C_{NR/SS}$ =10nF, C_{FF} = 10nF C_{OUT} = 47uF||10uF||10uF			7		μVrms
		BW = 10Hz TO 100kHz V_{IN} = 5.3V, V_{OUT} = 5.0V V_{BIAS} = 5V, I_{OUT} = 3A $C_{NR/SS}$ =100nF, C_{FF} = 100nF C_{OUT} = 47uF||10uF||10uF			11.9		μVrms
I_{GND}	GND pin current	V_{IN} =6.5V, I_{OUT} = 5mA			1		mA

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
		V_{IN} =1.4V, I_{OUT} = 1A		5		mA
		Shutdown, PG open V_{IN} =6.5V, V_{EN} =0.5V		3		μA
V_{PG_IT}	PG pin threshold	For falling V_{OUT}	80%	85%	90%	
V_{PG_Hys}	PG pin hysteresis	For rising V_{OUT}		6%		
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		160		℃
		Reset, temperature decreasing		140		℃
T_J	Operating junction temperature		-40		125	℃

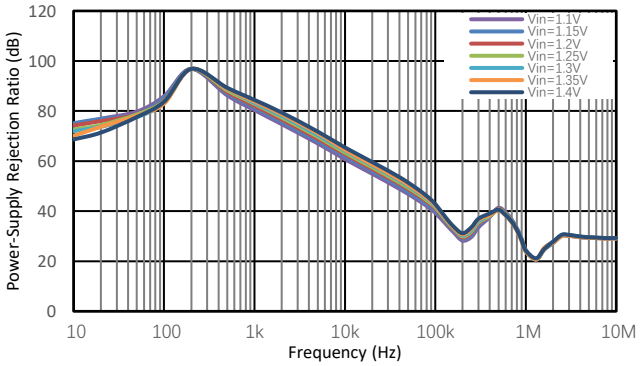
7.6 TYPICAL CHARACTERISTICS

at T_a = 25°C, V_{IN} = 1.4V or V_{IN} = $V_{OUT(nom)}$ + 0.4V (whichever is greater), V_{BIAS} = open, $V_{OUT(nom)}$ = 0.5V, V_{EN} = 1.1V, C_{IN} = 10µF, C_{OUT} = 47µF, $C_{NR/SS}$ = 0 nF, no C_{FF}, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted)



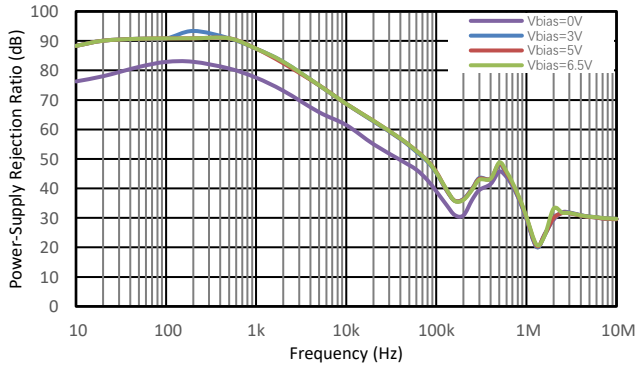
V_{IN} = 1.1V, V_{BIAS} = 5V, C_{OUT} = 47µF || 10µF || 10µF, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF

Figure 7-1. PSRR vs Frequency and I_{OUT}



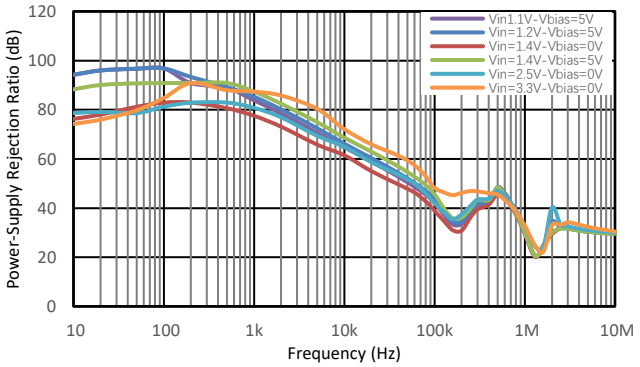
I_{OUT} = 3A, V_{BIAS} = 5V, C_{OUT} = 47µF || 10µF || 10µF, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF

Figure 7-2. PSRR vs Frequency and V_{IN} with Bias



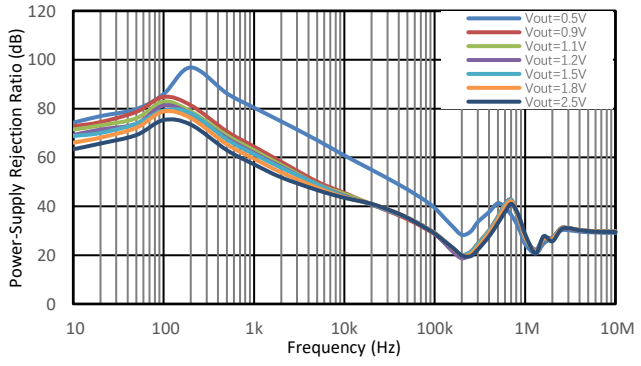
V_{IN} = 1.4V, I_{OUT} = 1A, C_{OUT} = 47µF || 10µF || 10µF, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF

Figure 7-3. PSRR vs Frequency and V_{BIAS}



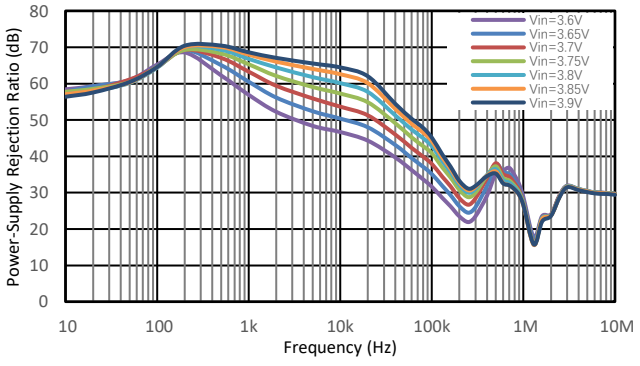
I_{OUT} = 1A, C_{OUT} = 47µF || 10µF || 10µF, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF

Figure 7-4. PSRR vs Frequency and V_{IN}



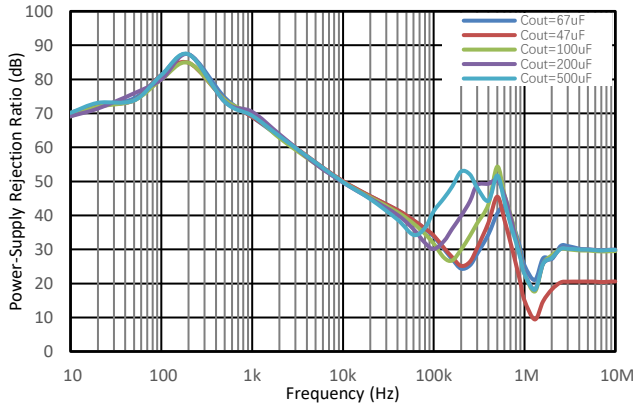
V_{IN} = V_{OUT} + 0.3V or V_{IN} = 1.1V (whichever is greater), V_{BIAS} = 5V, I_{OUT} = 3A, C_{OUT} = 47µF || 10µF || 10µF, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF

Figure 7-5. PSRR vs Frequency and V_{OUT} with Bias



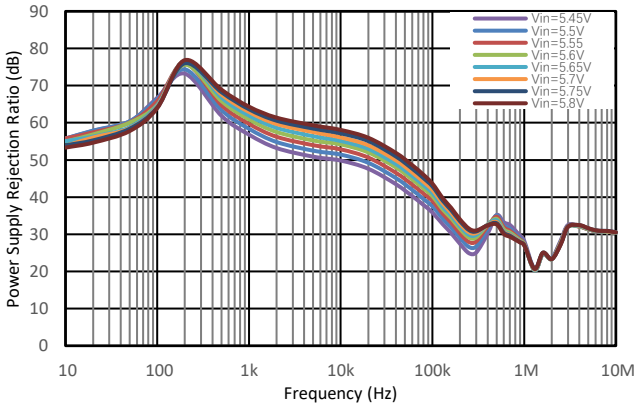
I_{OUT} = 3A, C_{OUT} = 47µF || 10µF || 10µF, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF

Figure 7-6. PSRR vs Frequency and V_{IN} (V_{OUT} = 3.3V)



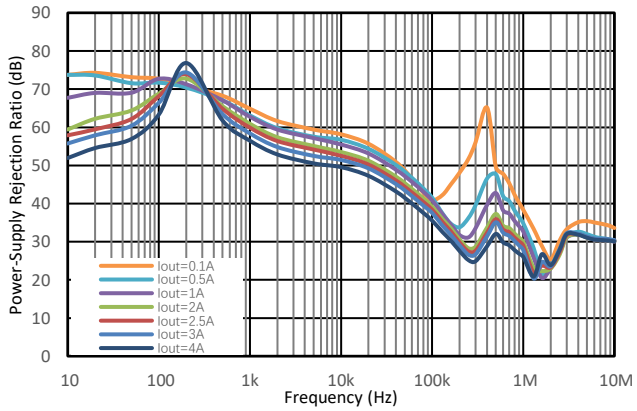
V_{IN} = 1.4V, V_{BIAS} = 5V, V_{OUT} = 1V, I_{OUT} = 3A, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF

Figure 7-7. PSRR vs Frequency and C_{OUT}



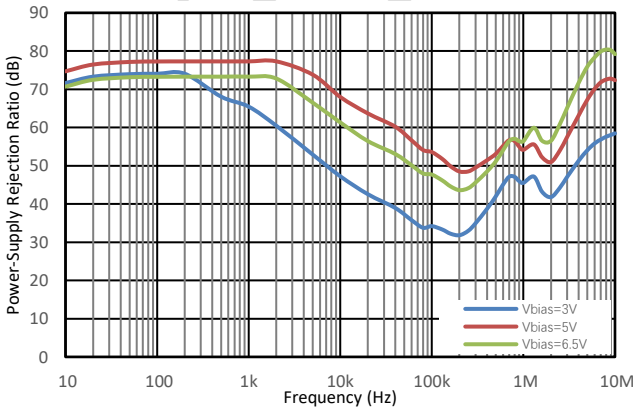
V_{OUT} = 5V, I_{OUT} = 3A, C_{OUT} = 47µF || 10µF || 10µF, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF

Figure 7-8. PSRR vs Frequency and V_{IN} (V_{OUT} = 5V)



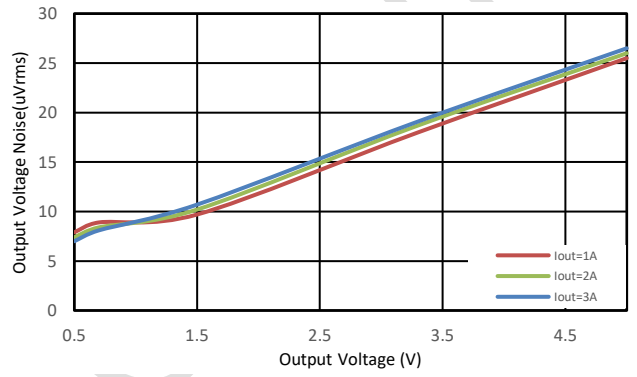
V_{IN} = 5.5V, V_{OUT} = 5V, I_{OUT} = 3A, C_{OUT} = 47µF || 10µF || 10µF, $C_{NR/SS}$ = 10nF, C_{FF} =10 nF

Figure 7-9. PSRR vs Frequency and I_{OUT} (V_{OUT} = 5V)



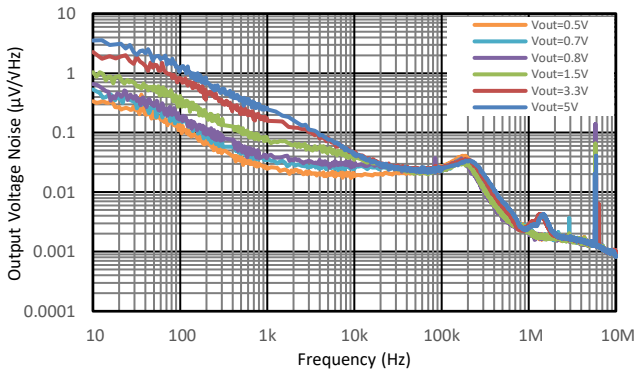
V_{IN} = V_{OUT} + 0.3V, V_{OUT} = 1V, I_{OUT} = 3A, C_{OUT} = 47µF || 10µF || 10µF, $C_{NR/SS}$ =10 nF, C_{FF} =10 nF

Figure 7-10. V_{BIAS} PSRR vs Frequency



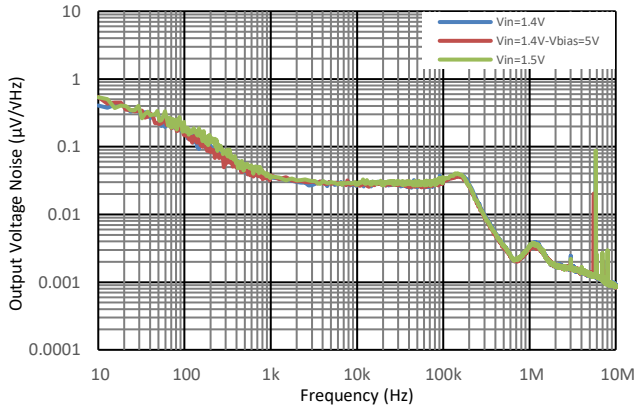
V_{IN} = V_{OUT} + 0.3V or V_{IN} = 1.1V (whichever is greater), V_{BIAS} = 5V for V_{IN} ≤ 2.2V, C_{OUT} = 47µF || 10µF || 10µF, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF, RMS noise BW = 10Hz to 100kHz

Figure 7-11. Output Voltage Noise vs V_{OUT}



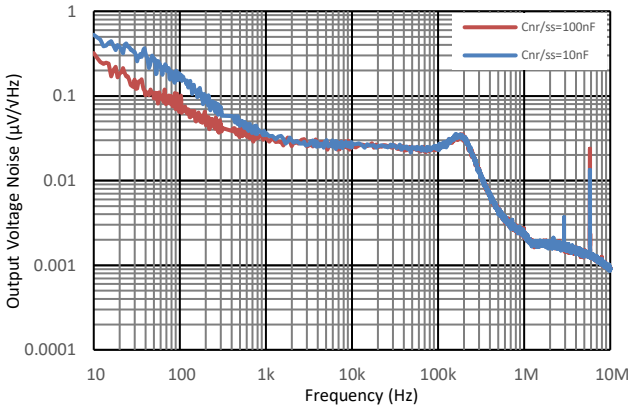
V_{IN} = V_{OUT} + 0.3V or V_{IN} = 1.1V (whichever is greater), V_{BIAS} = 5V for V_{IN} ≤ 2.2V, I_{OUT} = 3A, C_{OUT} = 47µF || 10µF || 10µF, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF

Figure 7-12. Output Noise vs Frequency and V_{OUT}



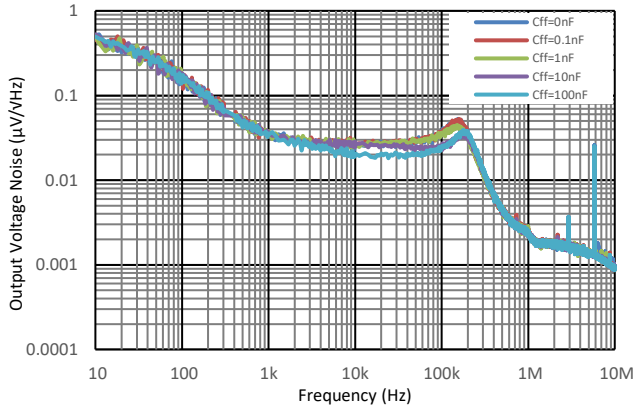
V_{OUT} = 0.7V, I_{OUT} = 3A, C_{OUT} = 47μF || 10μF || 10μF, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF

Figure 7-13. Output Noise vs Frequency and V_{IN}



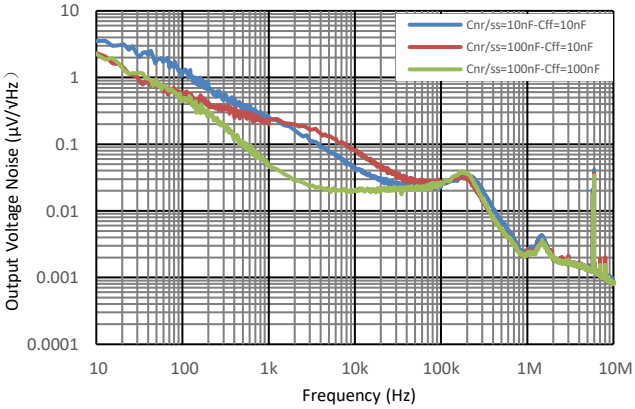
V_{OUT} = 0.7V, V_{IN} = 1.1V, V_{BIAS} = 5V, I_{OUT} = 3A, C_{OUT} = 47μF || 10μF || 10μF, C_{FF} = 10nF

Figure 7-14. Output Noise vs Frequency and $C_{NR/SS}$



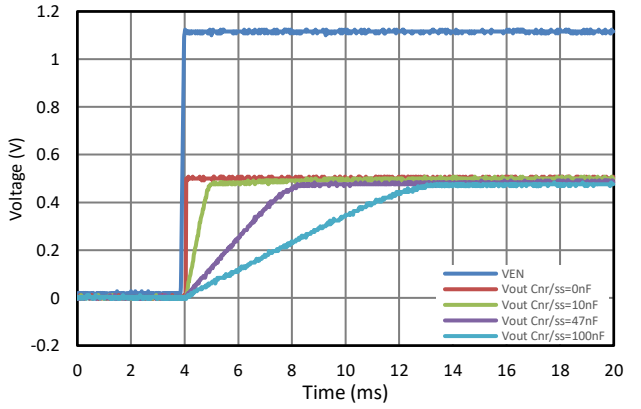
V_{OUT} = 0.7V, V_{IN} = 1.1V, V_{BIAS} = 5V, I_{OUT} = 3A, C_{OUT} = 47μF || 10μF || 10μF, $C_{NR/SS}$ = 10nF

Figure 7-15. Output Noise vs Frequency and C_{FF}



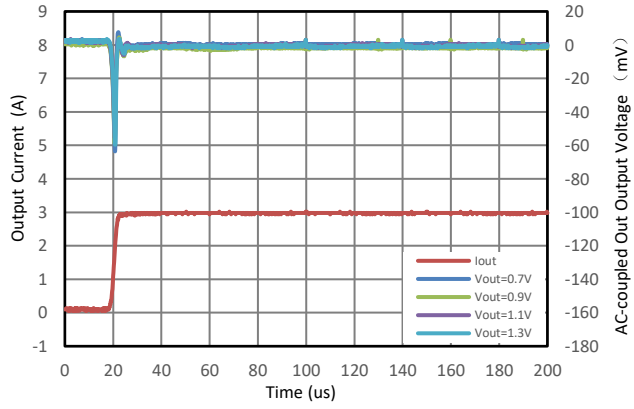
V_{IN} = V_{OUT} + 0.3V, V_{BIAS} = 5V, I_{OUT} = 3A, C_{OUT} = 47μF || 10μF || 10μF, C_{FF} = 10nF

Figure 7-16. Output Noise at 5-V Output



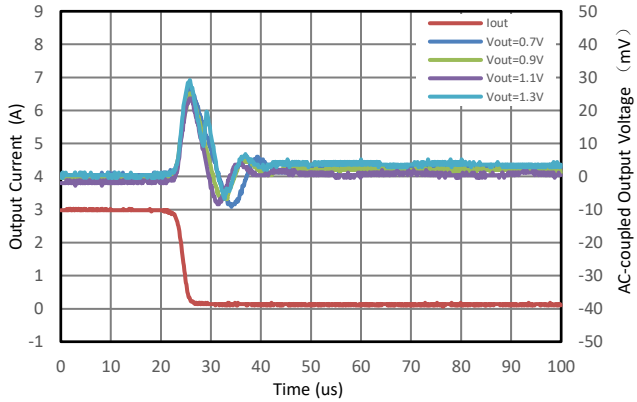
V_{IN} = 1.2V, V_{OUT} = 0.9V, V_{BIAS} = 5V, I_{OUT} = 3A, C_{OUT} = 47μF || 10μF || 10μF, C_{FF} = 10nF

Figure 7-17. Start-Up Waveform vs Time and $C_{NR/SS}$



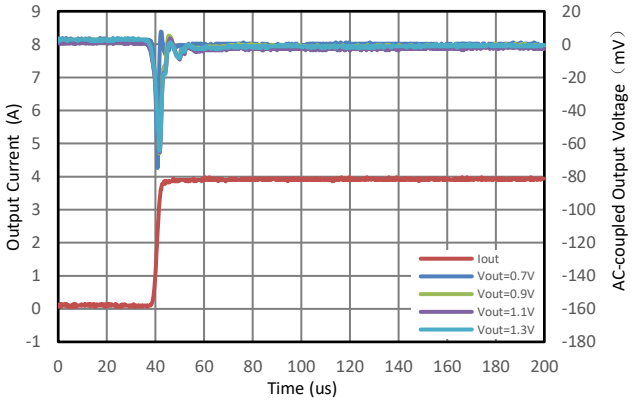
V_{IN} = V_{OUT} + 0.5V, V_{BIAS} = 5V, I_{OUT_DC} = 100mA - 3A, slew rate = 1A/μs, $C_{NR/SS}$ = C_{FF} = 10nF, C_{OUT} = 10μF || 10μF

Figure 7-18. Load Transient vs Time and V_{OUT} With Bias



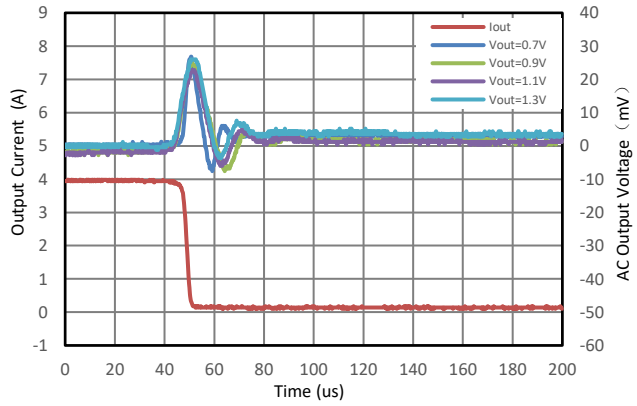
V_{IN} = V_{OUT} + 0.5V, V_{BIAS} = 5V, I_{OUT_DC} = 3A – 100mA, slew rate = 1A/µs, $C_{NR/SS}$ = C_{FF} = 10nF, C_{OUT} = 10µF || 10µF

Figure 7-19. Load Transient vs Time and V_{OUT} With Bias



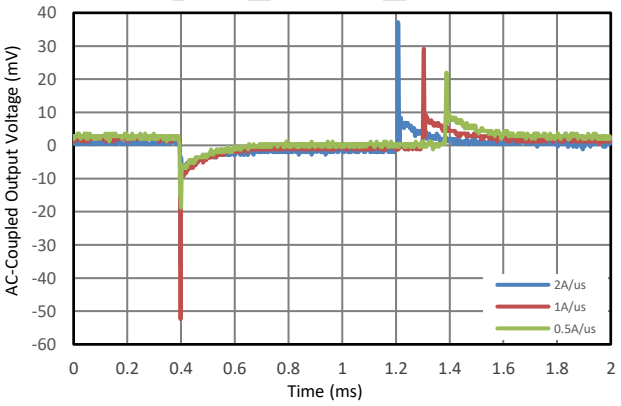
V_{IN} = V_{OUT} + 0.5V, V_{BIAS} = 5V, I_{OUT_DC} = 100mA - 4A, slew rate = 1A/µs, $C_{NR/SS}$ = C_{FF} = 10nF, C_{OUT} = 10µF || 10µF

Figure 7-20. Load Transient vs Time and V_{OUT} With Bias



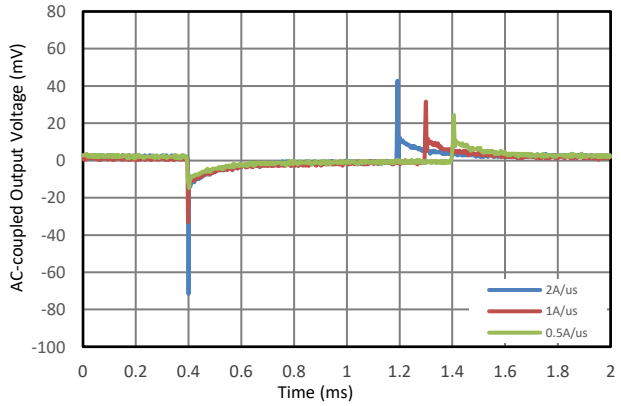
V_{IN} = V_{OUT} + 0.5V, V_{BIAS} = 5V, I_{OUT_DC} = 4A – 100mA, slew rate = 1A/µs, $C_{NR/SS}$ = C_{FF} = 10nF, C_{OUT} = 10µF || 10µF

Figure 7-21. Load Transient vs Time and V_{OUT} With Bias



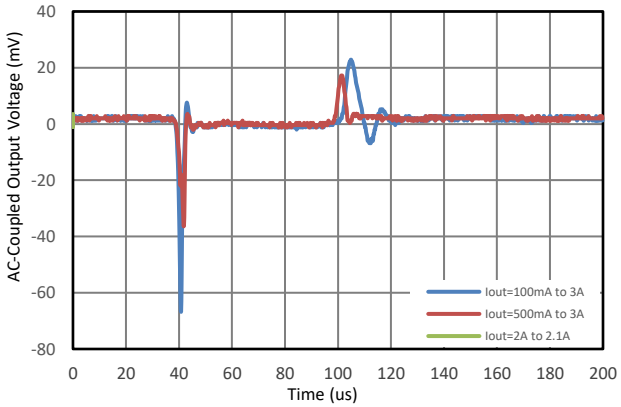
V_{OUT} = 5V, I_{OUT} = 100mA – 3A, I_{OUT} = 100mA to 3A, C_{OUT} = 10µF || 10µF, $C_{NR/SS}$ = C_{FF} = 10nF

Figure 7-22. Load Transient vs Time and Slew Rate



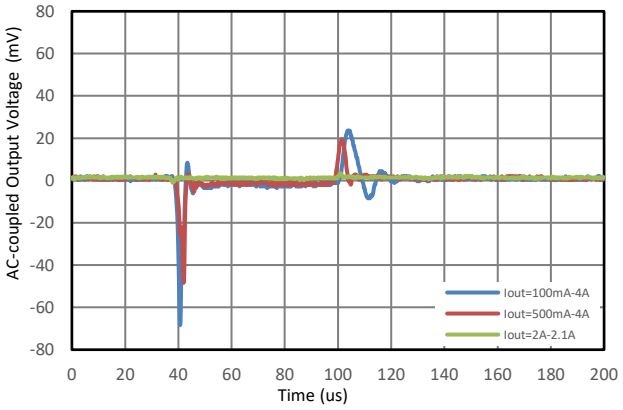
V_{OUT} = 5V, I_{OUT} = 100mA – 4A, I_{OUT} = 100mA to 4A, C_{OUT} = 10µF || 10µF, $C_{NR/SS}$ = C_{FF} = 10nF

Figure 7-23. Load Transient vs Time and Slew Rate



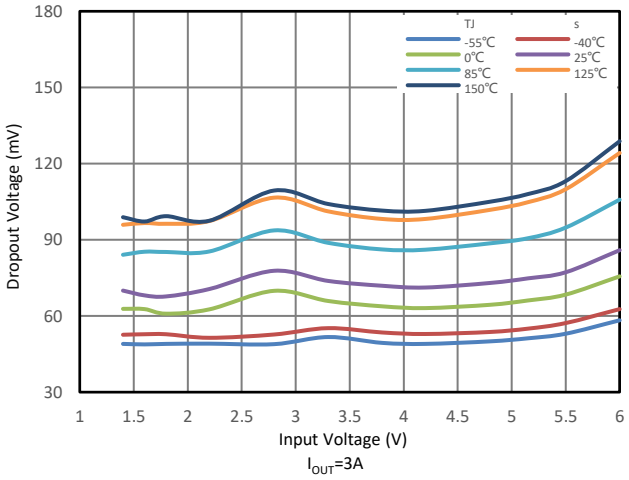
V_{IN} = 1.2V, V_{BIAS} = 5V, C_{OUT} = 10µF || 10µF, V_{OUT} = 0.9V, $C_{NR/SS}$ = C_{FF} = 10nF, slew rate = 1A/µs

Figure 7-24. Load Transient vs Time and DC Load



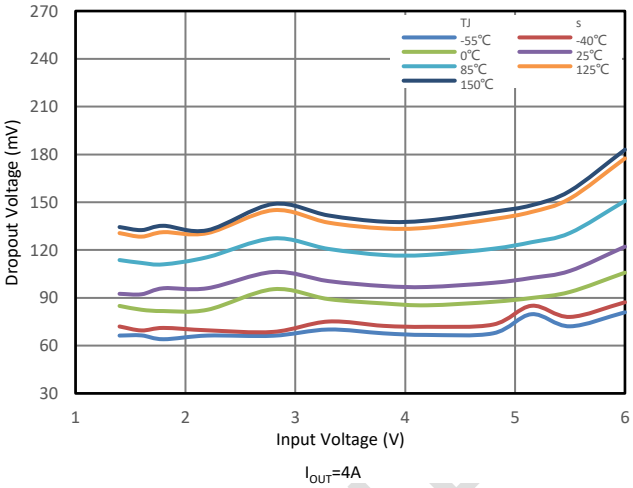
V_{IN} = 1.2V, V_{BIAS} = 5V, C_{OUT} = 10μF || 10μF, V_{OUT} = 0.9V,
$C_{NR/SS}$ = C_{FF} = 10nF, slew rate = 1A/μs

Figure 7-25. Load Transient vs Time and DC Load



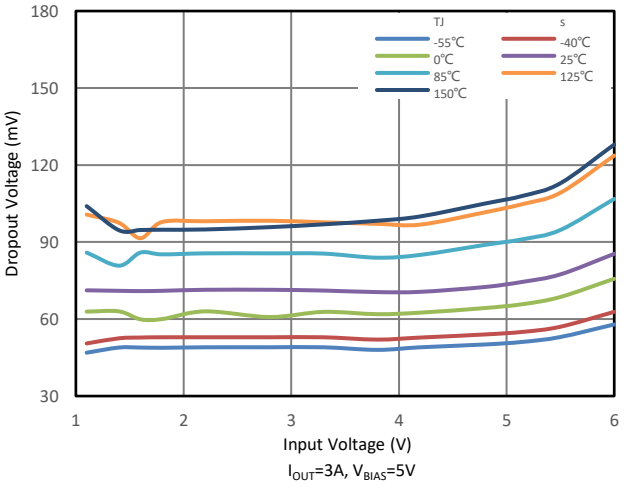
I_{OUT}=3A

Figure 7-26. Dropout Voltage vs V_{IN} Without Bias



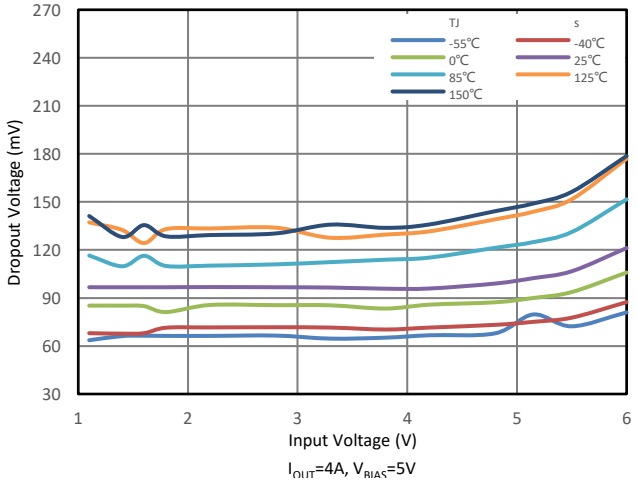
I_{OUT}=4A

Figure 7-27. Dropout Voltage vs V_{IN} Without Bias



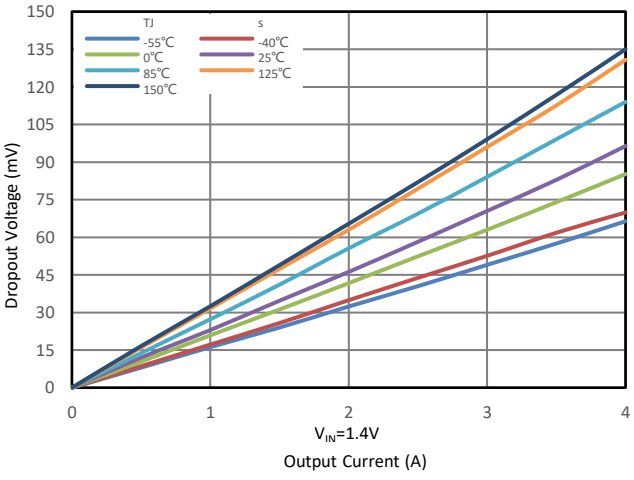
I_{OUT}=3A, V_{BIAS}=5V

Figure 7-28. Dropout Voltage vs V_{IN} With Bias



I_{OUT}=4A, V_{BIAS}=5V

Figure 7-29. Dropout Voltage vs V_{IN} With Bias



V_{IN}=1.4V

Figure 7-30. Dropout Voltage vs I_{OUT} Without Bias

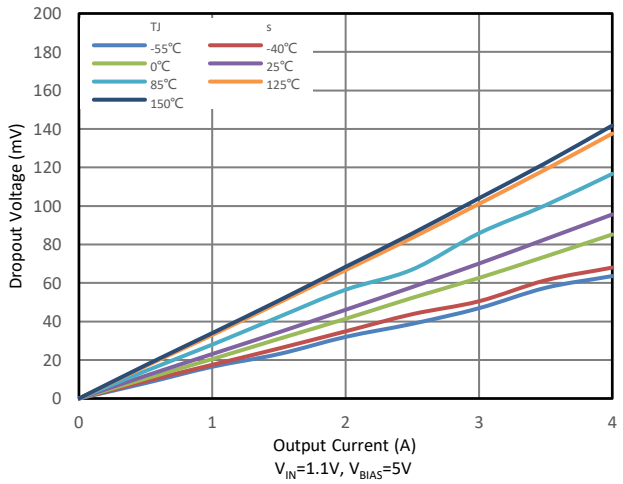


Figure 7-31. Dropout Voltage vs I_{OUT} With Bias

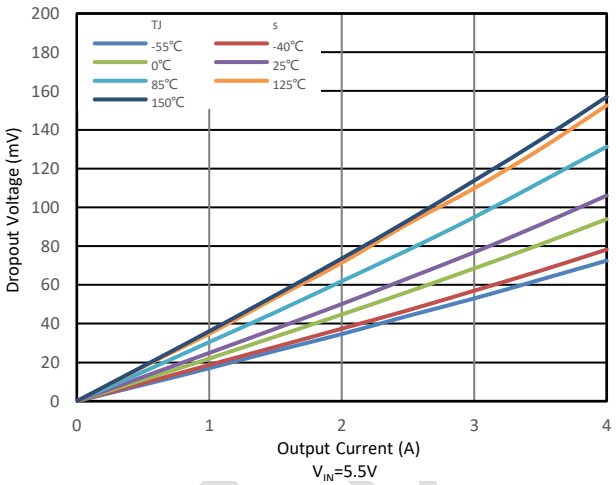


Figure 7-32. Dropout Voltage vs I_{OUT}

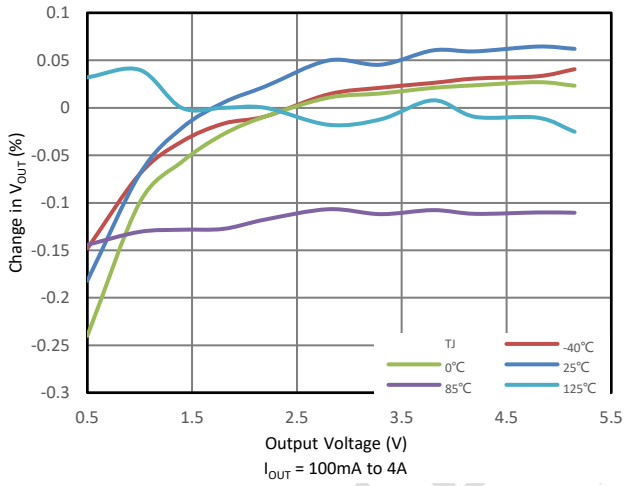


Figure 7-33. Load Regulation vs V_{OUT}

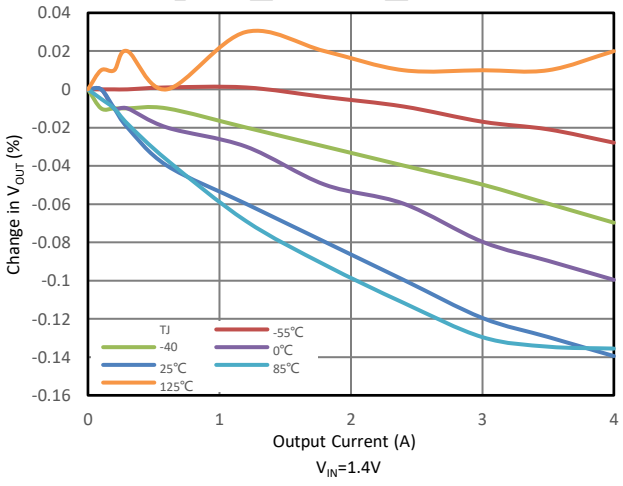


Figure 7-34. Load Regulation vs I_{OUT}

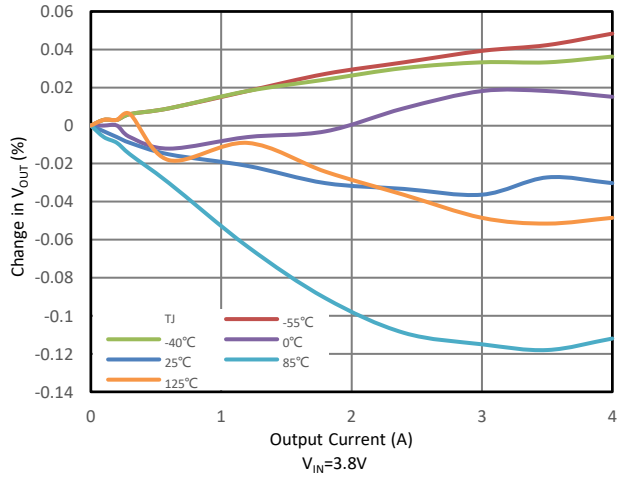


Figure 7-35. Load Regulation vs I_{OUT} (3.3-V Output)

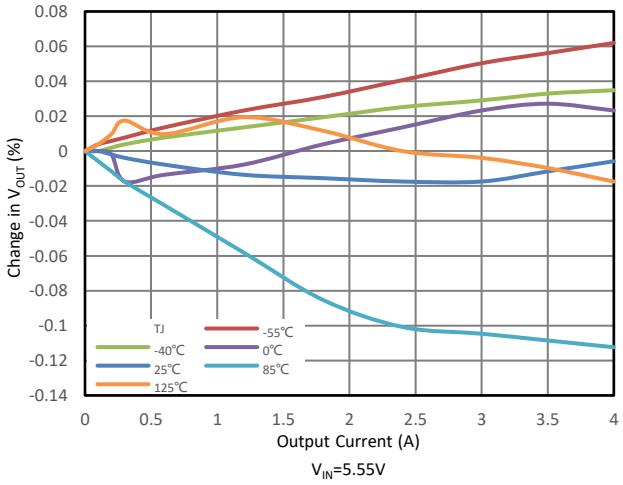
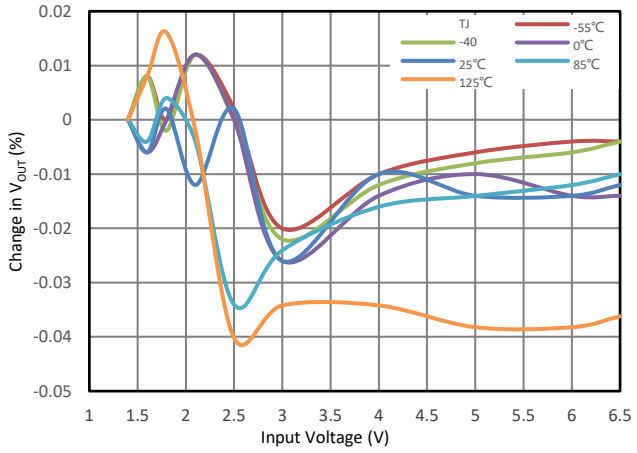
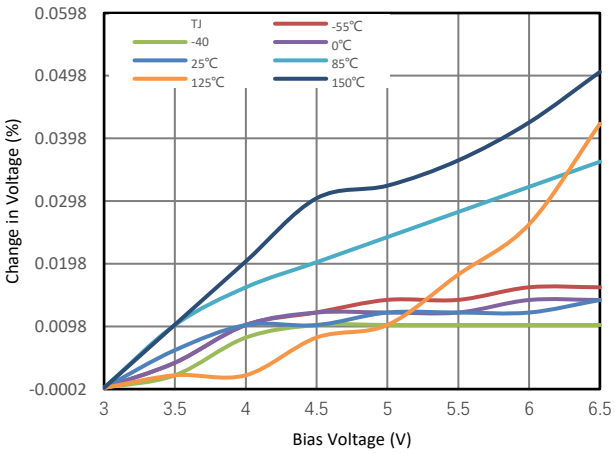


Figure 7-36. Load Regulation vs I_{OUT} (5.15-V Output)



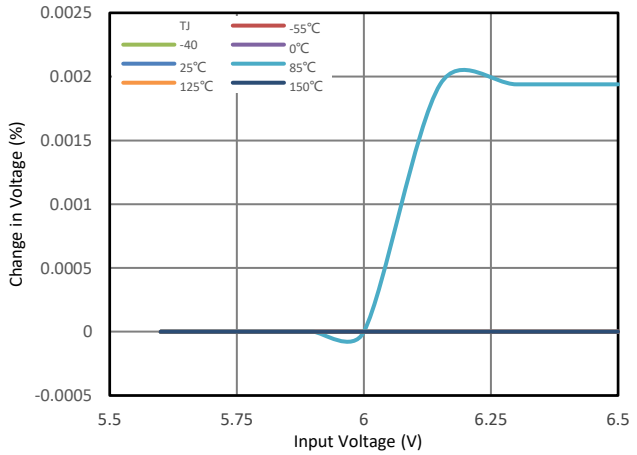
V_{OUT}=0.5V， I_{OUT}=5mA

Figure 7-37. Line Regulation vs V_{IN}



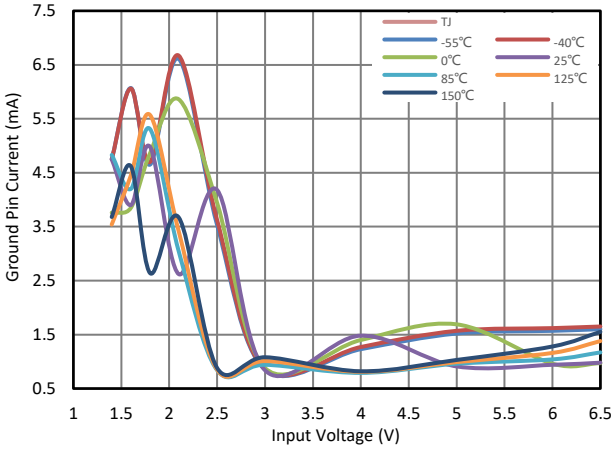
V_{IN}=1.1V, V_{OUT}=0.5V, I_{OUT}=5mA

Figure 7-38. Line Regulation vs V_{BIAS}



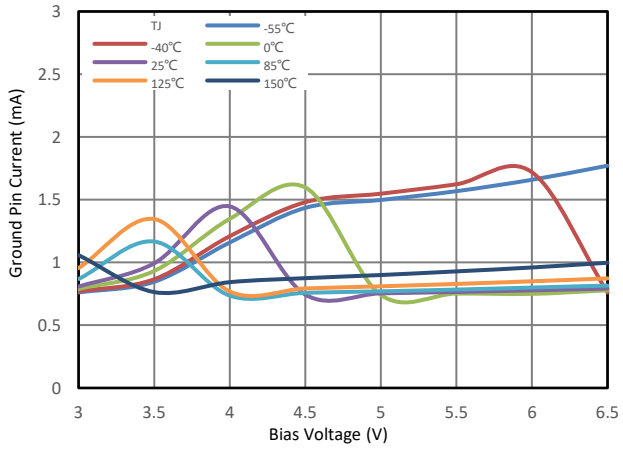
I_{OUT} = 5mA

Figure 7-39. Line Regulation vs V_{IN} (5.15-V Output)



V_{BIAS}=0V， I_{OUT}=5mA

Figure 7-40. Ground Pin Current vs V_{IN}



V_{IN}=1.1V, V_{OUT}=0.5V, I_{OUT}=5mA

Figure 7-41. Bias Pin Current vs V_{BIAS}

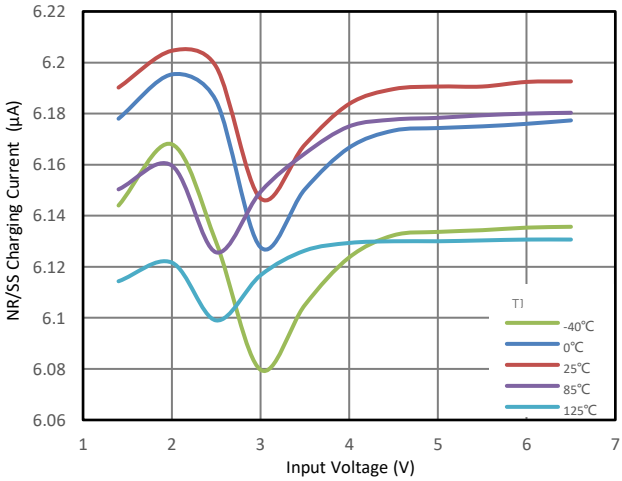


Figure 7-42. $I_{NR/SS}$ Current vs V_{IN}

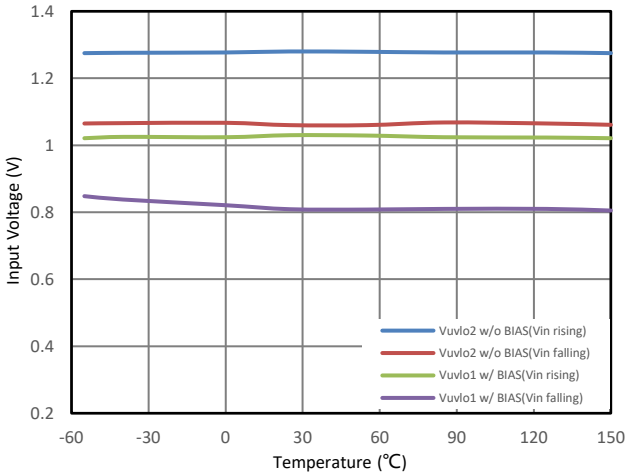


Figure 7-43. V_{IN} UVLO vs Temperature

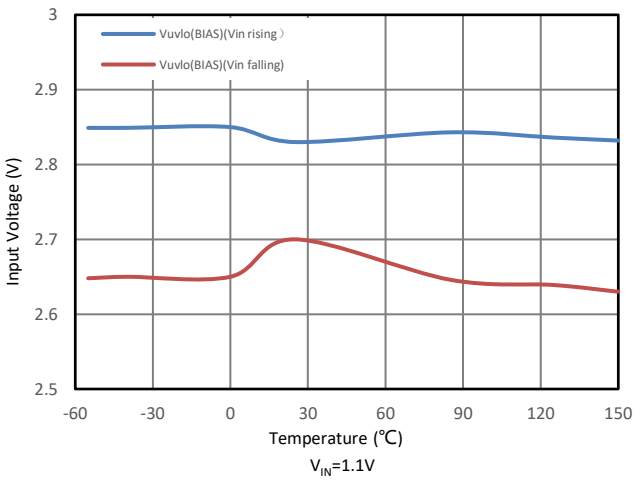


Figure 7-44. V_{BIAS} UVLO vs Temperature

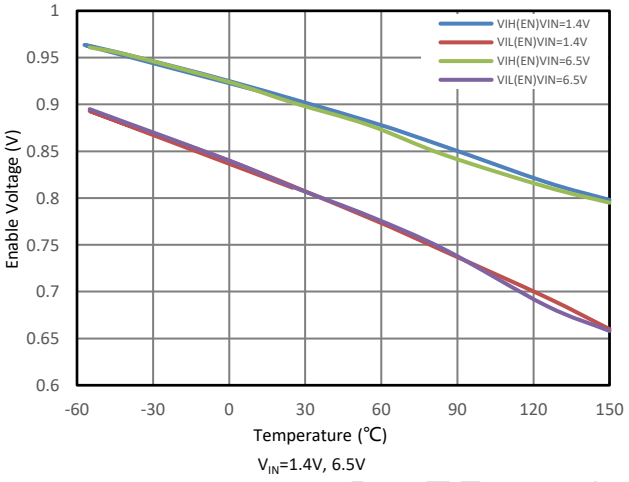


Figure 7-45. Enable Threshold vs Temperature

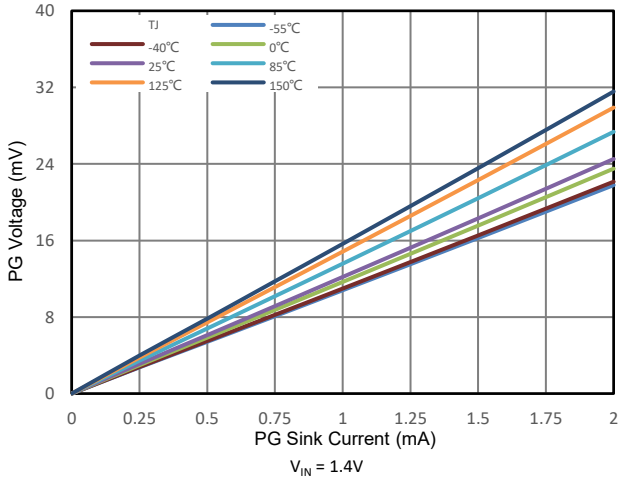


Figure 7-46. PG Voltage vs PG Current Sink

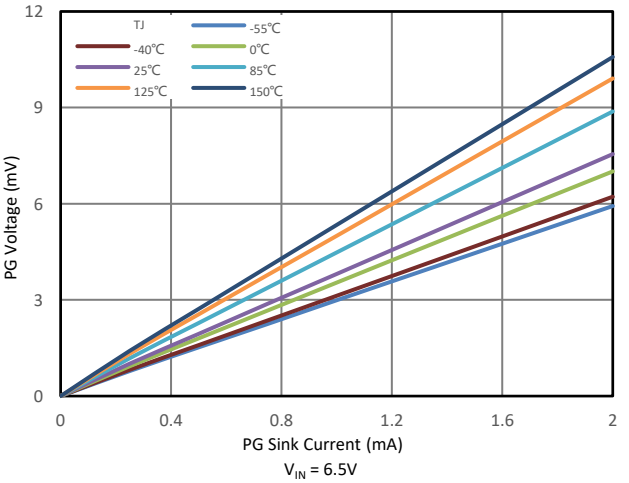


Figure 7-47. PG Voltage vs PG Current Sink

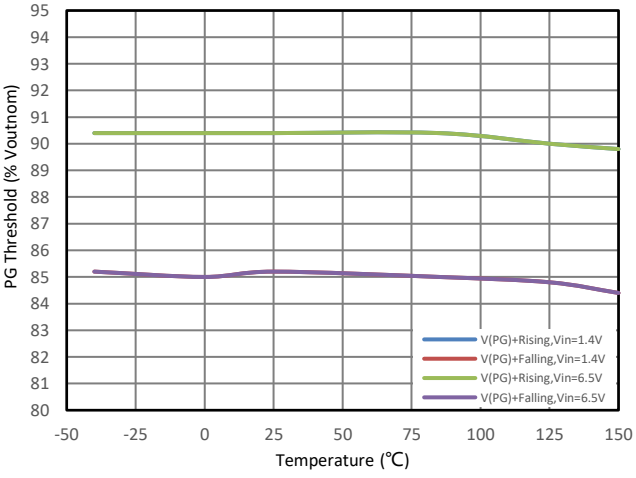


Figure 7-48. PG Threshold vs Temperature

8 FUNCTIONAL BLOCK DIAGRAM

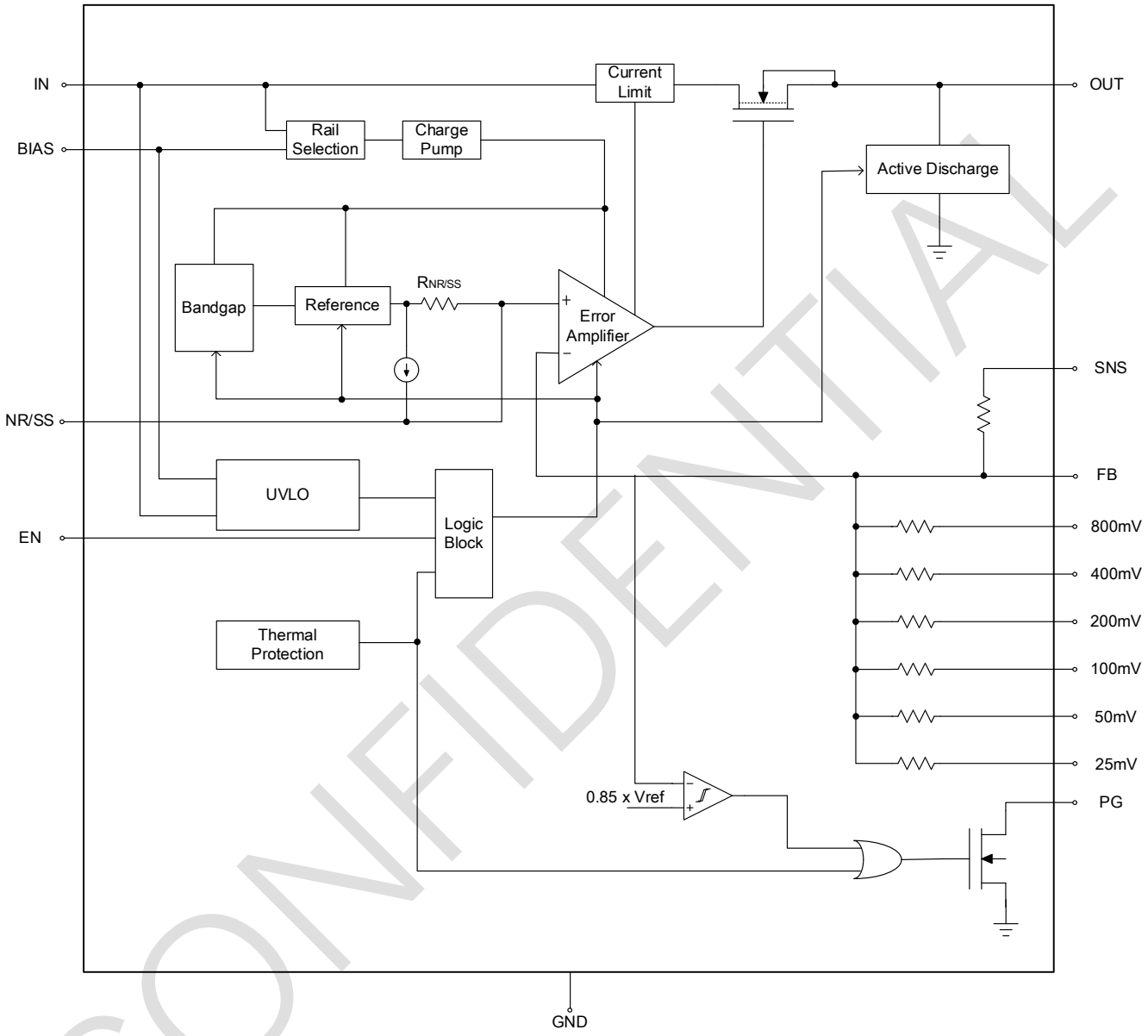


Figure 8-1. GBI5130 Block Diagram

9 DETAILED DESCRIPTION

9.1 Overview

GBI5130 is a high current (4A) low noise (7μVrms) high accuracy (1%) low-dropout linear voltage regulator (LDO) with maximum 160mV dropout voltage. The features make the device a robust solution for the application requirement of clean accurate power supply.

GBI5130 has several features that make the device useful in a variety of applications. As detailed in the functional Block Diagram section, the features include:

- Low noise, high PSRR output
- Flexible output voltage setting with internal resistor network
- Optional bias rail
- Power-good output
- Programmable soft-start
- Foldback current limit
- Enable function
- Active discharge
- Thermal protection

9.2 Feature Description

9.2.1 Low Noise, High PSRR output

GBI5130 includes a low noise reference and error amplifier ensuring minimal noise during operation. The NR/SS capacitor ($C_{NR/SS}$) and feed-forward capacitor (C_{FF}) are the easiest way to reduce device noise. $C_{NR/SS}$ filters the noise from the reference and C_{FF} filter the noise from the error amplifier. The noise contribution from the charge pump is minimal. The overall noise of the system at low output voltages can be reduced by using a bias rail because this rail provides more headroom for internal circuitry.

The high-power supply rejection ratio (PSRR) of GBI5130 ensures minimal coupling of input supply noise to the output. The PSRR performance is primarily results from a high bandwidth, high gain error amplifier.

9.2.2 Programmable fixed output voltage

An internal feedback resistance network is integrated, allowing GBI5130 output voltage to be programmed easily between 0.5V and 2.075V with 25mV step by tying the related program pins to ground. Tying the program pins to SNS increases the resolution but limits the range of the output voltage because the effective value of R1 is decreased.

9.2.3 Bias Rail

GBI5130 features a bias rail to enable low-input voltage, low-output voltage (LILO) operation by providing power to the internal circuitry of the device. The bias rail is required for operation with V_{IN}<1.4V.

An internal power MUX supplies the greater of either the input voltage or the bias voltage to an internal charge pump to power the internal circuitry. Unlike other LDOs that have a bias supply, GBI5130 does not have a minimum bias voltage with respect to the input supply because an internal charge pump is used instead.

9.2.4 Power-Good Function

The power-good circuits monitor the voltage at the feedback pin to indicate the status of the output voltage. When the feedback pin voltage falls below the PG threshold voltage (typically 85% of the reference voltage, 0.5V), the PG pin open drain output engages and pulls the PG pin close to GND. When the feedback voltage exceeds the $V_{IT(PG)}$ threshold by an amount greater than $V_{HYS(PG)}$ (typically 6%), the PG pin becomes high impedance. By connecting a pullup resistor to an external supply, any downstream device can receive power good as a logic signal that can be used for sequencing. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device or devices.

The use of a feed-forward capacitor (C_{FF}) can cause glitches on start-up, and the power-good circuit may not function normally below the minimum input supply range.

9.2.5 Programmable soft-start

Soft-start refers to the ramp-up time of the output voltage during LDO turn-on after EN and UVLO exceed the respective threshold voltages. The noise-reduction capacitor ($C_{NR/SS}$) serves dual purpose of both governing output noise reductor and programming the soft-start ramp time during turn-on. The start-up ramp is monotonic.

The majority of the ramp is linear; however, there is offset voltage in the error amplifier that can cause a small initial jump in output voltage.

9.2.6 Internal current limit

The internal current limit circuit is used to protect the LDO against high load current faults or shorting events. During a current-limit event, the LDO source constant current, therefore, the output voltage falls with decreased load impedance. Thermal shutdown can activate during a current limit event because of the high-power dissipation typically found in these conditions. To ensure proper operation of the current limit, minimize the inductance to the input and load. When LDO output voltage is lower than 170mV, the constant current is folded back to 2.4A, typically.

If $V_{OUT} > V_{IN} + 0.3V$, then reverse current can flow from the output to the input. The reverse current can cause damage to the device; therefore, limit this reverse current to 10% of the rated output current of the device.

9.2.7 Enable

The enable pin is active high. The output is turned on when the enable pin voltage is greater than its rising voltage threshold (1.1V) and the output is turned off when the enable pin voltage is less than its falling

voltage threshold (0.5V). a voltage less than 0.5V on the enable pin disables all the internal circuits. At the next turn-on this voltage ensures a normal start-up waveform with in-rush control, provided there is enough time to discharge the output capacitance.

9.2.8 Active discharge

GBI5130 has an internal pulldown MOSFET that connects a resistance of several hundred ohms to ground when the device is disabled to actively discharge the output voltage.

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can possibly flow from the output to the input. This reverse current flow can cause damage to the device. Limit reverse current to no more than 10% of the device rated current for a short period of time.

9.2.9 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuits monitor the input and bias voltage (V_{IN} and V_{BIAS}, respectively) to prevent the device from turning on before V_{IN} and V_{BIAS} rise above the lockout voltage. The UVLO circuits also disables the output of the device when V_{IN} or V_{BIAS} fall below the lockout voltage. The UVLO circuit responds quickly to glitches on V_{IN} or V_{BIAS} and attempt to disable the output of the device if either of these rail' s collapse. As a result of the fast response time of the input supply UVLO circuits, fast and short line transients well below the input supply UVLO falling threshold can cause momentary glitches when asserted or when recovered from the transient.

9.2.10 Thermal protection

A thermal shutdown circuit is integrated to disable the device when thermal junction temperature (T_j) of the main pass-FET exceeds 160℃ (typical). Thermal shutdown hysteresis assures that the LDO turns on when the temperature falls to 140℃ (typical). The thermal time-constant of the semiconductor die is fairly short, and thus the device cycles on and off when thermal shutdown is reached until the power dissipation is reduced.

For reliable operation, limit the junction temperature to a maximum of 125℃. Operation above 125℃ can cause the device to exceed its operational specifications. Although the internal protection circuitry of GBI5130 is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running GBI5130 into thermal shutdown or above a junction temperature of 125℃ reduces long-term reliability.

10 Application and Implementation

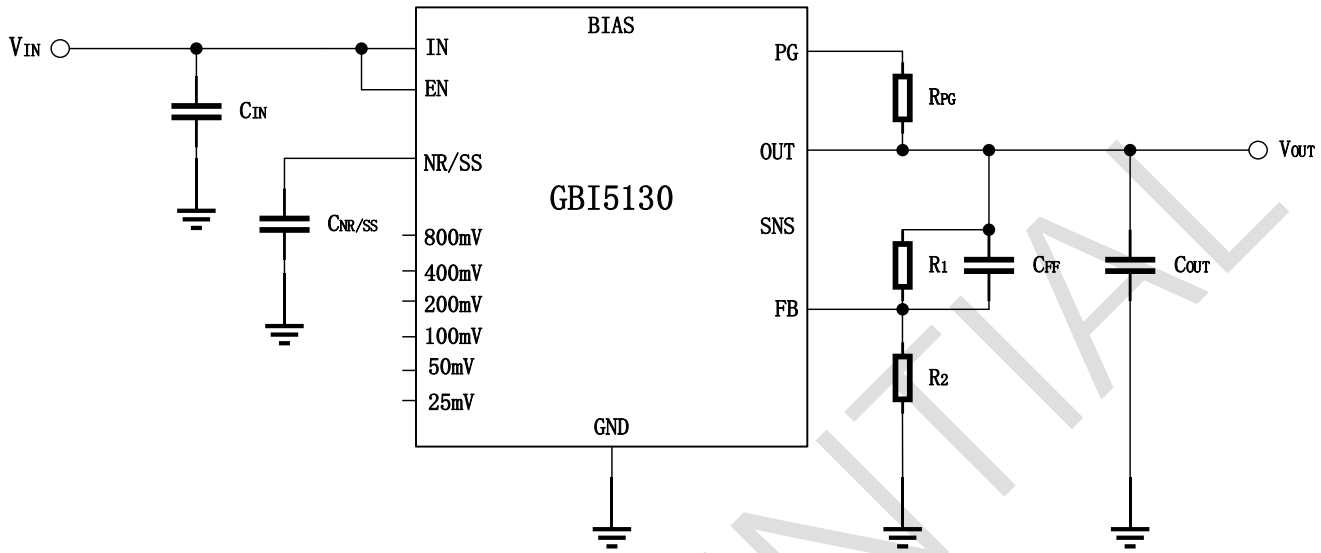


Figure 10-1 Adjustable Operation

10.1 Application Information

GBI5130 is a linear voltage regulator with an input range of 1.1V to 6.5V and an output voltage range of 0.5V to 5.15V with 1% accuracy and 4A maximum output current. GBI5130 has an integrated charge pump for ease of use and external bias rail to allow for the lowest dropout across the entire output voltage range.

10.1.1 Recommended Capacitor Types

GBI5130 is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input, output, and noise-reduction pin (NR/SS pin 13). Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgement. Ceramic capacitors that employ X7R, X5R and COG rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, ceramic capacitance varies with operating voltage and temperature. As a rule of thumb, derate ceramic capacitors by at least 50%. The input and output capacitors recommended herein account for a capacitance derating of approximately 50%, but at high V_{IN} and V_{OUT} conditions (that is, V_{IN}=5.5V to V_{OUT}=5.0V) the derating can be greater than 50% and must be taken into consideration.

10.1.1.1 Input and Output Capacitor Requirements (C_{IN} and C_{OUT})

GBI5130 is designed and characterized for operation with ceramic capacitors of 22uF or greater at the output and 10uF or greater at the input. Using at least a 22uF capacitor is highly recommended at the input to minimize input impedance. Place the input and output capacitors as near as practical to the respective input and output pins to minimize trace parasitic. If the trace inductance from the input supply to GBI5130 is high, a fast current transient can cause V_{IN} to ring above the absolute maximum voltage rating and damage the device. This situation can be mitigated by additional input capacitors to dampen the ringing and to keep it below the device absolute maximum ratings.

A combination of multiple output capacitors boosts the high-frequency PSRR, as illustrated in several of the PSRR curves. The combination of one 0805-sized, 22uF ceramic capacitor in parallel with two 0805-sized, 10uF ceramic capacitors with a sufficient voltage rating in conjunction with the PSRR boost circuit optimizes PSRR for the frequency range of 400kHz to 700kHz, a typical range for dc-dc supply switching frequency. This 22uF||10uF||10uF combination also ensures that at high input voltage and high output voltage configurations, the minimum effective capacitance is met. Many 0805-sized, 22uF ceramic capacitors have a voltage derating of approximately 60% to 80% at 5V, so the addition of two 10uF capacitors ensures that the capacitance is at or above 22uF.

10.1.1.2 Noise-Reduction and Soft-Start Capacitor ($C_{NR/SS}$)

GBI5130 features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor ($C_{NR/SS}$). The use of an external $C_{NR/SS}$ is highly recommended, especially to minimize in-rush current into the output capacitors. This soft-start eliminates power-up initialization problems when powering field-programmable gate arrays (FPGA), digital signal processors (DSPs), or other processors. The controlled voltage ramp of the output also reduces peak in-rush current during start-up, minimizing start-up transients to the input power bus.

To achieve a monotonic start-up, GBI5130 error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage approaches the internal reference. The soft-start ramp time depends on the soft-start charging current ($I_{NR/SS}$), the soft-start capacitance ($C_{NR/SS}$) and the internal reference ($V_{NR/SS}$). Soft-start ramp time can be calculated with Equation 1:

$$Tss = (V_{NR/SS} \times C_{NR/SS})/I_{NR/SS} \quad (1)$$

Note that $I_{NR/SS}$ is 6μA typically.

The noise-reduction capacitor, in conjunction with the noise-reduction resistor, forms a low-pass filter (LPF) that filters out the noise from the reference before being gained up with the error amplifier, thereby reducing the device noise floor. The LPF is a single-pole filter and the cutoff frequency can be calculated with Equation 2. The typical value of R_{NR} is 200kΩ. Increasing the $C_{NR/SS}$ capacitor has a greater impact because the output voltage increases when the noise from the reference is gained up even more at higher output voltages. For low-noise applications, a 10-nF to 1-uF $C_{NR/SS}$ is recommended.

$$F_{cutoff} = 1/(2 \times \pi \times R_{NR} \times C_{NR/SS}) \quad (2)$$

10.1.1.3 Feed-Forward Capacitor (C_{FF})

Although a feed-forward capacitor (C_{FF}) from the FB pin to the OUT pin is not required to achieve stability, a 10-nF external feed-forward capacitor optimizes the transient, noise, and PSRR performance. A higher capacitance C_{FF} can be used; however, the start-up time is longer and the power-good signal can incorrectly indicate that the output voltage is settled.

10.1.1.4 Soft-Start and In-Rush Current

Soft-start refer to the ramp-up characteristics of the output voltage during LDO turn-on after EN and UVLO achieve threshold voltage. The noise-reduction capacitor serves a dual purpose of both governing output noise reduction and programming the soft-start ramp during turn-on.

In-rush current is defined as the current into the LDO at the IN pin during start-up. In-Rush current then consists primarily of the sum of load current and the current used to charge the output capacitor. This current is difficult to measure because the input capacitor must be removed, which is not recommended. However, this soft-start current can be estimated by Equation 3:

$$I_{OUT(t)} = \frac{COUT * dVOUT(T)}{dt} + \frac{VOUT(t)}{Rload} \quad (3)$$

Where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turn-on ramp
- $dV_{OUT}(t)/dt$ is the slope of the VOUT ramp
- Rload is the resistive load impedance

10.1.1.5 Optimizing Noise and PSRR

The ultra-low noise floor and PSRR of the device can be improved by careful selection of:

- $C_{NR/SS}$ for the low-frequency range
- C_{FF} in the mid-band frequency range
- C_{OUT} for the high-frequency range
- $V_{IN} – V_{OUT}$ for all frequencies, and
- V_{BIAS} at lower input voltages

A larger noise-reduction capacitor improves low-frequency PSRR by filtering any noise coupling from the input into the reference. The feed-forward capacitor can be optimized to place a pole-zero pair near the edge of the loop bandwidth and push out the loop bandwidth, thus improving mid-band PSRR. Larger output capacitors and various output capacitors can be used to improve high-frequency PSRR.

A higher input voltage improves the PSRR by giving the device more headroom to respond to noise on the input. A bias rail also improves the PSRR at lower input voltages because greater headroom is provided for the internal circuits.

The noise-reduction capacitor filters out low-frequency output voltage noise. Additionally, a bias rail or higher input voltage improves the noise because greater headroom is provided for the internal circuits.

Below table lists the output voltage noise for the 10Hz to 100kHz band at a 5V output for a variety of conditions with an input voltage of 5.4V, an R1 of 12.1 kΩ, and a load current of 4A. The 5V output is chosen because this output is the worst-case condition for output voltage noise.

Table 10-1 Output Noise Voltage at a 5V Output

OUTPUT VOLTAGE NOISE (μVRMS) (10Hz-100kHz)	$C_{NR/SS}$(nF)	C_{FF}(nF)	C_{OUT}(μF)
26.5	10	10	47||10||10
17.1	100	10	47||10||10
11.9	100	100	47||10||10

10.1.1.6 Programmable Output Voltage

As with the adjustable operation, the output voltage is set according to Equation 4 except that R_1 AND R_2 are internally integrated and matched for higher accuracy. This resistive network must provide a current equal to or greater than 5 μA for dc accuracy.

$$V_{OUT} = V_{NR/SS} \times (1 + R_1/R_2) \quad (4)$$

10.1.1.7 ANY-OUT Programmable Output Voltage

GBI5130 can use either external resistors or the internally-matched flexible programmable feedback resistor network to set output voltage. The resistors are accessible via pin 2 and pins 5 to 11 and are used to program the regulated output voltage. Each pin can be connected to ground (active) or left open (floating), or connected to SNS. The programming is set as the sum of the internal reference voltage ($V_{NR/SS}$ =0.5V) plus the accumulated sum of the respective voltages assigned to each active pin; that is, 25mV (pin 5), 50mV (pin 6), 100mV (pin 7), 200mV (pin 9), 400mV (pin 10), or 800mV (pin 11). Table 10-2 summarizes these voltage values associated with each active pin setting for reference. By leaving all program pins open or floating, the output is thereby programmed to the minimum possible output voltage equal to V_{FB}.

$$V_{OUT} = V_{NR/SS} + (\sum \text{flexible program pins to Ground}) \quad (5)$$

Table 10-2 ANY-OUT Programmable Output Voltage

ANY-OUT Program PINs (Active Low)	ADDITIVE OUTPUT VOLTAGE LEVEL
Pin 5	25mV
Pin 6	50mV
Pin 7	100mV
Pin 8	200mV
Pin 9	400mV
Pin 10	800mV

Table 10-3 provides a full list of target output voltages and corresponding pin setting when the flexible programmable pins are only tied to ground left floating. The voltage setting pins have a binary weight; therefore, the output voltage can be programmed to any value from 0.5V to 2.075V in 25-mV steps when tying these pins to ground. There are several alternative ways to set the output voltage. The program pins can be driven using external general-purpose input/output pins (GPIOs), manually connected using 0Ω resistors (or left open), or hardwired by the given layout of the printed circuits board (PCB) to set the voltage.

Table 10-3A User-Configurable Output Voltage Settings

VOUT(NOM) (V)	25mV	50mV	100mV	200mV	400mV	800mV	VOUT(NOM) (V)	25mV	50mV	100mV	200mV	400mV	800mV
0.5	Open	Open	Open	Open	Open	Open	1.3	Open	Open	Open	Open	Open	GND
0.525	GND	Open	Open	Open	Open	Open	1.325	GND	Open	Open	Open	Open	GND
0.55	Open	GND	Open	Open	Open	Open	1.35	Open	GND	Open	Open	Open	GND
0.575	GND	GND	Open	Open	Open	Open	1.375	GND	GND	Open	Open	Open	GND
0.6	Open	Open	GND	Open	Open	Open	1.4	Open	Open	GND	Open	Open	GND
0.625	GND	Open	GND	Open	Open	Open	1.425	GND	Open	GND	Open	Open	GND
0.65	Open	GND	GND	Open	Open	Open	1.45	Open	GND	GND	Open	Open	GND
0.675	GND	GND	GND	Open	Open	Open	1.475	GND	GND	GND	Open	Open	GND
0.7	Open	Open	Open	GND	Open	Open	1.5	Open	Open	Open	GND	Open	GND
0.725	GND	Open	Open	GND	Open	Open	1.525	GND	Open	Open	GND	Open	GND
0.75	Open	GND	Open	GND	Open	Open	1.55	Open	GND	Open	GND	Open	GND
0.775	GND	GND	Open	GND	Open	Open	1.575	GND	GND	Open	GND	Open	GND
0.8	Open	Open	GND	GND	Open	Open	1.6	Open	Open	GND	GND	Open	GND
0.825	GND	Open	GND	GND	Open	Open	1.625	GND	Open	GND	GND	Open	GND
0.85	Open	GND	GND	GND	Open	Open	1.65	Open	GND	GND	GND	Open	GND
0.875	GND	GND	GND	GND	Open	Open	1.675	GND	GND	GND	GND	Open	GND
0.9	Open	Open	Open	Open	GND	Open	1.7	Open	Open	Open	Open	GND	GND
0.925	GND	Open	Open	Open	GND	Open	1.725	GND	Open	Open	Open	GND	GND
0.95	Open	GND	Open	Open	GND	Open	1.75	Open	GND	Open	Open	GND	GND
0.975	GND	GND	Open	Open	GND	Open	1.775	GND	GND	Open	Open	GND	GND
1	Open	Open	GND	Open	GND	Open	1.8	Open	Open	GND	Open	GND	GND
1.025	GND	Open	GND	Open	GND	Open	1.825	GND	Open	GND	Open	GND	GND
1.05	Open	GND	GND	Open	GND	Open	1.85	Open	GND	GND	Open	GND	GND
1.075	GND	GND	GND	Open	GND	Open	1.875	GND	GND	GND	Open	GND	GND
1.1	Open	Open	Open	GND	GND	Open	1.9	Open	Open	Open	GND	GND	GND
1.125	GND	Open	Open	GND	GND	Open	1.925	GND	Open	Open	GND	GND	GND
1.15	Open	GND	Open	GND	GND	Open	1.95	Open	GND	Open	GND	GND	GND
1.175	GND	GND	Open	GND	GND	Open	1.975	GND	GND	Open	GND	GND	GND
1.2	Open	Open	GND	GND	GND	Open	2	Open	Open	GND	GND	GND	GND
1.225	GND	Open	GND	GND	GND	Open	2.025	GND	Open	GND	GND	GND	GND
1.25	Open	GND	GND	GND	GND	Open	2.05	Open	GND	GND	GND	GND	GND
1.275	GND	GND	GND	GND	GND	Open	2.075	GND	GND	GND	GND	GND	GND

10.1.2 VIN Undervoltage Lockout (UVLO)

The UVLO circuits has 200mV hysteresis with bias or 220mV hysteresis without bias input respectively. This function ensures that the device stays disabled before its input or bias supplies reach the minimum operational voltage range, and ensures that the device properly shuts down when either the input or bias supply collapses.

Figure 10-2 and Table 10-4 explain one of the UVLO circuits being triggered to various input voltage events, assuming $V_{EN} \geq V_{IH(EN)}$.

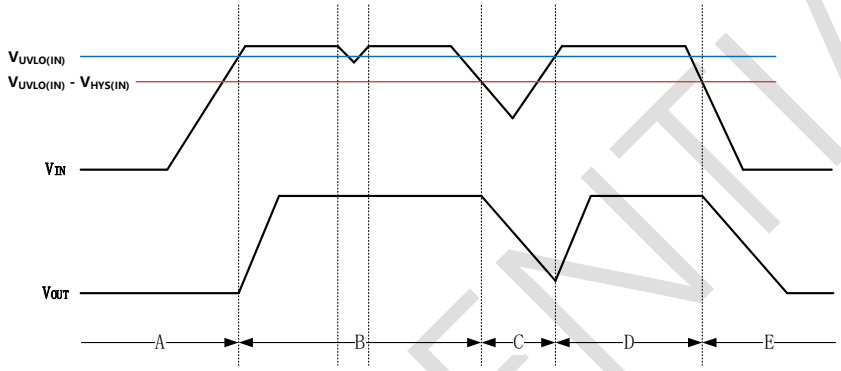


Figure 10-2 Typical UVLO Operation

Table 10-4 Typical UVLO Operation Description

REGION	EVENT	VOUT STATUS	COMMENT
A	Turn on, $V_{IN} \geq V_{UVLO\_1,2(IN)}$ and $V_{BIAS} \geq V_{UVLO(BIAS)}$	OFF	Start up
B	Regulation, $V_{IN} \geq V_{UVLO\_1,2(IN)}$ - $V_{HYS1,2(IN)}$ or $V_{BIAS} \geq V_{UVLO(BIAS)} - V_{HYS(BIAS)}$	ON	Regulates to target V_{OUT}
C	Brownout, $V_{IN} < V_{UVLO\_1,2(IN)} - V_{HYS\_1,2(IN)}$ or $V_{BIAS} \geq V_{UVLO(BIAS)} - V_{HYS(BIAS)}$	OFF	The device is disabled and the output falls because of the load and active discharge circuit.
D	Turn on, $V_{IN} \geq V_{UVLO\_1,2(IN)}$ and $V_{BIAS} \geq V_{UVLO(BIAS)}$	ON	The device is reenabled when the UVLO fault is removed when either the IN or BIAS UVLO rising threshold is reached by the input or bias voltage and a normal start-up then follows.
E	Turn on, $V_{IN} < V_{UVLO\_1,2(IN)} - V_{HYS\_1,2(IN)}$ or $V_{BIAS} \geq V_{UVLO(BIAS)} - V_{HYS(BIAS)}$	OFF	The output falls because of the load and active discharge circuit.

10.1.3 Power Good (PG)

The PG circuit monitors the voltage at the feedback pin to indicate the status of the output voltage. The PG circuit asserts whenever FB, V_{IN}, or EN are below their thresholds. The PG operation versus the output voltage is shown in Figure 10-3, which is described by Table 10-5.

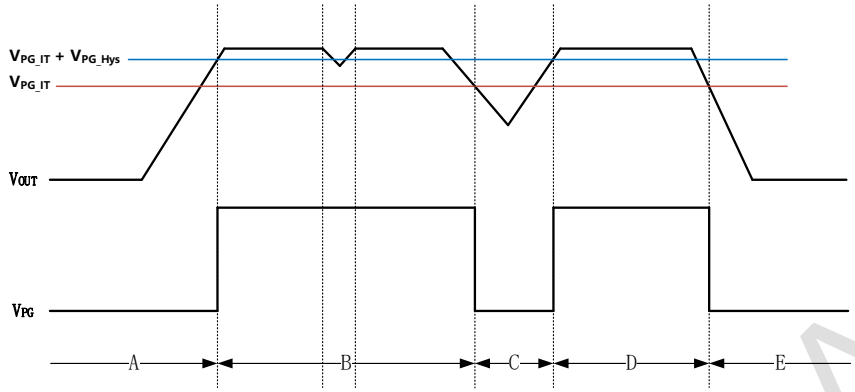


Figure 10-3 Typical PG Operation

Table 10-5 Typical PG Operation Description

REGION	EVENT	PG STATUS	FB VOLTAGE
A	Turn on	LOW	$V_{FB} < V_{IT(PG)} + V_{HYS(PG)}$
B	Regulation	HIGH	$V_{FB} > V_{IT(PG)}$
C	Output voltage dip	LOW	$V_{FB} < V_{IT(PG)}$ till $V_{FB} < V_{IT(PG)} + V_{HYS(PG)}$
D	Regulation	HIGH	$V_{FB} > V_{IT(PG)}$
E	Turn off	LOW	$V_{FB} < V_{IT(PG)}$

The PG pin is open-drain, and connecting a pullup resistor to an external supply enables others devices to receive Power Good as a logic signal that can be used for sequencing. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device or devices. To ensure proper operation of the PG circuit, the pullup resistor value must be from 10kΩ and 100kΩ. The lower limit of 10kΩ results from the maximum pulldown strength of the PG transistor, and the upper limit of 100kΩ results from the maximum leakage current at the PG node. If the pullup resistor is outside of this range, then the PG signal may not read a valid digital logic level.

10.1.4 Transient Performance

There are two key transitions during a load transient response: the transition from a light to a heavy load and the transition from a heavy to a light load. The regions shown in Figure 10-4 are broken down in this section and are described in Table 10-6. Regions A, E, and H are where the output voltage is in steady-state.

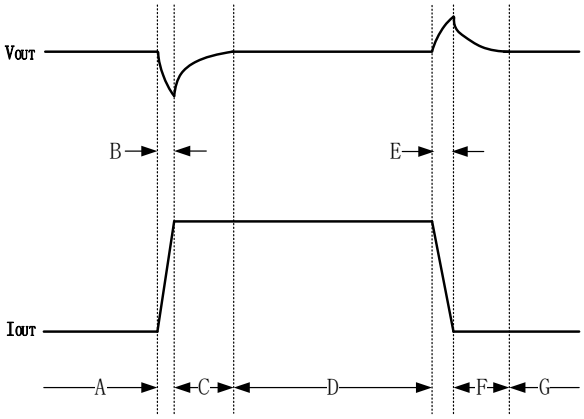


Figure 10-4 Load Transient Waveform

Table 10-6 Typical PG Operation Description

REGION	DESCRIPTION	COMMENT
A	Regulation	-
B	Output current ramping	Initial voltage dip is a result of the depletion of the output capacitor charge
C	LDO responding to transient	Recovery from the dip results from the LDO increasing its sourcing current, and leads to output voltage regulation
D	Regulation	-
E	Output current ramping	Initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase
F	LDO responding to transient	Recovery from the rise results from the LDO decreasing its sourcing current in combination with the load discharging the output capacitor
G	Recovery from the rise results from the LDO decreasing its sourcing current in combination with the load discharging the output capacitor.	-

10.1.5 Negatively Biased Output

The GBI5130 output can be negatively biased to the absolute maximum rating, without affecting start-up condition.

10.1.5.1 Reverse Current Protection

As with most LDOs, this device can be damaged by excessive reverse current. Reverse current is current that flows through the body diode on the pass element instead of the normal conducting channel. This current flow, at high enough magnitudes, degrades long-term reliability of the device resulting from risks of electromigration and excess heat being dissipated across the device. If the current flow gets high enough, a latch-up condition can be entered. Conditions where excessive reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of V_{OUT}>V_{IN}+0.3 V:

- If the device has a large C_{OUT} and the input supply collapses quickly with little or no-load current
- The output is biased when the input supply is not established, or
- The output is biased above the input supply

If excessive reverse current flow is expected in the application, then external protection must be used to protect the device. Figure 10-5 illustrates one approach of protecting the device

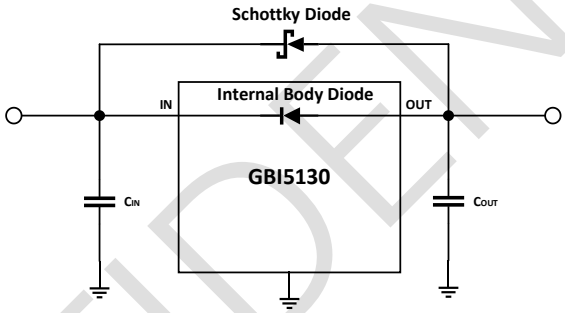


Figure 10-5 Example Circuit for Reverse Current Protection Using a Schottky Diode

10.2 Typical Application

10.2.1 ANY-OUT configuration

The GBI5130 device uses the ANY-OUT configuration to regulate a 4A load requiring good PSRR at high frequency with low-noise at 1.5V using a 1.8V input voltage and a 5V bias supply. The schematic for this typical application circuit is provided in Figure 10-6.

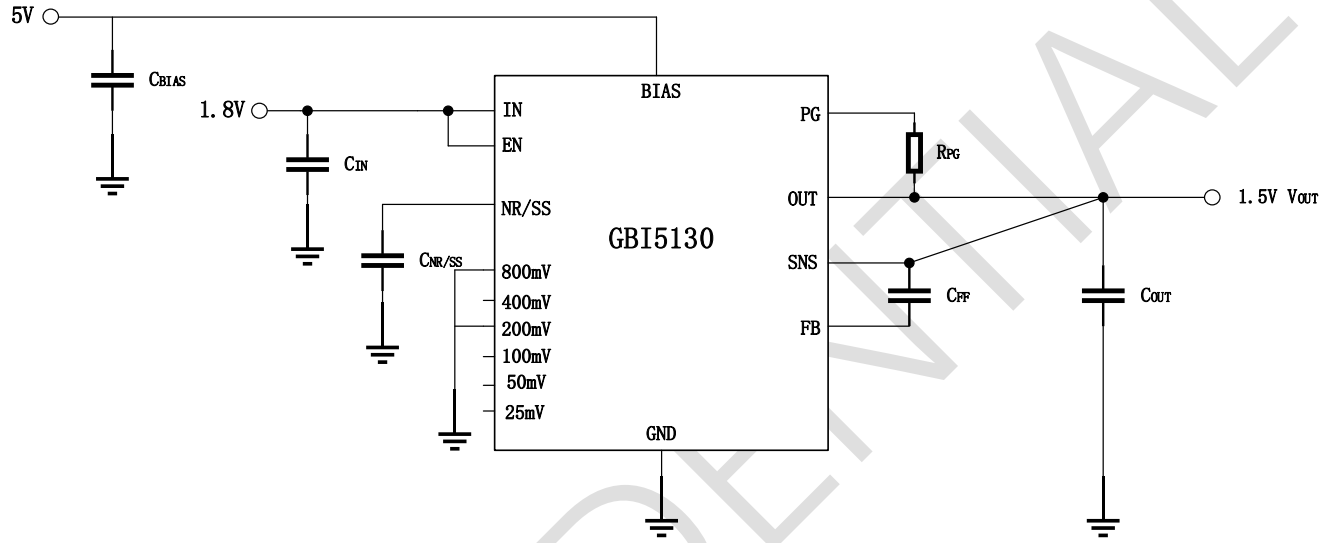


Figure 10-6 GBI5130 ANYOUT configuration

10.2.1.1 Design Requirement

The design parameters are listed in Table 10-7

Table 10-7 GBI5130 design parameters

PARAMETER	DESIGN REQUIREMENT
INPUT VOLTAGE	1.8V, 2%
BIAS VOLTAGE	5V, 5%
OUTPUT VOLTAGE	1.5V, 1%
OUTPUT CURRENT	4A max
RMS noise, 10Hz-100kHz	<10μVrms
PSRR@500kHz	>40dB
Startup time	<20ms

10.2.1.2 Design Procedure

The dropout of the GBI5130 has 160mV maximum dropout over temperature at 4A load current, thus a 300mV headroom is sufficient for operation over both input and output voltage accuracy. The bias rail is provided for better performance for the LILO conditions. The PSRR is greater than 40dB in these conditions, and noise is less than 10μVRMS. The ANY-OUT internal resistor network is also used for maximum accuracy.

To achieve 1.5V on the output, the 800mV and 200mV pins are grounded. The voltage value of 800mV and 200mV is added to the 0.5V internal reference voltage, so the V_{OUT} can be calculated as

$$V_{OUT} = V_{NR/SS} + 0.2V + 0.8V = 1.5V$$

Input and output capacitors are selected in accordance with the External Component Selection section. Ceramic capacitances of 47µF for the input and one 22µF capacitor in parallel with two 10µF capacitors for the output are selected.

To satisfy the required start-up time and still maintain low-noise performance, a 47nF $C_{NR/SS}$ is selected. This value is calculated with Equation 1.

11 Layout

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close as possible to each other, connected by a wide, component-side, copper surface. The use of vias and long traces to the input and output capacitors is strongly discouraged and negatively affects system performance. The grounding and layout scheme shown in Figure 11-1 minimizes inductive parasitic, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. GOSEMICON also recommends a ground reference plane either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similarly to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

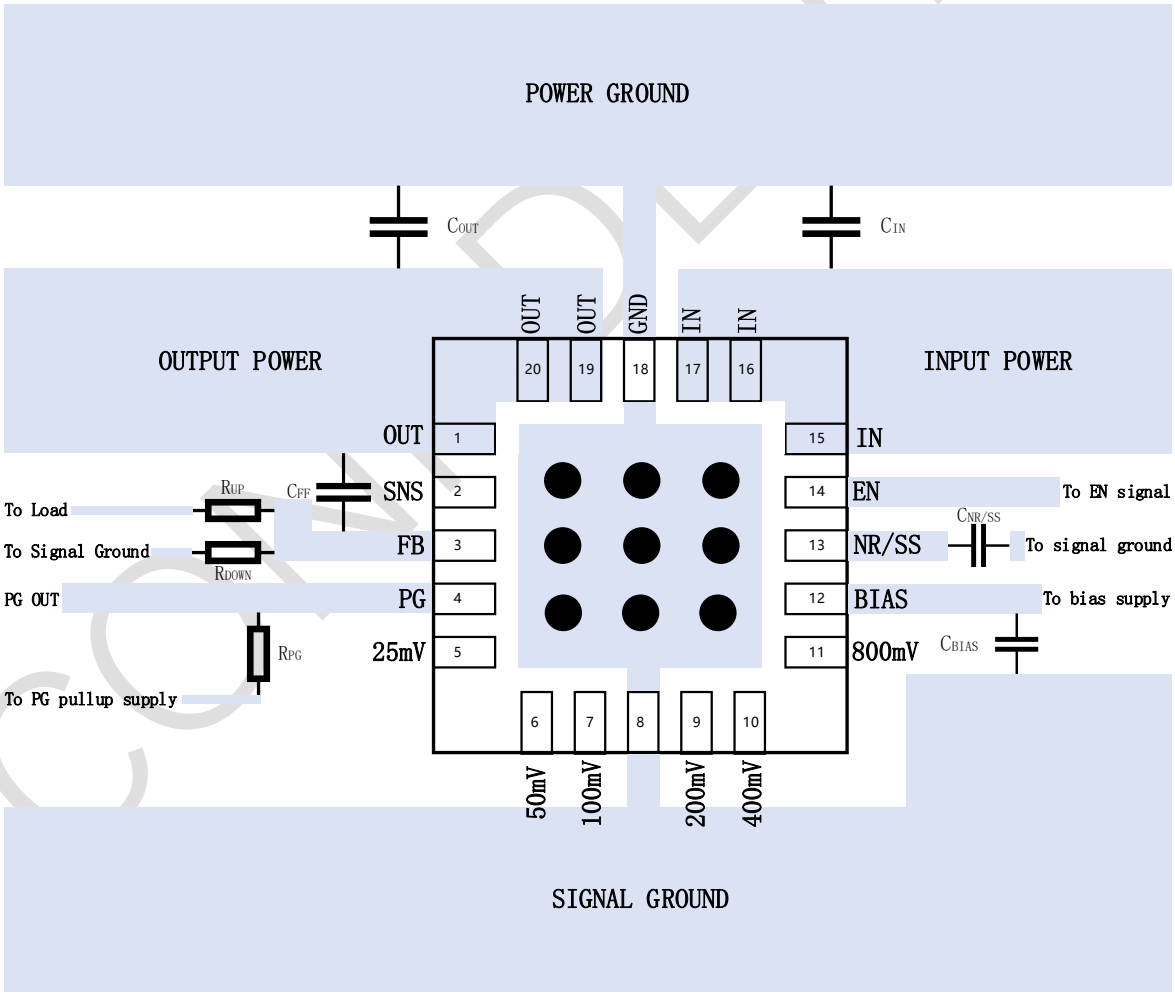
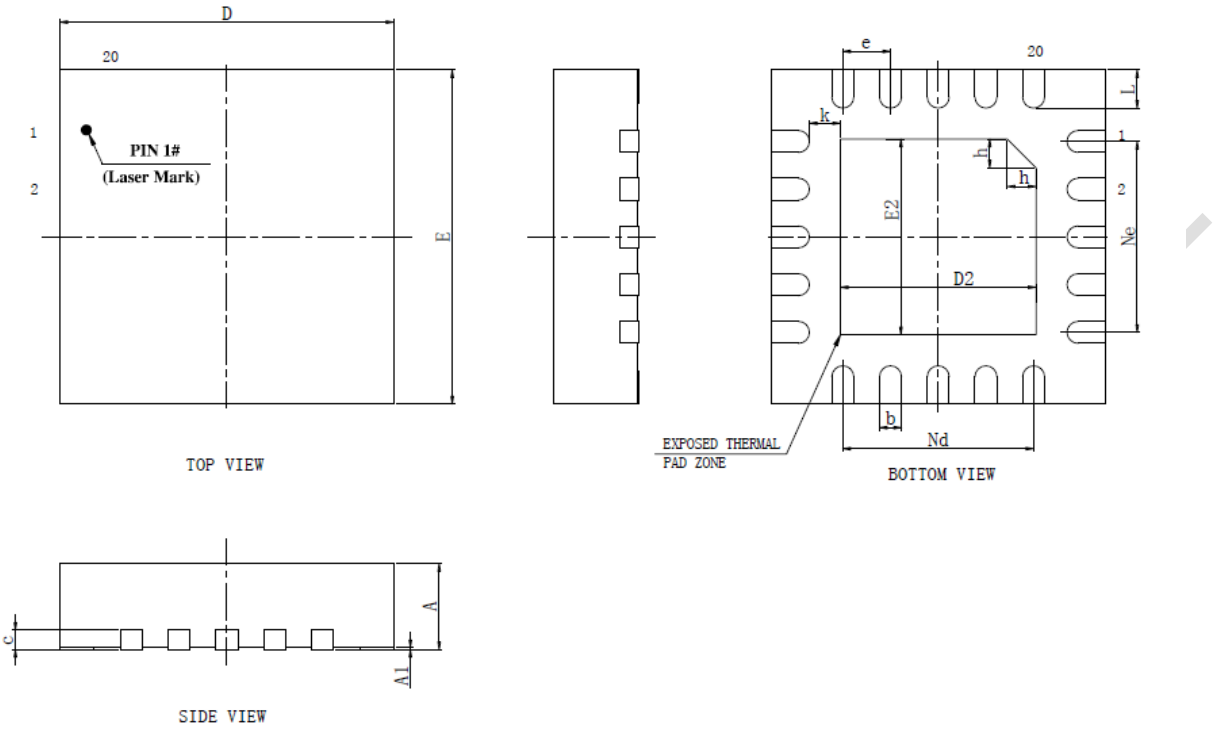


Figure 11-1 Recommended PCB layout

Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.85	0.9	0.95
A1	0	0.02	0.05
b	0.18	0.23	0.30
c		0.203REF	
D	3.40	3.50	3.60
D2	1.95	2.05	2.15
e		0.50BSC	
Nd		2.00BSC	
E	3.40	3.50	3.60
E2	1.95	2.05	2.15
Ne		2.00BSC	
L	0.35	0.40	0.45
K	0.275	0.325	0.375
h	0.25	0.30	0.35