1 MSPS, 3.3 V – 4.8 V, ULTRA LOW POWER, 12-BIT SAR ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 12-Bit Resolution
- Fast Throughput Rate: 1 MSPS
- Single 3.3 V to 4.8 V Supply Operation for XC2365E
- Low Power (typical):
  2.40mW (3.3V，1 MSPS)
  10.0mW (4.5V，1 MSPS)
- ±1LSB INL,±1LSB DNL
- No Data Latency
- SPI/ MICROWIRE™ Compatible Serial Interface
- Guaranteed Operation from –40°C to 85°C
- 6-Pin SOT-23 Package
- Second-Source for LTC2365

DESCRIPTION

The XC2365E is a 12-bit, high speed, low power, and small-sized Successive-Approximation-Register (SAR) ADC. The supply current drops at lower sampling rates because the device automatically power down after conversion. The full-scale input of the XC2365E is 0 V to VDD or VREF. This device can operate from a single 3.3 V to 4.8 V supply with a 1-MSPS throughput.

The XC2365E is available in a 6-pin SOT-23 package and has an operating temperature range of -40°C to 85°C.

The XC2365E is a drop-in replacement for the LTC2365.

APPLICATIONS

- Communication Systems
- Data Acquisition Systems
- Handheld Portable Devices
- Medical Imaging
- Uninterrupted Power Supplies
- Battery-Operated Systems
- Automotive

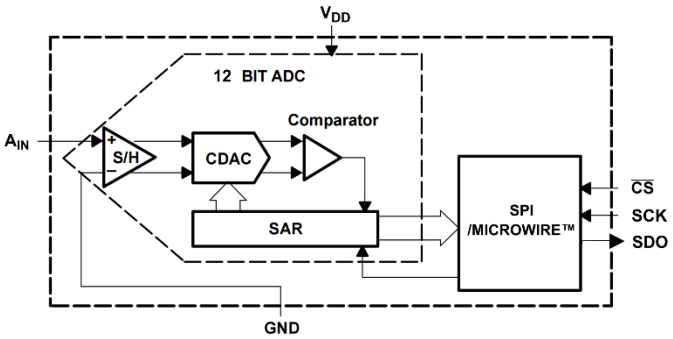


Figure 1. Functional Block Diagram

SPECIFICATIONS

At-40℃ to 85℃, f_{SAMPLE} = 1 MSPS and f_{SCLK} = 16.6 MHz if 3.3 V ≤ V_{DD} ≤ 4.8 V. (unless otherwise noted)

PARAMETER	TEST CONDITIONS	XC2365E			UNITS
		MIN	TYP	MAX	
SYSTEM PERFORMANCE					
Resolution			**12**		Bits
No missing codes		**12**			Bits
Integral linearity			**0.5**		LSB
Differential linearity			**0.5**		LSB
f_{SAMPLE} Throughput rate	f_{SCLK} = 16.6 MHz, 3.3 V ≤ V_{DD} ≤ 4.8 V			**1**	MSPS
SNR	f_{IN} = 100 kHz		**72.5**		dB
THD	f_{IN} = 100 kHz		**-85**		dB

XC2365E

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{DD} Supply current, normal operation	Digital inputs = 0 V or V_{DD}	f_{SAMPLE} = 1000 KSPS, f_{SCLK} = 16.6 MHz, V_{DD} = 3.3 V		**0.69**	**1.54**	mA
		f_{SAMPLE} = 1000 KSPS, f_{SCLK} = 16.6 MHz, V_{DD} = 4.5 V		**2.17**	**3.40**	
		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 3.3 V		**0.60**	**1.28**	
		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 4.5 V		**1.80**	**2.80**	
POWER DISSIPATION, XC2365E						
Normal operation		f_{SAMPLE} = 1000 KSPS, f_{SCLK} = 16.6 MHz, V_{DD} = 3.3 V		**2.30**	**5.10**	mW
		f_{SAMPLE} = 1000 KSPS, f_{SCLK} = 16.6 MHz, V_{DD} = 4.5 V		**9.80**	**15.3**	mW

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

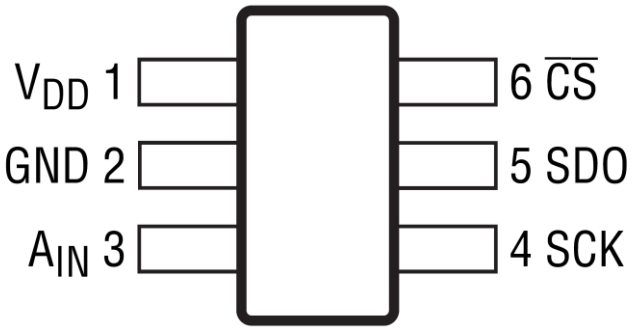


Figure 2. Pin Configuration

TERMINAL		DESCRIPTION
NAME	NO.	
V_{DD}	1	Power Supply Input.
GND	2	The ground return for the supply and signals.
A_{IN}	3	Analog Input. This signal can range from 0 V to V_{DD}.
SCK	4	Digital clock input. This clock directly controls the conversion and readout processes.
SDO	5	Digital data output. The output samples are clocked out of this pin on falling edges of the SCK pin.
$\overline{CS}$	6	Chip Select. On the falling edge of $\overline{CS}$, a conversion process begins.

TYPICAL CONNECTION

Figure 3 shows a typical connection diagram for the XC2365E. The 3.3 V supply should come from a stable power supply such as an LDO. The supply to XC2365E should be decoupled to the ground. Two decoupling capacitors, one 1-µF and one 10-nF, are suggested to be inserted between the V_{DD} and GND pins of the converter. The capacitors should be placed as close as possible to the pins of the device. Always set the V_{DD} supply to be greater than or equal to the maximum input signal to avoid saturation of codes.

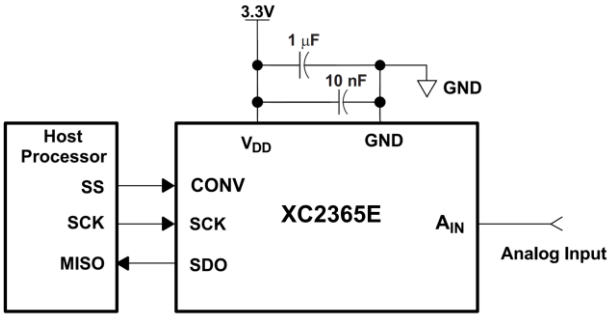


Figure 3. Typical Circuit Configuration

TIMING DIAGRAM

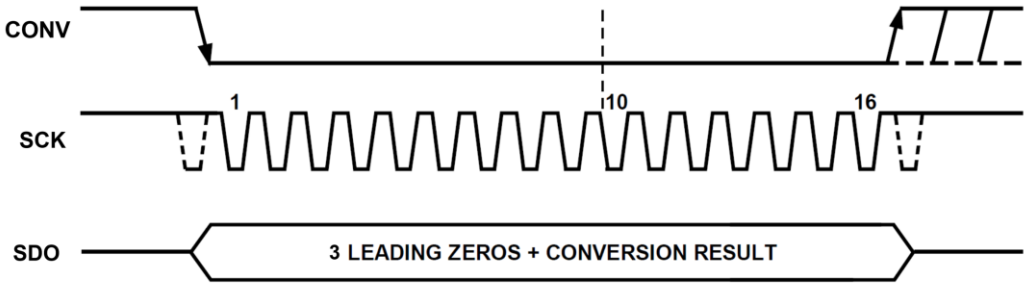


Figure 4. Timing Diagram

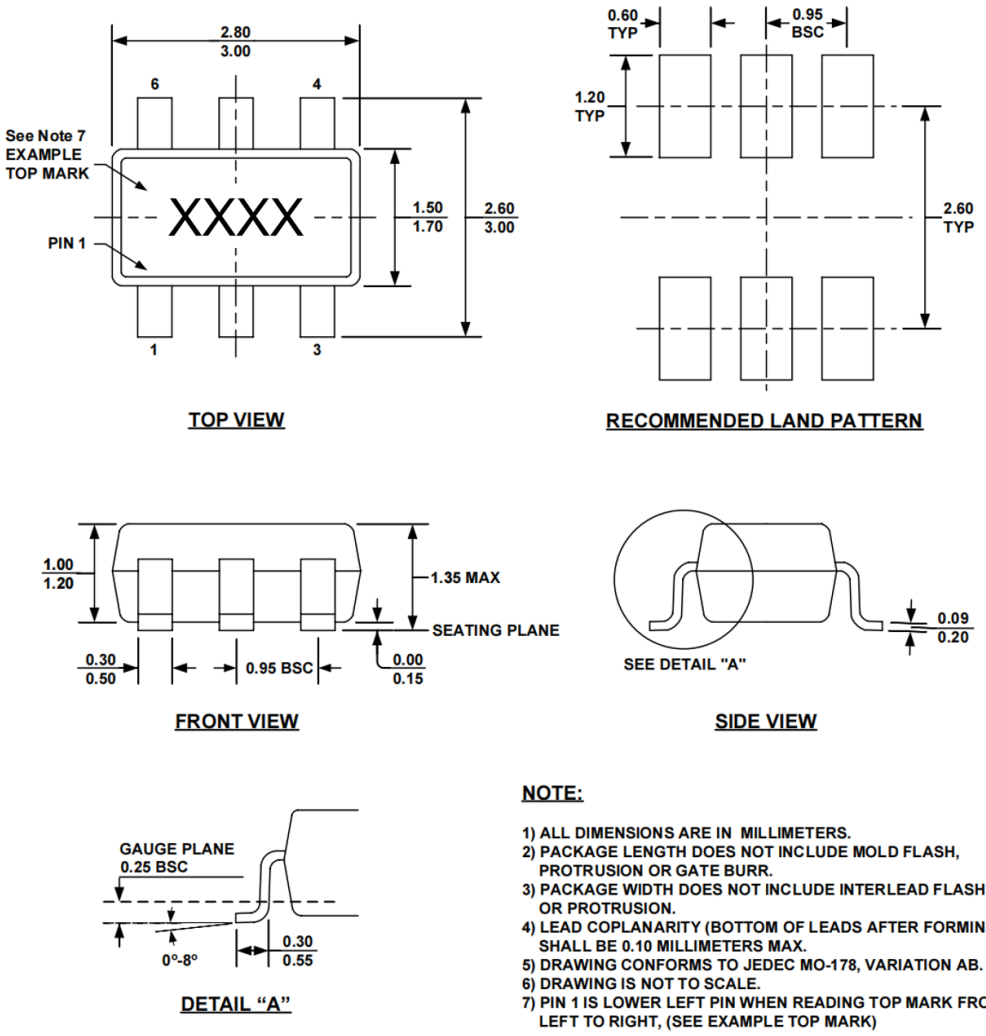
The LTC2365 series conversion result is output through SDO after the second SCK falling edge following the $\overline{CS}$ falling edge. The XC2365E series will output three leading zeros following the 12-bit conversion result from the SDO, after the fourth SCK falling edge following the falling edge of $\overline{CS}$. After that, SDO enters a tri-state stage and the conversion cycle ends up.

POWER-DOWN MODE

The XC2365E has an auto power-down feature. Besides powering down all circuitry, the converter consumes only a small amount of current in this mode. The device automatically wakes up when $\overline{CS}$ falls. However, not all of the functional blocks are fully powered until sometime before the third falling edge of SCK. The device powers down once it reaches the end of conversion which is the 16th falling edge of SCK for the XC2365E. The device enters power down mode if $\overline{CS}$ goes high before the 10th SCK falling edge. Ongoing conversion stops and SDO goes to three-state under this power down condition.

These converters achieve lower power dissipation for a fixed throughput rate by using higher SCK frequencies. Higher SCK frequencies reduce the acquisition time and conversion time. This means the converters spend more time in auto power-down mode per conversion cycle. For a particular SCK frequency, the acquisition time and conversion time are fixed. Therefore, a lower throughput increases the proportion of the time the converters are in power down, thereby reducing power consumption.

OUTLINE DIMENTIONS



NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-178, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

NOTES

1. Unpacked ICs, tube-mounted ICs, etc. must be stored in a drying cabinet, and the humidity in the drying cabinet < 20% R.H.
2. After access, the components are stored in an electrostatic packaging protective bag.
3. Anti-static damage: the device is an electrostatic sensitive device, and sufficient anti-static measures should be taken during transmission, assembly and testing.
4. The user should conduct a visual inspection before use, and the bottom, side and surrounding of the circuit can be welded only if it is bright. If oxidation occurs, the circuit can be processed by means of oxidation, and the circuit must be soldered within 12 hours after processing.