1. DESCRIPTION

The XD4553 −digit BCD counter consists of 3 negative edge triggered BCD counters that are cascaded synchronously. A quad latch at the output of each counter permits storage of any given count. The information is then time division multiplexed, providing one BCD number or digit at a time. Digit select outputs provide display control. All outputs are TTL compatible.

An on−chip oscillator provides the low−frequency scanning clock which drives the multiplexer output selector.

This device is used in instrumentation counters, clock displays, digital panel meters, and as a building block for general logic applications.

2. FEATURES

- TTL Compatible Outputs
- On−Chip Oscillator
- Cascadable
- Clock Disable Input
- Pulse Shaping Permits Very Slow Rise Times on Input Clock
- Output Latches
- Master Reset
- These Devices are Pb−Free and are RoHS Compliant

3. BLOCK DIAGRAM

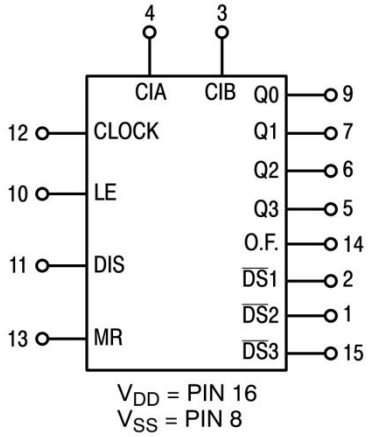


Figure 1. Block Diagram

4. MAXIMUM RATINGS(Voltages Referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	−0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	V_{in}, V_{out}	−0.5 to V_{DD} + 0.5	V
Input Current (DC or Transient) per Pin	I_{in}	±10	mA
Output Current (DC or Transient) per Pin	I_{out}	+20	mA
Power Dissipation, per Package (Note 1)	P_D	500	mW
Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Lead Temperature (8−Second Soldering)	T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

5. TRUTH TABLE

Inputs				Outputs
Master Reset	Clock	Disable	LE	
0		0	0	No Change
0		0	0	Advance
0	X	1	X	No Change
0	1		0	Advance
0	1		0	No Change
0	0	X	X	No Change
0	X	X		Latched
0	X	X	1	Latched
1	X	X	0	Q0 = Q1 = Q2 = Q3 = 0

6. ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−40°C Min	−40°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	85°C Min	85°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	–	0.	–	0	0.	–	0.	Vdc
		10	–	050.	–	0	050.	–	050.	
		15	–	050.	–	0	050.	–	050.	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	–05	4.95	5.	–05	4.95	–05	Vdc
		10	9.95	–	9.95	01	–	9.95	–	
		15	14.95	–	14.95	01	–	14.95	–	
Input Voltage "0" Level	V_{IL}					5				Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.	–	2.	1.	–	1.	
(V_O = 9.0 or 1.0 Vdc)		10	–	53.	–	254.	53.	–	53.	
(V_O = 13.5 or 1.5 Vdc)		15	–	04.	–	506.	04.	–	04.	
"1" Level	V_{IH}			0		75	0		0	Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.	–	3.	2.	–	3.	–	
(V_O = 1.0 or 9.0 Vdc)		10	57.	–	57.	755.	–	57.	–	
(V_O = 1.5 or 13.5 Vdc)		15	01	–	01	508.	–	01	–	
Output Drive Current (V_{OH} = 4.6 Vdc) Source – (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}		1		1	25		1		mAdc
		5.0	−0.25	–	−0.2	−0.36	–	−0.14	–	
		10	−0.62	–	−0.5	−0.9	–	−0.35	–	
		15	−1.8	–	−1.5	−3.5	–	−1.1	–	
(V_{OH} = 4.6 Vdc) Source – (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc) Outputs		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	mAdc
		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink – (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0	0.	–	0.	0.	–	0.	–	mAdc
		10	51.	–	40.	882.	–	280.	–	
		15	11.	–	91.	25	–	651.	–	
(V_{OL} = 0.4 Vdc) Sink – Other (V_{OL} = 0.5 Vdc) Outputs (V_{OL} = 1.5 Vdc)		5.0	3.8	–	2.5	4.8	–	1.20	–	mAdc
		10	06.	–	55.	08.	–	63.	–	
		15	01 8	–	01 5	02 0	–	5 10	–	
Input Current	I_{in}	15	–	±0.1	–	±0.000 01	±0.1	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package) MR = V_{DD}	I_{DD}	5.0	–	5.	–	0.	5.0	–	150	µAdc
		10	–	01	–	0100.	10	–	300	
		15	–	02	–	0200.	20	–	600	
Total Supply Current (Note 3, 4) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0		0	I_T = 030 (0.35 µA/kHz) f + I_{DD} I_T = (0.85 µA/kHz) f + I_{DD} I_T = (1.50 µA/kHz) f + I_{DD}					µAdc
		10								
		15								

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF: IT(CL) = IT(50 pF) + (CL – 50) Vfk where: IT is in µA (per package), CL in pF, V = (VDD – VSS) in volts, f in kHz is input frequency, and k = 0.004.

7. SWITCHING CHARACTERISTICS(Note 5) (C_L = 50 pF, T_A = 25˚C)

Characteristic	Figure	Symbol	V_{DD}	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	2a	t_{TLH}, t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Clock to BCD Out	2a	t_{PLH}, t_{PHL}	5.0 10 15	– – –	900 500 200	1800 1000 400	ns
Clock to Overflow	2a	t_{PHL}	5.0 10 15	– – –	600 400 200	1200 800 400	ns
Reset to BCD Out	2b	t_{PHL}	5.0 10 15	– – –	900 500 300	1800 1000 600	ns
Clock to Latch Enable Setup Time Master Reset to Latch Enable Setup Time	2b	t_{su}	5.0 10 15	600 400 200	300 200 100	– – –	ns
Removal Time Latch Enable to Clock	2b	t_{rem}	5.0 10 15	– 80 – 10 0	– 200 – 70 – 50	– – –	ns
Clock Pulse Width	2a	$t_{WH(cl)}$	5.0 10 15	550 200 150	275 100 75	– – –	ns
Reset Pulse Width	2b	$t_{WH(R)}$	5.0 10 15	1200 600 450	600 300 225	– – –	ns
Reset Removal Time	–	t_{rem}	5.0 10 15	– 80 0 20	– 180 – 50 – 30	– – –	ns
Input Clock Frequency	2a	f_{cl}	5.0 10 15	– – –	1.5 5.0 7.0	0.9 2.5 3.5	MHz
Input Clock Rise Time	2b	t_{TLH}	5.0 10 15	No Limit			ns
Disable, MR, Latch Enable Rise and Fall Times	–	t_{TLH}, t_{THL}	5.0 10 15	– – –	– – –	15 5.0 4.0	µs
Scan Oscillator Frequency (C1 measured in µF)	1	f_{osc}	5.0 10 15	– – –	1.5/C1 4.2/C1 7.0/C1	– – –	Hz

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

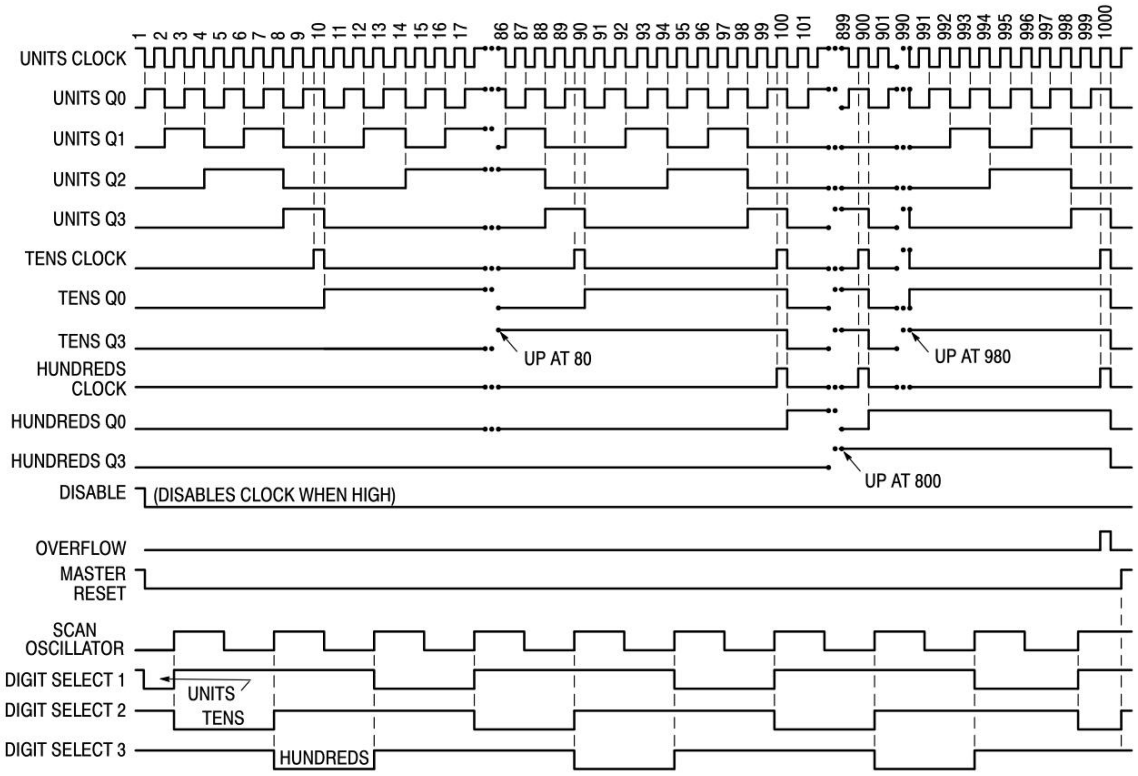


Figure 2. 3−Digit Counter Timing Diagram (Reference Figure 4)

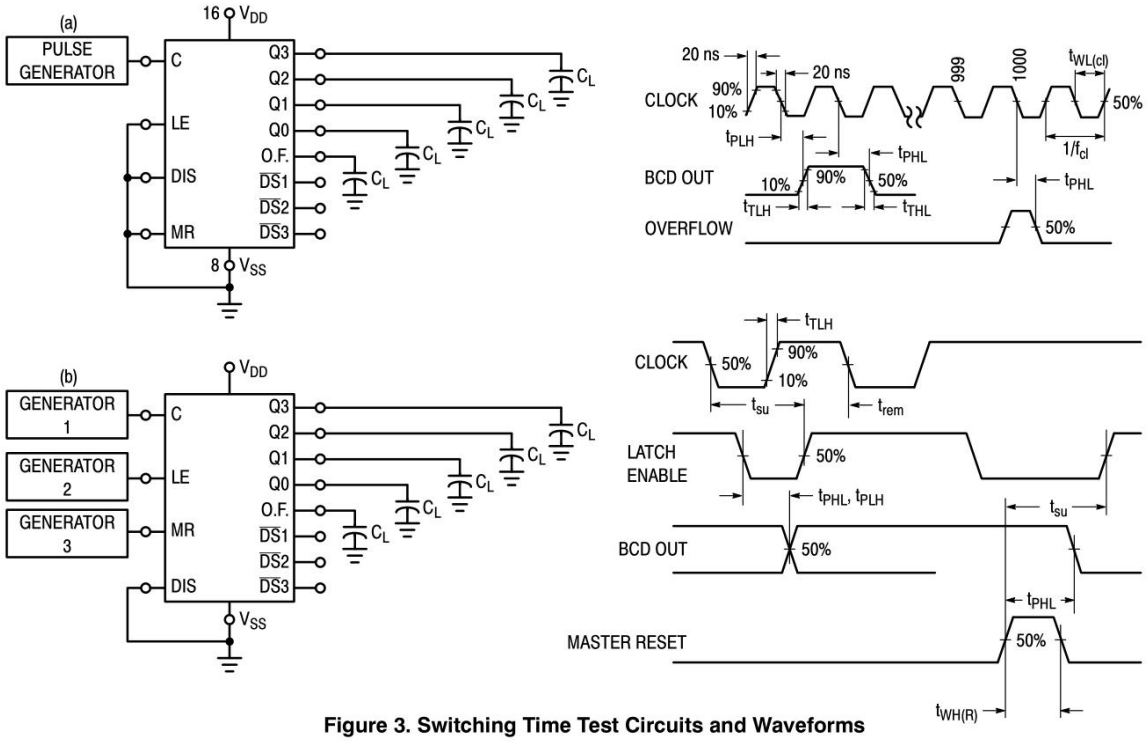


Figure 3. Switching Time Test Circuits and Waveforms

The XD4553 three−digit counter, shown in Figure 4, consists of three negative edge−triggered BCD counters which are cascaded in a synchronous fashion. A quad latch at the output of each of the three BCD counters permits storage of any given count. The three sets of BCD outputs (active high), after going through the latches, are time division multiplexed, providing one BCD number or digit at a time. Digit select outputs (active low) are provided for display control. All outputs are TTL compatible. An on−chip oscillator provides the low frequency scanning clock which drives the multiplexer output selector. The frequency of the oscillator can be controlled externally by a capacitor between pins 3 and 4, or it can be overridden and driven with an external clock at pin 4. Multiple devices can be cascaded using the overflow output, which provides one pulse for every 1000 counts.

The Master Reset input, when taken high, initializes the three BCD counters and the multiplexer scanning circuit. While Master Reset is high the digit scanner is set to digit one; but all three−digit select outputs are disabled to prolong display life, and the scan oscillator is inhibited. The Disable input, when high, prevents the input clock from reaching the counters, while still retaining the last count. A pulse shaping circuit at the clock input permits the counters to continue operating on input pulses with very slow rise times. Information present in the counters when the latch input goes high, will be stored in the latches and will be retained while the latch input is high, independent of other inputs. Information can be recovered from the latches after the counters have been reset if Latch Enable remains high during the entire reset cycle.

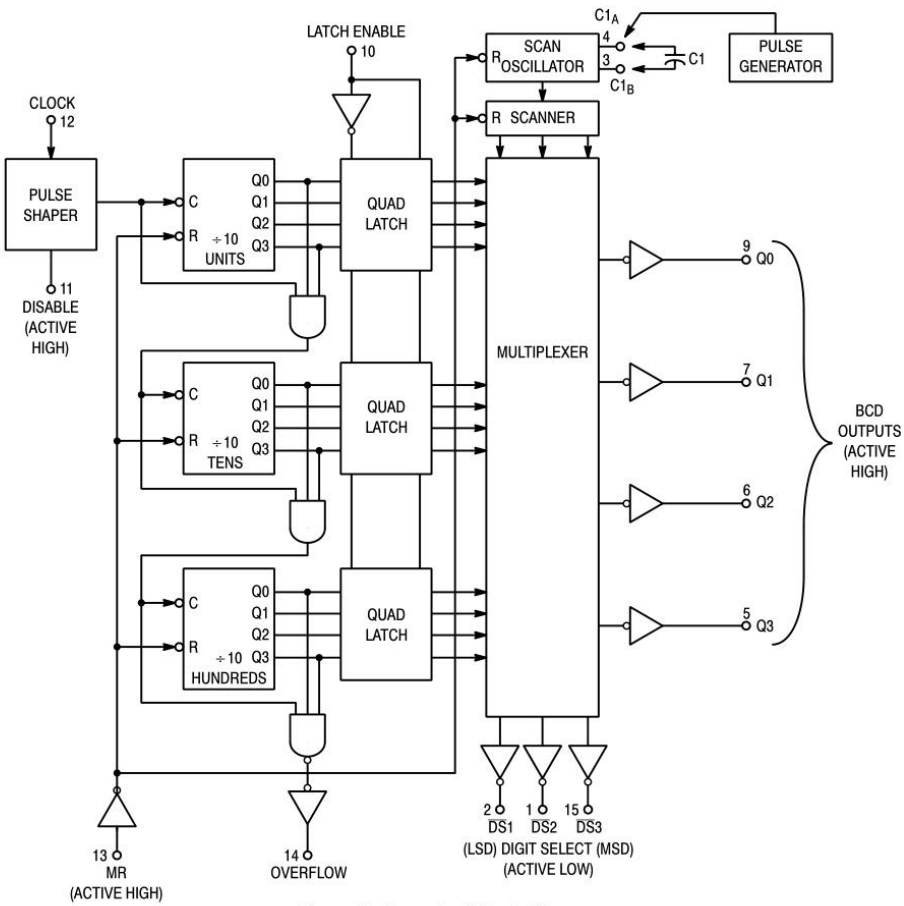


Figure 4. Expanded Block Diagram

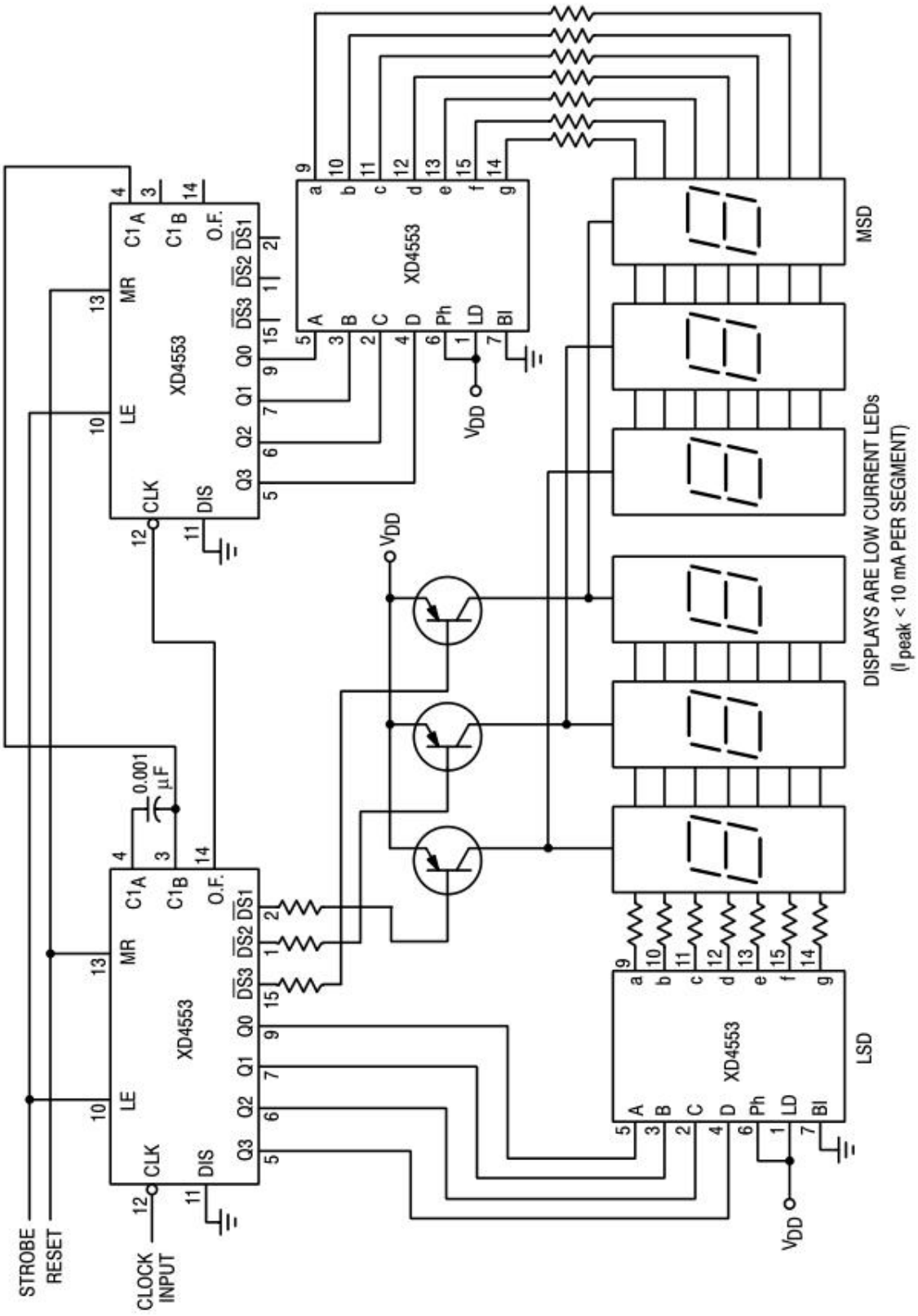


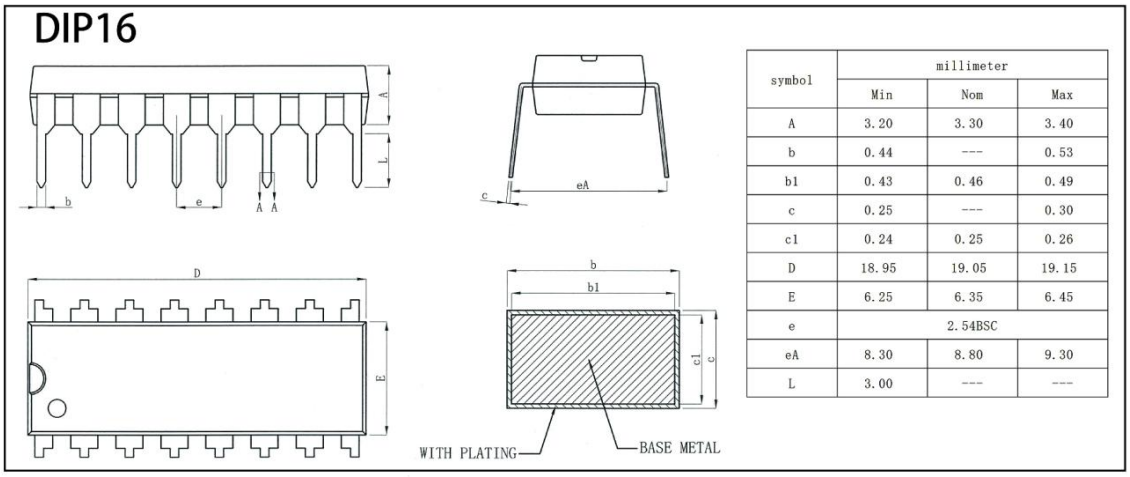
Figure 5. Six-Digit Display

8. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (℃)	MSL	Transport Media	Package Quantity
XD4553	XD4553	DIP16	19.05 * 6.35	- 40 to 85	MSL3	Tube 25	1000

9. DIMENSIONAL DRAWINGS



symbol	millimeter		
	Min	Nom	Max
A	3.20	3.30	3.40
b	0.44	---	0.53
b1	0.43	0.46	0.49
c	0.25	---	0.30
c1	0.24	0.25	0.26
D	18.95	19.05	19.15
E	6.25	6.35	6.45
e	2.54BSC		
eA	8.30	8.80	9.30
L	3.00	---	---