

Features

- Super Low Gate Charge
- Green Device Available
- Excellent Cdv/dt effect decline
- Advanced high cell density Trench technology
- 100% EAS Guaranteed

Bvdss

100V

-100V

Rdson

70mΩ

180mΩ

ID

15A

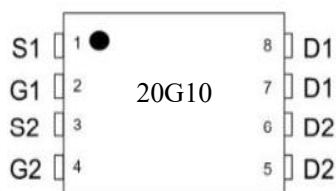
-7A

Application

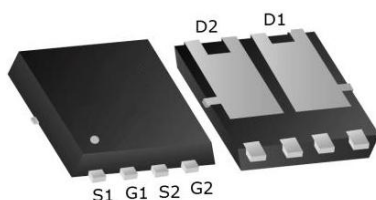
- Power management in half bridge and inverters
- Load Switch
- DC-DC Converter

RoHS

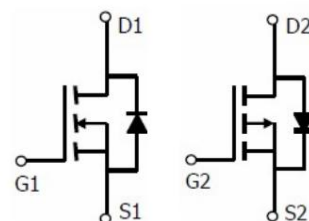
Package



Marking and pin assignment



PDFN5*6-8L top view



N-channel

P-channel

Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
20G10	20G10F	PDFN5*6-8L	5000

Absolute Maximum Ratings

Parameter	Symbol	Value		Unit
		N-Channel	P-Channel	
Drain-Source Voltage	V_{DS}	100	-100	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current	$I_D@T_c=25^\circ\text{C}, V_{GS}@10V^1$	15	-7	A
	$I_D@T_c=70^\circ\text{C}, V_{GS}@10V^1$	10	-4.5	A
Pulsed Drain Current ²	I_{DM}	25	-9.5	A
Single Pulsed Avalanche Energy ³	EAS	22.5	35.3	mJ
Avalanche Current	I_{AS}	22.6	-26.6	A
Total Power Dissipation ⁴	$P_D@T_c=25^\circ\text{C}$	3.5	3.5	W
Operating Junction Temperature Range	T_J	-55 ~ +150		$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55 ~ +150		$^\circ\text{C}$



Thermal Resistance Ratings

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-Ambient ¹	$R_{\theta JA}$	75	$^{\circ}\text{C}/\text{W}$
Thermal Resistance Junction-Case ¹	$R_{\theta JC}$	62.5	$^{\circ}\text{C}/\text{W}$

Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HL20G10F	PDFN5*6-8L	2,4	5,6,7,8	1,3	Tape Reel

N-Channel Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$	-	-	1	μA
Gate to Body Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	-	2.5	V
Static Drain-Source On-Resistance ⁴	$R_{DS(ON)}$	$V_{GS}=10V, I_D=5A$	-	65	90	m Ω
		$V_{GS}=4.5V, I_D=3A$	-	75	105	
Forward Transconductance ⁴	g_{fs}	$V_{DS}=5V, I_D=5A$	-	12	-	S
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	-	1220	-	pF
Output Capacitance	C_{oss}		-	53	-	
Reverse Transfer Capacitance	C_{rss}		-	42	-	
Gate Resistance	R_g	$f=1\text{MHz}$	-	1.3	-	Ω
Total Gate Charge	Q_g	$V_{GS}=10V, V_{DS}=50V, I_D=5A$	-	20.6	-	nC
Gate-Source Charge	Q_{gs}		-	4	-	
Gate-Drain Charge	Q_{gd}		-	3.7	-	
Turn-On Delay Time	$T_{d(on)}$	$V_{GS}=10V, V_{DD}=50V,$ $R_G=3\Omega, I_D=5A$	-	4.7	-	ns
Rise Time	T_r		-	21	-	
Turn-Off Delay Time	$T_{d(off)}$		-	20	-	
Fall Time	T_f		-	16	-	
Diode Forward Voltage	V_{SD}	$I_S=1A, V_{GS}=0V$	-	-	1.2	V
Continuous Source Current	I_S	$T_C=25^{\circ}\text{C}$	-	-	15	A

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^{\circ}\text{C}$.



- The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- The EAS data shows Max.rating.The test condition is $V_{DD}=25\text{V}$, $V_{GS}=10\text{V}$, $L=0.4\text{mH}$, $I_{AS}=8\text{A}$.
- The power dissipation is limited by 150°C junction temperature.
- The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

P-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{V}, I_D=-250\mu\text{A}$	-100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-80\text{V}, V_{GS}=0\text{V}$	-	-	-1	μA
Gate to Body Leakage Current	I_{GSS}	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=-250\mu\text{A}$	-1.2	-	-2.5	V
Static Drain-Source On-Resistance ²	$R_{DS(ON)}$	$V_{GS}=-10\text{V}, I_D=-3\text{A}$	-	180	220	$\text{m}\Omega$
		$V_{GS}=-4.5\text{V}, I_D=-2\text{A}$	-	210	255	
Input Capacitance	C_{iss}	$V_{DS}=-30\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$	-	1228	-	pF
Output Capacitance	C_{oss}		-	41	-	
Reverse Transfer Capacitance	C_{rss}		-	29	-	
Gate Resistance	R_g	$V_{DS}=0\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$	-	13	-	Ω
Total Gate Charge(-10V)	Q_g	$V_{GS}=-10\text{V}, V_{DS}=-50\text{V}, I_D=-2\text{A}$	-	19	-	nC
Gate-Source Charge	Q_{gs}		-	3.4	-	
Gate-Drain Charge	Q_{gd}		-	2.9	-	
Turn-On Delay Time	$T_{d(on)}$	$V_{GS}=-10\text{V}, V_{DD}=-30\text{V},$ $R_G=3.3\Omega, I_D=-1\text{A}$	-	9	-	ns
Rise Time	T_r		-	6	-	
Turn-Off Delay Time	$T_{d(off)}$		-	39	-	
Fall Time	T_f		-	33	-	
Diode Forward Voltage ²	V_{SD}	$V_{GS}=0\text{V}, I_S=-1\text{A}, T_J=25^\circ\text{C}$	-	-	-1.2	V
Continuous Source Current ^{1,5}	I_S	$V_G=V_D=0\text{V}, \text{Force Current}$	-	-	-7	A

Notes:

- The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- The EAS data shows Max. rating . The test condition is $V_{DD}=-25\text{V}, V_{GS}=-10\text{V}, L=0.5\text{mH}, I_{AS}=-14\text{A}$
- The power dissipation is limited by 150°C junction temperature
- The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

N-Channel Typical Characteristics

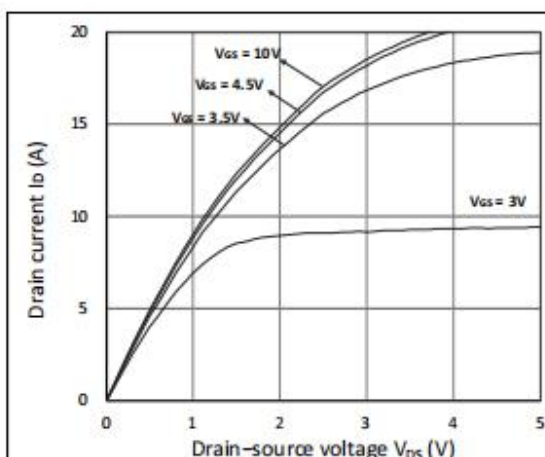


Figure 1. Output Characteristics

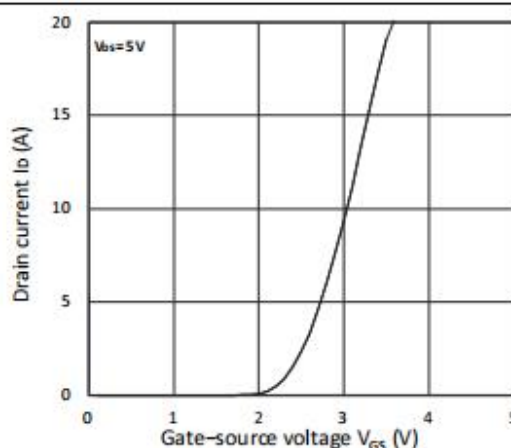


Figure 2. Transfer Characteristics

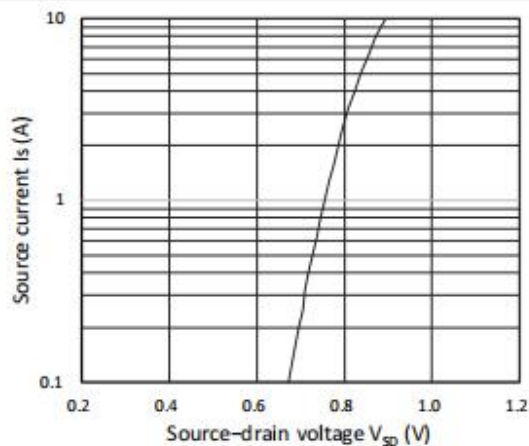


Figure 3. Forward Characteristics of Reverse

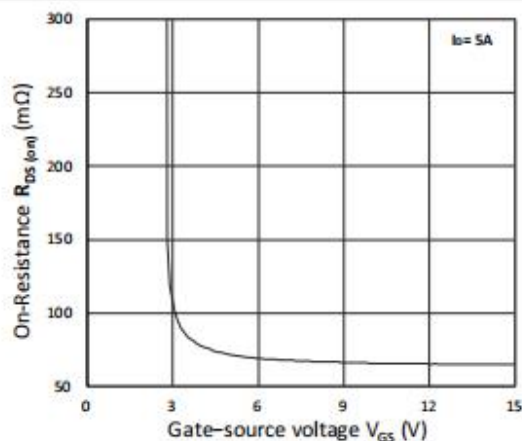


Figure 4. $R_{DS(on)}$ vs. V_{GS}

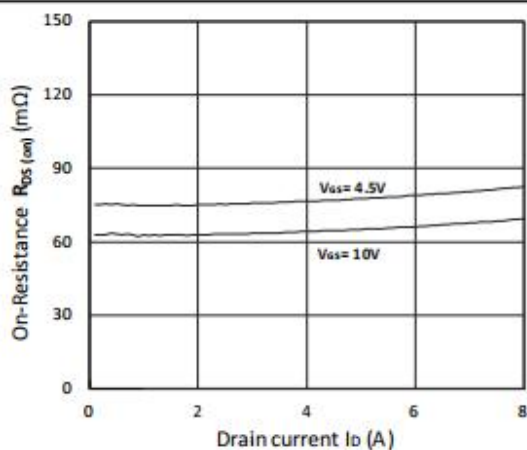


Figure 5. $R_{DS(on)}$ vs. I_D

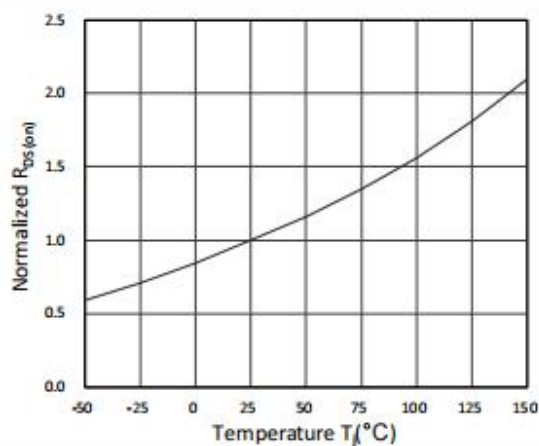


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

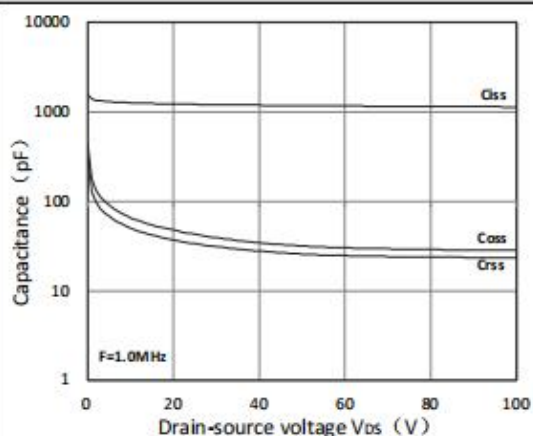


Figure 7. Capacitance Characteristics

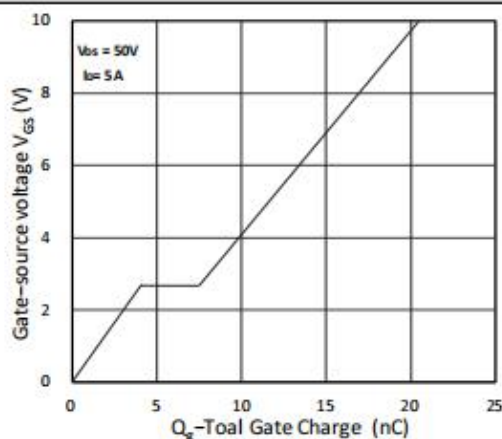


Figure 8. Gate Charge Characteristics

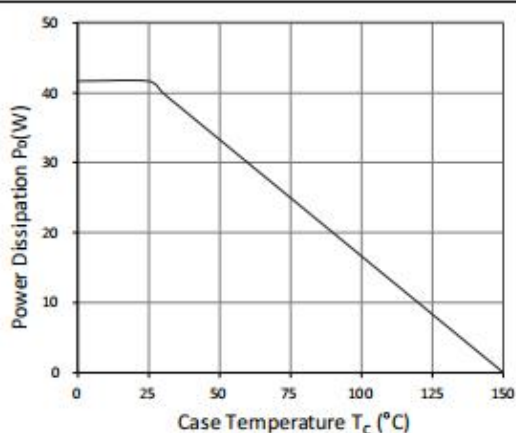


Figure 9. Power Dissipation

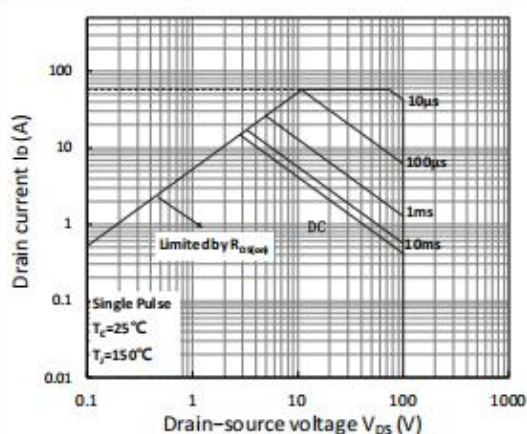


Figure 10. Safe Operating Area

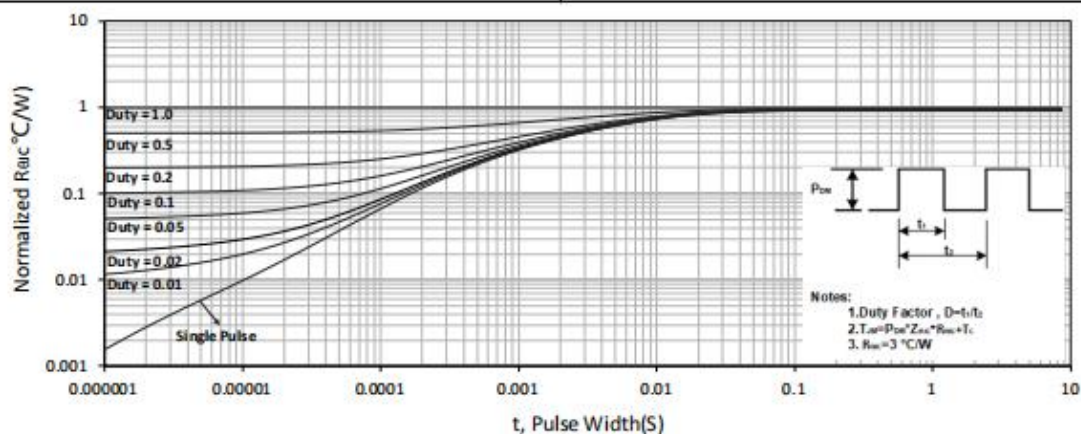


Figure 11. Normalized Maximum Transient Thermal Impedance

P-Channel Typical Characteristics

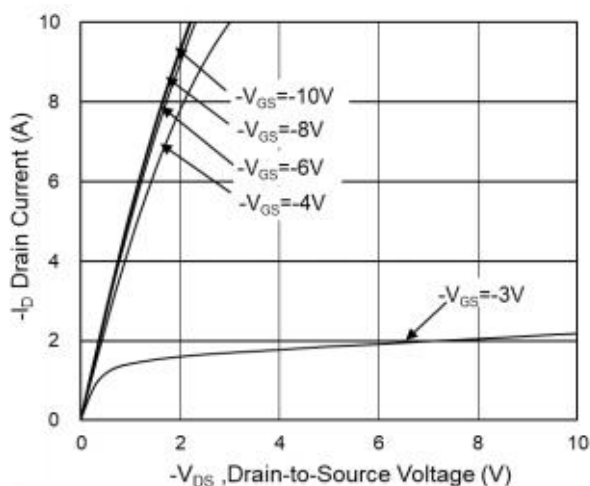


Fig.1 Typical Output Characteristics

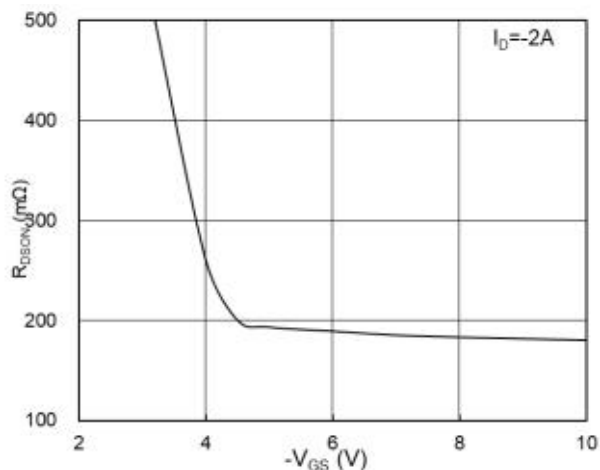


Fig.2 On-Resistance vs G-S Voltage

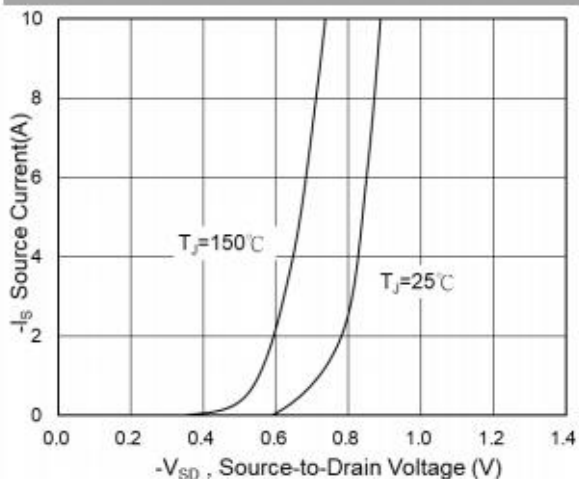


Fig.3 Source Drain Forward Characteristics

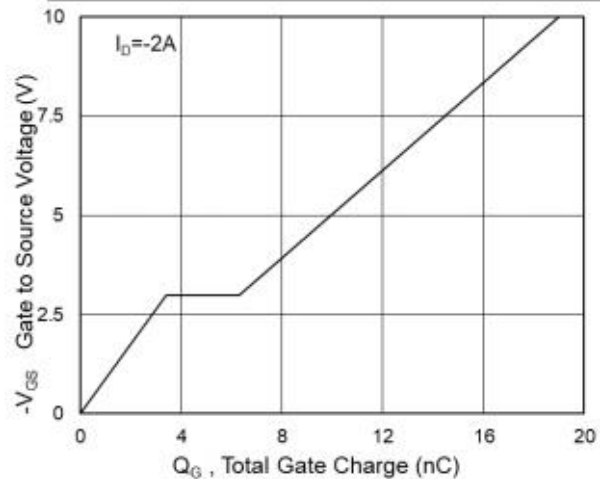


Fig.4 Gate-Charge Characteristics

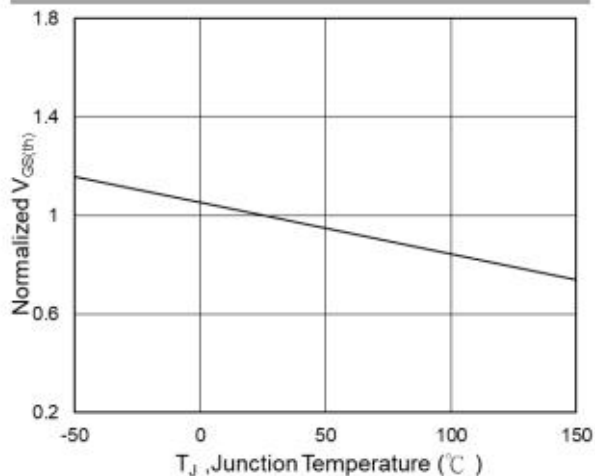


Fig.5 Normalized $V_{GS(th)}$ vs T_J

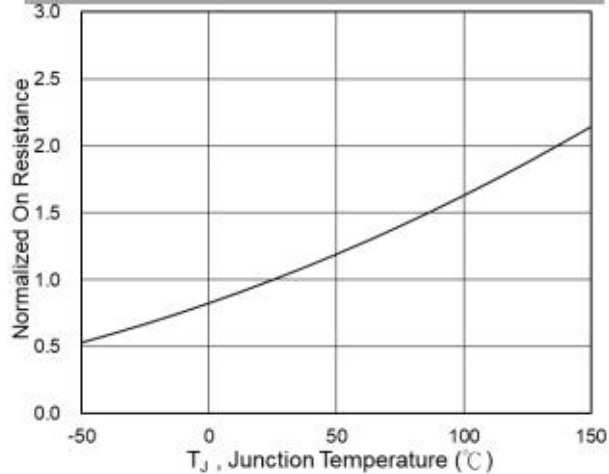


Fig.6 Normalized $R_{DS(on)}$ vs T_J

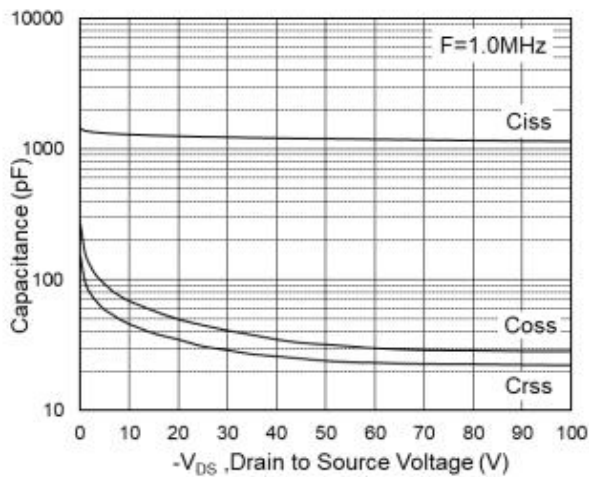


Fig.7 Capacitance

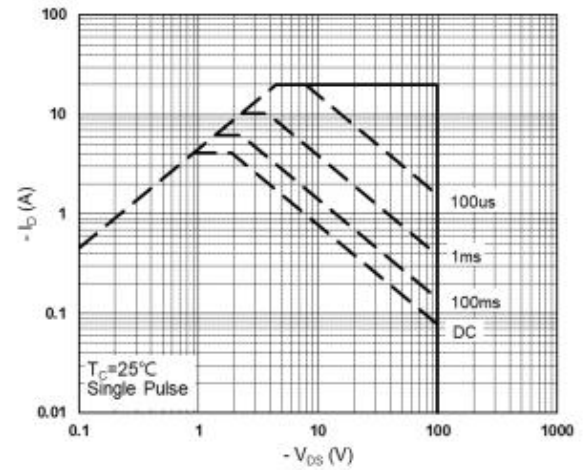


Fig.8 Safe Operating Area

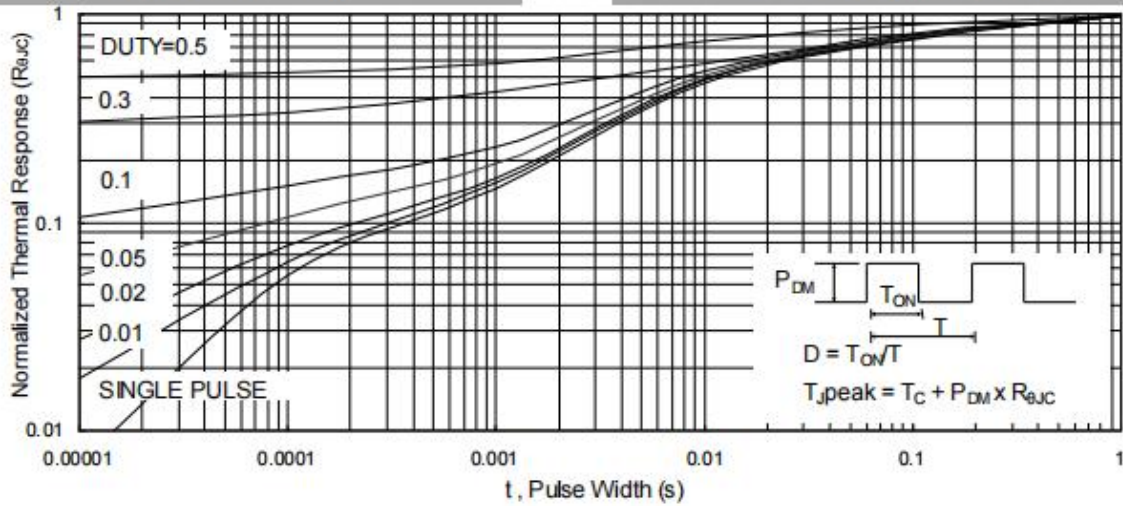


Fig.9 Normalized Maximum Transient Thermal Impedance

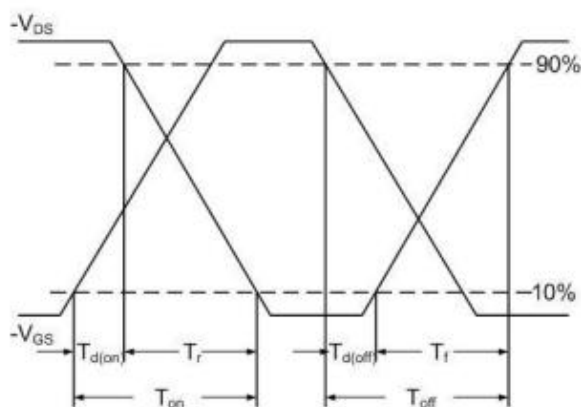


Fig.10 Switching Time Waveform

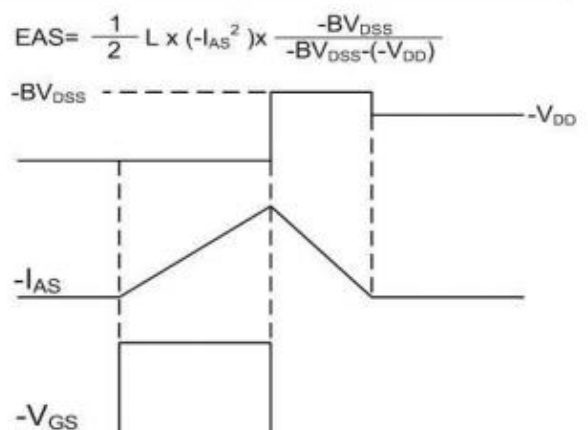
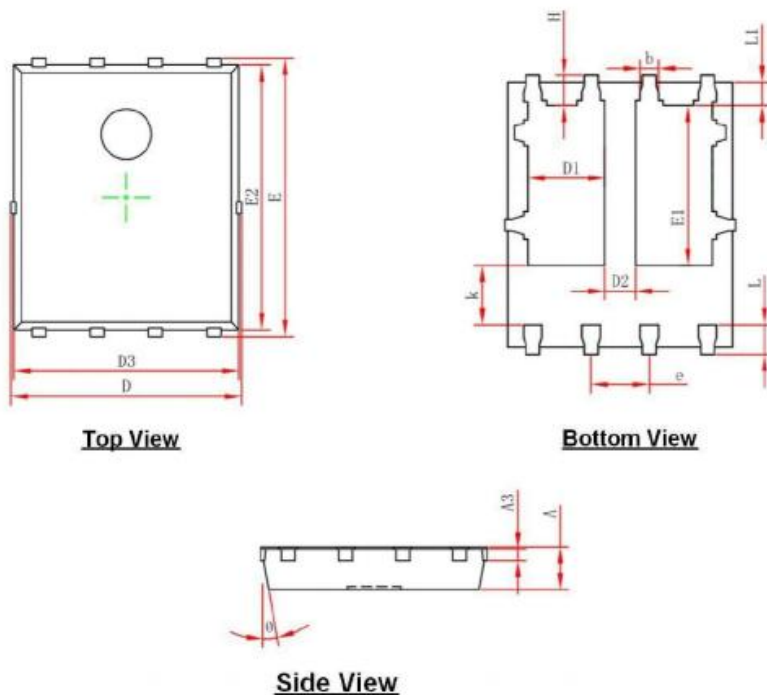


Fig.11 Unclamped Inductive Waveform

Package Dimensions PDFN5*6-8L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.154REF.		0.006REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	1.470	1.870	0.058	0.074
D2	0.470	0.870	0.019	0.034
E1	3.375	3.575	0.133	0.141
D3	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

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