芯伯乐®
XINBOLE

Product Specification

XBLW SN74LS194

4-bit Bidirectional Universal Shift Register

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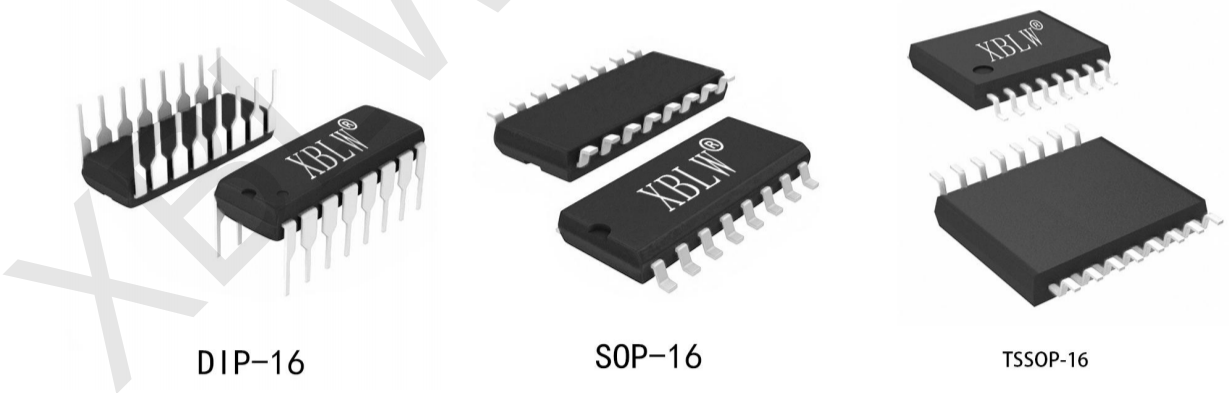
Description

The SN74LS194 is a 4-bit bidirectional universal shift register. The synchronous operation of the device is determined by the mode select inputs (S0, S1). In parallel load mode (S0 and S1 HIGH) data appearing on the D0 to D3 inputs, when S0 and S1 are HIGH, is transferred to the Q0 to Q3 outputs. When S0 is HIGH and S1 is LOW data is entered serially via DSL and shifted from left to right; when S0 is LOW and S1 is HIGH data is entered serially via DSR and shifted from right to left. DSR and DSL allow multistage shift right or shift left data transfers without interfering with parallel load operation. If both S0 and S1 are LOW, existing data is retained in a hold mode. Mode select and data inputs are edge-triggered, responding only to the LOW-to-HIGH transition of the clock (CP). Therefore, the only timing restriction is that the mode control and selected data inputs must be stable one set-up time prior to the positive transition of the clock pulse. When LOW, the asynchronous master reset (MR) overrides all other input conditions and forces the Q outputs LOW. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of VCC.

Features

- Supply voltage range:2V to 6V
- CMO SInput levels
- Shift-left and shift right capability
- Synchronous parallel and serial data transfer
- Easily expanded for both serial and parallel operation
- Asynchronous master reset
- Temperature range:-20℃ to +85℃
- Packaging information: DIP16/SOP16/TSSOP16



DIP-16　　SOP-16　　TSSOP-16

Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW SN74LS194N	DIP-16	74LS194N	Tube	1000Pcs/Box
XBLW SN74LS194DTR	SOP-16	74LS194	Tape	2500Pcs/Reel
XBLW SN74LS194TDTR	TSSOP-16	74LS194	Tape	3000Pcs/Reel

Block Diagram

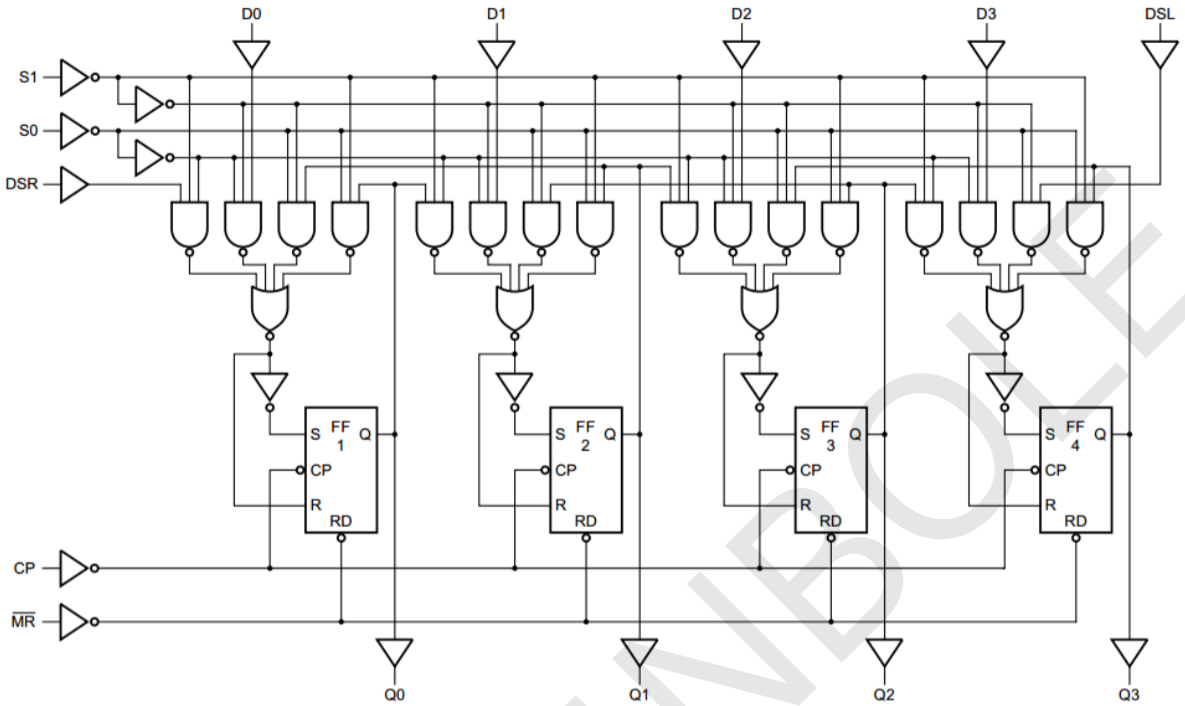


Figure 1. Logic symbol

Pin Configurations

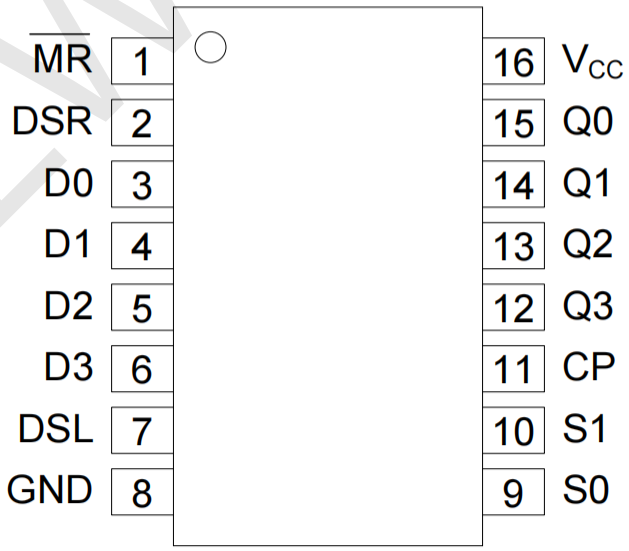


Figure 2. Pin configurations

Pin Description

Pin No.	Pin Name	Description
1	$\overline{MR}$	Asynchronous master reset input(active low)
2	DSR	serious data input(shift right)
3	D0	parallel data input
4	D1	parallel data input
5	D2	parallel data input
6	D3	parallel data input
7	DSL	Serial data input(shift left)
8	GND	ground (0V)
9	S0	mode control input
10	S1	mode control input
11	CP	Clock input(LOW-to-HIGH edge-triggered)
12	Q3	Parallel output
13	Q2	Parallel output
14	Q1	Parallel output
15	Q0	Parallel output
16	V_{CC}	supply voltage

Function Table

Operation mode	inputs							Outputs			
	CP	$\overline{MR}$	S1	S0	DSR	DSL	Dn	Q0	Q1	Q2	Q3
reset(clear)	X	L	X	X	X	X	X	L	L	L	L
Hold(do nothing)	X	H	l	l	X	X	X	Q0	Q1	Q2	Q3
Shift left	↑	H	h	l	X	l	X	Q1	Q2	Q3	L
	↑	H	h	l	X	h	X	Q1	Q2	Q3	H
Shift right	↑	H	l	h	l	X	X	L	Q0	Q1	Q2
	↑	H	l	h	h	X	X	H	Q0	Q1	Q2
Parallel load	↑	H	h	h	X	X	Dn	D0	D1	D2	D3

Note:
H=HIGH voltage level; L=LOW voltage level.
h=HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition.
l=LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition.
X=don't care.
↑=LOW to HIGH CP transition.

Electrical Parameter

Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{CC}	-		-0.5	+7	V
supply current	I_{CC}	-		-	50	mA
ground current	I_{GND}	-		-50	-	mA
input clamping current	I_{IK}	V_I<-0.5V or V_I>V_{CC}+0.5V		-	±20	mA
output clamping current	I_{OK}	V_O<-0.5V or V_O>V_{CC}+0.5V		-	±20	mA
output current	I_O	-0.5V<V_O<V_{CC}+0.5V		-	±25	mA
storage temperature	T_{stg}	-		-65	+150	℃
soldering temperature	T_L	10s	DIP	245		℃
			SOP/TSSOP	260		

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
ambient temperature	T_{amb}	-	-20	-	+85	℃

Electrical Characteristics

DC Characteristics

(T_{amb}=-20℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	V_{CC}	Conditions	Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	2.0V	-	1.5	1.2	-	V
		4.5V	-	3.15	2.4	-	V
		6.0V	-	4.2	3.2	-	V
LOW-level input voltage	V_{IL}	2.0V	-	-	0.8	0.5	V
		4.5V	-	-	2.1	1.35	V
		6.0V	-	-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	2.0V	I_O=-20uA	1.9	2.0	-	V
		4.5V	I_O=-20uA	4.4	4.5	-	V
		6.0V	I_O=-20uA	5.9	6.0	-	V
		4.5V	I_O=-4.0mA	3.84	4.32	-	V
		6.0V	I_O=-5.2mA	5.34	5.81	-	V
LOW-level output voltage	V_{OL}	2.0V	I_O=20uA	-	0	0.1	V
		4.5V	I_O=20uA	-	0	0.1	V
		6.0V	I_O=20uA	-	0	0.1	V
		4.5V	I_O=4.0mA	-	0.15	0.33	V
		6.0V	I_O=5.2mA	-	0.16	0.33	V
input leakage current	I_I	6.0V	V_I=V_{CC} or GND	-	-	±1	uA
supply current	I_{CC}	6.0V	V_I=V_{CC} or GND; I_O=0A	-	-	80	uA

AC Characteristics

(T_{amb}=-20℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	V_{CC}	Conditions		Min.	Typ.	Max.	Unit
CP to Qn propagation delay	t_{PLH}, t_{PHL}	2.0V	C_L=50pF	see Figure 4	-	47	155	ns
		4.5V	C_L=50pF		-	17	36	ns
		6.0V	C_L=50pF		-	14	31	ns
$\overline{MR}$ to Qn propagation delay	t_{PHL}	2.0V	C_L=50pF	see Figure 5	-	39	175	ns
		4.5V	C_L=50pF		-	14	35	ns
		6.0V	C_L=50pF		-	11	30	ns
transition time	t_{THL}, t_{TLH}	2.0V	C_L=50pF	see Figure 5	100	17	-	ns
		4.5V	C_L=50pF		20	6	-	ns
		6.0V	C_L=50pF		17	5	-	ns
clock pulse width	tw	2.0V	C_L=50pF	see Figure 4	100	17	-	ns
		4.5V	C_L=50pF		20	6	-	ns
		6.0V	C_L=50pF		17	5	-	ns
master reset pulse	tw	2.0V	C_L=50pF	see Figure 5	100	17	-	ns
		4.5V	C_L=50pF		20	6	-	ns
		6.0V	C_L=50pF		17	5	-	ns
$\overline{MR}$ to CP removal time	trem	2.0V	C_L=50pF	see Figure 5	60	17	-	ns
		4.5V	C_L=50pF		12	6	-	ns
		6.0V	C_L=50pF		10	5	-	ns
Dn to CP set-up time	tsu	2.0V	C_L=50pF	see Figure 6	90	17	-	ns
		4.5V	C_L=50pF		18	6	-	ns
		6.0V	C_L=50pF		15	5	-	ns
S0, S1 to CP set-up time		2.0V	C_L=50pF	see Figure 7	100	22	-	ns
		4.5V	C_L=50pF		20	8	-	ns
		6.0V	C_L=50pF		17	6	-	ns
DSR, DSL to CP set-up time		2.0V	C_L=50pF	see Figure 6	90	19	-	ns
		4.5V	C_L=50pF		18	7	-	ns
		6.0V	C_L=50pF		15	6	-	ns
Dn to CP hold time	th	2.0V	C_L=50pF	see Figure 6	0	-14	-	ns
		4.5V	C_L=50pF		0	-5	-	ns
		6.0V	C_L=50pF		0	-4	-	ns
S0, S1 to CP hold time		2.0V	C_L=50pF	see Figure 7	0	-11	-	ns
		4.5V	C_L=50pF		0	-4	-	ns
		6.0V	C_L=50pF		0	-3	-	ns
DSR, DSL to CP hold time		2.0V	C_L=50pF	see Figure 6	0	-17	-	ns
		4.5V	C_L=50pF		0	-6	-	ns
		6.0V	C_L=50pF		0	-5	-	ns
maximum clock pulse frequency	fmax	2.0V	C_L=50pF	see Figure 4	4.8	31	-	MHz
		4.5V	C_L=50pF		24	93	-	MHz
		6.0V	C_L=50pF		28	111	-	MHz

Testing Circuit

AC Testing Circuit

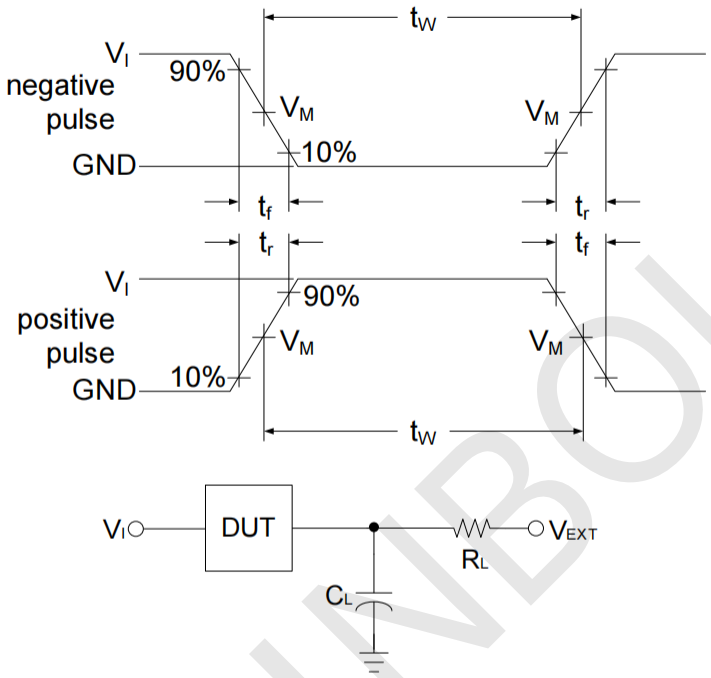


Figure 3. Test circuit for measuring switching times

C_L includes probe and jig capacitance.

Test Data

Type	Input		Load		V_{EXT}		
	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}/t_{PHL}	t_{PLZ}/t_{PZL}	t_{PHZ}/t_{PZH}
SN74LS194	V_{CC}	6.0ns	50pF	1KΩ	Open	V_{CC}	GND

AC Testing Waveforms

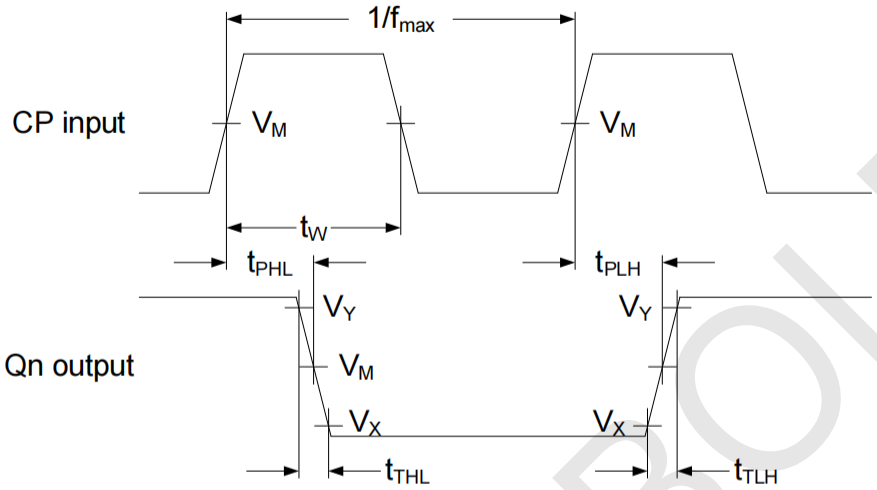


Figure 4. Waveforms showing the clock (CP) to output (Qn) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency

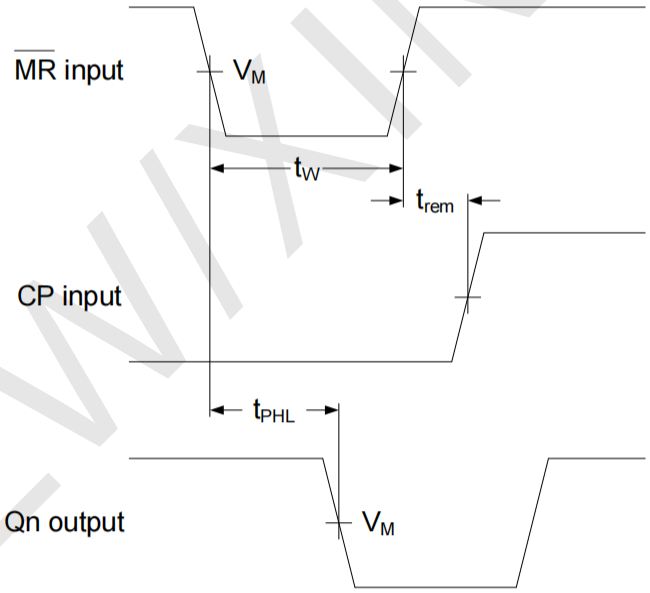


Figure 5. Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to output (Qn) propagation delays and the master reset to clock (CP) removal time

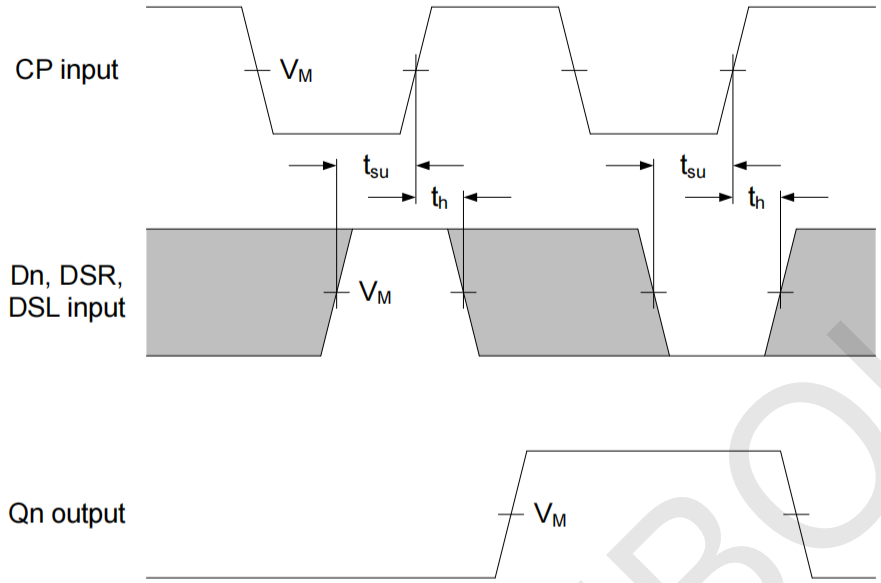


Figure 6. Waveforms showing the set-up and holdtimes from the data inputs (Dn, DSR and DSL) to the clock (CP).

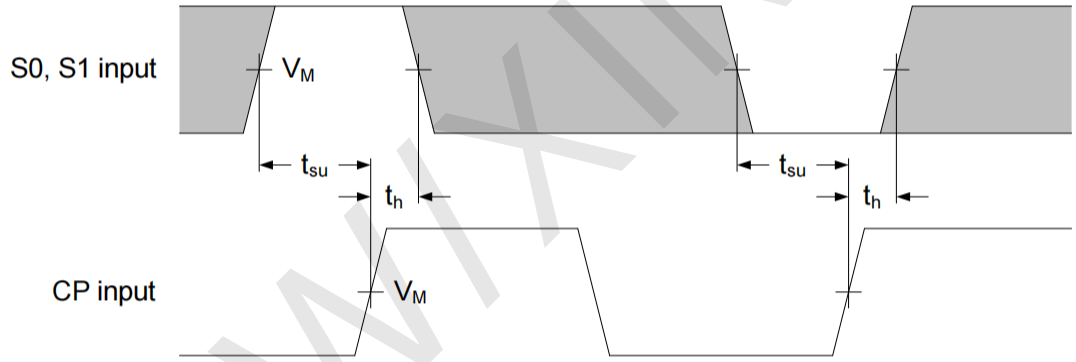


Figure 7. Waveforms showing the set-up and hold times from the mode control inputs (Sn) to the clock input (CP).

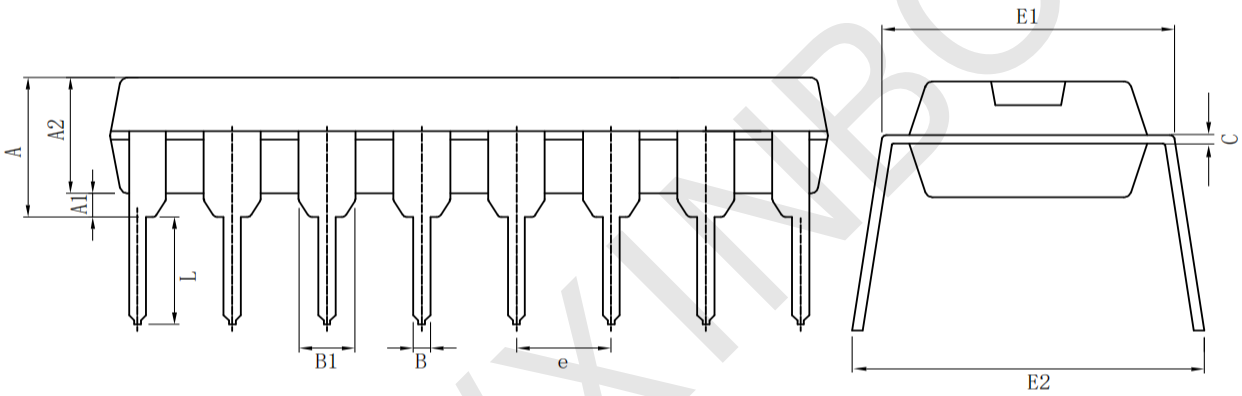
Measurement Points

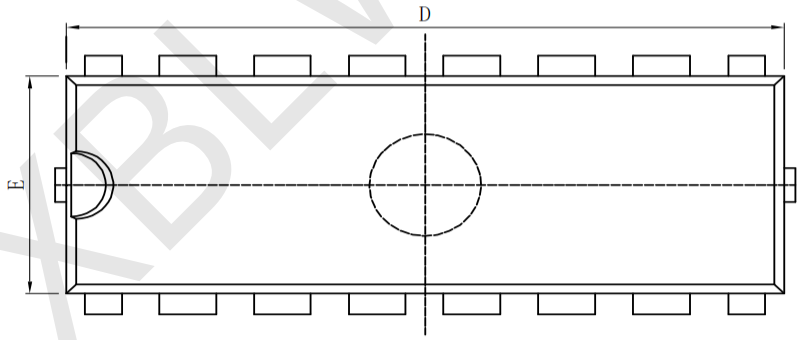
Type	Input	Output		
	V_M	V_M	V_X	V_Y
SN74LS194	$0.5\times V_{CC}$	$0.5\times V_{CC}$	$0.1\times V_{CC}$	$0.9\times V_{CC}$

Package Information

· DIP-16

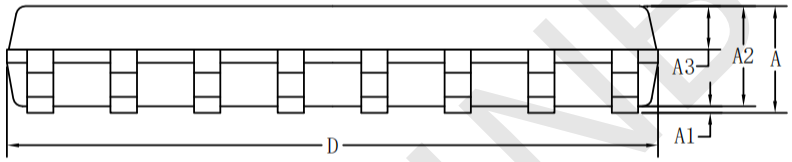
Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	3.710	4.310	A	0.146	0.170
A1	0.510		A1	0.020	
A2	3.200	3.600	A2	0.126	0.142
B	0.380	0.570	B	0.015	0.022
B1	1.524(BSC)		B1	0.060(BSC)	
C	0.204	0.360	C	0.008	0.014
D	18.80	19.20	D	0.740	0.756
E	6.200	6.600	E	0.244	0.260
E1	7.320	7.920	E1	0.288	0.312
e	2.540(BSC)		e	0.100(BSC)	
L	3.000	3.600	L	0.118	0.142
E2	8.400	9.000	E2	0.331	0.354

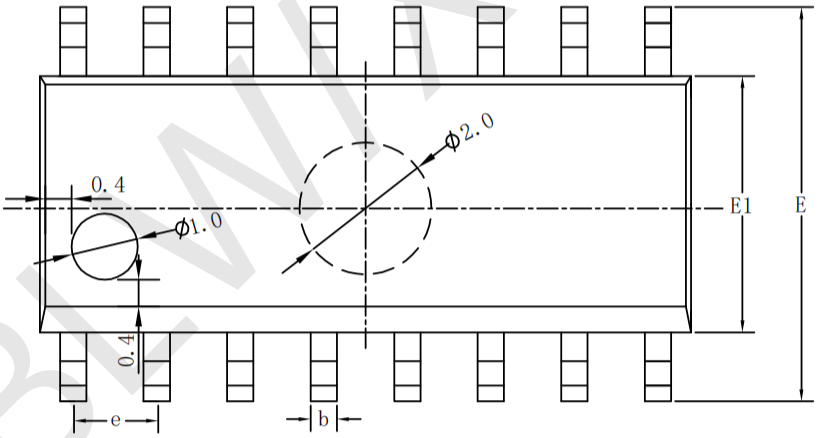


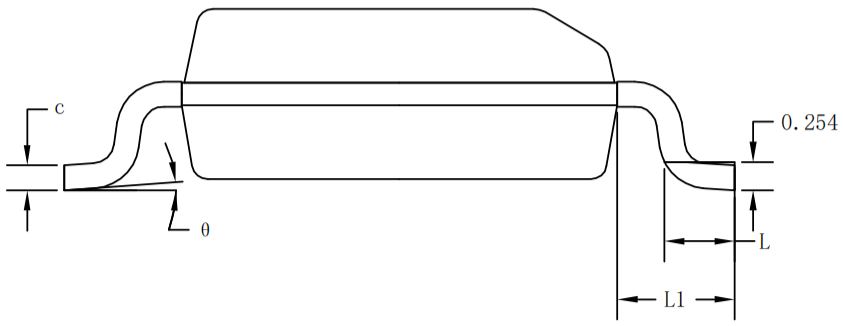


· SOP-16

Size / Symbol	Dimensions In Millimeters			Size / Symbol	Dimensions In Inches		
	Min(mm)	Nom(mm)	Max(mm)		Min(in)	Nom(in)	Max(in)
A	1.500	1.600	1.700	A	0.059	0.063	0.067
A1	0.100	0.150	0.250	A1	0.004	0.006	0.010
A2	1.400	1.450	1.500	A2	0.055	0.057	0.059
A3	0.600	0.650	0.700	A3	0.024	0.026	0.028
b	0.300	0.400	0.500	b	0.012	0.016	0.020
c	0.150	0.200	0.250	c	0.006	0.008	0.010
D	9.800	9.900	10.00	D	0.386	0.390	0.394
E	5.800	6.000	6.200	E	0.228	0.236	0.244
E1	3.850	3.900	3.950	E1	0.152	0.154	0.156
e	1.27(BSC)			e	0.050(BSC)		
L	0.500	0.600	0.700	L	0.020	0.024	0.028
L1	1.05(BSC)			L1	0.041(BSC)		
θ	0°	4°	8°	θ	0°	4°	8°

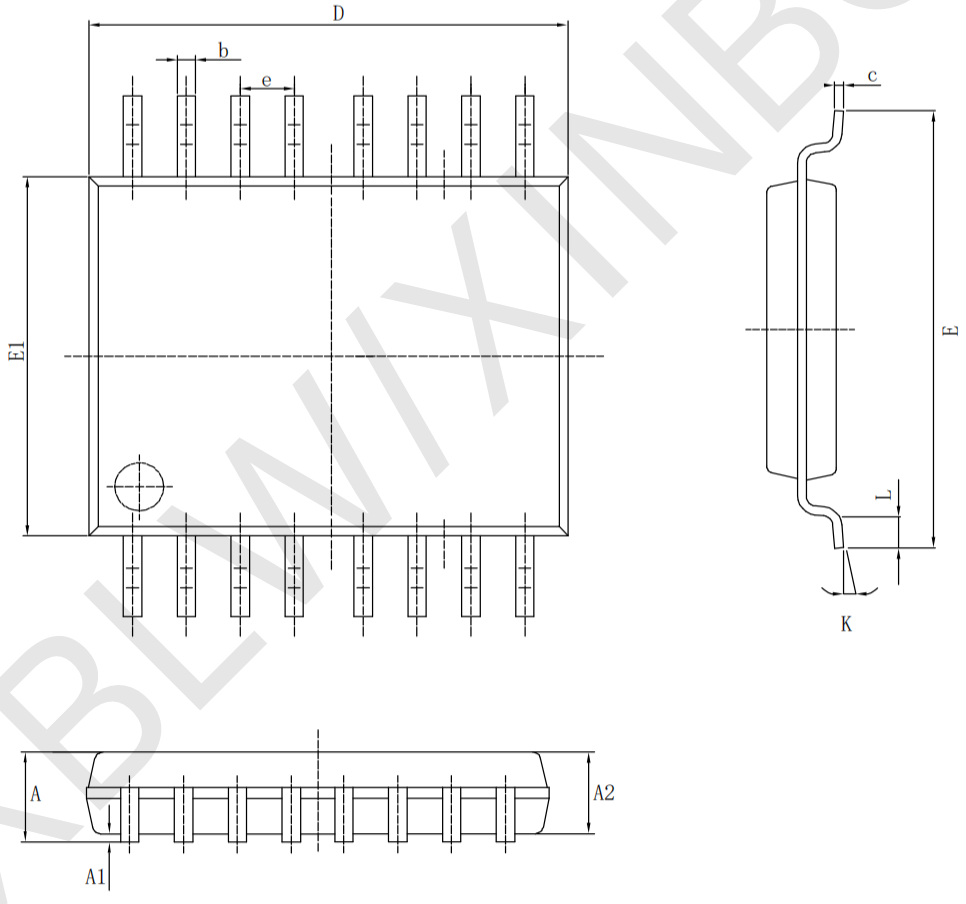






· TSSOP-16

Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A		1.200	A		0.047
A1	0.050	0.150	A1	0.002	0.006
A2	0.800	1.050	A2	0.031	0.041
b	0.190	0.300	b	0.007	0.012
c	0.090	0.200	c	0.004	0.0089
D	4.900	5.100	D	0.193	0.201
E	6.200	6.600	E	0.244	0.260
E1	4.300	4.480	E1	0.169	0.176
e	0.65(BSC)		e	0.0256(BSC)	
K	0°	8°	K	0°	8°
L	0.450	0.750	L	0.018	0.030



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