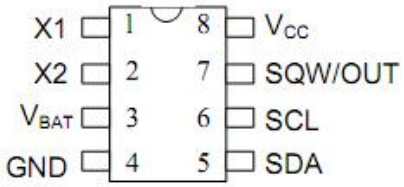
64 X 8 Serial Real Time Clock--DS1307ZN-TD

FEATURES:

- 1Real time clock counts seconds, minutes, hours, date of the month, month, day of the week, and year with leap year compensation valid up to 2100
- 56 byte nonvolatile RAM for data storage
- 2-wire serial interface
  Programmable squarewave output signal
- Automatic power-fail detect and switch Circuitry
- Consumes less than 1uA in battery backup mode with oscillator running
- Optional industrial temperature range -40°C to +85°C
- Recognized by Underwriters Laboratory DS1307ZN-TDCompatible



PIN DESCRIPTION:

VCC: Primary Power Supply
X1, X2: 32.768 kHz Crystal Connection
VBAT: +3V Battery Input
GND: Ground
SDA：Serial Data
SCL ： Serial Clock
SQW/OUT：Square wave/Output Driver

DESCRIPTION

The DS1307ZN-TDSerial Real Time Clock is a low power, full BCD clock/ calendar plus 56 bytes of nonvolatile SRAM. Address and data are transferred serially via a 2-wire bi-directional bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with less than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator.

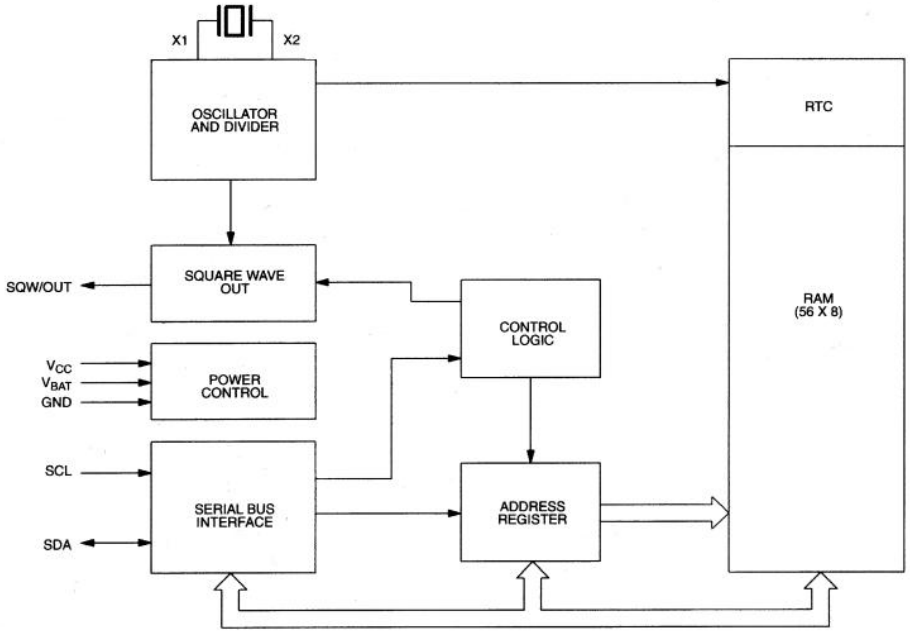
The DS1307ZN-TD has a built-in power sense circuit which detects power failures and automatically switches to the battery supply.

OPERATION

The DS1307ZN-TDoperates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code followed by a register address. Subsequent registers can be accessed sequentially until a STOP condition is executed. When V_{CC} falls below 1.15 x V_{BAT} the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from an out of tolerance system. When V_{CC} falls below V_{BAT} the device switches into a low current battery backup mode. Upon power up, the device switches from battery to V_{CC} when V_{CC} is greater than V_{BAT} +0.2V and recognizes inputs when V_{CC} is greater than 1.15 x V_{BAT}. The block diagram in Figure 1 shows the main elements of the Serial Real Time Clock.

DS1307ZN-

TD**BLOCK DIAGRAM：**



SIGNAL DESCRIPTIONS

VCC, GND - DC power is provided to the device on these pins. VCC is the +5 volt input. When 5 volts is applied within normal limits, the device is fully accessible and data can be written and read. When a 3-volt battery is connected to the device and VCC is below 1.15 x VBAT, reads and writes are inhibited. However, the Timekeeping function continues unaffected by the lower input voltage. As VCC falls below VBAT the RAM and timekeeper are switched over to the external power supply (nominal 3.0V DC) at VBAT.

VBAT - Battery input for any standard 3-volt lithium cell or other energy source. Battery voltage must be held between 2.0 and 3.5 volts for proper operation. The nominal write protect trip point voltage at which access to the real time clock and user RAM is denied is set by the internal circuitry as 1.15 x VBAT nominal. A lithium battery with 100 mAhr or greater will back up the DS1307ZN-TDfor more than 10 years in the absence of power at 25 degrees C.

SCL (Serial Clock Input) - SCL is used to synchronize data movement on the serial interface.

SDA (Serial Data Input/Output) - SDA is the input/output pin for the 2-wire serial interface. The SDA pin is open drain which requires an external pullup resistor.

SQW/OUT (Square Wave/ Output Driver) - When enabled, the SQWE bit set to 1, the SQW/OUT pin outputs one of four square wave frequencies (1 Hz, 4 kHz, 8 kHz, 32 kHz). The SQW/OUT pin is open drain which requires an external pullup resistor. SQW/OUT will operate with either Vcc or Vbat applied.

X1, X2 - Connections for a standard 32.768 kHz quartz crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 12.5 pF.

RTC AND RAM ADDRESS MAP

The address map for the RTC and RAM registers of the DS1307ZN-TDis shown in Figure 2. The real-time clock registers are located in address locations 00h to 07h. The RAM registers are located in address locations 08h to 3Fh. During a multi-byte access, when the address pointer reaches 3Fh, the end of RAM space, it wraps around to location 00h, the beginning of the clock space.

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DS1307ZN-TD**ADDRESS MAP** Figure 2

SECONDS	00H
MINUTES	
HOURS	
DAY	
DATE	
MONTH	
YEAR	
CONTROL	07H
RAM	08H
56 x 8	3FH

CLOCK AND CALENDAR

The time and calendar information is obtained by reading the appropriate register bytes. The real time clock registers are illustrated in Figure 3. The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the Binary-Coded Decimal (BCD) format. Bit 7 of Register 0 is the Clock Halt (CH) bit. When this bit is set to a 1, the oscillator is disabled. When cleared to a 0, the oscillator is enabled.

Please note that the initial power on state of all registers is not defined. Therefore it is important to
enable the oscillator (CH bit=0) during initial configuration.

The DS1307ZN-TDcan be run in either 12-hour or 24-hour mode.
Bit 6 of the hours register is defined
as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 24-hour mode, bit 5 is the second 10 hour bit (20- 23 hours).

On a 2-wire START, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This

	BIT7						BIT0	
00H	CH	10 SECONDS			SECONDS			00–59
	X	10 MINUTES			MINUTES			00–59
	X	12/24	10 HR A/P	10 HR	HOURS			01–12 / 00–23
	X	X	X	X	X	DAY		1–7
	X	X	10 DATE		DATE			01–28/29 / 01–30 / 01–31
	X	X	X	10 MONTH	MONTH			01–12
	10 YEAR				YEAR			00–99
07H	OUT	X	X	SQWE	X	X	RS1	RS0

eliminates the need to re- read the registers in case of an update of the main registers during a read.

DS1307ZN-TD**TIMEKEEPER REGISTERS** Figure 3

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CONTROL REGISTER

The DS1307ZN-TDControl Register is used to control S e operation of the SQW/OUT pin.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OUT	X	X	SQWE	X	X	RS1	RS0

OUT (Output control): This bit controls the output level of the SQW/OUT pin when the square wave output is disabled. If SQWE=0, the logic level on the SQW/OUT pin is 1 if OUT=1 and is 0 if OUT=0.

SQWE (Square Wave Enable): This bit, when set to a logic 1, will enable the oscillator output. The frequency of the square wave output depends upon the value of the RS0 and RS1 bits.

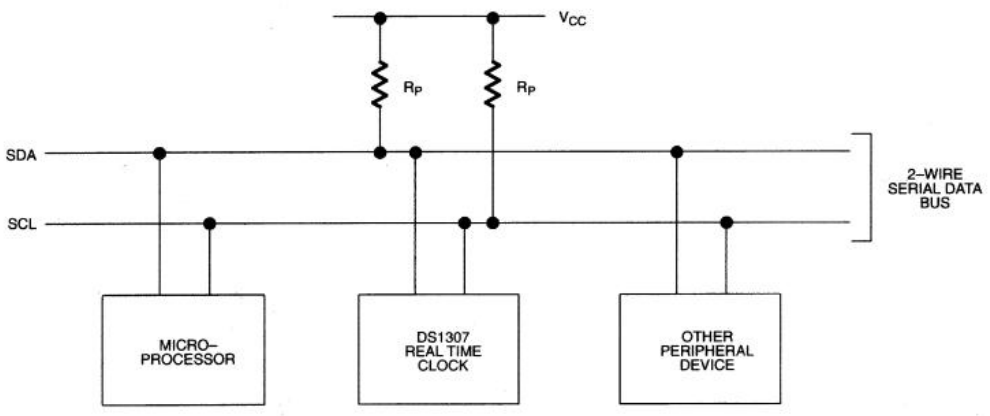
RS (Rate Select):
These bits controD S e frequency of the square wave output when the square wave output has been enabled. Table 1 lists the square wave frequencies that can be selected with the RS bits.

SQUAREWAVE OUTPUT FREQUENCY Table 1

RS1	RS0	SQW OUTPUT FREQUENCY
0	0	1 Hz
0	1	4.096 kHz
1	0	8.192 kHz
1	1	32.768 kHz

2-WIRE SERIAL DATA BUS

The DS1307ZN-TDsupports a bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1307ZN-TDoperates as a slave on the 2-wire bus. A typical bus configuration using this 2-wire pr



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TYPICAL 2-WIRE BUS CONFIGURATION Figure 4

Figures 5, 6, and 7 detail how data is transferred on the 2-wire bus.

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

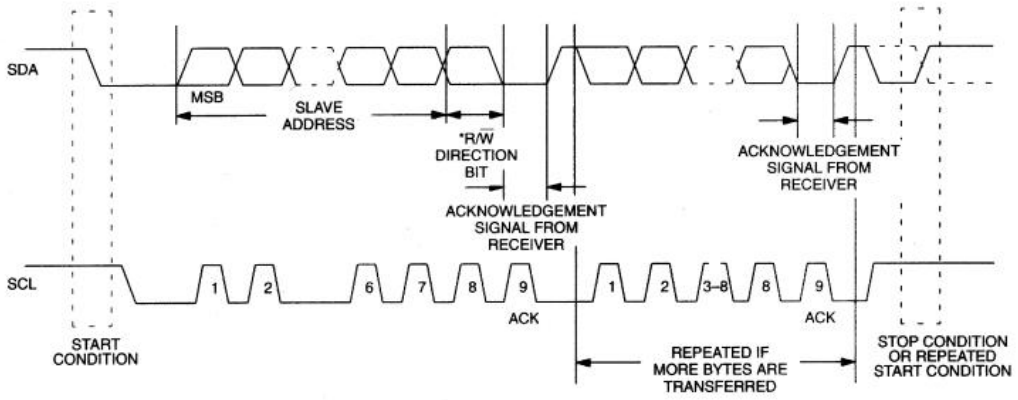
Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit. Within the 2-wire bus specifications a regular mode (100 kHz clock rate) and a fast mode (400 kHz clock rate) are defined. The DS1307ZN-TDoperates in the regular mode (100 kHz) only.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

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DATA TRANSFER ON 2-WIRE SERIAL BUS Figure 5



Depending upon the state of the R/W bit, two types of data transfer are possible:

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

2. **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. This is followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a ’not acknowledge’ is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released. Data is transferred with the most significant bit (MSB) first.

The DS1307ZN-TDmay operate in the following two modes:

1. **Slave receiver mode (**DS1307ZN-TD**write mode):**Serial data and clock are received through SDA andSCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is

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performed by

hardware after reception of the slave address and *direction bit (See Figure 6). The address byte is

the first byte received after the start condition is generated by the master. The address byte contains

the 7 bit DS1307ZN-TDaddress,which is 1101000,followed by the *direction bit (R/W) which, fora write,

is a 0. After receiving and decoding the address byte the device outputs an acknowledge on the SDA

line. After the DS1307ZN-TDacknowledges the slave address +

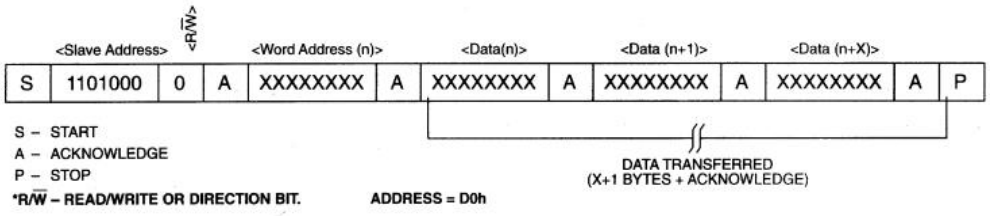
write bit,

the master transmits a register address to the DS1307ZN-TDThis will set the register pointer on the DS1307ZN-TD. The master will then begin

transmitting each byte of data with the DS1307ZN-TDacknowledging each byte received.Themaster will

generate a stop condition to terminate the data write.

DATA WRITE - SLAVE RECEIVER MODE Figure 6



2. **Slave transmitter mode(**DS1307ZN-TD**read mode):**The first byte is received and handled as in the slave receiver mode. However, in this mode, the *direction bit will indicate that the transfer direction is

reversed.

Serial data is transmitted on SDA by the DS1307ZN-TDwhile the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (See

Figure 7). The address byte is the first byte received after the start condition is generated by the

master. The address byte contains the 7-bit DS1307ZN-TDaddress,

which is 1101000,followed by the

*direction bit (R/W) which, for a read, is a 1. After receiving and decoding the address byte the

device inputs an acknowledge on the SDA line.

The DS1307ZN-TDthen begins to transmit data starting

with the register address pointed to by the register pointer. If the register pointer is not written to

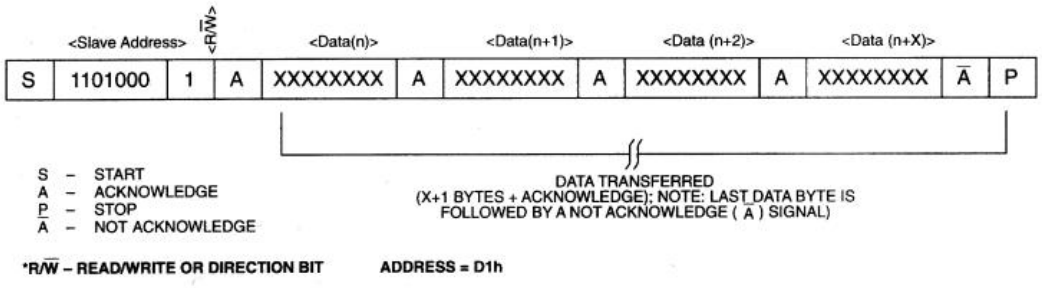
before the initiation of a read mode the first address that is read is the last one stored in the

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register

pointer. The DS1307ZN-TDmust receive a Not Acknowledge to end a read.

DATA READ - SLAVE TRANSMITTER MODE Figure 7



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	0° C to 70° C (-40° C to 85° C for industrial)
Storage Temperature	-55° C to +125° C
Soldering Temperature	260° C for 10 seconds DIP See JPC/JEDEC Standard J-STD-020A for Surface Mount Devices

* This is a stress rating only and functional operation of the device at these or any other conditions above

those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0° C to 70° C or -40° C to +85° C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
VBAT Battery Voltage	V_{BAT}	2.0		3.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0° C to 70° C or -40° C to +85° C; VCC =4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{LI}			1	uA	10
I/O Leakage	I_{LO}			1	uA	11
Logic 0 Output	V_{OL}			0.4	V	2

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Active Supply Current	I_{CCA}			1	mA	9
Standby Current	I_{CCS}			500	uA	3
Battery Current (OSC ON); SQW/OUT OFF	I_{BAT1}		1	2	uA	4
Battery Current (OSC ON); SQW/OUT ON (32 kHz)	I_{BAT2}		1.2	2	uA	4

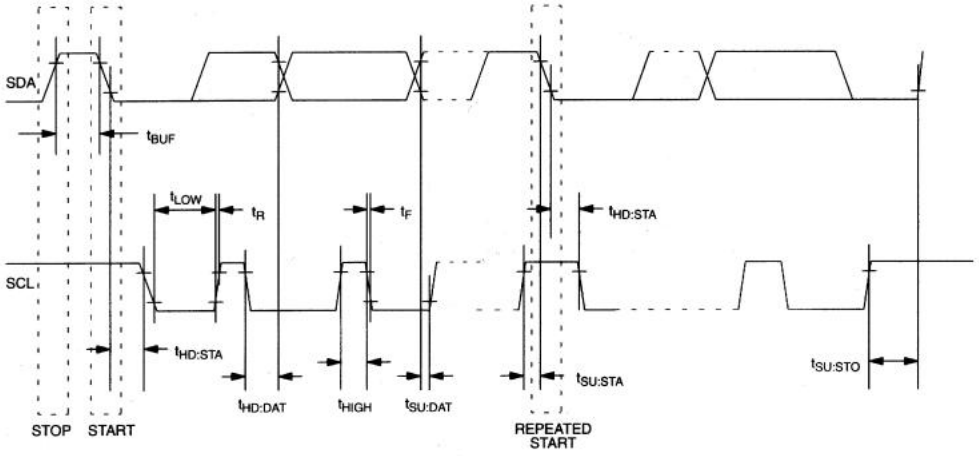
AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
SCL Clock Frequency	f_{SCL}	0		100	kHz	
Bus Free Time Between a STOP and START Condition	t_{BUF}	4.7		1	us	
Hold Time (Repeated) START Condition	$t_{HD:STA}$	4.0			us	5
LOW Period of SCL Clock	t_{LOW}	4.7			us	
HIGH Period of SCL Clock	t_{HIGH}	4.0			us	
Set-up Time for a Repeated START Condition	$t_{SU:STA}$	4.7			us	
Data Hold Time	$t_{HD:DAT}$	0			us	6,7
Data Set-up Time	$t_{SU:DAT}$	250			ns	
Rise Time of Both SDA and SCL Signals	t_R			1000	ns	
Fall Time of Both SDA and SCL Signals	t_F			300	ns	
Set-up Time for STOP Condition	$t_{SU:STO}$	4.7			us	
Capacitive Load for each Bus Line	C_B			400	pF	8
I/O Capacitance	$C_{I/O}$		10		pF	
Crystal Specified Load Capacitance			12.5		pF	

NOTES:

1. All voltages are referenced to ground.
2. Logic zero voltages are specified at a sink current of 5 mA at V_{CC}=4.5V, V_{OL}=GND for capacitiveloads.
3. I_{CCS} specified with V_{CC}=5.0V and SDA, SCL=5.0V.
4. V_{CC}=0V, V_{BAT}=3V.
5. After this period, the first clock pulse is generated.
6. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIHMIN of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
7. The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
8. CB - total capacitance of one bus line in pF.
9. I_{CCA} - SCL clocking at max frequency = 100 kHz.
10. SCL only.
11. SDA and SQW/OUT

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TIMING DIAGRAM Figure 8

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