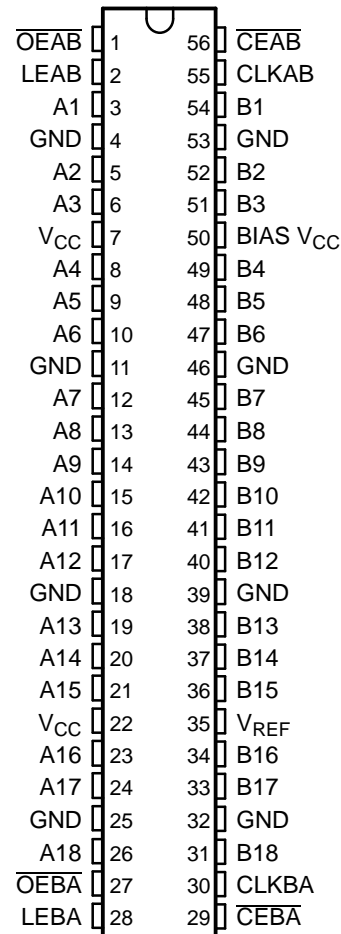


FEATURES

- Member of the Texas Instruments Widebus™ Family
- UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, and Clock-Enabled Modes
- TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes
- OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference
- Bidirectional Interface Between GTLP Signal Levels and LVTTTL Logic Levels
- LVTTTL Interfaces Are 5-V Tolerant
- Medium-Drive GTLP Outputs (50 mA)
- LVTTTL Outputs (–24 mA/24 mA)
- GTLP Rise and Fall Times Designed for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads
- I_{off} , Power-Up 3-State, and BIAS V_{CC} Support Live Insertion
- Bus Hold on A-Port Data Inputs
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DGG OR DGV PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The SN74GTLPH16912 is a medium-drive, 18-bit UBT™ transceiver that provides LVTTTL-to-GTLP and GTLP-to-LVTTTL signal-level translation. It allows for transparent, latched, clocked, and clock-enabled modes of data transfer. The device provides a high-speed interface between cards operating at LVTTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard TTL or LVTTTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The medium drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 19 Ω.

GTLP is the Texas Instruments (TI™) derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH16912 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL ($V_{TT} = 1.2$ V and $V_{REF} = 0.8$ V) or GTLP ($V_{TT} = 1.5$ V and $V_{REF} = 1$ V) signal levels.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTTL logic levels, but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B-port differential input reference voltage.

This device is fully specified for live-insertion applications using I_{off} , power-up 3-state, and BIAS V_{CC} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

Active bus-hold circuitry holds unused or undriven LVTTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable (\overline{OE}) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTLPH16912GR	GTLPH16912
	TVSOP – DGV	Tape and reel	SN74GTLPH16912VR	GL912

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTIONAL DESCRIPTION

The SN74GTLPH16912 is a medium-drive (50-mA), 18-bit UBT transceiver containing D-type latches and D-type flip-flops for data-path operation in transparent, latched, clocked, or clock-enabled modes and can replace any of the functions shown in Table 1. Data polarity is noninverting.

Table 1. SN74GTLPH16912 UBT Transceiver Replacement Functions

FUNCTION	8 BIT	9 BIT	10 BIT	16 BIT	18 BIT
Transceiver	'245, '623, '645	'863	'861	'16245, '16623	'16863
Buffer/driver	'241, '244, '541		'827	'16241, '16244, '16541	'16825
Latched transceiver	'543			'16543	'16472
Latch	'373, '573	'843	'841	'16373	'16843
Registered transceiver	'646, '652			'16646, '16652	'16474
Flip-flop	'374, '574		'821	'16374	
Standard UBT					'16500, '16501
Universal bus driver					'16835
Registered transceiver with clock enable	'2952			'16470, '16952	
Flip-flop with clock enable	'377	'823			'16823
Standard UBT with clock enable					'16600, '16601
SN74GTLPH16912 UBT transceiver replaces all above functions					

Data flow in each direction is controlled by clock enables (\overline{CEAB} and \overline{CEBA}), latch enables (LEAB and LEBA), clock (CLKAB and CLKBA), and output enables (\overline{OEAB} and \overline{OEBA}). \overline{CEAB} and \overline{CEBA} and \overline{OEAB} and \overline{OEBA} control the 18 bits of data for the A-to-B and B-to-A directions, respectively.

For A-to-B data flow, when \overline{CEAB} is low, the device operates on the low-to-high transition of CLKAB for the flip-flop and on the high-to-low transition of LEAB for the latch path, i.e., if \overline{CEAB} and LEAB are low, the A data is latched, regardless of the state of CLKAB (high or low). If LEAB is high, the device is in transparent mode. When \overline{OEAB} is low, the outputs are active. When \overline{OEAB} is high, the outputs are in the high-impedance state.

The data flow for B to A is similar to that of A to B, except \overline{CEBA} , \overline{OEBA} , LEBA, and CLKBA are used.

FUNCTION TABLE⁽¹⁾

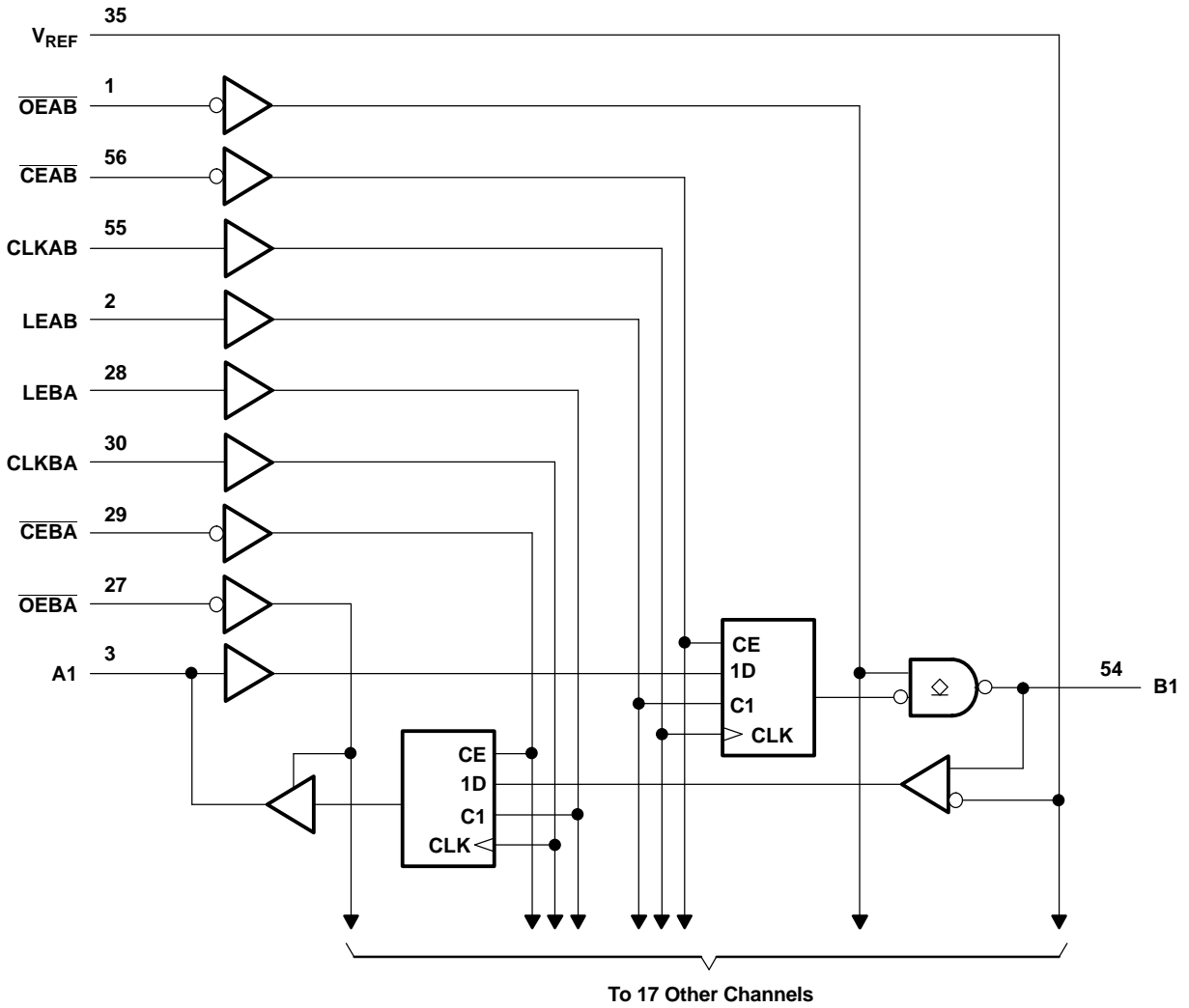
INPUTS					OUTPUT B	MODE
\overline{CEAB}	\overline{OEAB}	LEAB	CLKAB	A		
X	H	X	X	X	Z	Isolation
L	L	L	H	X	$B_0^{(2)}$	Latched storage of A data
L	L	L	L	X	$B_0^{(3)}$	
X	L	H	X	L	L	True transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	$B_0^{(3)}$	Clock inhibit

- (1) A-to-B data flow is shown. B-to-A data flow is similar, but uses \overline{CEBA} , \overline{OEBA} , LEBA, and CLKBA. The condition when \overline{OEAB} and \overline{OEBA} are both low at the same time is not recommended.
- (2) Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low
- (3) Output level before the indicated steady-state input conditions were established

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LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC} BIAS V_{CC}	Supply voltage range	-0.5	4.6	V
V_I	Input voltage range ⁽²⁾	A-port and control inputs		V
		-0.5	7	
		-0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state	A port		V
		-0.5	7	
		-0.5	4.6	
I_O	Current into any output in the low state	A port		mA
			48	
			100	
I_O	Current into any A-port output in the high state ⁽³⁾		48	mA
	Continuous current through each V_{CC} or GND		±100	mA
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	DGG package		°C/W
			64	
			48	
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This current flows only when the output is in the high state and $V_O > V_{CC}$.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

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Recommended Operating Conditions⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

		MIN	NOM	MAX	UNIT
V_{CC} BIAS V_{CC}	Supply voltage	3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.2	1.26	V
		GTLP	1.35	1.65	
V_{REF}	Reference voltage	GTL	0.8	0.87	V
		GTLP	0.87	1.1	
V_I	Input voltage	B port		V_{TT}	V
		Except B port		V_{CC}	
V_{IH}	High-level input voltage	B port	$V_{REF} + 0.05$		V
		Except B port	2		
V_{IL}	Low-level input voltage	B port	$V_{REF} - 0.05$		V
		Except B port	0.8		
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current	A port		-24	mA
I_{OL}	Low-level output current	A port		24	mA
		B port		50	
$\Delta t/\Delta V$	Input transition rise or fall rate	Outputs enabled		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	20			μ s/V
T_A	Operating free-air temperature	-40		85	$^{\circ}$ C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
- (2) Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS $V_{CC} = 3.3$ V first, I/O second, and $V_{CC} = 3.3$ V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.
- (3) V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
- (4) V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT} . TI-OPC circuitry is enabled in the A-to-B direction and is activated when $V_{TT} > 0.7$ V above V_{REF} . If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

Electrical Characteristics

over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IK}		$V_{CC} = 3.15\text{ V}$,	$I_I = -18\text{ mA}$				-1.2	V
V_{OH}	A port	$V_{CC} = 3.15\text{ V to }3.45\text{ V}$,	$I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC} - 0.2$			V
		$V_{CC} = 3.15\text{ V}$	$I_{OH} = -12\text{ mA}$		2.4			
			$I_{OH} = -24\text{ mA}$		2			
V_{OL}	A port	$V_{CC} = 3.15\text{ V to }3.45\text{ V}$,	$I_{OL} = 100\text{ }\mu\text{A}$				0.2	V
		$V_{CC} = 3.15\text{ V}$	$I_{OL} = 12\text{ mA}$				0.4	
			$I_{OL} = 24\text{ mA}$				0.5	
	B port	$V_{CC} = 3.15\text{ V to }3.45\text{ V}$,	$I_{OL} = 100\text{ }\mu\text{A}$				0.2	
		$V_{CC} = 3.15\text{ V}$	$I_{OL} = 10\text{ mA}$				0.2	
			$I_{OL} = 40\text{ mA}$				0.4	
		$I_{OL} = 50\text{ mA}$				0.55		
$I_I^{(2)}$	A-port and control inputs	$V_{CC} = 3.45\text{ V}$	$V_I = 0\text{ or }V_{CC}$				± 10	μA
	B port		$V_I = 5.5\text{ V}$				± 20	
			$V_I = 0\text{ to }1.5\text{ V}$				± 10	
$I_{BHL}^{(3)}$	A port	$V_{CC} = 3.15\text{ V}$,	$V_I = 0.8\text{ V}$		75		μA	
$I_{BHH}^{(4)}$	A port	$V_{CC} = 3.15\text{ V}$,	$V_I = 2\text{ V}$		-75		μA	
$I_{BHLO}^{(5)}$	A port	$V_{CC} = 3.45\text{ V}$,	$V_I = 0\text{ to }V_{CC}$		500		μA	
$I_{BHHO}^{(6)}$	A port	$V_{CC} = 3.45\text{ V}$,	$V_I = 0\text{ to }V_{CC}$		-500		μA	
I_{CC}	A or B port	$V_{CC} = 3.45\text{ V}$, $I_O = 0$, V_I (A-port or control input) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high		50		mA	
			Outputs low		50			
			Outputs disabled		50			
$\Delta I_{CC}^{(7)}$		$V_{CC} = 3.45\text{ V}$, One A-port or control input at $V_{CC} - 0.6\text{ V}$, Other A-port or control inputs at V_{CC} or GND			1.5		mA	
C_i	Control inputs	$V_I = 3.15\text{ V or }0$			4		5.5	pF
C_{io}	A port	$V_O = 3.15\text{ V or }0$			7		8.5	pF
	B port	$V_O = 1.5\text{ V or }0$			8.5		9.5	

- (1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.
- (2) For I/O ports, the parameter I_I includes the off-state output leakage current.
- (3) The bus-hold circuit can sink at least the minimum low sustaining current at V_{ILmax} . I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{ILmax} .
- (4) The bus-hold circuit can source at least the minimum high sustaining current at V_{IHmin} . I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IHmin} .
- (5) An external driver must source at least I_{BHLO} to switch this node from low to high.
- (6) An external driver must sink at least I_{BHHO} to switch this node from high to low.
- (7) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Hot-Insertion Specifications for A Port

over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	$V_{CC} = 0$,	BIAS $V_{CC} = 0$,	V_I or $V_O = 0\text{ to }5.5\text{ V}$	10		μA
I_{OZPU}	$V_{CC} = 0\text{ to }1.5\text{ V}$,	$V_O = 0.5\text{ V to }3\text{ V}$,	$\overline{OE} = 0$	± 30		μA
I_{OZPD}	$V_{CC} = 1.5\text{ V to }0$,	$V_O = 0.5\text{ V to }3\text{ V}$,	$\overline{OE} = 0$	± 30		μA

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Live-Insertion Specifications for B Port

over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
I_{off}	$V_{CC} = 0,$	BIAS $V_{CC} = 0,$	V_I or $V_O = 0$ to 1.5 V		10 μA
I_{OZPU}	$V_{CC} = 0$ to 1.5 V,	BIAS $V_{CC} = 0,$	$V_O = 0.5$ V to 1.5 V, $\overline{OE} = 0$		± 30 μA
I_{OZPD}	$V_{CC} = 1.5$ V to 0,	BIAS $V_{CC} = 0,$	$V_O = 0.5$ V to 1.5 V, $\overline{OE} = 0$		± 30 μA
I_{CC} (BIAS V_{CC})	$V_{CC} = 0$ to 3.15 V	BIAS $V_{CC} = 3.15$ V to 3.45 V,	V_O (B port) = 0 to 1.5 V		5 mA
	$V_{CC} = 3.15$ V to 3.45 V				10 μA
V_O	$V_{CC} = 0,$	BIAS $V_{CC} = 3.3$ V,	$I_O = 0$		0.95 1.05 V
I_O	$V_{CC} = 0,$	BIAS $V_{CC} = 3.15$ V to 3.45 V,	V_O (B port) = 0.6 V		-1 μA

Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature,

$V_{TT} = 1.5$ V and $V_{REF} = 1$ V for GTLP (unless otherwise noted)

		MIN	MAX	UNIT
f_{clock}	Clock frequency	175		MHz
t_w	Pulse duration	LEAB or LEBA high	2.8	ns
		CLKAB or CLKBA high or low	2.8	
t_{su}	Setup time	A before CLKAB \uparrow	1.8	ns
		B before CLKBA \uparrow	1.5	
		A before LEAB \downarrow	1	
		B before LEBA \downarrow	2	
		\overline{CEAB} before CLKAB \uparrow	1.5	
		\overline{CEBA} before CLKBA \uparrow	1.4	
t_h	Hold time	A after CLKAB \uparrow	0.3	ns
		B after CLKBA \uparrow	0.4	
		A after LEAB \downarrow	1.1	
		B after LEBA \downarrow	0.4	
		\overline{CEAB} after CLKAB \uparrow	1	
		\overline{CEBA} after CLKBA \uparrow	1	

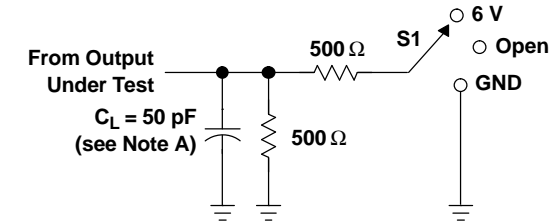
Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature,
 $V_{TT} = 1.5\text{ V}$ and $V_{REF} = 1\text{ V}$ for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP ⁽¹⁾	MAX	UNIT
f_{max}			175			MHz
t_{PLH}	A	B	2.1		6	ns
t_{PHL}			2.1		6	
t_{PLH}	LEAB	B	2.2		6.3	ns
t_{PHL}			2.2		6.3	
t_{PLH}	CLKAB	B	2.2		6.5	ns
t_{PHL}			2.2		6.5	
t_{en}	\overline{OEAB}	B	2		6.5	ns
t_{dis}			2		6.1	
t_r	Rise time, B outputs (20% to 80%)		2.4			ns
t_f	Fall time, B outputs (80% to 20%)		2			ns
t_{PLH}	B	A	1.8		5.8	ns
t_{PHL}			1.8		5.8	
t_{PLH}	LEBA	A	0.4		5.3	ns
t_{PHL}			0.4		5.3	
t_{PLH}	CLKBA	A	0.6		5.6	ns
t_{PHL}			0.6		5.7	
t_{en}	\overline{OEBA}	A	0.3		6.2	ns
t_{dis}			0.3		5.9	

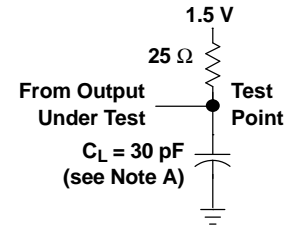
(1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION

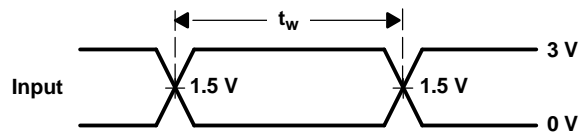


LOAD CIRCUIT FOR A OUTPUTS

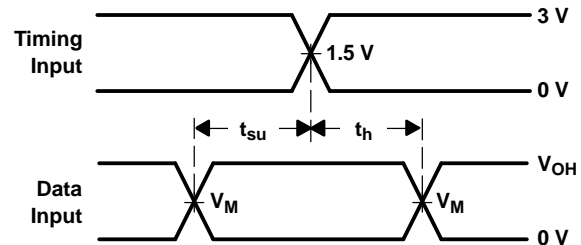
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



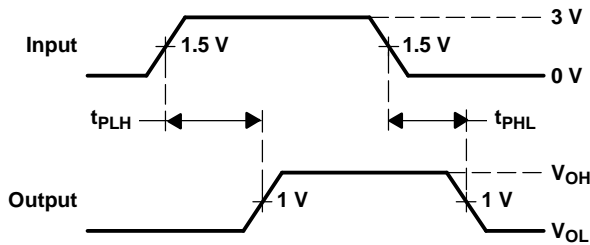
LOAD CIRCUIT FOR B OUTPUTS



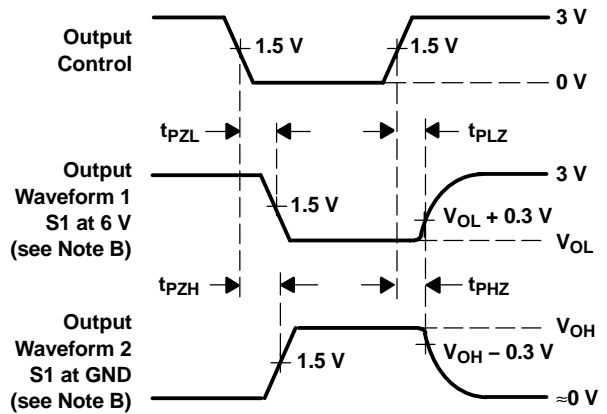
VOLTAGE WAVEFORMS
PULSE DURATION



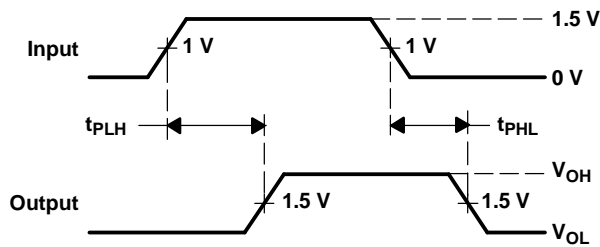
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
($V_M = 1.5$ V for A port and 1 V for B port)
($V_{OH} = 3$ V for A port and 1.5 V for B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR \approx 10 MHz, $Z_O = 50 \Omega$, $t_r \approx 2$ ns, $t_f \approx 2$ ns.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

Distributed-Load Backplane Switching Characteristics

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

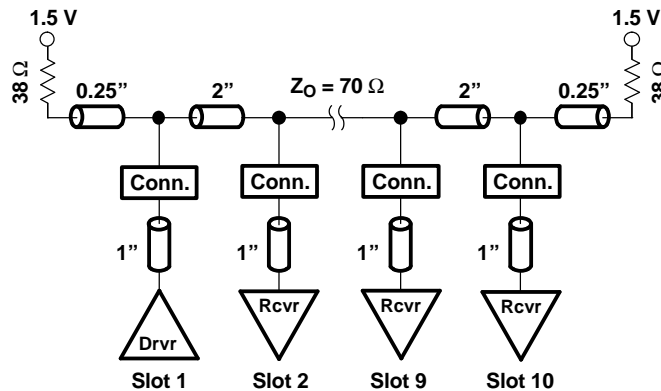


Figure 2. Medium-Drive Test Backplane

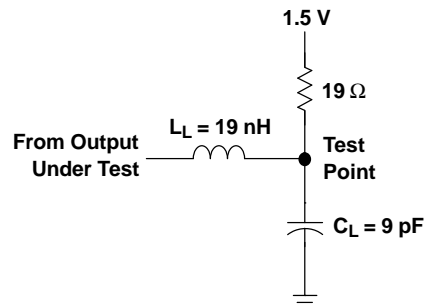


Figure 3. Medium-Drive RLC Network

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Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature,
 $V_{TT} = 1.5\text{ V}$ and $V_{REF} = 1\text{ V}$ for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TYP ⁽¹⁾	UNIT
t_{PLH}	A	B	4.5	ns
t_{PHL}			4.5	
t_{PLH}	LEAB	B	4.7	ns
t_{PHL}			4.7	
t_{PLH}	CLKAB	B	4.7	ns
t_{PHL}			4.7	
t_{en}	\overline{OEAB}	B	4.8	ns
t_{dis}			4.4	
t_r	Rise time, B outputs (20% to 80%)		1.2	ns
t_f	Fall time, B outputs (80% to 20%)		2.5	ns

(1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$. All values are derived from TI-SPICE models.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74GTLPH16912GR	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GTLPH16912
SN74GTLPH16912GR.B	Active	Production	null (null)	2000 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See SN74GTLPH16912GR	GTLPH16912
SN74GTLPH16912GRG4.B	Active	Production	null (null)	2000 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See SN74GTLPH16912GRG4	GTLPH16912

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

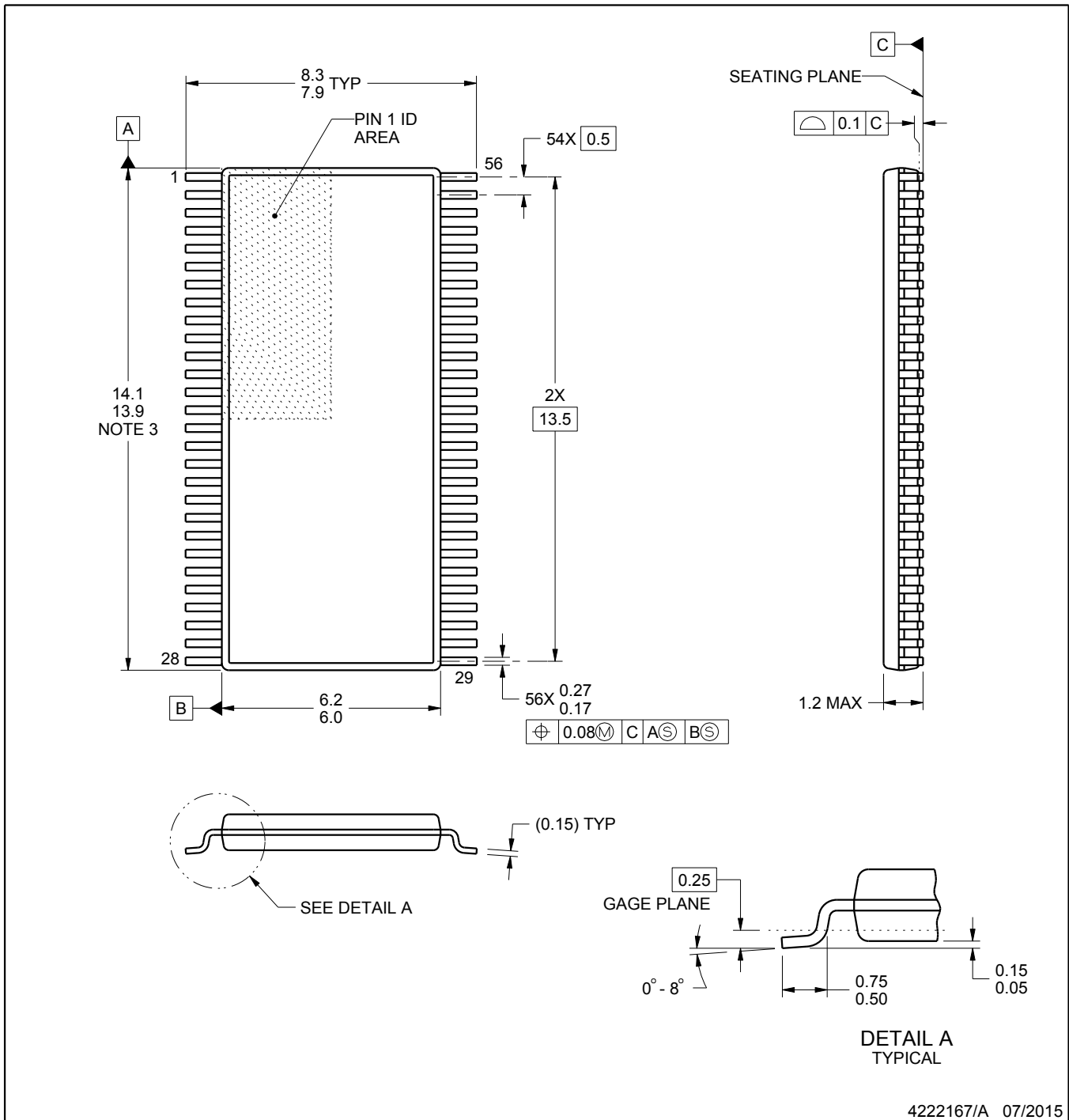
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74GTLPH16912GR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74GTLPH16912GR	TSSOP	DGG	56	2000	367.0	367.0	45.0



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NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

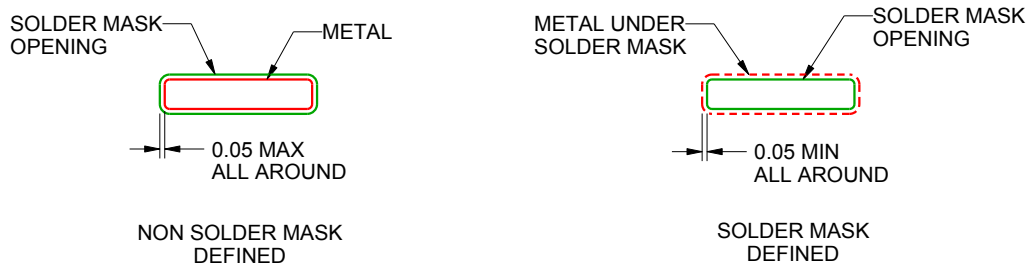
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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