Broadband, Fully-Differential, 14-/16-Bit ADC DRIVER AMPLIFIER

Check for Samples: THS770006

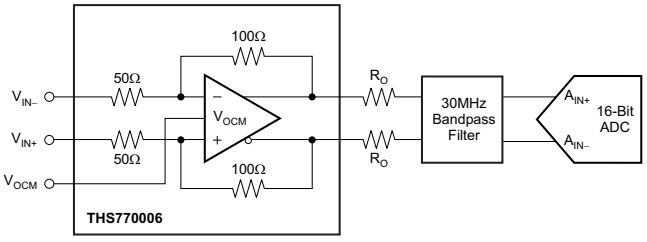
FEATURES

- **2.4GHz Bandwidth**
- **3100V/µs Slew Rate, V_{OUT} =2V Step**
- **Fixed Voltage Gain: +6dB**
- **IMD_3: –107dBc, V_{OUT} = $2V_{PP}$, R_L = 400Ω, f = 100MHz**
- **OIP3: 48dBm, f = 100MHz**
- **Noise Figure: 11dB, f = 100MHz**

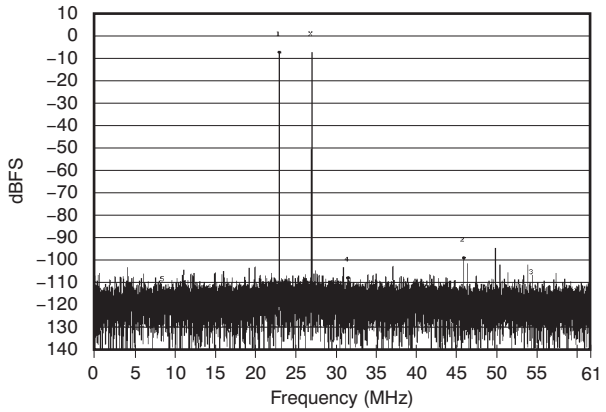
APPLICATIONS

- **14-/16-bit ADC Driver**
- **ADC Driver for Wireless Base Station Signal Chains: GSM, WCDMA, MC-GSM**
- **ADC Driver for High Dynamic Range Test and Measurement Equipment**

THS770006 Driving 16-Bit ADC



FFT Plot with Two-Tone Input at 96MHz and 100MHz (see *Application Information* section).



DESCRIPTION

The THS770006 is a fixed-gain of +6dB, wideband, fully-differential amplifier designed and optimized specifically for driving 16-bit analog-to-digital converters (ADCs) at input frequencies up to 130MHz, and 14-bit ADCs at input frequencies up to 200MHz. This device provides high bandwidth, high-voltage output with low distortion and low noise, critical in high-speed data acquisition systems that require very high dynamic range, such as wireless base stations and test and measurement applications. This device also makes an excellent differential amplifier for general-purpose, high-speed differential signal chain and short line driver applications.

The THS770006 operates on a nominal +5V single supply, offers very fast, 7.5ns maximum recovery time from overdrive conditions, and has a power-down mode for power saving. The THS770006 is offered in a Pb-free (RoHS compliant) and green, QFN-24 thermally-enhanced package. It is characterized for operation over the industrial temperature range of –40°C to +85°C.

RELATED DEVICES

DEVICE	DESCRIPTION
THS4509	Wideband, low-noise, low-distortion, fully-differential amplifier
PGA870	Wideband, low-noise, low-distortion, fully-differential, digitally-programmable gain amplifier
ADS5481 to ADS5485	16-bit, 80MSPS to 200MSPS ADCs
ADS6145	14-bit, 125MSPS ADC
ADS6149	14-bit, 250MSPS ADC

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

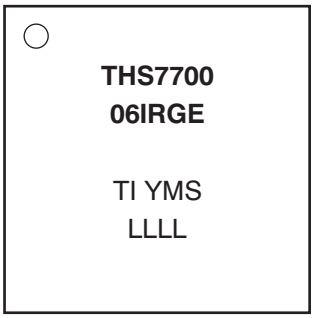
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE TYPE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
THS770006	VQFN-24	RGE	–40°C to +85°C	THS770006IGRE	THS770006IRGET	Tape and reel, 250
				THS770006IGRE	THS770006IRGER	Tape and reel, 3000

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

DEVICE MARKING INFORMATION



◯ = Pin 1 designator
THS770006IRGE = device name
TI = TI LETTERS
YM = YEAR MONTH DATE CODE
S = ASSEMBLY SITE CODE
LLLL = ASSY LOT CODE

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		THS770006	UNIT
Power supply (V_{S+} to GND)		5.5	V
Input voltage range		Ground to V_{S+}	V
Differential input voltage, V_{ID}		Ground to V_{S+}	V
Continuous input current, I_I		10	mA
Continuous output current, I_O		100	mA
Storage temperature range, T_{stg}		–40°C to +125°C	°C
Maximum junction temperature, T_J		+150	°C
Maximum junction temperature, continuous operation, long term reliability		+125	°C
ESD ratings	Human body model (HBM)	2500	V
	Charged device model (CDM)	1000	V
	Machine model (MM)	100	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

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THERMAL INFORMATION

THERMAL METRIC(1)		THS770006 RGE 24 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	44.1	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	35	
θ_{JB}	Junction-to-board thermal resistance	19	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	18.8	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	8.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

Test conditions are at T_A = +25°C, V_{S+} = +5V, V_{OCM} = +2.5V, V_{OUT} = $2V_{PP}$, R_L = 400Ω differential, G = +6dB, differential input and output, and input and output referenced to midsupply, unless otherwise noted. Measured using evaluation module as discussed in *Test Circuits* section.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE							
Small-signal bandwidth	V_{OUT} = $200mV_{PP}$			2.4		GHz	C
Large-signal bandwidth	V_{OUT} = $2V_{PP}$			780		MHz	C
	V_{OUT} = $3V_{PP}$			485		MHz	C
Bandwidth for 0.1dB flatness	V_{OUT} = $2V_{PP}$			360		MHz	C
	V_{OUT} = $3V_{PP}$			325		MHz	C
Slew rate	V_{OUT} = 2V step			3100		V/µs	C
	V_{OUT} = 4V step			3200		V/µs	C
Rise time	V_{OUT} = 2V step			0.6		ns	C
Fall time	V_{OUT} = 2V step			0.6		ns	C
Settling time to 0.1%	V_{OUT} = 2V step			2.2		ns	C
Input return loss, s11	See *s-Parameters* section, f < 200MHz			–20		dB	C
Output return loss, s22	See *s-Parameters* section, f < 200MHz			–20		dB	C
Reverse isolation, s12	See *s-Parameters* section, f < 200MHz			–70		dB	C
Second-order harmonic distortion	f = 10MHz			–87		dBc	C
	f = 50MHz			–81		dBc	C
	f = 100MHz			–78		dBc	C
	f = 200MHz			–74		dBc	C
Third-order harmonic distortion	f = 10MHz			–103		dBc	C
	f = 50MHz			–91		dBc	C
	f = 100MHz			–86		dBc	C
	f = 200MHz			–77		dBc	C
Second-order intermodulation distortion	f = 50MHz, 10MHz spacing			–80		dBc	C
	f = 100MHz, 10MHz spacing			–79		dBc	C
	f = 150MHz, 10MHz spacing			–77		dBc	C
	f = 200MHz, 10MHz spacing			–76		dBc	C
Third-order intermodulation distortion	f = 50MHz, 10MHz spacing			–107		dBc	C
	f = 100MHz, 10MHz spacing			–107		dBc	C
	f = 150MHz, 10MHz spacing			–97		dBc	C
	f = 200MHz, 10MHz spacing			–82		dBc	C
1dB compression point	f = 100MHz	R_L = 20Ω		19.6		dBm	C
		R_L = 400Ω		8.7		dBm	C

(1) Test levels: (A) 100% tested at +25°C. Over-temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

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ELECTRICAL CHARACTERISTICS (continued)

Test conditions are at T_A = +25°C, V_{S+} = +5V, V_{OCM} = +2.5V, V_{OUT} = $2V_{PP}$, R_L = 400Ω differential, G = +6dB, differential input and output, and input and output referenced to midsupply, unless otherwise noted. Measured using evaluation module as discussed in *Test Circuits* section.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL(1)
Output third-order intercept point	At device outputs, R_L = 400Ω, f = 100MHz			48		dBm	C
Input-referred voltage noise	f > 100kHz			1.7		nV/√Hz	C
Ouput-referred voltage noise	f > 100kHz			3.4		nV/√Hz	C
Noise figure	100Ω differential source	f = 50 MHz		10.5		dB	C
		f = 100 MHz		11		dB	C
		f = 200 MHz		13		dB	C
Overdrive recovery	Overdrive = ±0.5V			5	7.5	ns	B
Output balance error	f = 200MHz			–60		dB	C
Output impedance	f = 100MHz			4.4		Ω	C
DC PERFORMANCE							
Gain	T_A = +25°C, R_L = 400Ω		5.75	6	6.25	dB	A
	T_A = +25°C, R_L = 100Ω		5.5	5.7	5.9	dB	B
	T_A = –40°C to +85°C, R_L = 400Ω		5.7		6.3	dB	B
	T_A = –40°C to +85°C, R_L = 100Ω		5.45		5.95	dB	B
Output offset	T_A = +25°C		–10	±1	10	mV	A
	T_A = –40°C to +85°C		–12.5		12.5	mV	B
Common-mode rejection ratio	T_A = +25°C		36	60		dB	A
	T_A = –40°C to +85°C		35			dB	B
INPUT							
Differential input resistance			85	100	115	Ω	A
Input common-mode range	Inputs shorted together, V_{OCM} = 2.5V		2.25		2.75	V	A
	V_{OCM} = 2.5V, V_{OUT} = $3V_{PP}$, HD degradation < 3dB, see Figure 13		1.5		3.1	V	C
OUTPUT							
Most positive output voltage	Each output with 200Ω to midsupply	T_A = +25°C	3.64	3.7		V	A
		T_A = –40°C to +85°C	3.59			V	B
Least positive output voltage	Each output with 200Ω to midsupply	T_A = +25°C		1.3	1.4	V	A
		T_A = –40°C to +85°C			1.45	V	B
Most positive output voltage	Each output with 50Ω to midsupply	T_A = +25°C	3.59	3.6		V	A
		T_A = –40°C to +85°C	3.54			V	B
Least positive output voltage	Each output with 50Ω to midsupply	T_A = +25°C		1.3	1.5	V	A
		T_A = –40°C to +85°C			1.55	V	B
Differential output voltage	T_A = +25°C, R_L = 400Ω		4.4	4.85		V_{PP}	B
	T_A = –40°C to +85°C, R_L = 400Ω		4.2			V_{PP}	B
Differential output current drive	T_A = +25°C, R_L = 10Ω			80		mA	B
	T_A = –40°C to +85°C, R_L =10Ω			80		mA	B
OUTPUT COMMON-MODE VOLTAGE CONTROL							
V_{OCM} small-signal bandwidth	V_{OUT_CM} = $200mV_{PP}$			525		MHz	C
V_{OCM} slew rate	V_{OUT_CM} = $500mV_{PP}$			180		V/µs	C
V_{OCM} voltage range	Supplied by external source(2)		2.25	2.5	2.75	V	C
V_{OCM} gain	V_{OCM} = 2.5V		0.98	1	1.02	V/V	A
Output common-mode offset from V_{OCM} input	V_{OCM} = 2.5V		–30	12	30	mV	A
V_{OCM} input bias current	2.25V ≤ V_{OCM} ≤ 2.75V		–400	±30	400	µA	A

(2) Limits set by best harmonic distortion with V_{OUT} = $3V_{PP}$. V_{OCM} voltage range can be extended if lower output swing is used or distortion degradation is allowed, and increased bias current into pin is acceptable. For more information, see Figure 12 and Figure 31.

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ELECTRICAL CHARACTERISTICS (continued)

Test conditions are at T_A = +25°C, V_{S+} = +5V, V_{OCM} = +2.5V, V_{OUT} = $2V_{PP}$, R_L = 400Ω differential, G = +6dB, differential input and output, and input and output referenced to midsupply, unless otherwise noted. Measured using evaluation module as discussed in *Test Circuits* section.

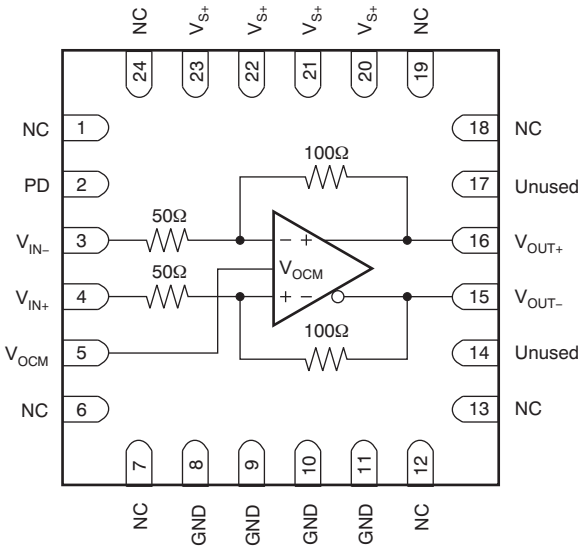
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
POWER SUPPLY						
Specified operating voltage		4.75	5	5.25	V	C
Quiescent current	T_A = +25°C	85	100	115	mA	A
	T_A = –40°C to +85°C	80		125	mA	B
Power-supply rejection ratio	T_A = +25°C, VCC ±0.25V	60	90		dB	A
	T_A = –40°C to +85°C, VCC ±0.5V	59			dB	B
POWER-DOWN						
Enable voltage threshold	Device powers on below 0.5V			0.5	V	A
Disable voltage threshold	Device powers down above 2.0V	2			V	A
Power-down quiescent current			0.8	3	mA	A
Input bias current			80	100	µA	A
Turn-on time delay	Time to V_{OUT} = 90% of final value		10		µs	C
Turn-off time delay	Time to V_{OUT} = 10% of original value		0.15		µs	C
THERMAL CHARACTERISTICS						
Specified operating range		–40		+85	°C	C
Thermal resistance, θ_{JC}(3)	Junction to case (bottom)		8.9		°C/W	C
Thermal resistance, θ_{JA}(3)	Junction to ambient		44.1		°C/W	C

(3) Tested using JEDEC High-K test PCB. Thermal management of the final printed circuit board (PCB) should keep the junction temperature below +125°C for long term reliability.

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PIN CONFIGURATION

RGE PACKAGE
VQFN-24
(TOP VIEW)



PIN DESCRIPTIONS

PIN		DESCRIPTION
NO.	NAME	
1	NC	No internal connection
2	PD	Power down. High = low power (sleep) mode. Low = active.
3	$V_{IN–}$	Inverting input pin
4	V_{IN+}	Noninverting input pin
5	V_{OCM}	Output common-mode voltage control input pin
6, 7	NC	No internal connection
8, 9, 10, 11	GND	Ground. Must be connected to thermal pad.
12, 13	NC	No internal connection
14	Unused	Bonded to die, but not used. Tie to GND.
15	$V_{OUT–}$	Inverting output pin
16	V_{OUT+}	Noninverting output pin
17	Unused	Bonded to die, but not used. Tie to GND.
18, 19	NC	No internal connection
20, 21, 22, 23	V_{S+}	Power supply pins, +5V nominal
24	NC	No internal connection
Thermal pad		Thermal pad on bottom of device is used for heat dissipation and must be tied to GND

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TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS

At T_A = +25°C, V_{S+} = +5V, V_{OCM} = +2.5V, V_{OUT} = $2V_{PP}$, R_L = 400Ω differential, G = +6dB, differential input and output, and input and output pins referenced to midsupply, unless otherwise noted. Measured using EVM as discussed in *Test Circuits* section.

FREQUENCY RESPONSE MAGNITUDE (WITH TRANSFORMERS)

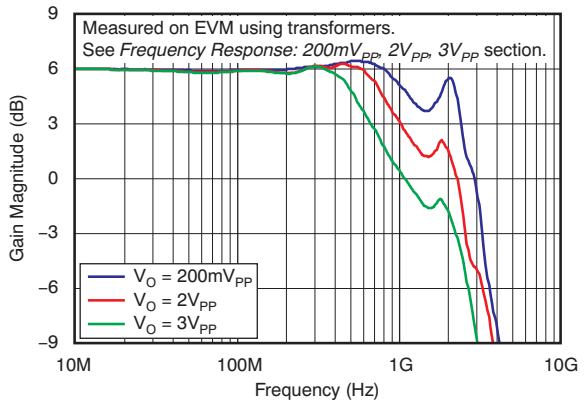


Figure 1.

FREQUENCY RESPONSE MAGNITUDE (NO TRANSFORMERS)

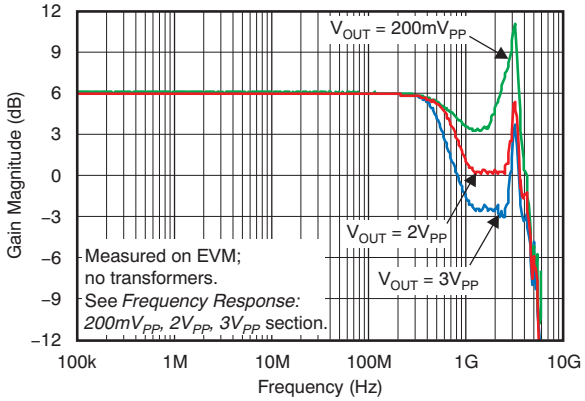


Figure 2.

FREQUENCY RESPONSE PHASE (NO TRANSFORMERS)

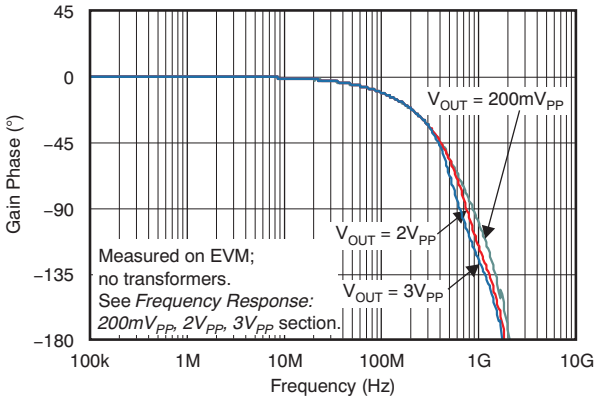


Figure 3.

SMALL- AND LARGE-SIGNAL PULSE RESPONSE

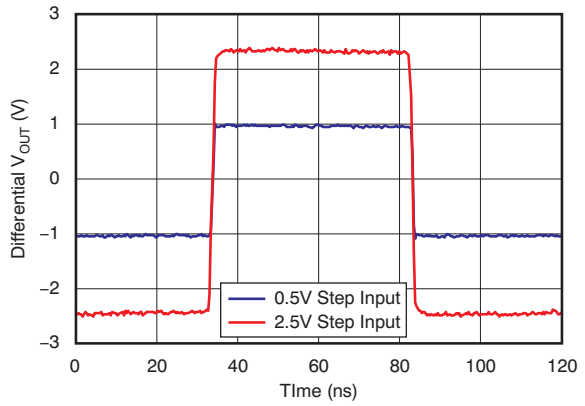


Figure 4.

SLEW RATE vs OUTPUT VOLTAGE STEP

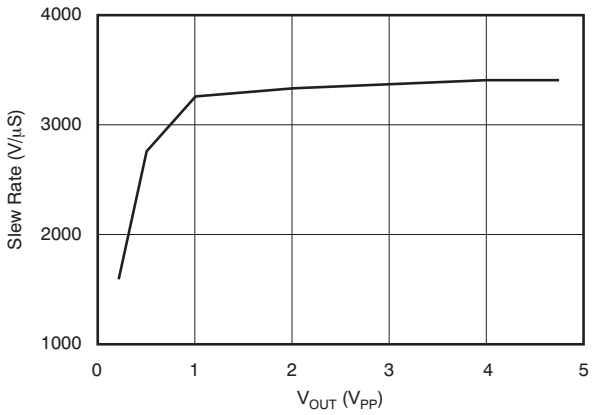


Figure 5.

OVERDRIVE RECOVERY

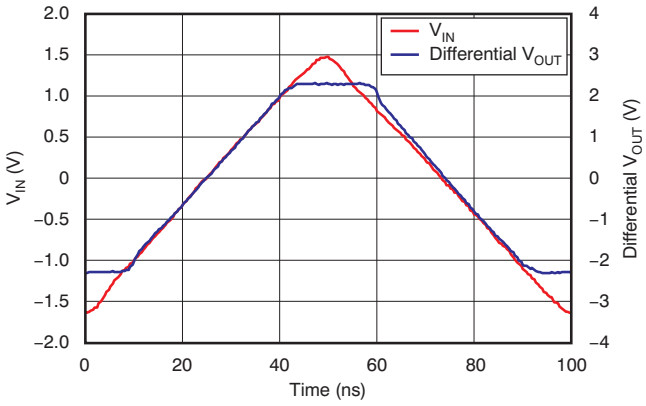


Figure 6.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{S+} = +5V, V_{OCM} = +2.5V, V_{OUT} = 2V_{PP}, R_L = 400Ω differential, G = +6dB, differential input and output, and input and output pins referenced to midsupply, unless otherwise noted. Measured using EVM as discussed in *Test Circuits* section.

SINGLE-ENDED INPUT HARMONIC DISTORTION vs FREQUENCY

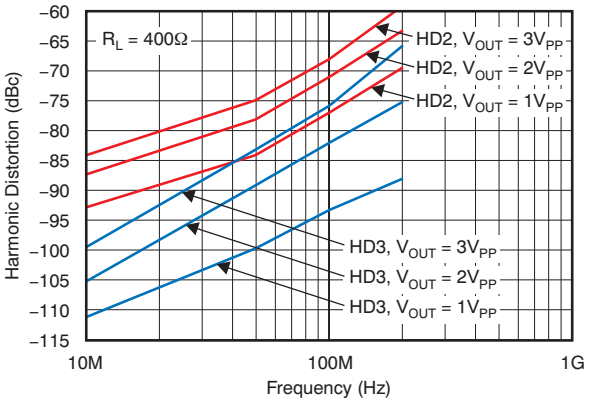


Figure 7.

HARMONIC DISTORTION vs FREQUENCY

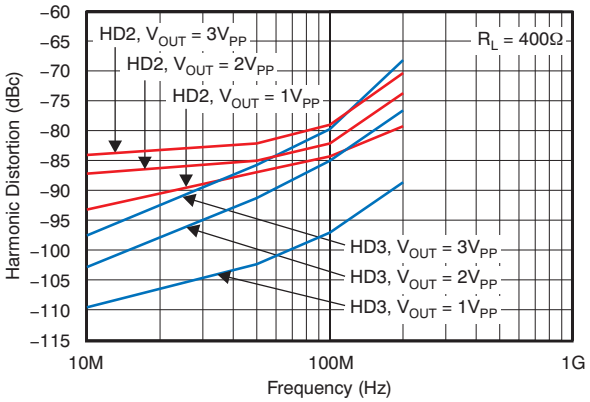


Figure 8.

HARMONIC DISTORTION vs FREQUENCY V_{OUT} = 0.9V_{PP}

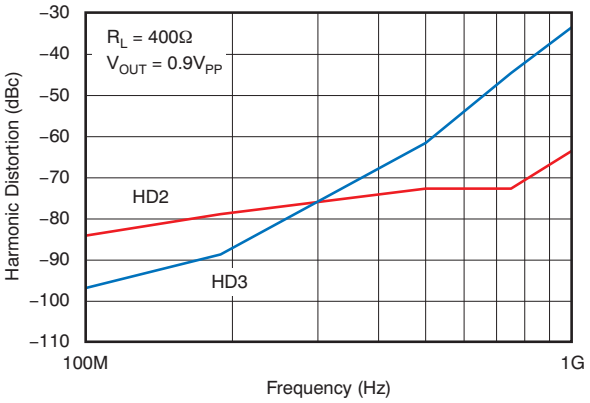


Figure 9.

HARMONIC DISTORTION vs V_{OUT}

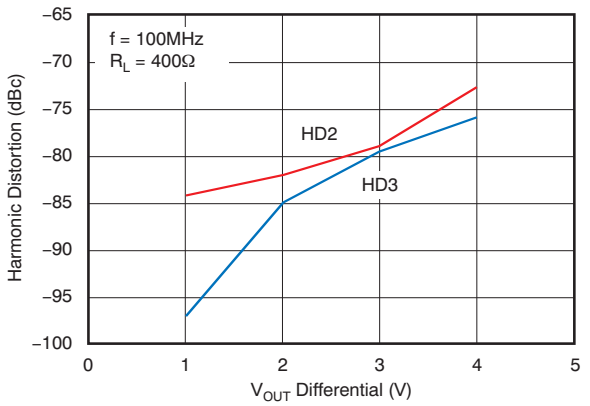


Figure 10.

HARMONIC DISTORTION vs R_L

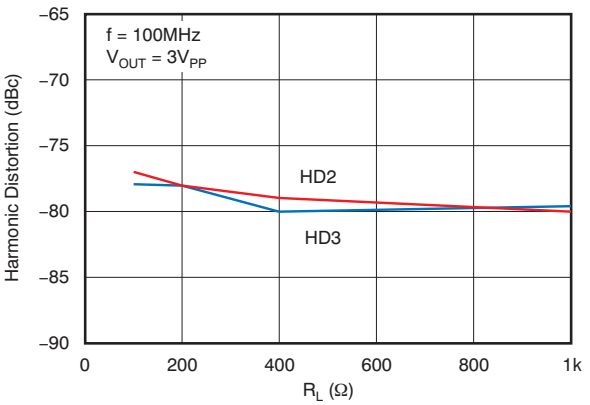


Figure 11.

HARMONIC DISTORTION vs V_{OCM}

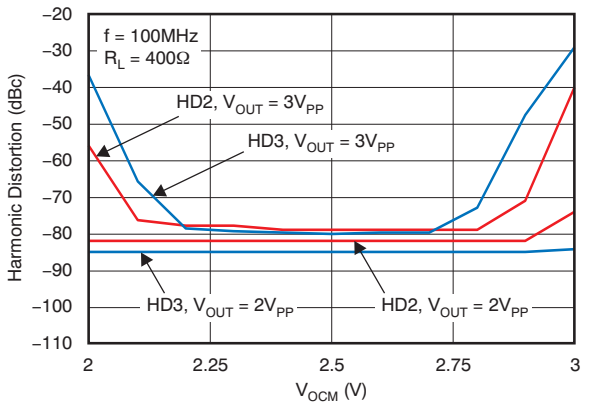


Figure 12.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{S+} = +5V, V_{OCM} = +2.5V, V_{OUT} = 2V_{PP}, R_L = 400Ω differential, G = +6dB, differential input and output, and input and output pins referenced to midsupply, unless otherwise noted. Measured using EVM as discussed in *Test Circuits* section.

HARMONIC DISTORTION vs INPUT COMMON-MODE RANGE

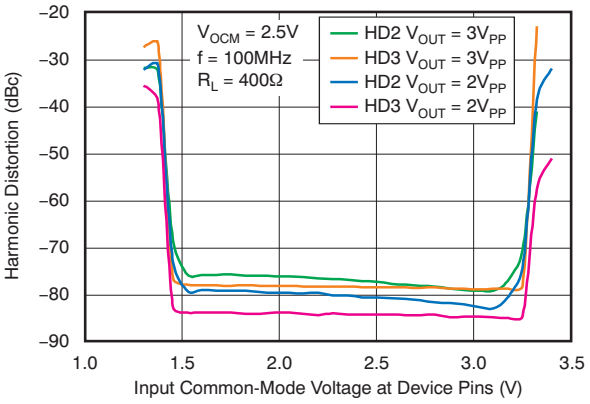


Figure 13.

INTERMODULATION DISTORTION vs FREQUENCY, V_{OUT} = 2V_{PP}, 3V_{PP} ENVELOPE

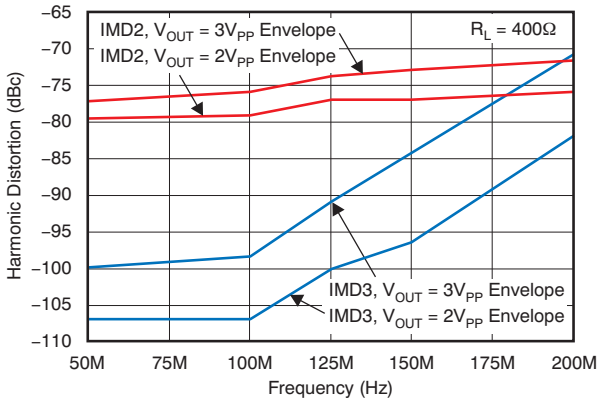


Figure 14.

INTERMODULATION DISTORTION vs FREQUENCY, V_{OUT} = 0.9V_{PP} ENVELOPE

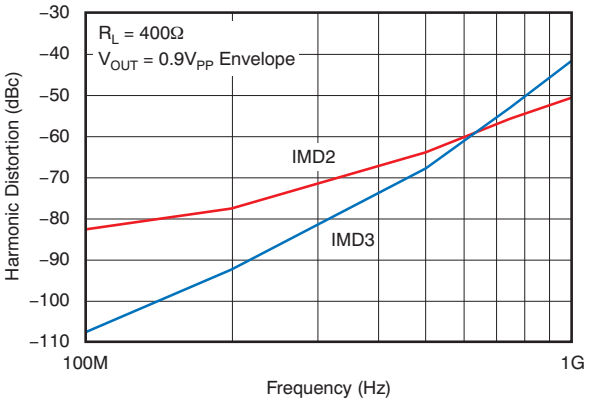


Figure 15.

OUTPUT INTERCEPT POINT vs FREQUENCY

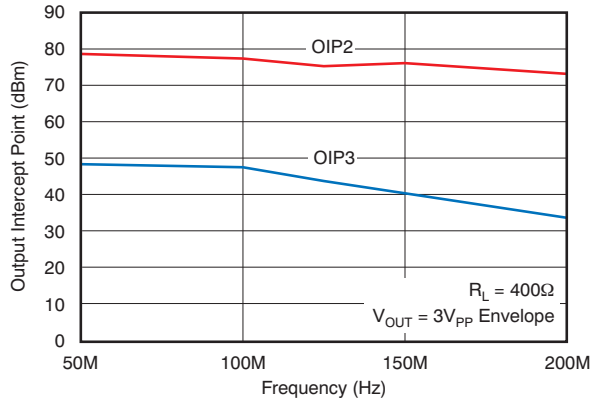


Figure 16.

MAXIMUM DIFFERENTIAL OUTPUT VOLTAGE SWING PEAK-TO-PEAK vs DIFFERENTIAL LOAD RESISTANCE

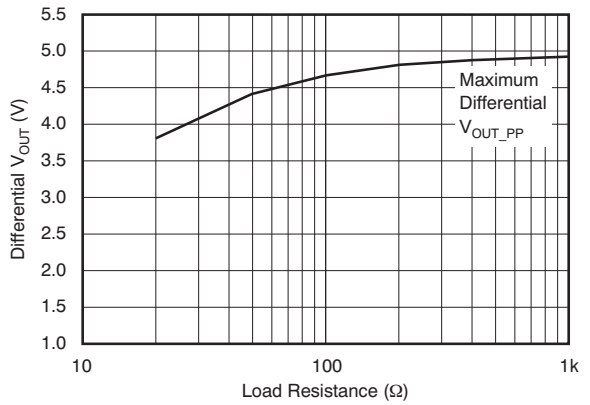


Figure 17.

MAXIMUM/MINIMUM SINGLE-ENDED OUTPUT VOLTAGE vs DIFFERENTIAL LOAD RESISTANCE

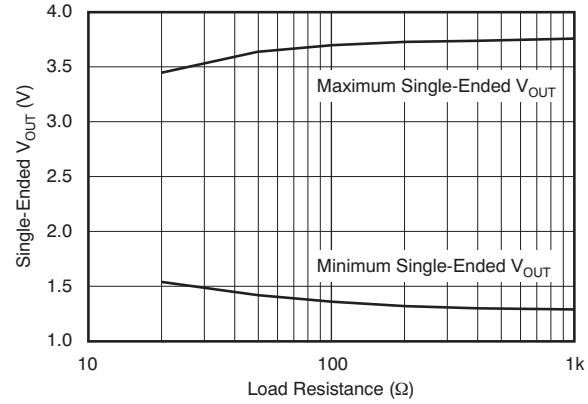


Figure 18.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{S+} = +5V, V_{OCM} = +2.5V, V_{OUT} = $2V_{PP}$, R_L = 400Ω differential, G = +6dB, differential input and output, and input and output pins referenced to midsupply, unless otherwise noted. Measured using EVM as discussed in *Test Circuits* section.

DIFFERENTIAL OUTPUT IMPEDANCE vs FREQUENCY

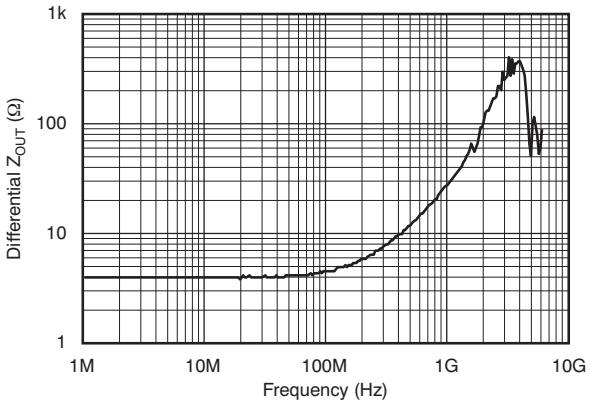


Figure 19.

s-PARAMETERS (MAGNITUDE)

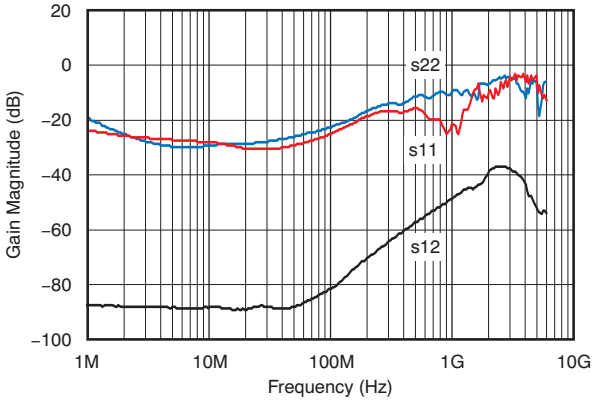


Figure 20.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

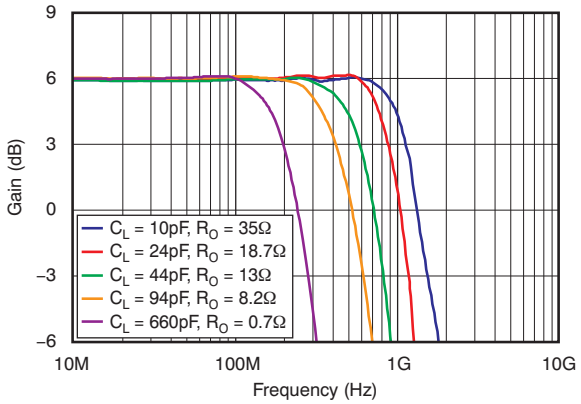


Figure 21.

RECOMMENDED R_O vs CAPACITIVE LOAD

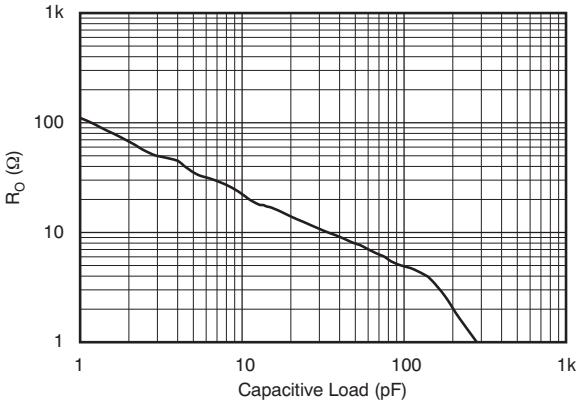


Figure 22.

COMMON-MODE REJECTION RATIO vs FREQUENCY

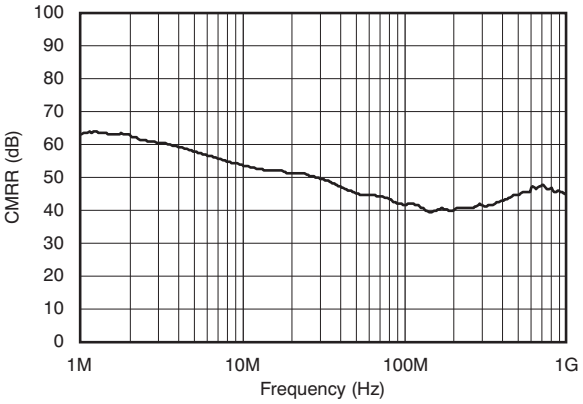


Figure 23.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

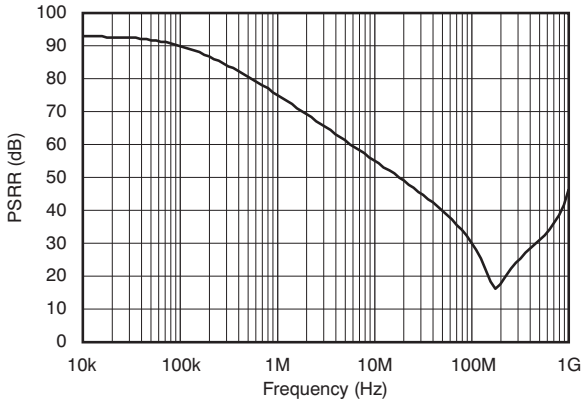


Figure 24.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{S+} = +5V, V_{OCM} = +2.5V, V_{OUT} = $2V_{PP}$, R_L = 400Ω differential, G = +6dB, differential input and output, and input and output pins referenced to midsupply, unless otherwise noted. Measured using EVM as discussed in *Test Circuits* section.

V_{OCM} PULSE RESPONSE

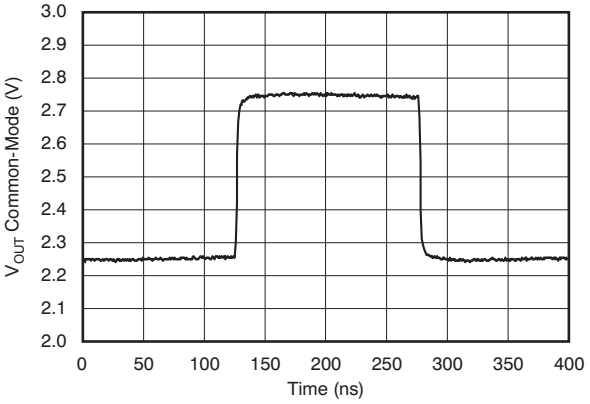


Figure 25.

TURN-ON TIME

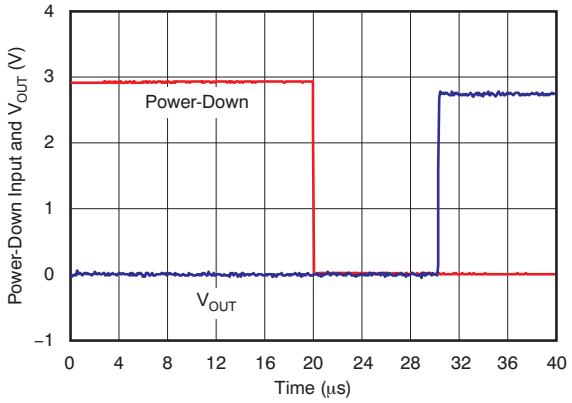


Figure 26.

TURN-OFF TIME

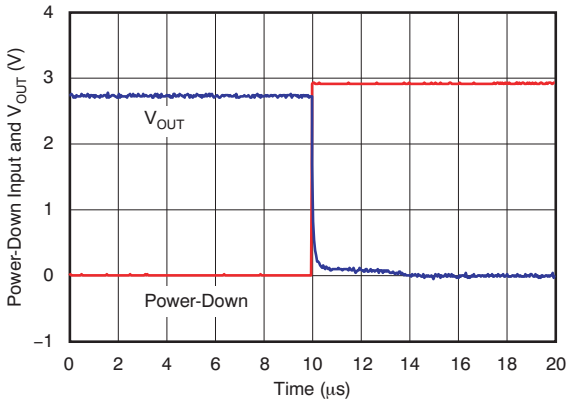


Figure 27.

INPUT AND OUTPUT VOLTAGE NOISE vs FREQUENCY

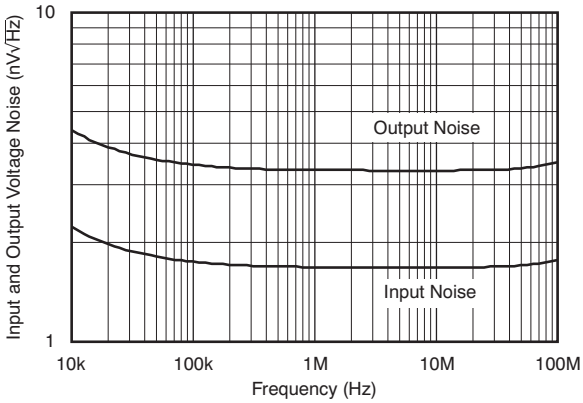


Figure 28.

OUTPUT BALANCE ERROR vs FREQUENCY

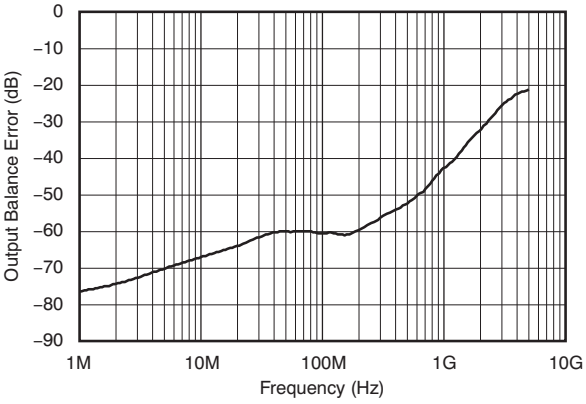


Figure 29.

V_{OCM} SMALL-SIGNAL FREQUENCY RESPONSE

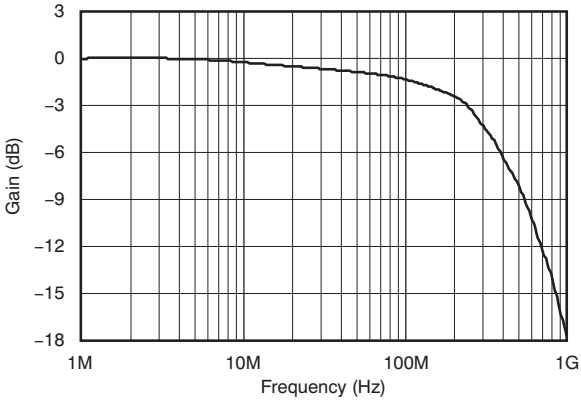


Figure 30.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{S+} = +5V, V_{OCM} = +2.5V, V_{OUT} = $2V_{PP}$, R_L = 400Ω differential, G = +6dB, differential input and output, and input and output pins referenced to midsupply, unless otherwise noted. Measured using EVM as discussed in *Test Circuits* section.

V_{OCM} INPUT BIAS CURRENT vs V_{OCM} INPUT VOLTAGE

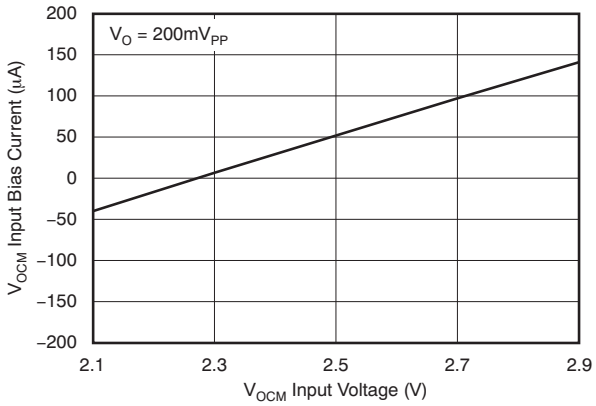


Figure 31.

NOISE FIGURE vs FREQUENCY

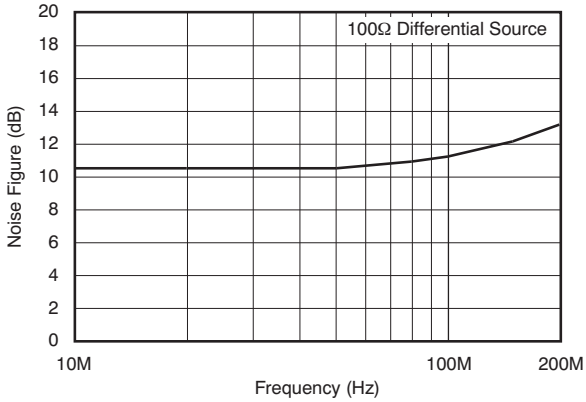


Figure 32.

TEST CIRCUITS

OVERVIEW

The standard THS770006 evaluation module (EVM) is used for testing the typical performance shown in the Typical Characteristics, with changes as noted below. The EVM schematic is shown in Figure 33. The signal generators and analyzers used for most tests have single-ended 50Ω input and output impedance. The THS770006 EVM is configured to convert to and from a differential 50Ω impedance by using RF transformers or baluns (CX2156NL from Pulse, supplied as a standard configuration of the EVM). For line input termination, two 49.9Ω resistors (R5 and R6) are placed to ground on the input transformer output pins (terminals 1 and 3). In combination with the 100Ω input impedance of the device, the total impedance seen by the line is 50Ω.

A resistor network is used on the amplifier output to present various loads (R_L) and maintain line output termination to 50Ω. Depending on the test conditions, component values are changed as shown in Table 1, or as otherwise noted. As a result of the voltage divider on the output formed by the load component values, the amplifier output is attenuated. The *Loss* column in Table 1 shows the attenuation expected from the resistor divider. The output transformer causes slightly more loss, so these numbers are approximate.

Table 1. Load Component Values(1)

LOAD R_L	R15 AND R17	R16	LOSS
100Ω	25Ω	Open	6dB
200Ω	86.6Ω	69.8Ω	16.8dB
400Ω	187Ω	57.6Ω	25.5dB
1kΩ	487Ω	52.3Ω	31.8dB

(1) The total load includes 50Ω termination by the test equipment. Components are chosen to achieve load and 50Ω line termination through a 1:1 transformer.

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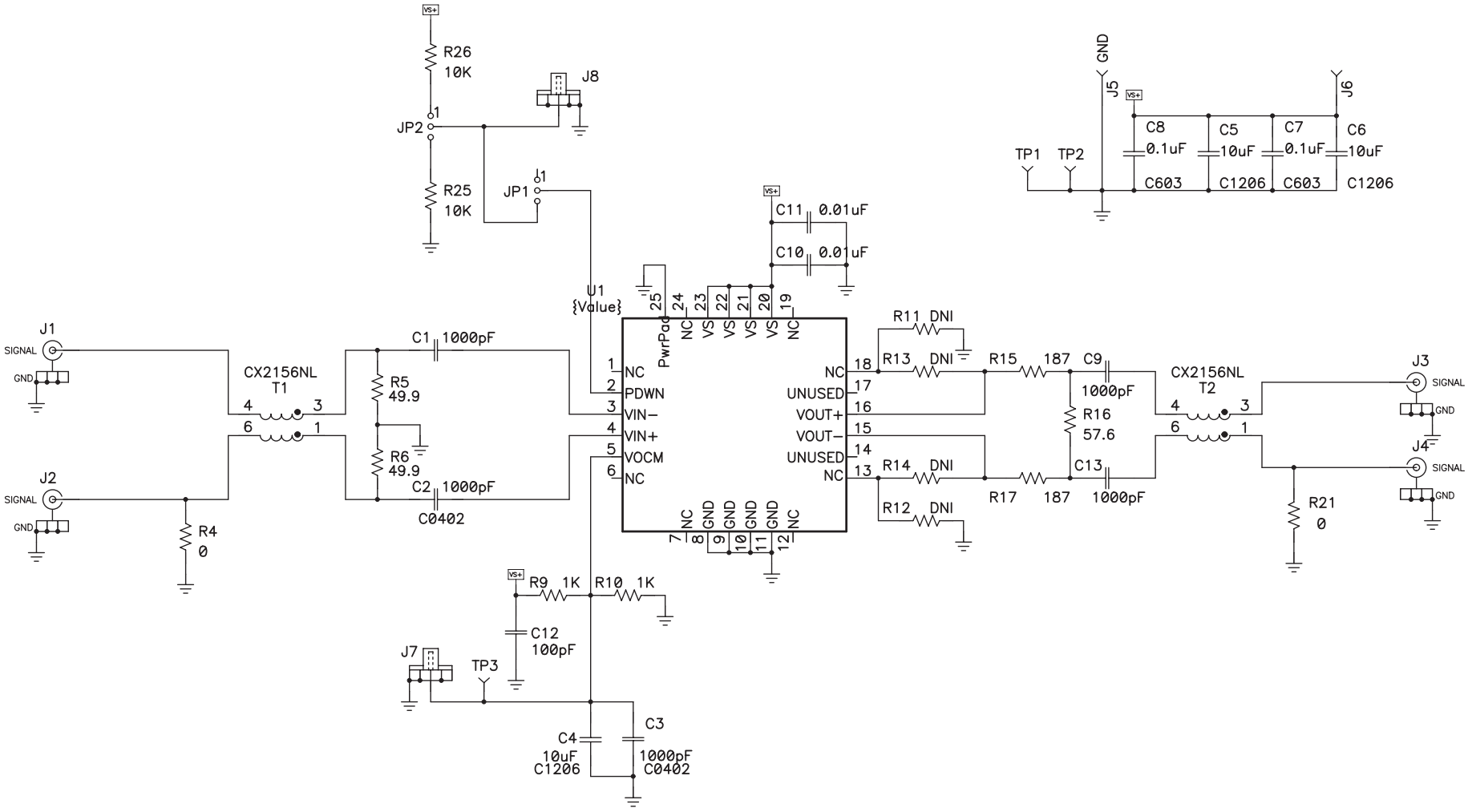


Figure 33. THS770006IRGE EVM Schematic

TEST DESCRIPTIONS

The following sections describe how the tests were performed, as well as the EVM circuit modifications that were made (if any). Modifications made for test purposes include changing capacitors to resistors, resistors to capacitors, the shorting/opening of components, etc., as noted. Unless otherwise noted, C1, C2, C9, and C13 are all changed to 0.1µF.

Frequency Response: 200mV$_{PP}$, 2V$_{PP}$, 3V$_{pp}$

This test is run with and without transformers in the signal path.

For tests with transformers, the standard EVM is used and only the gain magnitude is shown. A network analyzer is connected to the input and output of the EVM with 50Ω coaxial cables and set to measure the forward transfer function (s21). The input signal frequency is swept with the signal level set for the desired output amplitude. The use of transformers gives better magnitude response that correlates best with detailed design simulation in terms of peaking in the response due to better control of parasitic capacitance at the device output pins, but also results in excess phase shift. So only magnitude is plotted.

For tests without transformers, the standard EVM is used, with the gain magnitude and phase shown. A network analyzer is connected to the input of the EVM with 50Ω coaxial cable, the output is terminated with a 50Ω load, and a high impedance differential probe is used for the measurement. The analyzer is set to measure the forward transfer function (s21). The analyzer with a probe input is calibrated at the input pins of the device and signal is measured at the output pin, thus effectively removing the transformers from the transfer function. The input signal frequency is swept with signal level set for desired output amplitude. Not using transformers gives better phase response that correlates best with detailed design simulations, but as a result of extra parasitic capacitance at the device output pins gives significantly more peaking in the magnitude response. The –3dB points of the magnitude response measured without transformers correlates better with measured slew rate, so both magnitude and phase are plotted.

s-Parameters: s11, s22, and s12

The standard EVM is used with both R15 and R17 = 24.9Ω, and R16 = open, to test the input return loss, output return loss, and reverse isolation. A network analyzer is connected to the input and output of the EVM with 50Ω coaxial cables and set to measure the appropriate transfer function: s11, s22, or s12. Note the transformers are included in the signal chain in order to retrieve proper measurements with single-ended test equipment. The impact is minimal from 10MHz to 200MHz, but further analysis is required to fully de-embed the respective effects.

Frequency Response with Capacitive Load

The standard EVM is used with R15 and R17 = R_O, R16 = C_{LOAD}, C9 and C13 = 953Ω, R21 = open, T2 removed, and jumpers placed across terminals 3 to 4 and 1 to 6. A network analyzer is connected to the input and output of the EVM with 50Ω coaxial cables and set to measure the forward transfer function (s21). Different values of load capacitance are placed on the output (at R16) and the output resistor values (R15 and R17) changed until an optimally flat frequency response is achieved with maximum bandwidth.

Distortion

The standard EVM is used for measurement of single-tone harmonic distortion and two-tone intermodulation distortion. For differential distortion measurements, the standard EVM is used with no modification. For single-ended input distortion measurements, the standard EVM is used with with T1 removed and jumpers placed across terminals 3 to 4 and 1 to 6, and R5 and R6 = 100Ω. A signal generator is connected to the J1 input of the EVM with 50Ω coaxial cables, with filters inserted inline to reduce distortion from the generator. The J3 output of the EVM is connected with 50Ω coaxial cables to a spectrum analyzer to measure the fundamental(s) and distortion products.

Noise Figure

The standard EVM is used with T1 changed to a 1:2 impedance ratio transformer (Mini-Circuits ADT2), R15 and R17 = 24.9Ω, and R5, R6, and R16 = open. A noise figure analyzer is connected to the input and output of the EVM with 50Ω coaxial cables. The noise figure analyzer provides a 50Ω (noise) source so that the data are adjusted to refer to a 100Ω source.

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Transient Response, Slew Rate, Overdrive Recovery

The standard EVM is used with T1 and T2 removed and jumpers placed across terminals 3 to 4 and 1 to 6; R15, R17, and R25 = 49.9Ω; C1, C2, C9, and C13 = 0Ω; and R5, R6, R16, and R21 = open. A differential waveform generator is connected to the input of the EVM with 50Ω coaxial cables at J1 and J2. The differential output at J3 and J4 is connected with 50Ω coaxial cables to an oscilloscope to measure the outputs. Waveform math in the oscilloscope is used to combine the differential output of the device.

Power-Down

The standard EVM is used with T1 and T2 removed, jumpers placed across terminals 3 to 4 and 1 to 6, R15 and R17 = 49.9Ω, C9 and C13 = 0Ω, and R5, R6, R16, and R21 = open. A waveform generator is connected to the power-down input of the EVM with a 50Ω coaxial cable at J8. The differential output at J3 and J4 is connected with 50Ω coaxial cables to an oscilloscope to measure the outputs. J1 is left disconnected so that the output is driven to the V_{OCM} voltage when the device is active, and discharged through the resistive load on the output when disabled. Both outputs are the same and only one is shown.

Differential Z-out

The standard EVM is used with R15 and R17 = 24.9Ω, and R16 = open. A network analyzer is connected to the output of the EVM at J3 with 50Ω coaxial cable, both inputs are terminated with a 50Ω load, and a high-impedance differential probe is used for the measurement. The analyzer is set to measure the forward transfer function (s21). The analyzer with probe input is calibrated across the open resistor pads of R16 and the signal is measured at the output pins of the device. The output impedance is calculated using the known resistor values and the attenuation caused by R15 and R17.

Output Balance Error

The standard EVM is used with R15 and R17 = 100Ω, and R16 = 0Ω. A network analyzer is connected to the input of the EVM with 50Ω coaxial cable, the output is left open, and a high-impedance differential probe is used for the measurement. The analyzer is set to measure the forward transfer function (s21). The analyzer with probe input is calibrated at the input pins of the device and the signal is measured from the shorted pads of R16 to ground.

Common-Mode Rejection

The standard EVM is used with T1 removed and jumpers place across terminals 3 to 4, 1 to 6, and 1 to 3. A network analyzer is connected to the input and output of the EVM with 50Ω coaxial cable and set to measure the forward transfer function (s21).

V_{OCM} Frequency Response

The standard EVM is used with T2 removed and jumpers across terminals 3 to 4 and 1 to 6; R10, R15, and R17 = 49.9Ω; C3 and C4 = 0Ω; and R9, R16, and R21 = open. A network analyzer is connected to the V_{OCM} input of the EVM at J7 and output of the EVM with 50Ω coaxial cable, and set to measure the forward transfer function (s21). The input signal frequency is swept with the signal level set for 200mV. Each output at J3 and J4 is measured as single-ended, and because both are the same, only one output is shown.

V_{OCM} Slew Rate and Pulse Response

The standard EVM is used with T2 removed and jumpers across terminals 3 to 4 and 1 to 6; R10, R15, and R17 = 49.9Ω; C9 and C13 = 0Ω; and C3, C4, R9, R16, and R21 = open. A waveform generator is connected to the V_{OCM} input of the EVM at J7 with 50Ω coaxial cable. The differential output at J3 and J4 is connected with 50Ω coaxial cable to an oscilloscope to measure the outputs. J1 is left disconnected so that the output is driven to the V_{OCM} voltage. Both outputs are the same, so only one is shown.

Input/Output Voltage Noise, Settling Time, and Power-Supply Rejection

These parameters are taken from simulation.

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THEORY OF OPERATION

GENERAL DESCRIPTION

The THS770006 is a fixed-gain of +6dB, wideband, fully-differential amplifier designed and optimized specifically for driving 14-bit and 16-bit ADCs at input frequencies up to 200MHz. This device provides high bandwidth, low distortion, and low noise, which are critical parameters in high-speed data acquisition systems that require very high dynamic range, such as wireless base stations and test and measurement applications. It also makes an excellent differential amplifier for general-purpose, high-speed differential signal chain and short line-driver applications. The device has an operating power-supply range of 4.75V to 5.5V. The THS770006 has proprietary circuitry to provide very fast recovery from overdrive conditions and has a power-down mode for power saving. The THS770006 is offered in a Pb-free (RoHS compliant) and green, QFN-24 thermally-enhanced package. It is characterized for operation over the industrial temperature range of –40°C to +85°C.

The amplifier uses two negative-feedback loops. One is for the primary differential amplifier and the other controls the common-mode operation.

Primary Differential Amplifier

The primary amplifier of the THS770006 is a fully-differential op amp with on-chip gain setting resistors (R_F = 100Ω and R_G = 50Ω) that fix the differential gain at 2V/V, or 6dB, by use of negative feedback.

V_{OCM} Control Loop

The output common-mode voltage is controlled through a second negative-feedback loop. The output common-mode voltage is internally sensed and compared to the V_{OCM} pin. The loop then works to drive the difference, or error voltage, to zero in order to maintain the output common-mode voltage = V_{OCM} (within the loop gain and bandwidth of the loop). For more details on fully-differential amplifier theory and use, see application report SLOA054, *Fully-Differential Amplifiers*, available for download from www.ti.com.

OPERATION

Differential to Differential

The THS770006 is a fixed gain of 6dB, fully-differential amplifier that can be used to amplify differential input signals to differential output signals. A basic block diagram of the circuit is shown in Figure 34. The differential input to differential output configuration gives the best performance; the signal source and load should be balanced.

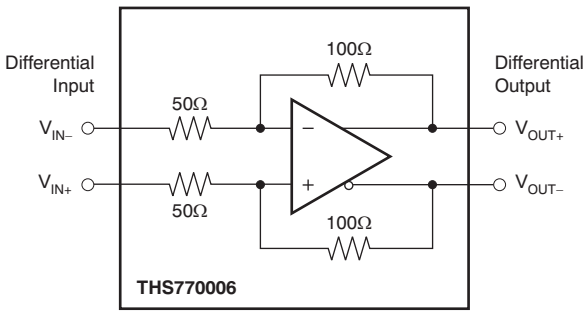


Figure 34. Differential Input to Differential Output Amplifier

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Single-Ended to Differential

The THS770006 can be used to amplify and convert single-ended input signals to differential output signals. A basic block diagram of the circuit is shown in Figure 35. The gain from the single-ended input to the differential output is 6dB. In order to maintain proper balance in the amplifier and avoid offsets at the output, the alternate input must be biased and the impedance matched to the signal input. For example, if a 50Ω source biased to 2.5V provides the input, the alternate input should be tied to 2.5V through 50Ω. If a 50Ω source is ac-coupled to the input, the alternate input should be ac-coupled to ground through 50Ω. Note that the ac coupling should provide a similar frequency response to balance the gain over frequency.

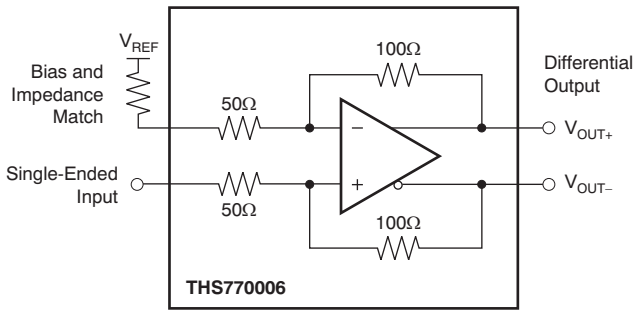


Figure 35. Single-Ended Input to Differential Output Amplifier

Setting the Output Common-Mode Voltage

The V_{OCM} input controls the output common-mode voltage. V_{OCM} has no internal biasing network and must be driven by an external source or resistor divider network to the positive power supply. In ac-coupled applications, the V_{OCM} input impedance and bias current are not critical, but in dc-coupled applications where more accuracy is desired, the input bias current of the pin should be considered. For best harmonic distortion with V_{OUT} = $3V_{PP}$, the V_{OCM} input should be maintained within the operating range of 2.25V to 2.75V. The V_{OCM} input voltage can be operated outside this range if lower output swing is used or distortion degradation is allowed, and increased bias current into the pin is acceptable. For more information, see Figure 12 and Figure 31. It is recommended to use a 0.1µF decoupling capacitor from the V_{OCM} pin to ground to prevent noise and other spurious signals from coupling into the common-mode loop of the amplifier.

Input Common-Mode Voltage Range

The THS770006 is designed primarily for ac-coupled operation. With input dc blocking, the input common-mode voltage of the device is driven to the same voltage as V_{OCM} by the outputs. Therefore, as long as the V_{OCM} input is maintained within the operating range of 2.25V to 2.75V, the input common-mode of the main amplifier is also maintained within its linear operating range of 2.25V to 2.75V. If the device is used with dc coupled input, the driving source needs to bias the input to its linear operating range of 2.25V to 2.75V for proper operation.

Operation with Split Supply ±2.5V

The THS770006 can be operated using a split ±2.5V supply. In this case, V_{S+} is connected to +2.5V, and GND (and any other pin noted to be connected to GND) is connected to –2.5V. As with any device, the THS770006 is impervious to what the user decides to name the levels in the system. In essence, it is simply a level shift of the power pins by –2.5V. If everything else is level-shifted by the same amount, the device sees no difference. With a ±2.5V power supply, the V_{OCM} range is 0V ±0.25V; therefore, power-down levels are –2.5V = on and +2.5V = off, and input and output voltage ranges are symmetrical about 0V. This design has certain advantages in systems where signals are referenced to ground, and as noted in the following section, for driving ADCs with low input common-mode voltage requirements in dc-coupled applications.

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Driving Capcitive Loads

The THS770006 is tested as described previously, with the data shown in the typical graphs. As a result of the fixed gain architecture of the device, the only practical means to avoid stability problems such as overshoot/ringing, gain peaking, and oscillation when driving capacitive loads is to place small resistors in series with the outputs (R_O) to isolate the phase shift caused by the capacitive load from the feedback loop of the amplifier. The Typical Characteristics graphs show recommended values for an optimally flat frequency response with maximum bandwidth. Smaller values of R_O can be used if more peaking is allowed, and larger values can be used to reduce the bandwidth.

Driving ADCs

The THS770006 is designed and optimized for the highest performance to drive differential input ADCs. Figure 36 shows a generic block diagram of the THS770006 driving an ADC. The primary interface circuit between the amplifier and the ADC is usually a filter of some type for antialias purposes, and provides a means to bias the signal to the input common-mode voltage required by the ADC. Filters range from single-order real RC poles to higher-order LC filters, depending on the requirements of the application. Output resistors (R_O) are shown on the amplifier outputs to isolate the amplifier from any capacitive loading presented by the filter.

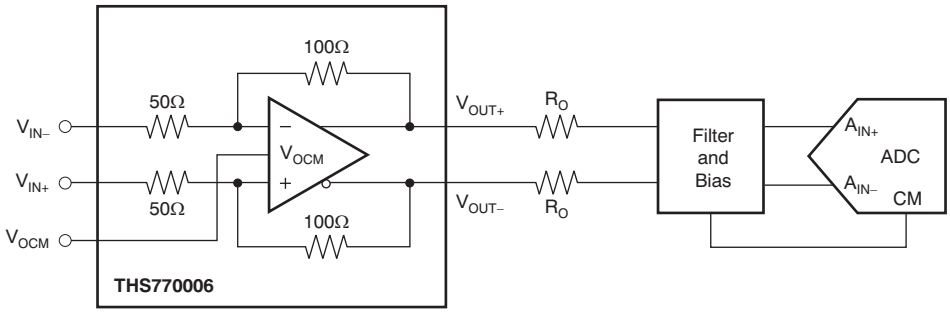


Figure 36. Generic ADC Driver Block Diagram

The key points to consider for implementation are described in the following three subsections.

SNR Considerations

The signal-to-noise ratio (SNR) of the amplifier and filter can be calculated from the amplitude of the signal and the bandwidth of the filter. The noise from the amplifier is band-limited by the filter with the equivalent brick-wall filter bandwidth. The amplifier and filter noise can be calculated using the following equations:

$$SNR_{AMP+FILTER} = 10 \cdot \log \left(\frac{V^2_O}{e^2_{FILTEROUT}} \right) = 20 \cdot \log \left(\frac{V_O}{e_{FILTEROUT}} \right)$$

Where:

$e_{FILTEROUT} = e_{NAMPOUT} \cdot \sqrt{ENB}$

$e_{NAMPOUT}$ = the output noise density of the THS770006 (3.4nV/$\sqrt{Hz}$)

ENB = the brick-wall equivalent noise bandwidth of the filter

V_O is the amplifier output signal. (1)

For example, with a first-order (N = 1) band-pass or low-pass filter with 30MHz cutoff, the ENB is 1.57 • $f_{–3dB}$ = 1.57 • 30MHz = 47.1MHz. For second-order (N = 2) filters, the ENB is 1.22 • $f_{–3dB}$. As the filter order increases, the ENB approaches $f_{–3dB}$ (N = 3 → ENB = 1.15 • $f_{–3dB}$; N = 4 → ENB = 1.13 • $f_{–3dB}$). Both V_O and $e_{FILTEROUT}$ are in RMS voltages. For example, with a $2V_{PP}$ ($0.707V_{RMS}$) output signal and 30MHz first-order filter, the SNR of the amplifier and filter is 70.7dB with $e_{FILTEROUT}$ = 3.4nV/$\sqrt{Hz}$ • $\sqrt{47.1MHz}$ = $23\mu V_{RMS}$.

The SNR of the amplifier, filter, and ADC sum in RMS fashion, as shown in Equation 2 (SNR values in dB):

$$SNR_{SYSTEM} = -20 \cdot \log \left(\sqrt{10^{\frac{-SNR_{AMP+FILTER}}{10}} + 10^{\frac{-SNR_{ADC}}{10}}} \right)$$

(2)

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This formula shows that if the SNR of the amplifier and filter equals the SNR of the ADC, the combined SNR is 3dB lower (worse). Thus, for minimal impact (< 1dB) on the ADC SNR, the SNR of the amplifier and filter should be ≥ 10dB greater than the ADC SNR. The combined SNR calculated in this manner is usually accurate to within ±1dB of actual implementation.

SFDR Considerations

The SFDR of the amplifier is usually set by second-order or third-order harmonic distortion for single-tone inputs, and by second-order or third-order intermodulation distortion for two-tone inputs. Harmonics and second-order intermodulation distortion can be filtered to some degree, but third-order intermodulation spurs cannot be filtered. The ADC generates the same distortion products as the amplifier, but as a result of the sampling and clock feedthrough, additional spurs (not linearly related to the input signal) are included.

When the spurs from the amplifier and filter are known, each individual spur can be directly added to the same spur from the ADC, as shown in Equation 3, to estimate the combined spur (spur amplitudes in dBc):

$$HDx_{SYSTEM} = -20 \cdot \log\left[10^{\frac{-HDx_{AMP+FILTER}}{20}} + 10^{\frac{-HDx_{ADC}}{20}}\right] \quad (3)$$

This calculation assumes the spurs are in phase, but usually provides a good estimate of the final combined distortion.

For example, if the spur of the amplifier and filter equals the spur of the ADC, then the combined spur is 6dB higher. To minimize the amplifier contribution (< 1dB) to the overall system distortion, it is important that the spur from the amplifier and filter be ~15dB better than the converter. The combined spur calculated in this manner is usually accurate to within ±6dB of actual implementation; however, higher variations have been observed as a result of phase shift in the filter, especially in second-order harmonic performance.

This worst-case spur calculation assumes that the amplifier/filter spur of interest is in phase with the corresponding spur in the ADC, such that the two spur amplitudes can be added linearly. There are two phase-shift mechanisms that cause the measured distortion performance of the amplifier-ADC chain to deviate from the expected performance calculated using Equation 3: common-mode phase shift and differential phase shift.

Common-mode phase shift is the phase shift seen equally in both branches of the differential signal path including the filter. Common-mode phase shift nullifies the basic assumption that the amplifier/filter and ADC spur sources are in phase. This phase shift can lead to better performance than predicted as the spurs become phase shifted, and there is the potential for cancellation as the phase shift reaches 180°. However, there is a significant challenge in designing an amplifier-ADC interface circuit to take advantage of common-mode phase shift for cancellation: the phase characteristic of the ADC spur sources are unknown, thus the necessary phase shift in the filter and signal path for cancellation is also unknown.

Differential phase shift is the difference in the phase response between the two branches of the differential filter signal path. Differential phase shift in the filter as a result of mismatched components caused by nominal tolerance can severely degrade the even-order distortion of the amplifier-ADC chain. This effect has the same result as mismatched path lengths for the two differential traces, and causes more phase shift in one path than the other. Ideally, the phase response over frequency through the two sides of a differential signal path are identical, such that even-order harmonics remain optimally out of phase and cancel when the signal is taken differentially. However, if one side has more phase shift than the other, then the even-order harmonic cancellation is not as effective.

Single-order RC filters cause very little differential phase shift with nominal tolerances of 5% or less, but higher-order LC filters are very sensitive to component mismatch. For instance, a third-order Butterworth bandpass filter with 100MHz center frequency and 20MHz bandwidth shows up to a 20° differential phase imbalance in a Spice Monte Carlo analysis with 2% component tolerances. Therefore, while a prototype may work, production variance is unacceptable. In ac-coupled applications that require second- and higher-order filters between the THS770006 and ADC, a transformer or balun is recommended at the ADC input to restore the phase balance. For dc-coupled applications where a transformer or balun at the ADC input cannot be used, it is recommended to use first- or second-order filters to minimize the effect of differential phase shift because of component tolerance.

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ADC Input Common-Mode Voltage Considerations—AC-Coupled Input

The input common-mode voltage range of the ADC must be respected for proper operation. In an ac-coupled application between the amplifier and the ADC, the input common-mode voltage bias of the ADC is accomplished in different ways depending on the ADC. Some ADCs use internal bias networks such that the analog inputs are automatically biased to the required input common-mode voltage if the inputs are ac-coupled with capacitors (or if the filter between the amplifier and ADC is a bandpass filter). Other ADCs supply their required input common-mode voltage from a reference voltage output pin (often called CM or V_{CM}). With these ADCs, the ac-coupled input signal can be re-biased to the input common-mode voltage by connecting resistors from each input to the CM output of the ADC, as Figure 37 illustrates. However, the signal is attenuated because of the voltage divider created by R_{CM} and R_O.

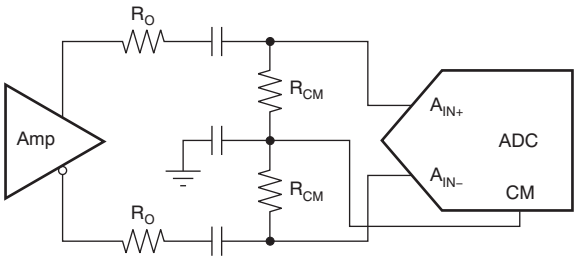


Figure 37. Biasing AC-Coupled ADC Inputs Using the ADC CM Output

The signal can be re-biased when ac coupling; thus, the output common-mode voltage of the amplifier is a *don't care* for the ADC.

ADC Input Common-Mode Voltage Considerations—DC-Coupled Input

DC-coupled applications vary in complexity and requirements, depending on the ADC. One typical requirement is resolving the mismatch between the common-mode voltage of the driving amplifier and the ADC. Devices such as the ADS5424 require a nominal 2.4V input common-mode, while others such as the ADS5485 require a nominal 3.1V input common-mode; still others such as the ADS6149and the ADS4149 require 1.5V and 0.95V, respectively. As shown in Figure 38, a resistor network can be used to perform a common-mode level shift. This resistor network consists of the amplifier series output resistors and pull-up or pull-down resistors to a reference voltage. This resistor network introduces signal attenuation that may prevent the use of the full-scale input range of the ADC. ADCs with an input common-mode closer to the typical 2.5V THS770006 output common-mode are easier to dc-couple, and require little or no level shifting.

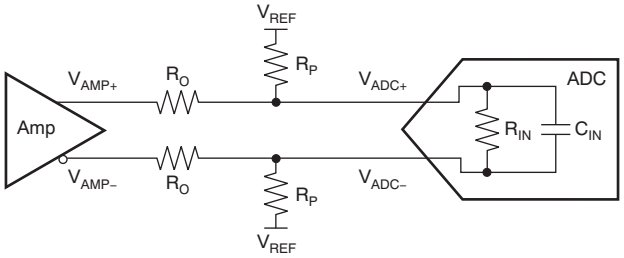


Figure 38. Resistor Network to DC Level-Shift Common-Mode Voltage

For common-mode analysis of the circuit in Figure 38, assume that $V_{AMP\pm} = V_{OCM}$ and $V_{ADC\pm} = V_{CM}$ (the specification for the ADC input common-mode voltage). V_{REF} is chosen to be a voltage within the system higher than V_{CM} (such as the ADC or amplifier analog supply) or ground, depending on whether the voltage must be pulled up or down, respectively; R_O is chosen to be a reasonable value, such as 24.9Ω. With these known values, R_P can be found by using Equation 4:

$$R_P = R_O \left(\frac{V_{ADC} - V_{REF}}{V_{AMP} - V_{ADC}} \right) \quad (4)$$

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Shifting the common-mode voltage with the resistor network comes at the expense of signal attenuation. Modeling the ADC input as the parallel combination of a resistance (R_{IN}) and capacitance (C_{IN}) using values taken from the ADC data sheet, the approximate differential input impedance (Z_{IN}) for the ADC can be calculated at the signal frequency. The effect of C_{IN} on the overall calculation of gain is typically minimal and can be ignored for simplicity (that is, $Z_{IN} = R_{IN}$). The ADC input impedance creates a divider with the resistor network; the gain (attenuation) for this divider can be calculated by Equation 5:

$$GAIN = \left(\frac{2R_P \parallel Z_{IN}}{2R_O + 2R_P \parallel Z_{IN}} \right) \quad (5)$$

With ADCs that have internal resistors that bias the ADC input to the ADC input common-mode voltage, the effective R_{IN} is equal to twice the value of the bias resistor. For example, the ADS5485 has a 1kΩ resistor tying each input to the ADC V_{CM}; therefore, the effective differential R_{IN} is 2kΩ.

The introduction of the R_P resistors also modifies the effective load seen by the amplifier. Equation 6 shows the effective load seen by the amplifier:

$$R_L = 2R_O + 2R_P \parallel Z_{IN} \quad (6)$$

The R_P resistors act in parallel to the ADC input such that the effective load (output current) seen by the amplifier is increased. Higher current loads limit the THS770006 differential output swing.

Using the gain and knowing the full-scale input of the ADC ($V_{ADC\ FS}$), the required amplitude to drive the ADC with the network can be calculated using Equation 7:

$$V_{AMP\ PP} = \frac{V_{ADC\ FS}}{GAIN} \quad (7)$$

Using the ADC examples given previously, Table 2 shows sample calculations of the value of R_P and $V_{AMP\ FS}$ for full-scale drive, and then for –1dB (often times, the ADC drive is backed off from full-scale in applications, so lower amplitudes may be acceptable). All voltage values are in volts, resistor values in ohms (the nearest standard value should be used), and gain values are as noted. Table 2 does not include the ADS5424 because no level shift is required with this device.

Table 2. Example R_P for Various ADCs

ADC	V_{AMP} (V_{DC})	V_{ADC} (V_{DC})	V_{REF} (V_{DC})	ADC R_{IN} (Ω)	R_O (Ω)	R_P (Ω)	GAIN (V/V)	GAIN (dB)	$V_{ADC\ FS}$ (V_{PP})	$V_{AMP\ PP}$ FOR 0dBFS(V_{PP})	$V_{AMP\ PP}$ FOR –1dBFS (V_{PP})
ADS5485	2.5	3.1	5	2k	50	158.3	0.73	–2.72	3	4.10	3.66
ADS6149	2.5	1.5	0	6k(1)	50	75.0	0.59	–4.56	2	3.38	3.01
ADS4149	2.5	0.95	0	5k(1)	50	30.6	0.38	–8.49	2	5.31	4.74
	0(2)	0.95	2.5	5k(1)	50	81.6	0.61	–4.31	2	3.28	2.93
	0(2)	0.95	5	5k(1)	50	213.2	0.79	–2.05	2	2.53	2.26

(1) At 70MHz.
(2) THS770006 with ±2.5V supply.

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The calculated values for the ADS5485 give the lowest attenuation. As a result of the high V_{FS} of $3V_{PP}$, $3.66V_{PP}$ is required from the amplifier to drive to –1dBFS. Performance of the THS770006 is still very good up to 130MHz at this level, but for best performance, back off further from full-scale and consider trading reduced SNR performance for better SFDR performance.

The values calculated for the ADS6149 show reasonable design targets and should work with good performance. Note the ADS6149 does not have buffered inputs, and the inputs have equivalent resistive impedance that varies with sampling frequency. The calculation shown in Table 2 uses a value of 70MHz for R_{IN}, taken from the ADS6149 data sheet.

The values calculated for the low input common-mode voltage of the ADS4149 result in a large attenuation of the amplifier signal leading to $5.31V_{PP}$ being required for full-scale ADC drive. This amplitude is greater than the maximum capability of the device. With a single +5V supply, the THS770006 is not suitable to drive this ADC in dc-coupled applications unless the ADC input is backed off towards –6dBFS.

Another option is to operate the THS770006 with a split ±2.5V supply. The R_P and gains are shown in the last two rows of Table 2 for pull-up voltages of 2.5V and 5V. For this situation, if the +2.5V is used as the pull-up reference voltage, only $2.93V_{PP}$ is required for the –1dBFS input to the ADS4149. If a 5V reference is used, only 2.26VPP is required to reach the –1dBFS input to the ADS4149. See the *Operation with Split Supply ±2.5V* section for more detail. Note that, similar to the ADS6149, the ADS4149 does not have buffered inputs and the inputs have equivalent resistive impedance that varies with sampling frequency. The R_{IN} value at 70MHz taken from the ADS4149 data sheet was used in the calculation.

As with any design, testing is recommended to validate whether it meets the specific design goals.

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APPLICATION INFORMATION

THS770006 DRIVING 16-BIT ADC

To illustrate the performance of the THS770006 as an ADC driver, the device is tested with a 16-bit ADC.

TESTING WITH AN AC-COUPLED BANDPASS FILTER

For testing purposes, a 30MHz, third-order Butterworth bandpass filter with center frequency at 100MHz is designed. The design target for the source impedance is 40Ω differential, and for load impedance is 400Ω differential. Therefore, approximately 1dB insertion loss is expected in the pass-band, requiring the amplifier output amplitude to be $2.5V_{PP}$ to drive the ADC to –1dBFS.

The output noise voltage specification for the THS770006 is 3.4 nV/$\sqrt{Hz}$. With $2.5V_{PP}$ amplifier output voltage swing and 30MHz bandwidth, the expected SNR from the amplifier + antialias filter is 93.5dB. When added in combination with the 16-bit ADC, the expected total SNR is 75.1dBFS for the typical case.

Figure 39 shows the resulting FFT plot when driving the ADC to –1dBFS with a single-tone 100MHz sine wave, and sampling at 125MSPS. Test results show 98dBc SFDR from the second-order harmonic and 75.6 dBFS SNR; analysis of the plot is shown in Table 3 versus typical ADC specifications. The test results from circuit board to circuit board shows over 10dB of variation in the second order harmonic and a balun is inserted between the filter and ADC inputs to get repeatable performance. With balun, the minimum expected results should be better than 90dBc SFDR and 75dBFS SNR.

Figure 39 shows the same circuit with a two-tone input at 96MHz and 100MHz. The near-in 3rd order intermodulation terms are about -100dBc.

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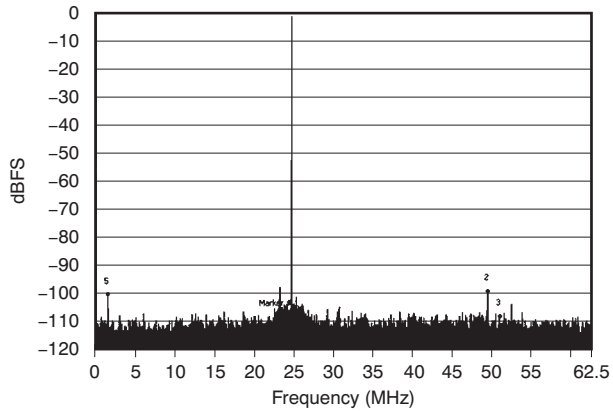


Figure 39. FFT Plot of THS770006 + 30MHz BPF + 16-Bit ADC with Single-Tone at 100MHz

Table 3. Analysis of FFT for THS770006 + BPF + 16-Bit ADC at 100MHz vs Typical ADC Specifications

CONFIGURATION	ADC INPUT	SNR	HD2	HD3
THS770006 + BPF + 16-Bit ADC	–1dBFS	75.6dBFS	–98dBc	–107dBc
16-Bit ADC Only (typ)	–1dBFS	75.2dBFS	–100dBc	–100dBc

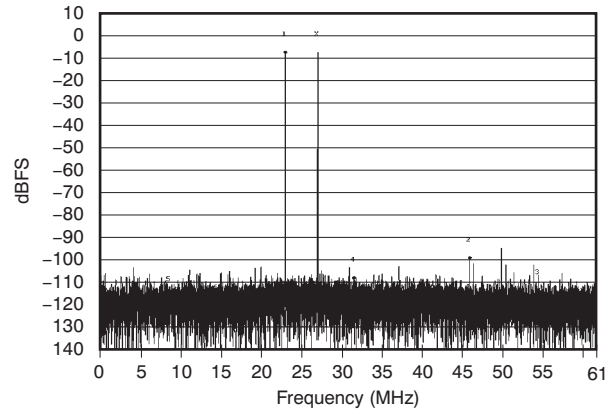


Figure 40. FFT Plot of THS770006 + 30MHz BPF + 16-Bit ADC with Two-Tone Input at 96MHz and 100MHz

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TESTING WITH AN AC-COUPLED LOW-PASS FILTER

For testing purposes, a 150MHz, first-order, low-pass filter is built. The design gives approximately 1.6dB insertion loss at low frequency, requiring the amplifier signal be $2.7V_{PP}$ in order to drive the ADC to –1dBFS.

With $2.7V_{PP}$ amplifier output voltage swing and 180MHz (–3dB) bandwidth, the expected SNR from the amplifier + antialias filter is 84.4dB. When added in combination with the 16-bit, 130MSPS ADC, the total expected SNR is 74.7dBFS for the typical case. Note the frequency response is approximately –1dB at 100MHz, which requires even higher amplitude for the following test.

Figure 41 shows the resulting FFT plot when driving the ADC to –1dBFS with a 100MHz sine wave, and sampling at 125MSPS. Test results showed 91dBc SFDR from second- and third-order harmonic and 73.1dBFS SNR; analysis of the plot is shown in Table 4 versus typical ADC specifications. As a result of harmonic attenuation and phase shift between the amplifier and ADC, harmonic performance is better than predicted from the worst-case scenario described previously. Typical expected results should be approximately 90dBc SFDR and 73dBFS SNR.

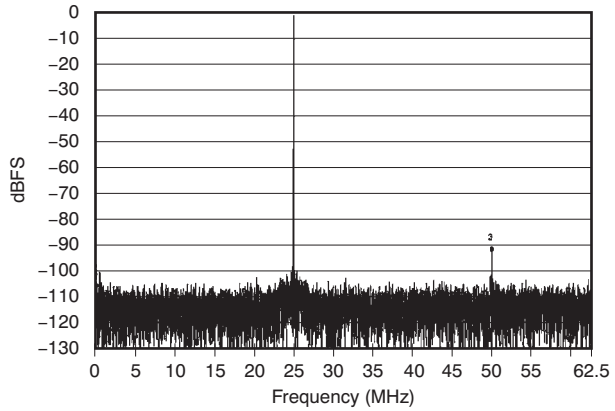


Figure 41. FFT Plot of THS770006 + 180MHz LPF + 16-Bit ADC with Single-Tone at 100MHz

Table 4. Analysis of FFT for THS770006 + 180MHz LPF + 16-Bit ADC at 100MHz vs Typical ADC Specifications

CONFIGURATION	ADC INPUT	SNR	HD2	HD3
THS770006 + BPF + 16-Bit ADC	–1dBFS	73.1dBFS	–91dBc	–91dBc
16-Bit ADC Only (typ)	–1dBFS	75.2dBFS	–100dBc	–100dBc

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EVM AND LAYOUT RECOMMENDATIONS

Figure 33 is the THS770006RGE EVM schematic, and Figure 42 through Figure 45 show the layout details of the EVM PCB. Table 5 is the bill of materials for the EVM as supplied from TI. It is recommended to follow the layout of the external components as close as possible to the amplifier, ground plane construction, and power routing. General layout guidelines are:

1. Place a 2.2µF to 10µF capacitor on each supply pin within 2 inches from the device. It can be shared among other op amps.
2. Place a 0.01µF to 0.1µF capacitor on each supply pin to ground as close as possible to the device. Placement within 1mm of the device supply pins ensures best performance.
3. Keep input and output traces as short as possible to minimize parasitic capacitance and inductance. Doing so reduces unwanted characteristics such as reduced bandwidth and peaking in the frequency response, overshoot, and ringing in the pulse response, and results in a more stable design.
4. To reduce parasitic capacitance, ground plane and power-supply planes should be removed from device input pins and output pins.
5. The V_{OCM} pin must be biased to a voltage between 2.25V to 2.75V for proper operation. Place a 0.1µF to 0.22µF capacitor to ground as close as possible to the device to prevent noise coupling into the common-mode.
6. For best performance, drive circuits and loads should be balanced and biased to keep the input and output common-mode voltage between 2.25V to 2.75V. AC-coupling is a simple way to achieve this performance.
7. The THS770006 is provided in a thermally enhanced PowerPAD™ package. The package is constructed using a downset leadframe on which the die is mounted. This arrangement results in low thermal resistance to the thermal pad on the underside of the package. Excellent thermal performance can be achieved by following the guidelines in TI application reports SLMA002, PowerPAD™ Thermally-Enhanced Package and SLMA004, PowerPAD™ Made Easy. For proper operation, the thermal pad on the bottom of the device must be tied to the same voltage potential as the GND pin on the device.

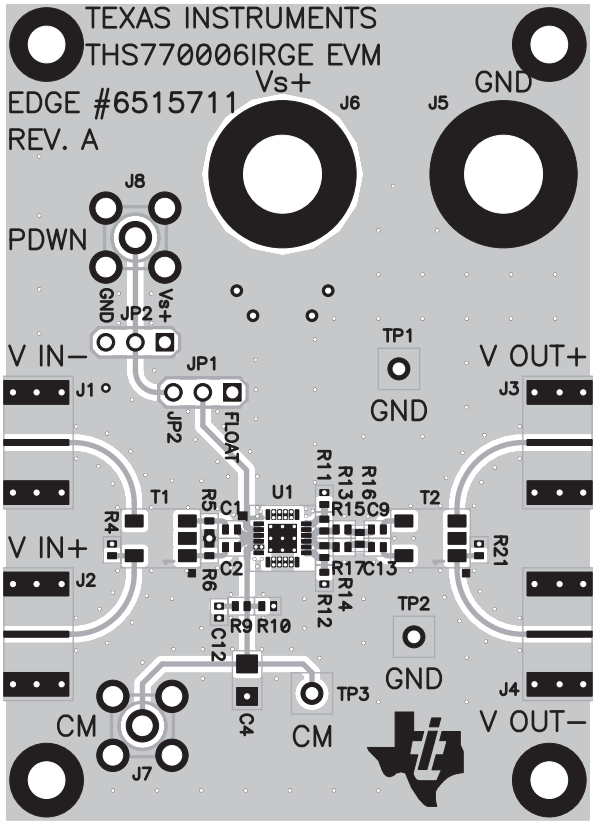


Figure 42. EVM Layout: Top Layer

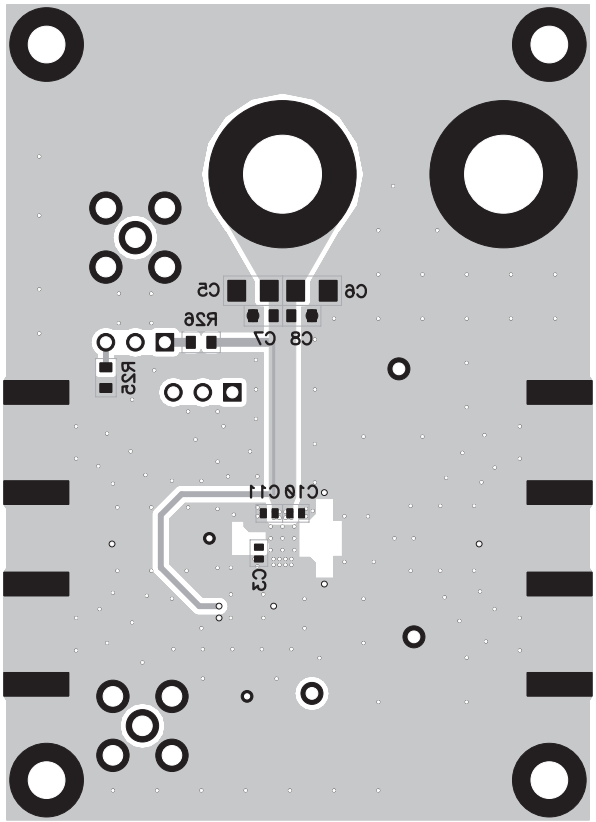


Figure 43. EVM Layout: Bottom Layer

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Figure 44. EVM Layout: Layer 2

Figure 45. EVM Layout: Layer 3

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Table 5. THS770006RGE EVM Bill of Materials

ITEM	DESCRIPTION	SMD SIZE	REFERENCE DESIGNATOR	QTY	MANUFACTURER PART NUMBER	DISTRIBUTOR PART NUMBER
1	CAP, 10.0uF, CERAMIC, X7R, 10V	1206	C4, C5, C6	3	(TDK) C3216X7R1A106K	(DIGI-KEY) 445-4043-1-ND
2	CAP, 0.1uF, CERAMIC, X7R, 16V	0603	C7, C8	2	(AVX) 0603YC104KAT2A	(DIGI-KEY) 478-1239-1-ND
3	CAP, 0.01uF, CERAMIC, X7R, 16V	0402	C10, C11	2	(AVX) 0402YC103KAT2A	(DIGI-KEY) 478-1114-1-ND
4	CAP, 100pF, CERAMIC, NPO, 50V	0402	C12	1	(AVX) 04025A101KAT2A	(DIGI-KEY) 478-4979-1-ND
5	CAP, 1000pF, CERAMIC, X7R, 50V	0402	C1, C2, C3, C9, C13	5	(AVX) 04025C102KAT2A	(DIGI-KEY) 478-1101-1-ND
6	OPEN	0402	R11, R12, R13, R14	4		
7	RESISTOR, 0 OHM	0402	R4, R21	2	(PANASONIC) ERJ-2GE0R00X	(DIGI-KEY) P0.0JCT-ND
8	RESISTOR, 49.9 OHM, 1/10W, 1%	0402	R5, R6	2	(PANASONIC) ERJ-2RKF49R9X	(DIGI-KEY) P49.9LCT-ND
9	RESISTOR, 57.6 OHM, 1/10W, 1%	0402	R16	1	(PANASONIC) ERJ-2RKF57R6X	(DIGI-KEY) P57.6LCT-ND
10	RESISTOR, 187 OHM, 1/10W, 1%	0402	R15, R17	2	(PANASONIC) ERJ-2RKF1870X	(DIGI-KEY) P187LCT-ND
11	RESISTOR, 1K OHM, 1/10W, 1%	0402	R9, R10	2	(PANASONIC) ERJ-2RKF1001X	(DIGI-KEY) P1.00KLCT-ND
12	RESISTOR, 10K OHM, 1/10W, 1%	0603	R25, R26	2	(PANASONIC) ERJ-3EKF1002V	(DIGI-KEY) P10.0KHCT-ND
13	TRANSFORMER, BALUN		T1, T2	2	(PULSE) CX2156NL	(DIGI-KEY) 553-1499-ND
14	JACK, BANANA RECEPTANCE, 0.25" DIA. HOLE		J5, J6	3	(SPC) 15459	(NEWARK) 79K5034
15	CONNECTOR, SMA PCB JACK		J7, J8	2	(AMPHENOL) 901-144-8RFX	(NEWARK) 34C8151
16	CONNECTOR, EDGE, SMA PCB JACK		J1, J2, J3, J4	4	(JOHNSON) 142-0701-801	(NEWARK) 90F2624
17	HEADER, 0.1" CTRS, 0.025" SQ. PINS	3 POS.	JP1, JP2	2	(SULLINS) PBC36SAAN	(DIGI-KEY) S1011E-36-ND
18	SHUNTS		JP1, JP2	2	(SULLINS) SSC02SYAN	(DIGI-KEY) S9002-ND
19	TEST POINT, RED		TP3	1	(KEYSTONE) 5000	(DIGI-KEY) 5000K-ND
20	TEST POINT, BLACK		TP1, TP2	2	(KEYSTONE) 5001	(DIGI-KEY) 5001K-ND
21	IC, THS770006		U1	1	(TI) THS770006RGE	
22	STANDOFF, 4-40 HEX, 0.625" LENGTH			4	(KEYSTONE) 1808	(DIGI-KEY) 1808K-ND
23	SCREW, PHILLIPS, 4-40, .250"			4	PMSSS 440 0025 PH	(DIGI-KEY) H703-ND
24	BOARD, PRINTED CIRCUIT				(TI) EDGE# 6515711 REV.A	

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2011) to Revision B **Page**

- Replaced "ADS5493" with "16-Bit Driver" in figure and figure title 1
- Deleted ADS5493 from Related Devices table 1
- Deleted reference to ADS5493 from text 24
- Replaced references to "ADS5493" with "16-bit ADC" in *Application Information* section 25

Changes from Original (July 2010) to Revision A **Page**

- Changed large-signal bandwidth from 675 to 780 in Electrical Characteristics 3
- Added new row for Input Common-Mode Range parameter in Electrical Characteristics 4
- Added Figure 13, Harmonic Distortion vs Input Common-Mode Range 10
- Changed *SNR Considerations* section. 20
- Changed *SFDR Considerations* section 21
- Changed *ADC Input Common-Mode Voltage Considerations* section to show ac-coupled input. 22
- Added new subsection titled *ADC Input Common-Mode Voltage Considerations—DC-Coupled Input* 22
- Deleted figure and last two paragraphs from the *THS770006 Driving ADS5493* section 25
- Deleted text from first sentence in the *Testing the ADS5493 with an AC-Coupled Bandpass Filter* section 25
- Deleted text from first paragraph in the *Testing the ADS5493 with an AC-Coupled Low-Pass Filter* section 27

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 0V to +5.5V and the output voltage range of 0V to +5.5V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +85°C. The EVM is designed to operate properly with certain components above +85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS770006IRGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS7700 06IRGE
THS770006IRGER.Z	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS7700 06IRGE
THS770006IRGET	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS7700 06IRGE
THS770006IRGET.Z	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS7700 06IRGE

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

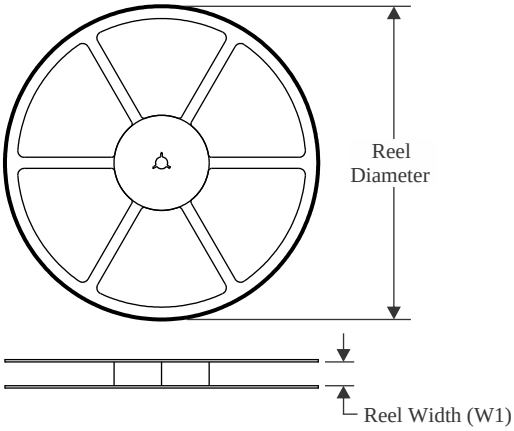
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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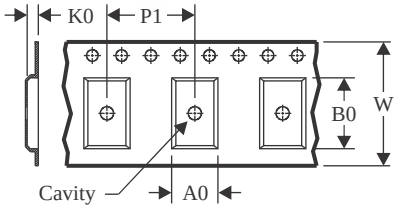
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

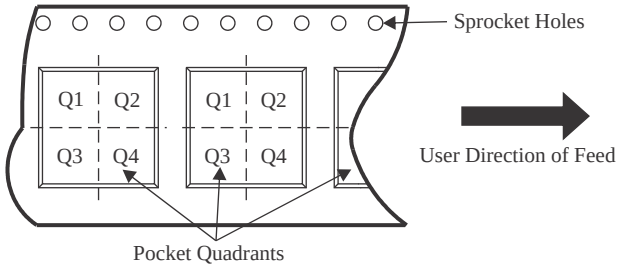


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

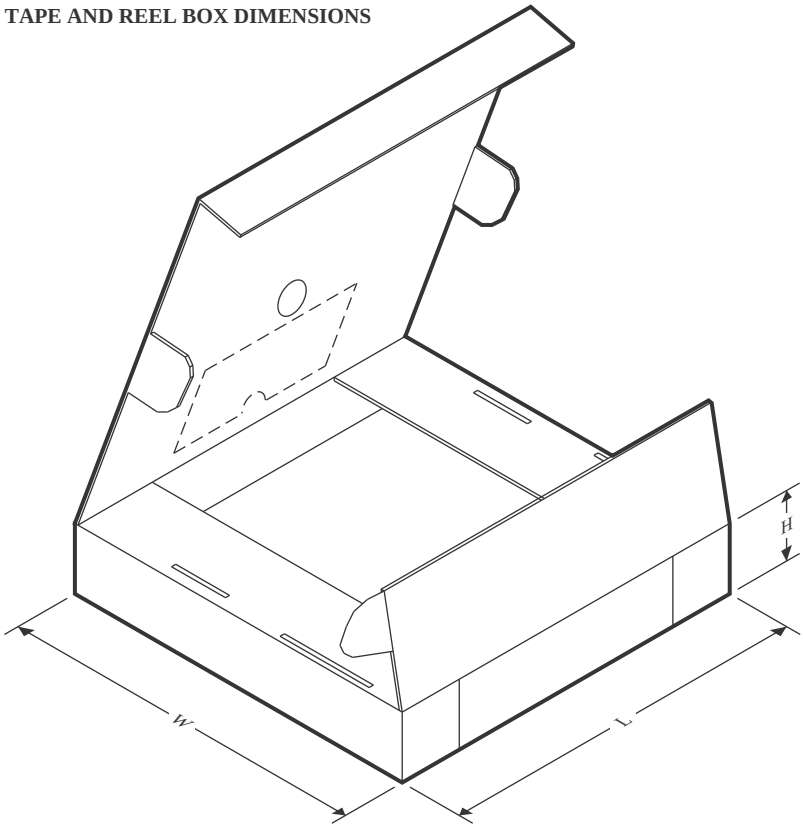
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS770006IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
THS770006IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



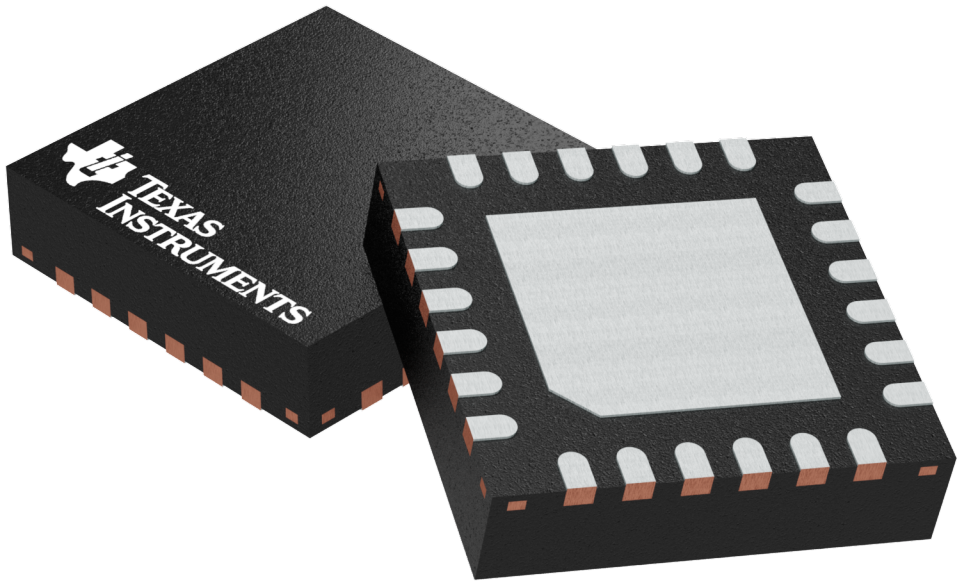
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS770006IRGER	VQFN	RGE	24	3000	356.0	356.0	35.0
THS770006IRGET	VQFN	RGE	24	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

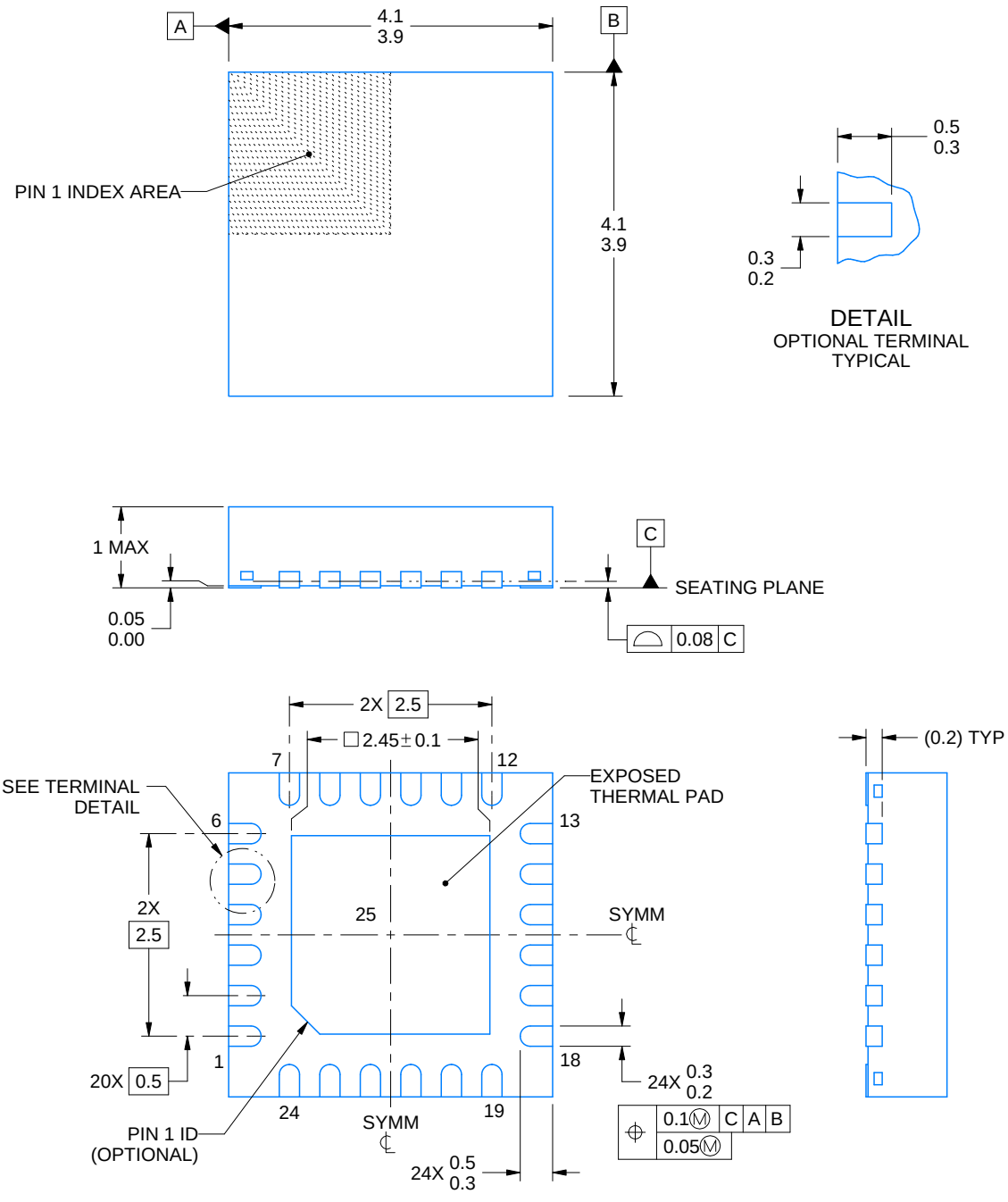
4204104/H

PACKAGE OUTLINE

RGE0024B

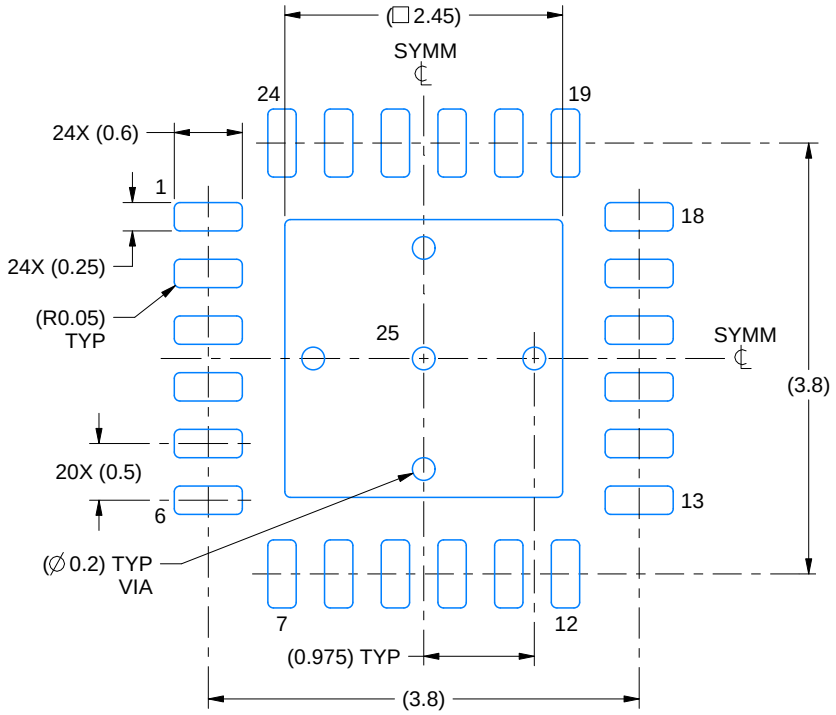
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

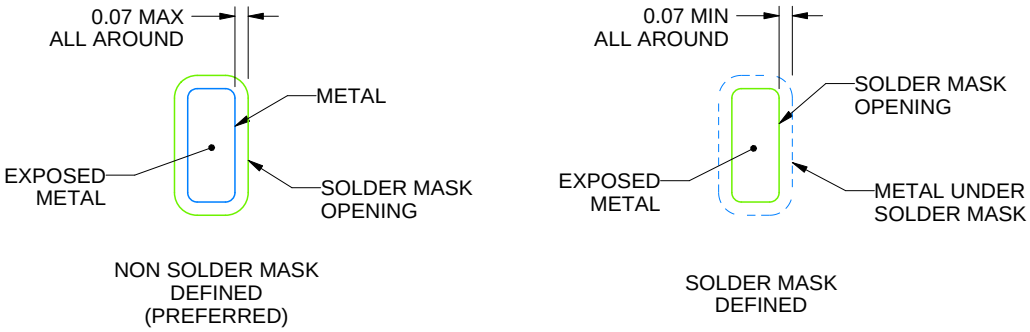


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

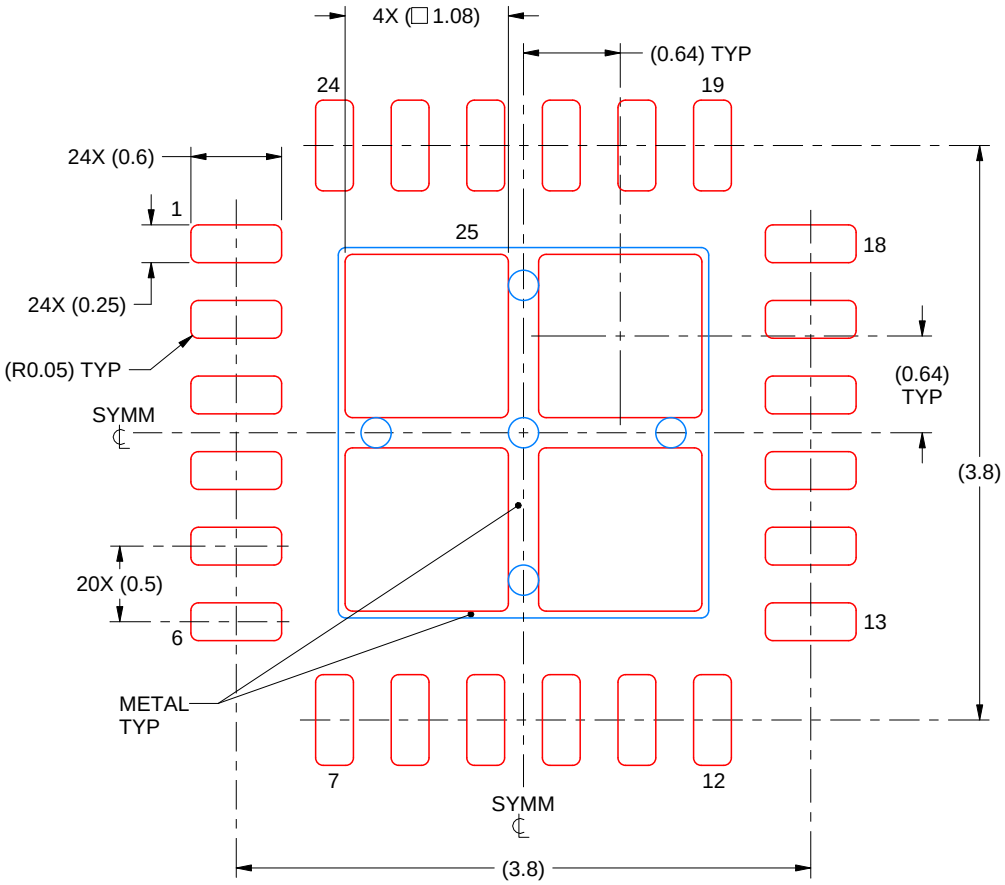


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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