XIAOHUA SEMICONDUCTOR

HC32L16x Series

32-bit ARM® Cortex®-M0+ Microcontroller

Datasheet

May 2024

Rev1.01

Features

Feature List

- 48MHz Cortex-M0+ 32-bit CPU platform
- HC32L16x Series has a flexible power management system, ultra-low power performance:
  - 0.8μA @ 3V Deep-sleep mode: all clocks off, power-on reset active, IO state retention, IO interrupt active, power consumption when all registers, RAM, and CPU data are kept
  - 1.5μA @3V deep sleep mode + RTC working
  - 23μA/MHz@3V@48MHz sleep mode: CPU stop, peripherals off, main clock running
  - 52μA/MHz@3V@48MHz working mode: CPU running, peripherals off, running program from Flash
  - 10μs ultra-low power consumption wake-up time, making mode switching more flexible and efficient, and system response more agile
- Maximum 256KB Flash memory, with erase and write protection function, support ISP, ICP, IAP
- Maximum 32KB RAM memory with parity check to enhance system stability
- General I/O pins: 72 IO/80 PIN, 56 IO/64 PIN, 40 IO/48 PIN, 26 IO/32 PIN
- Clock, crystal
  - XTH: 8~32MHz
  - XTL: 32.768kHz
  - RCH: 4/8/16/22.12/24MHz
  - RC48M: 4/6/32/48MHz
  - RCL: 32.768/38.4kHz
  - PLL: 8~48MHz
  - Hardware supports internal and external clock calibration and monitoring
- Timer/counter
  - Three 1-channel complementary output general-purpose 16-bit timers
  - One 3-channel complementary output general-purpose 16-bit timer
  - Two low-power 16-bit timers, support cascading
  - One ultra-low-power pulse counter PCNT, with automatic timing wake-up function in low-power mode, the maximum timing is 1024 seconds
  - Three high-performance 16-bit timers/counters, support PWM complementary, dead zone protection function
  - One programmable 16-bit timer PCA, support 5-channel capture and compare, 5-channel PWM output
  - One 20-bit programmable watchdog circuit, built-in dedicated 10kHz oscillator to provide WDT counting
  - One 7-bit programmable window watchdog
- Communication Interface
  - Up to 4-channel UART communication interface
  - Up to 2-channel LPUART low power communication interface, can work in deep sleep mode
  - Up to 2-channel SPI communication interface
  - 2-channel I2C communication interface
- Buzzer frequency generator, support complementary output
- Calendar RTC module
- Hardware CRC16/CRC32 module
- AES-128/192/256 hardware coprocessor
- TRNG true random number generator
- 2-channel DMAC
- 4*47 / 6*45 / 8*43 LCD driver
- 10-byte unique ID
- 12-bit 1Msps sampling high-speed SAR ADC with built-in input follower to measure signals with high output impedance
- 12-bit 500ksps DAC
- Integrate a multifunctional operational amplifier, which can be used as the output buffer of DAC
- Integrated 3-channel voltage comparators with 6-bit Resistor divider and programmable comparison reference

- Integrated low voltage detector, can be configured with 16-step comparison voltage, can monitor port voltage and power supply voltage
- SWD debugging solution, providing a full-featured debugger
- Working conditions: -40~85℃, 1.8~5.5V
- Package form: LQFP80/64/48, QFN32

Support Model

HC32L166MCTA-LQFP80	HC32L166MATA-LQFP80
HC32L166KCTA-LQFP64	HC32L166KATA-LQFP64
HC32L166KCTA-LQ64	HC32L166KATA-LQ64
HC32L166JCTA-LQ48	HC32L166JATA-LQ48
HC32L160FCUA-QFN32TR	HC32L160FAUA-QFN32TR

Statement

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Xiaohua Semiconductor Co., Ltd.

Address:	4th Floor, Building A, No. 1867, Zhongke Road, Pudong New Area, Shanghai
URL:	https://www.xhsc.com.cn/
Mail:	XHSC_MCU@xhsc.com.cn
Telephone:	021-38880888-887

Preface

Data format

- The 0x prefix indicates hexadecimal data
- The 0b prefix indicates binary data
- Numbers without a prefix represent decimal data

Security Statement

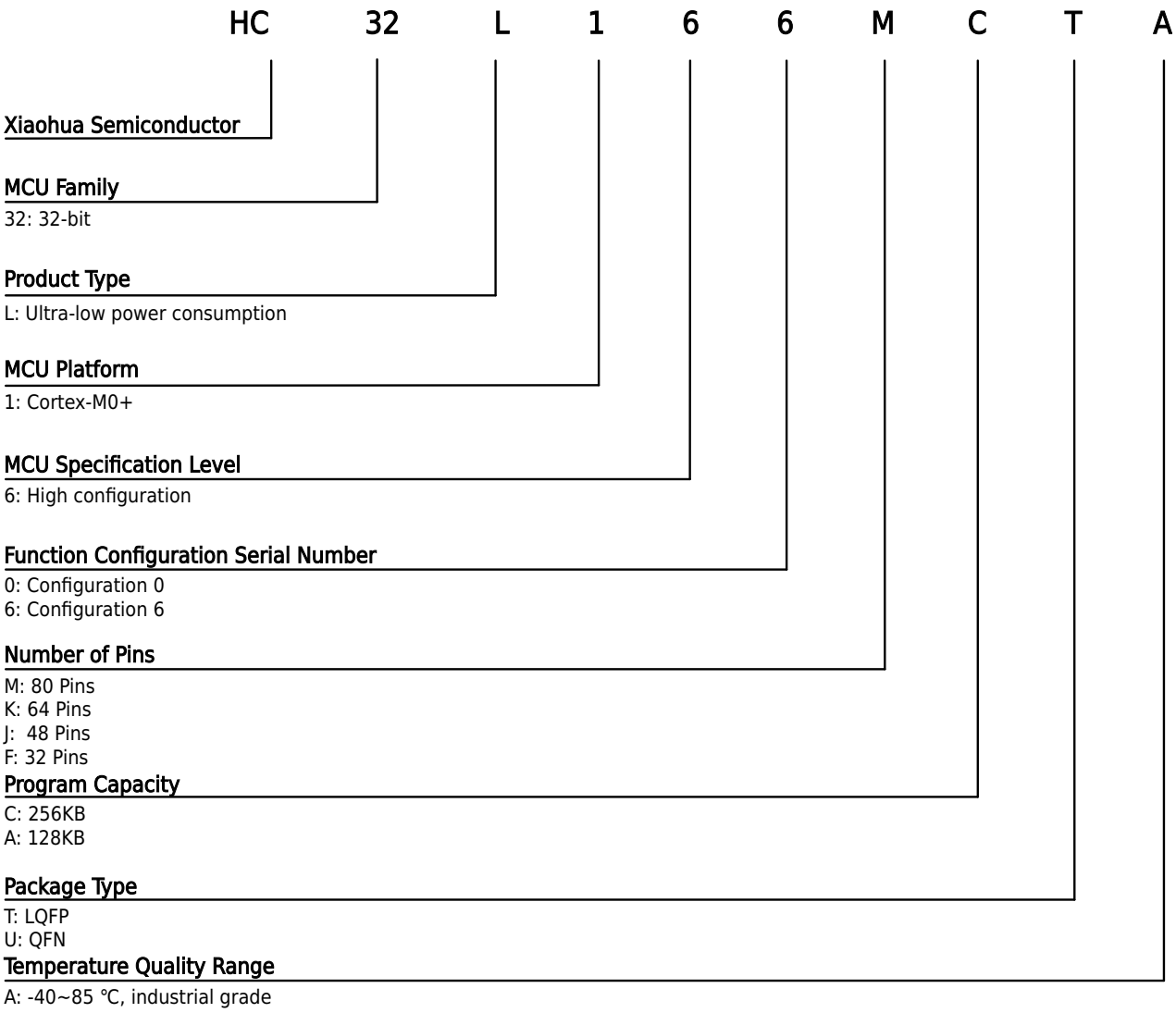
Since there may be potential security issues when using a certain function or protocol, a statement is needed to remind users to use it with caution and avoid security risks.

Table of Contents

1 Product Overview

1.1 Product Lineup

Product Name



Model Function Comparison Table

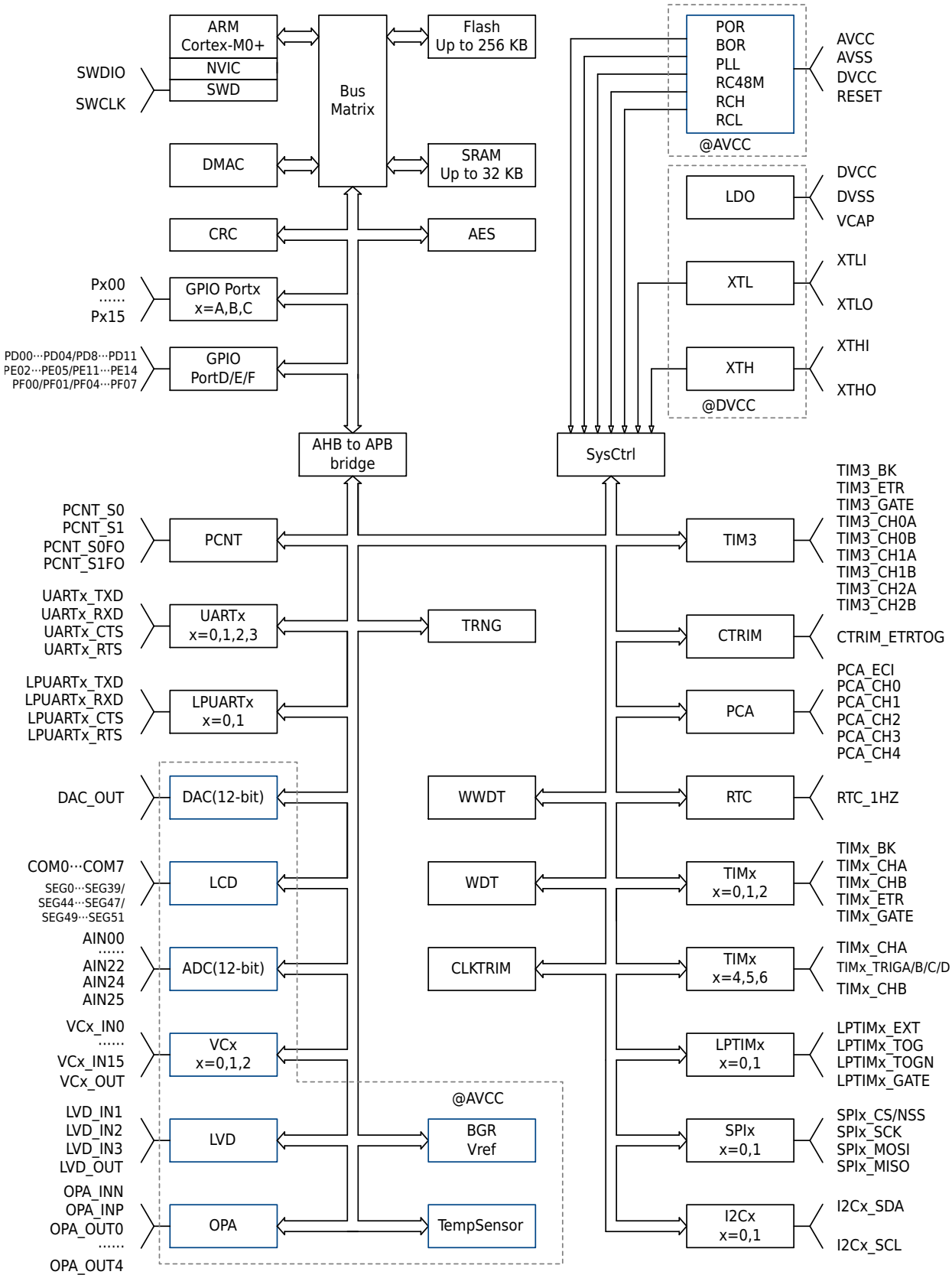
Product name		HC32L166MCTA	HC32L166KCTA	HC32L166JCTA	HC32L160FCUA	HC32L166MATA	HC32L166KATA	HC32L166JATA	HC32L160FAUA
Pin number		80	64	48	32	80	64	48	32
Number of GPIOs		72	56	40	26	72	56	40	26
CPU	Core	Cortex-M0+							
	Frequency	48MHz							
Storage	Flash	256KB				128KB			
	RAM	32KB				16KB			
Clock	Internal high speed clock	RCH 4/8/16/22.12/24MHz							
		RC48M 4/6/32/48MHz							
	Internal low speed clock	RCL 32.768/38.4kHz							
	PLL	8-48MHz							
	External high speed crystal	XTH 8~32MHz							
	External low-speed crystal	XTL 32.768kHz							
Supply voltage range		1.8~5.5V							
Single / dual power supply		Single power supply							
Temperature range		-40~85℃							
Port interrupt		72	56	40	26	72	56	40	26
DMAC		2ch							
Timer		General timer TIM0/1/2/3 Advanced Timer (TIM4/5/6) Low Power Timer LPTIM0/1							
RTC		1							
Watchdog Timer		Independent Watchdog*1 Window Watchdog*1							
PCNT		1							
Communication Interface		UART0/1/2/3 LPUART0/1 I2C0/1 SPI0/1		UART0/1 LPUART0/1 I2C0/1 SPI0/1	UART0/1(1) LPUART0 I2C0/1 SPI0	UART0/1/2/3 LPUART0/1 I2C0/1 SPI0/1		UART0/1 LPUART0/1 I2C0/1 SPI0/1	UART0/1(1) LPUART0 I2C0/1 SPI0

Product name	HC32L166MCTA	HC32L166KCTA	HC32L166JCTA	HC32L160FCUA	HC32L166MATA	HC32L166KATA	HC32L166JATA	HC32L160FAUA
ADC, 12-bit	25ch	23ch	17ch	8ch	25ch	23ch	17ch	8ch
DAC, 12-bit	1							
OPA	1		-		1		-	
VC	VC0/1/2							
LCD	4*47/6*45/8*43	4*40/6*38/8*36	4*26	-	4*47/6*45/8*43	4*40/6*38/8*36	4*26	-
LVD	1							
Buzzer	Support							
Flash security protection	Support							
RAM parity	Support							
CRC	Support							
TRNG	Support							
AES	Support							
CLKTRIM/CTRIM	Support							
Debug function	SWD debug interface							
Unique identification code	Support							
Package type	LQFP80(12*12mm)	LQFP64(10*10mm) LQFP64(7*7mm)	LQFP48(7*7mm)	QFN32(4*4mm)	LQFP80(12*12mm)	LQFP64(10*10mm) LQFP64(7*7mm)	LQFP48(7*7mm)	QFN32(4*4mm)

Note

1. QFN32 package, UART1 lacks RTS function pin.

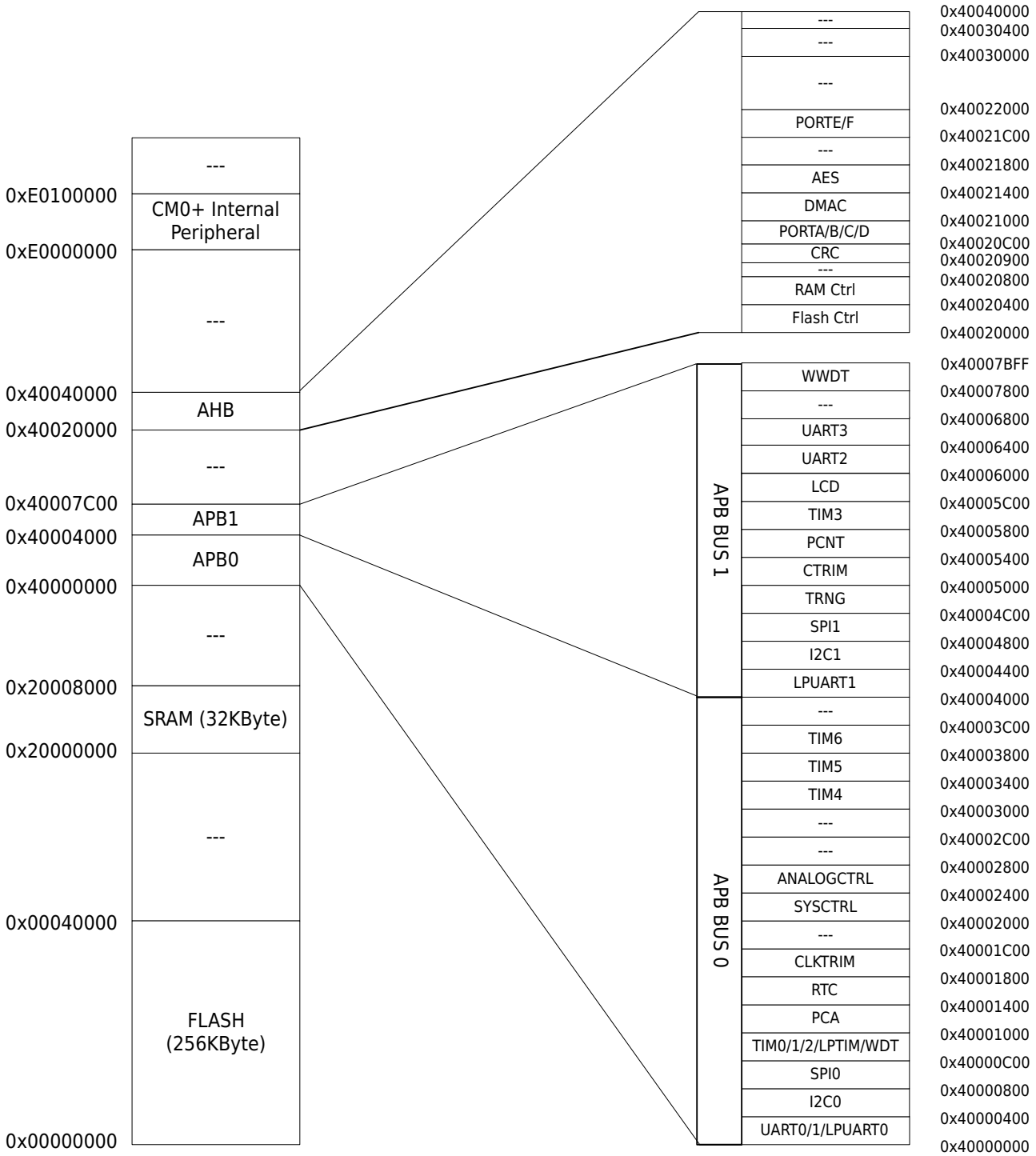
1.2 Functional Block Diagram



Note

Products with different packages support different numbers of resources. For detailed support information, please refer to Model Function Comparison Table.

1.3 Memory Map



Note

The PORTA/B/C/D and PORTE/F modules use two different address spaces.

The FLASH and SRAM sizes supported by products with different packages are different. You need to pay attention to the range of the address space when using them. For details, please refer to Model Function Comparison Table.

2 Functional Description

2.1 32-bit Cortex-M0+ Core

The ARM Cortex-M0+ processor is derived from Cortex-M0 and includes a 32-bit RISC processor with a computing power of 0.95 Dhrystone MIPS/MHz. At the same time, a number of new designs have been added to improve debugging and tracing capabilities, reduce the number of each instruction cycle (IPC) and improve the two-stage pipeline for Flash access, and incorporate energy-saving and consumption-reducing technologies. The Cortex-M0+ processor fully supports the integrated Keil & IAR debugger.

Cortex-M0+ Contains a hardware debugging circuit that supports a 2-pin SWD debugging interface.

ARM Cortex-M0+ features:

Instruction Set	Thumb / Thumb-2
Assembly line	2-stage assembly line
Performance efficiency	2.46 CoreMark / MHz
Performance efficiency	0.95 DMIPS / MHz in Dhrystone
Interrupt	32 fast interrupts
Interrupt priority	Configurable 4-level interrupt priority
Enhanced instruction	Single-cycle 32-bit multiplier
Debugging	Serial-wire debug port, supports 4 hard interrupts (break points) and 2 watch points (watch points)

2.2 256KB/128KB FLASH

Built-in fully integrated FLASH controller, no external high voltage input is required, high voltage is generated by the fully built-in circuit for programming Support ISP, IAP, ICP functions.

2.3 32KB/16KB RAM

According to different ultra-low power modes selected by customers, RAM data will be retained. With hardware parity bit, in case the data is accidentally damaged, when the data is read, the hardware circuit will immediately generate an interrupt to ensure the reliability of the system.

2.4 Clock System

- A internal clock RCH with a configurable frequency of 4/8/16/22.12/24MHz.
- A high-precision internal clock RC48M with a configurable frequency of 4/6/32/48MHz.
- An external crystal oscillator XTH with a frequency of 8~32MHz.
- An external crystal oscillator XTL with a frequency of 32.768kHz mainly provides the RTC real-time clock.
- An internal clock RCL with a frequency of 32.768/38.4 kHz.
- A PLL with 8~48 MHz output frequency.

2.5 Operating Mode

1. Running mode (Active Mode): CPU running, peripheral function modules running.
2. Sleep Mode (Sleep Mode): The CPU stops running, and the peripheral function modules running.
3. Deep sleep mode (Deep Sleep Mode): The CPU stops running and the high-speed clock module stops running.

2.6 Real Time Clock (RTC)

RTC (Real Time Counter) is a functional module that supports BCD data format. It generally uses a 32.768kHz crystal oscillator as its clock to realize the perpetual calendar function, and the interrupt period can be configured as month/day/hour/minute/second. 24/12 hour time mode, the hardware automatically corrects leap years. With accuracy compensation function, the highest accuracy is 0.95ppm. Internal temperature sensor or external temperature sensor can be used for accuracy compensation, software +1/-1 can be used to adjust year/month/day/hour/minute/second, and the minimum adjustable accuracy is 1 second.

The RTC calendar recorder used to indicate the time and date will not clear the retained value when the MCU is reset due to external factors. It is the best choice for measuring equipment and meters that require a permanent high-precision real-time clock.

2.7 Port Controller (GPIO)

It can provide up to 72 GPIO ports, some of which are multiplexed with analog ports. Each port is controlled by independent control register bits and supports FAST IO. Supports edge-triggered interrupts and level-triggered interrupts, and can wake up the MCU to working mode from various ultra-low power consumption modes. Support position, clear and clear operations. Support Push-Pull CMOS push-pull output, Open-Drain open-drain output. Built-in pull-up resistor, pull-down resistor, with Schmitt trigger input filter function. The output drive capability is configurable, and the maximum current drive capability is 16mA. All general-purpose IOs can support external asynchronous interrupts.

2.8 Interrupt Controller (NVIC)

The Cortex-M0+ processor has a built-in nested vectored interrupt controller (NVIC), which supports up to 32 interrupt request (IRQ) inputs; it has four interrupt priority levels, can handle complex logic, and can perform real-time control and interrupt processing.

2.9 Reset Controller (RESET)

This product has 8 reset signal sources, each reset signal can make the CPU run again, most of the registers will be reset again, and the program counter PC will point to the starting address.

- Digital area power-on/power-off reset POR
- External Reset PAD, low level is reset signal
- WWDT reset
- WDT reset
- PCA Reset
- LVD low voltage reset
- Cortex-M0+ SYSRESETREQ software reset
- Cortex-M0+ LOCKUP hardware reset

2.10 DMA Controller (DMAC)

The DMAC (Direct Memory Access Controller) function block can transmit data at high speed without passing through the CPU. Using DMAC can improve system performance.

- The DMAC is equipped with an independent bus, so even when the CPU bus is used, the DMAC can also perform transfer operations.
- Composed of 2 channels, capable of performing 2 independent DMA transfers.
- The transmission destination address, transmission source address, transmission data size, transmission request source, and transmission mode can be set, and the transmission operation start of each channel, the forced termination of transmission and the suspension of transmission can be controlled.
- It can control the start, forcibly terminate and pause of batch transmission of all channels.
- When multiple channels are operated at the same time, a fixed method or a cyclic method can be used to select the priority of the operating channel.
- Supports hardware DMA transfer using peripheral interrupt signals.
- Comply with system bus (AHB) and support 32-bit address space (4GB).

2.11 Timer (TIM)

Types of	Name	Bit width	Prescaler	Counting direction	PWM	capture	Complementary output
Universal timer	TIM0	16/32	1/2/4/8/16/32/64/256	Up count/down count/up and down count	2	2	1
	TIM1	16/32	1/2/4/8/16/32/64/256	Up count/down count/up and down count	2	2	1
	TIM2	16/32	1/2/4/8/16/32/64/256	Up count/down count/up and down count	2	2	1
	TIM3	16/32	1/2/4/8/16/32/64/256	Up count/down count/up and down count	6	6	3
Low power timer	LPTIM0	16	1/2/4/8/16/32/64/256	Up count	No	No	No
	LPTIM1	16	1/2/4/8/16/32/64/256	Up count	No	No	No
Programmable counting array	PCA	16	2/4/8/16/32	Up count	5	5	No
Advanced timer	TIM4	16	1/2/4/8/16/64/256/1024	Up count/down count/up and down count	2	2	1
	TIM5	16	1/2/4/8/16/64/256/1024	Up count/down count/up and down count	2	2	1

Types of	Name	Bit width	Prescaler	Counting direction	PWM	capture	Complementary output
Advanced timer	TIM6	16	1/2/4/8/16/64/256/1024	Up count/down count/up and down count	2	2	1

The general timer includes four timers TIM0/1/2/3, which have the following features:

- PWM independent output, complementary output
- Capture input
- Pulse Width Measurement
- Quadrature code counting function
- Single pulse mode
- External counting function
- DMA trigger
- Dead zone control
- Brake control
- Wave-by-wave current limiting
- Edge alignment, symmetric center alignment and asymmetric center alignment PWM output

TIM0/1/2 have exactly the same function. TIM0/1/2 is a synchronous timer/counter, which can be used as a 16-bit timer/counter with automatic reloading function, or as a 32-bit timer/counter without reloading function. Each timer of TIM0/1/2 has 2 channels of capture and comparison function, which can generate 2 channels of independent PWM output or 1 group of complementary PWM outputs. With dead zone control function.

TIM3 is a multi-channel general-purpose timer with all the functions of TIM0/1/2. It can generate 3 sets of complementary PWM outputs or 6 independent PWM outputs, and up to 6 input captures. With dead zone control function.

The low-power timer LPTIM is an asynchronous 16-bit timer/counter. After the system clock is turned off, it can still clock/count through the internal low-speed RC or external low-speed crystal oscillator. Wake up the system in low-power mode through interrupts.

The PCA (Programmable Counter Array) supports up to five 16-bit capture/compare modules. The timer/counter can be used as a common clock count/event counter capture/compare function. Each module of PCA can be independently programmed to provide input capture, output comparison or pulse width modulation. In addition, module 4 has an additional watchdog timer mode.

Advanced Timer Advanced Timer contains three timers TIM4/5/6. TIM4/5/6 is a high-performance counter with the same function, which can be used to count and generate different forms of clock waveforms. One timer can generate a complementary pair of PWM or independent 2-way PWM output, which can capture external input for pulse width or Period measurement.

The basic functions and features of Advanced Timer are shown in the table:

Table 2-3 Advanced Timer Basic Features

Basic Features	Description
Waveform Mode	Sawtooth wave, triangle wave

Basic Features	Description
Basic Functions	Incremental and decremental counting direction
	Software synchronization
	Hardware synchronization
	Cache function
	Capturing Input
	Pulse width/period measurement
	External input count
	Orthogonal Encoding Count
	General purpose PWM output
	Dead zone control
	Protection Mechanism
	AOS associated actions
Interrupt Type	Count compare match interrupt
	Count period match interrupt
	Dead time error interrupt
	Same high and same low interrupt

2.12 Pulse Counter (PCNT)

The PCNT (Pulse Counter) module is used to count external pulses and supports single-channel and dual-channel (quadrature code and non-interleaved code) pulses. It can count in low-power sleep mode without software involvement.

Pulse counter characteristics:

- 16-bit counter supporting reload function
- Single channel pulse count
- Dual channel non-intersecting pulse counting
- Dual channel quadrature pulse counting without missing codes
- Up/down counting overflow interrupt
- Pulse timeout interrupt
- 4 kinds of decoding error interrupt, non-intermittent pulse mode
- 1 direction change interrupt, quadrature pulse mode
- Multi-stage pulse width filtering
- Configurable input pulse polarity
- Support low-power mode counting
- Support waking up MCU in low power mode
- Support any pulse edge spacing not less than 1 count clock cycle
- With automatic timing wake-up function in low power consumption mode, the maximum timing is 1024 seconds

2.13 Watchdog (WDT)

WDT (Watch Dog Timer) is a configurable 20-bit timer that provides reset in the case of MCU abnormality; built-in 10kHz low-speed clock input is used as the counter clock. In debug mode, you can choose to pause or continue to run; WDT can only be restarted by writing a specific sequence.

WWDT is a 7-bit timer. When external interference or unforeseen logic conditions cause the application program to deviate from the normal running sequence, WWDT can detect such software failures and generate interrupts or resets.

2.14 Universal Asynchronous Receiver/Transmitter (UART)

4-channel universal synchronous asynchronous receiver/transmitter (Universal Asynchronous Receiver/Transmitter), UART0~UART3.

Basic functions of universal UART:

- Synchronous half-duplex, asynchronous full-duplex, single-line half-duplex transmission
- Programmable serial communication function
  - Two character lengths: 8-bit and 9-bit
  - Three check modes: no check, odd check, even check
  - Three stop lengths: 1-bit, 2-bit, 1.5-bit
- 16-bit baud rate counter
- Hardware flow control (RTS, CTS)
- Multi-machine communication, automatic address recognition
- Supports data transfer via DMA

2.15 Low Power Universal Asynchronous Receiver/Transmitter (LPUART)

2-channel synchronous asynchronous transceiver (Low Power Universal Asynchronous Receiver/Transmitter) that can work in low power consumption mode, LPUART0/LPUART1.

Basic functions of LPUART:

- Configuration clock PCLK
- Transmission clock SCLK (SCLK can select XTL, RCL and PCLK)
- Sending and receiving data in low power mode
- Synchronous half-duplex, asynchronous full-duplex, single-line half-duplex transmission
- Programmable serial communication function
  - Two character lengths: 8-bit and 9-bit
  - Three check modes: no check, odd check, even check
  - Three stop lengths: 1-bit, 2-bit, 1.5-bit
- 16-bit baud rate counter
- Hardware flow control (RTS, CTS)
- Multi-machine communication, automatic address recognition
- Supports data transfer via DMA

2.16 Serial Peripheral Interface (SPI)

2-channel synchronous serial interface (Serial Peripheral Interface)

Basic characteristics of SPI:

- Support SPI master mode and SPI slave mode
- Support standard four-wire full-duplex communication

- Supports configuration of serial clock polarity and phase
- The maximum division factor of the host mode is PCLK/2, and the maximum communication rate is 16Mbps
- The maximum division factor of slave mode is PCLK/4, and the maximum communication rate is 6Mbps
- The frame length is fixed at 8 bits
- Support DMA hardware transfer handshake

2.17 I2C Bus

2-channel I2C, using serial synchronous clock, can realize data transmission between devices at different rates.

Basic characteristics of I2C:

- Supports four working modes: master send/receive, slave send/receive
- Supports three working speeds: Standard (100kbps) / Fast (400kbps) / Fast Plus (1Mbps)
- Support 7-bit addressing function
- Support noise filtering function
- Support three slave addresses
- Support broadcast address
- Support interrupt status query function

2.18 Buzzer

4 general-purpose timers and 2 low-power timers function multiplexing output to provide programmable driving frequency for Buzzer. The buzzer port can provide 16mA sink current, complementary output, no additional transistor is needed.

2.19 Clock Calibration Circuit Module (CLKTRIM)

The built-in clock calibration circuit can calibrate the internal RC clock through an external accurate crystal clock, and can also use the internal RC clock to check whether the external crystal clock is working properly.

Basic features of clock calibration:

- Calibration mode
- Monitoring mode
- 32-bit reference clock counter can be loaded with initial value
- 32-bit clock counter to be calibrated with configurable overflow value
- 6 reference clock sources
- 5 clock sources to be calibrated
- Support interrupt mode

2.20 Clock Calibration (CTRIM)

When the module works in calibration mode, it can automatically calibrate the output frequency of RCH/RC48M/RCL in real time, so that the accuracy of RCH/RC48M/RCL output frequency is close to the target value. When the module works in timer mode, it has general timing function and can still work normally under DeepSleep.

2.21 Device Electronic Signature

Each chip has a unique 10-byte device identification number before leaving the factory, including wafer-lot information and chip coordinate information. The UID addresses are: 0x00101E94~0x00101E9D.

2.22 Cyclic Redundancy Check (CRC)

CRC16 conforms to the polynomial given in ISO/IEC13239: $X^{16}+X^{12}+X^{5}+1$.

CRC32 conforms to the polynomial given in ISO/IEC13239:
$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^{8}+x^{7}+x^{5}+x^{4}+x^{2}+x+1$.

2.23 Advanced Encryption Standard Module (AES)

AES (The Advanced Encryption Standard) is a new data encryption standard officially announced by the National Institute of Standards and Technology (NIST) of the United States on November 26, 2001. AES is fixed at 128 bits, while the key length supports 128/192/256 bits.

2.24 True Random Number Generator (TRNG)

TRNG is a true random number generator, used to generate true random numbers.

2.25 Analog to Digital Converter (ADC)

A 12-bit successive approximation analog-to-digital converter with monotonous and no missing codes, when working under a 24MHz ADC clock, the sampling rate reaches 1Msps. The reference voltage can be selected from the on-chip precision voltage (1.5V or 2.5V) or from an external input or power supply voltage.

Basic characteristics of SAR ADC:

- 12-bit conversion accuracy;
- 1Msps conversion speed;
- Up to 28 input channels, including 25 external pin inputs, 1 internal temperature sensor voltage, 1 1/3 AVCC voltage, and 1 DAC internal output;
- 4 reference sources: AVCC voltage, EXVREF pin, built-in 1.5V reference voltage, built-in 2.5V reference voltage;
- ADC voltage input range: 0~Vref;
- 4 conversion modes: single conversion, SQR scan continuous conversion, JQR scan continuous conversion, continuous conversion accumulation;
- Input channel voltage threshold monitoring;
- Software configurable ADC conversion rate;
- Built-in signal follower, capable of converting high impedance signals;
- Supports automatic triggering of ADC conversion by on-chip peripherals, effectively reducing chip power consumption and improving the real-time performance of conversion.

2.26 Digital to Analog Converter (DAC)

1-channel 12-bit 500ksps DAC, capable of digital-to-analog conversion.

2.27 Analog Voltage Comparator (VC)

Built-in 3-channel VC, chip pin voltage monitoring/comparison circuit. 16 configurable positive external input channels (including DAC output voltage), 11 configurable negative external input channels (including DAC output voltage); 4 internal negative input channels, including 1 internal temperature sensor voltage, 1 ADC reference voltage, 1 64-step resistor divider and 1 VCAP voltage. VC output can be used

for general-purpose timer TIM0/1/2/3, low-power timer LPTIM and programmable counting array PCA for capturing, gating, and external counting clock. An asynchronous interrupt can be generated according to the rising/falling edge to wake up the MCU from the low-power mode. Configurable software anti-shake function.

2.28 Low Voltage Detector (LVD)

Detect chip power supply voltage or chip pin voltage. 16-shift voltage monitoring values (1.8~3.3V). An asynchronous interrupt or reset can be generated based on the rising/falling edge. With hardware hysteresis circuit and configurable software anti-shake function.

Basic characteristics of LVD:

- 4-channel monitoring sources, AVCC, PC13, PB08, PB07;
- 16-stage threshold voltage, 1.8~3.3V optional;
- 8 trigger conditions, combinations of high level, rising edge and falling edge;
- 2 trigger results, reset and interrupt;
- 8-stage filter configuration to prevent false triggering;
- With hysteresis function, strong anti-interference.

2.29 Operational Amplifier (OPA)

The OPA can be flexibly configured for simple filter and voltage follower applications. It can be used as a DAC output buffer or configured as an operational amplifier.

2.30 LCD controller (LCD)

The LCD Controller is a digital controller/driver for monochrome passive Liquid Crystal Displays (LCDs) with up to 8 common terminals (COM) to drive 188 (4x47), 270 (6x45), or 344 (8x43) LCD picture elements. You can choose either capacitor voltage divider or resistor voltage divider to support internal resistor divider. The internal resistance divider can adjust the contrast. Support DMA hardware data transfer.

Basic characteristics of LCD:

- Highly flexible frame rate control
- Supports static, 1/2, 1/3, 1/4, 1/6 and 1/8 duty cycles
- Support 1/2, 1/3 bias
- Up to 16 registers of LCD data RAM
- LCD contrast can be configured via software
- 3 driving waveform generation methods
  - Internal resistance voltage division, external resistance voltage division, external capacitance voltage division
  - The power consumption of the internal resistor divider can be configured by software to match the capacitive charge required by the LCD panel
- Support low power mode: LCD controller can display in Active, Sleep, DeepSleep mode
- Configurable frame interruption
- Support LCD flashing function and can configure multiple flashing frequencies
- Unused LCD segments and common pins can be configured as digital or analog functions

2.31 Embedded Debugging System

Embedded debugging solution, providing a full-featured real-time debugger, with standard mature Keil/IAR and other debugging and development software. Support 4 hard breakpoints and multiple soft breakpoints.

2.32 Programming Mode

Two programming modes are supported: online programming and offline programming.

Support two programming protocols: ISP protocol, SWD protocol.

Support unified programming interface: ISP protocol and SWD protocol share SWD port.

When reset, BOOT0 (PF11) pin is high level, the chip works in ISP programming mode, and Flash can be programmed through ISP protocol.

When reset, BOOT0 (PF11) pin is low level, the chip works in user mode, the chip executes the program code in the Flash, and the Flash can be programmed through the SWD protocol.

2.33 High Security

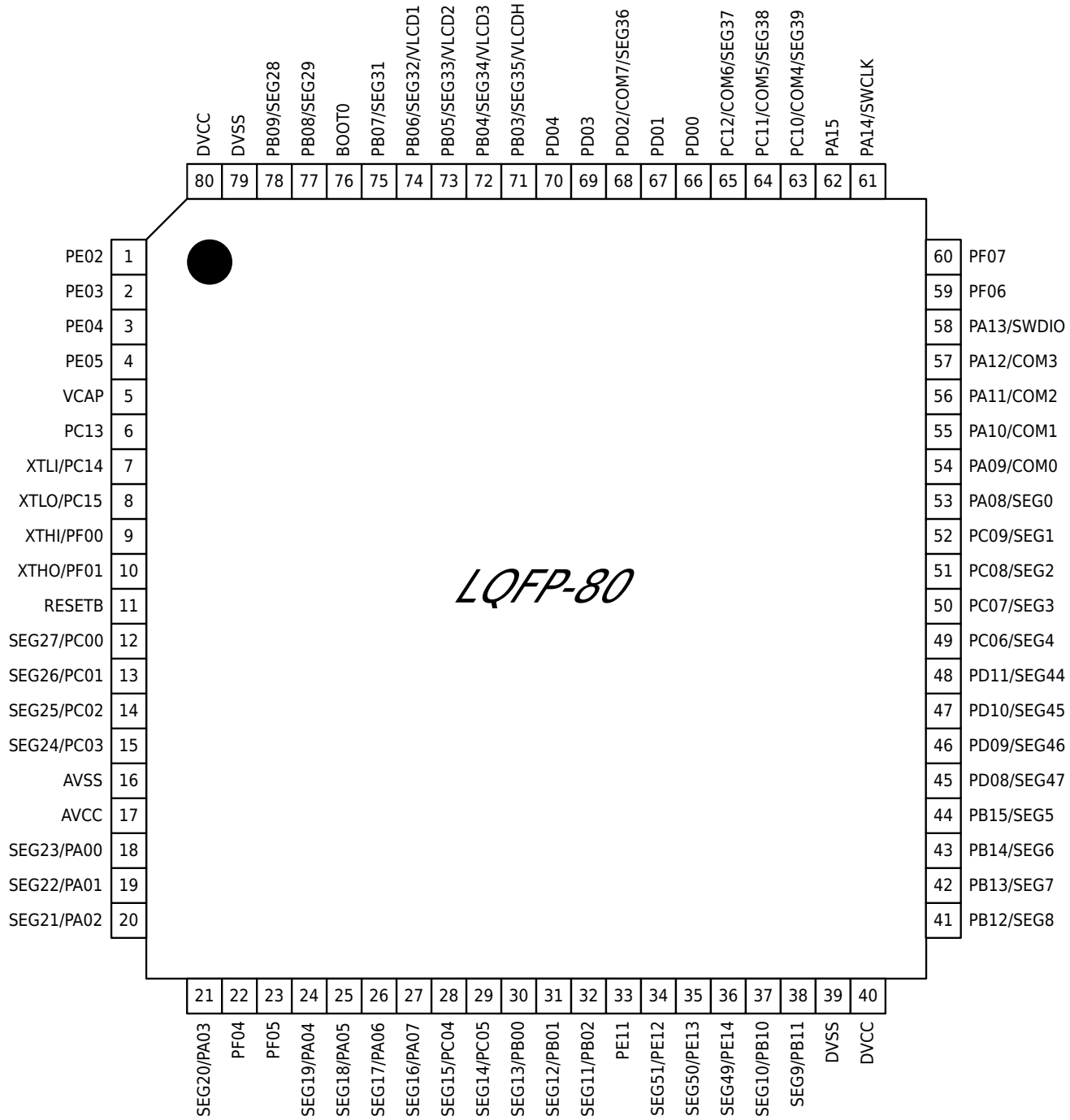
Encrypted embedded debugging solution, providing a full-featured real-time debugger.

3 Pin Definitions

3.1 Pin Configuration Diagram

3.1.1 LQFP80 Package

HC32L166MCTA-LQFP80/HC32L166MATA-LQFP80

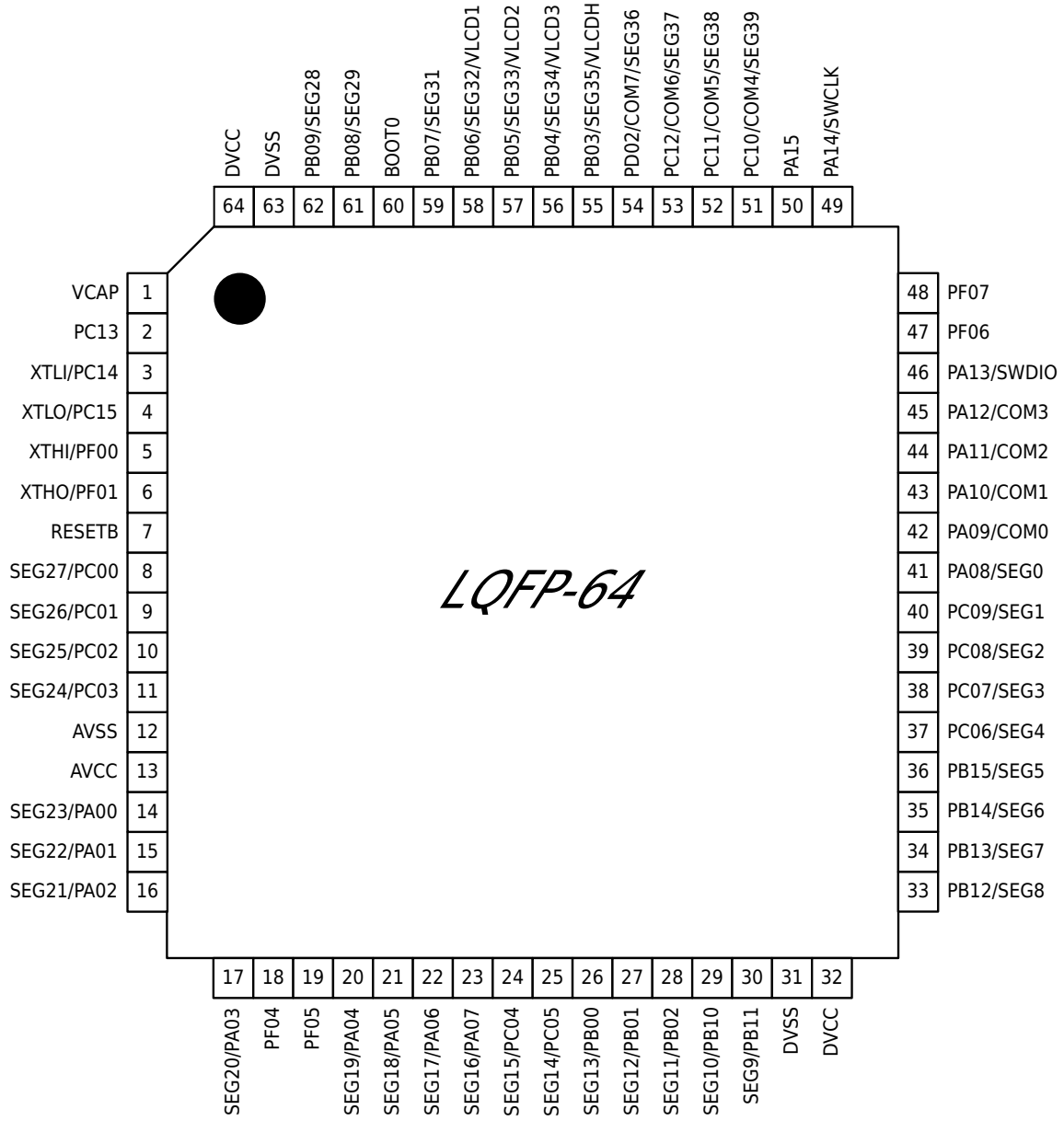


Note

- BOOT0 pin is used to control FLASH programming, see Module Signal Description.

3.1.2 LQFP64 Package

HC32L166KCTA-LQFP64/HC32L166KCTA-LQ64/HC32L166KATA-LQFP64/HC32L166KATA-LQ64

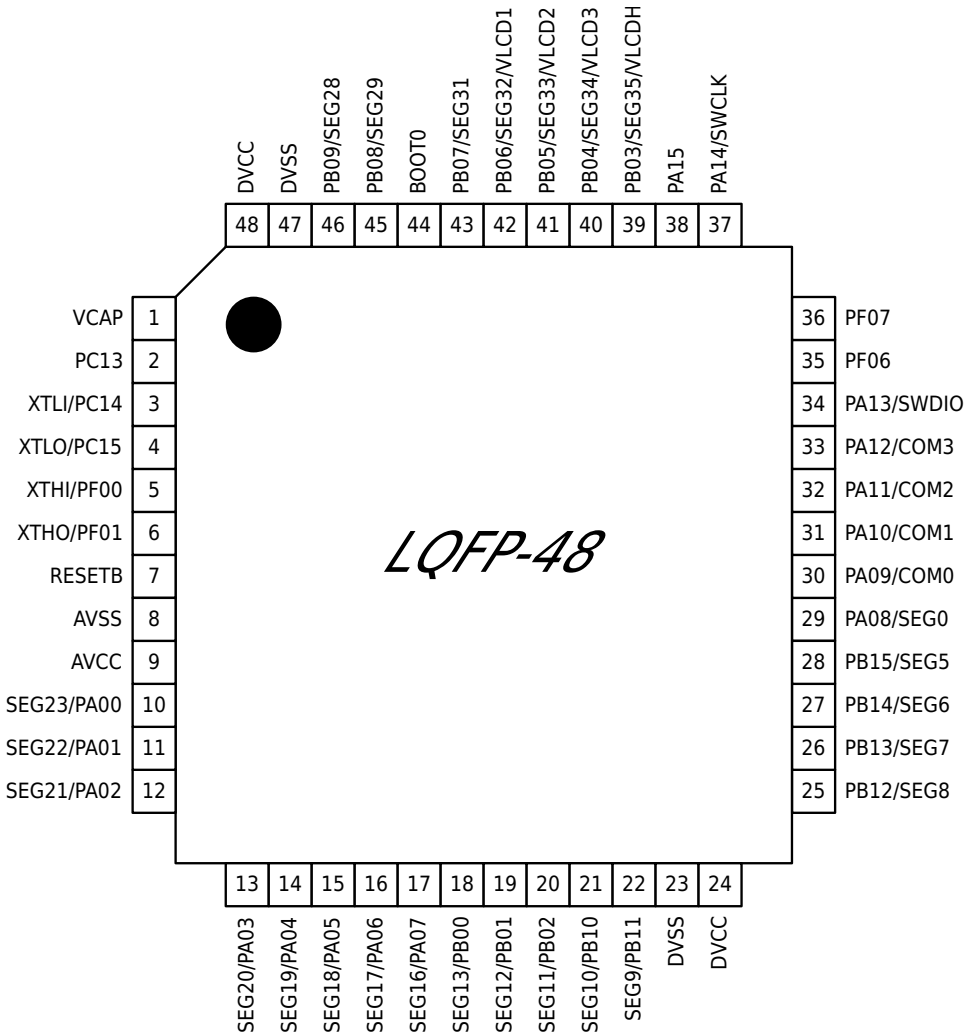


Note

- For details on the IOs not brought out by this package, please refer to Pin Function Description.
- BOOT0 pin is used to control FLASH programming, see Module Signal Description.

3.1.3 LQFP48 Package

HC32L166JCTA-LQ48/HC32L166JATA-LQ48

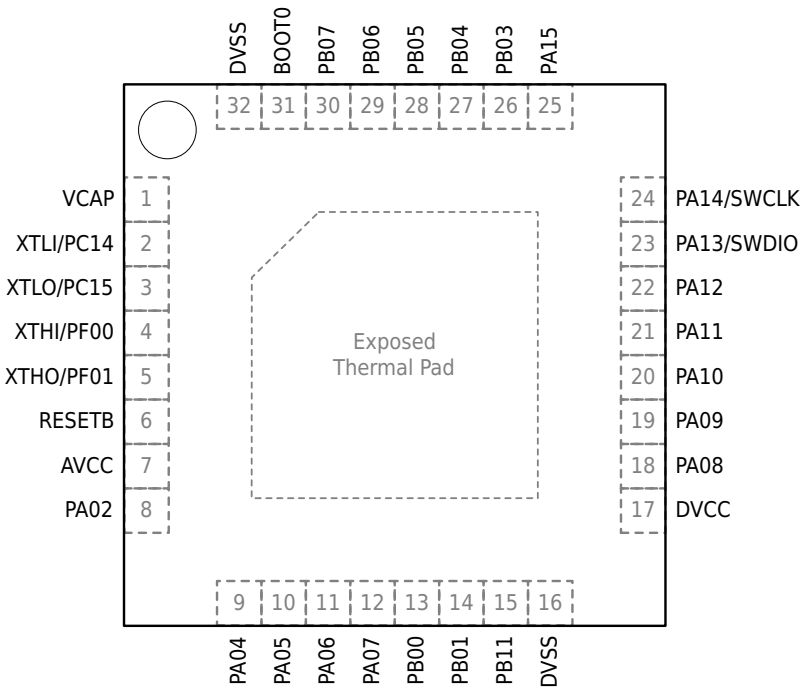


Note

- For details on the IOs not brought out by this package, please refer to Pin Function Description.
- BOOT0 pin is used to control FLASH programming, see Module Signal Description.

3.1.4 QFN32 Package

HC32L160FCUA-QFN32TR/HC32L160FAUA-QFN32TR



Note

- Exposed Thermal Pad needs to be connected to DVSS.
- For details on the IOs not brought out by this package, please refer to Pin Function Description.
- BOOT0 pin is used to control FLASH programming, see Module Signal Description.

3.2 Pin Function Description

LQFP80	LQFP64	LQFP48	QFN32	Name	ANALOG
1				PE02	-
2				PE03	-
3				PE04	-
4				PE05	-
5	1	1	1	VCAP	-
6	2	2		PC13	LVD0
7	3	3	2	PC14	XTLI
8	4	4	3	PC15	XTLO
9	5	5	4	PF00	XTHI
10	6	6	5	PF01	XTHO
11	7	7	6	RESETB	-
12	8			PC00	AIN10 VC0_INP0 VC1_INN0 SEG27
13	9			PC01	AIN11 VC0_INP1 VC1_INN1 SEG26
14	10			PC02	AIN12 VC0_INP2 VC1_INN2 SEG25
15	11			PC03	AIN13 VC0_INP3 VC1_INN3 SEG24
16	12	8		AVSS	-
17	13	9	7	AVCC	-
18	14	10		PA00	AIN0 VC0_INP4 VC0_INN0 VC1_INP0 VC1_INN4 SEG23
19	15	11		PA01	AIN1 VC0_INP5 VC0_INN1 VC1_INP1 VC1_INN5 SEG22
20	16	12	8	PA02	AIN2 VC0_INP6 VC0_INN2 VC1_INP2 SEG21

LQFP80	LQFP64	LQFP48	QFN32	Name	ANALOG
21	17	13		PA03	AIN3 VC0_INP7 VC0_INN3 VC1_INP3 SEG20
22	18			PF04	-
23	19			PF05	-
24	20	14	9	PA04	AIN4 VC0_INP8 VC0_INN4 VC1_INP4 DAC_OUT OPA_OUT0 SEG19
25	21	15	10	PA05	AIN5 VC0_INP9 VC0_INN5 VC1_INP5 VC2_INP0 VC2_INN0 OPA_OUT1 SEG18
26	22	16	11	PA06	AIN6 VC0_INP10 VC0_INN6 OPA_OUT2 SEG17
27	23	17	12	PA07	AIN7 VC0_INP11 VC0_INN7 OPA_OUT3 SEG16
28	24			PC04	AIN14 VC0_INN8 OPA_OUT4 SEG15
29	25			PC05	AIN15 VC0_INN9 OPA_INN SEG14
30	26	18	13	PB00	AIN8 VC1_INN6 OPA_INP SEG13
31	27	19	14	PB01	AIN9/EXVREF VC1_INP6 VC1_INN7 VC2_INP1 VC2_INN1 SEG12
32	28	20		PB02	AIN16 VC1_INP7 VC1_INN8 SEG11

LQFP80	LQFP64	LQFP48	QFN32	Name	ANALOG
33				PE11	VC2_INP4 VC2_INN2
34				PE12	SEG51
35				PE13	AIN25 VC2_INP5 SEG50
36				PE14	AIN24 VC2_INP6 SEG49
37	29	21		PB10	AIN17 VC1_INP8 SEG10
38	30	22	15	PB11	AIN18 VC2_INP8 VC2_INN4 SEG9
39	31	23	16	DVSS	-
40	32	24	17	DVCC	-
41	33	25		PB12	AIN19 VC1_INP9 SEG8
42	34	26		PB13	AIN20 VC1_INP10 SEG7
43	35	27		PB14	AIN21 VC1_INP11 VC2_INP9 VC2_INN5 SEG6
44	36	28		PB15	AIN22 SEG5
45				PD08	SEG47
46				PD09	VC2_INP10 SEG46
47				PD10	VC2_INP11 VC2_INN6 SEG45
48				PD11	VC2_INP12 VC2_INN7 SEG44
49	37			PC06	SEG4
50	38			PC07	VC2_INP13 VC2_INN8 SEG3
51	39			PC08	SEG2
52	40			PC09	SEG1
53	41	29	18	PA08	SEG0
54	42	30	19	PA09	COM0
55	43	31	20	PA10	COM1
56	44	32	21	PA11	COM2
57	45	33	22	PA12	COM3

LQFP80	LQFP64	LQFP48	QFN32	Name	ANALOG
58	46	34	23	PA13/SWDIO	-
59	47	35		PF06	-
60	48	36		PF07	-
61	49	37	24	PA14/SWCLK	-
62	50	38	25	PA15	-
63	51			PC10	COM4/SEG39
64	52			PC11	COM5/SEG38
65	53			PC12	COM6/SEG37
66				PD00	-
67				PD01	-
68	54			PD02	COM7/SEG36
69				PD03	-
70				PD04	-
71	55	39	26	PB03	VC1_INN9 SEG35/VLCDH
72	56	40	27	PB04	VC0_INP12 VC1_INP12 SEG34/VLCD3
73	57	41	28	PB05	VC0_INP13 SEG33/VLCD2
74	58	42	29	PB06	VC0_INP14 VC1_INP14 SEG32/VLCD1
75	59	43	30	PB07	VC1_INP15 LVD2 SEG31
76	60	44	31	BOOT0/PF11	SEG30
77	61	45		PB08	LVD1 SEG29
78	62	46		PB09	SEG28
79	63	47	32	DVSS	-
80	64	48		DVCC	-

The digital function of each pin is controlled by the PSEL bit field, as shown in the table below.

Table 3-2 Port Reuse Table

Px_SEL	1	2	3	4	5	6	7
PA00	UART1_CTS	LPUART1_TXD	TIM0_ETR	VC0_OUT	TIM1_CHA	TIM3_ETR	TIM0_CHA
PA01	UART1_RTS	LPUART1_RXD	TIM0_CHB	TIM1_ETR	TIM1_CHB	HCLK_OUT	SPI1_MOSI
PA02	UART1_TXD	TIM0_CHA	VC1_OUT	TIM1_CHA	TIM2_CHA	PCLK_OUT	SPI1_MISO
PA03	UART1_RXD	TIM0_GATE	TIM1_CHB	TIM2_CHB	SPI1_CS	TIM3_CH1A	TIM5_CHA
PA04	SPI0_CS	UART1_TXD	PCA_CH4	TIM2_ETR	TIM5_CHA	LVD_OUT	TIM3_CH2B
PA05	SPI0_SCK	TIM0_ETR	PCA_ECI	TIM0_CHA	TIM5_CHB	XTL_OUT	XTH_OUT
PA06	SPI0_MISO	PCA_CH0	TIM3_BK	TIM1_CHA	VC0_OUT	TIM3_GATE	LPUART0_CTS
PA07	SPI0_MOSI	PCA_CH1	HCLK_OUT	TIM3_CH0B	TIM2_CHA	VC1_OUT	TIM4_CHB
PA08	UART0_TXD	TIM3_CH0A	CTRIM_ETRTOG	-	TIM1_GATE	TIM4_CHA	TIM3_BK
PA09	UART0_TXD	TIM3_CH1A	TIM0_BK	I2C0_SCL	-	HCLK_OUT	TIM5_CHA
PA10	UART0_RXD	TIM3_CH2A	TIM2_BK	I2C0_SDA	TIM2_GATE	PCLK_OUT	TIM6_CHA
PA11	UART0_CTS	TIM3_GATE	I2C1_SCL	-	VC0_OUT	SPI0_MISO	TIM4_CHB
PA12	UART0_RTS	TIM3_ETR	I2C1_SDA	-	VC1_OUT	SPI0_MOSI	PCNT_S0
PA13	IR_OUT	UART0_RXD	LVD_OUT	TIM3_ETR	RTC_1HZ	PCNT_S1	VC2_OUT
PA14	UART1_TXD	UART0_TXD	TIM3_CH2A	LVD_OUT	RCH_OUT	RCL_OUT	PLL_OUT
PA15	SPI0_CS	UART1_RXD	LPUART1_RTS	TIM0_ETR	TIM0_CHA	TIM3_CH1A	-
PB00	PCA_CH2	TIM3_CH1B	LPUART0_TXD	TIM5_CHB	RCH_OUT	RCL_OUT	PLL_OUT
PB01	PCA_CH3	PCLK_OUT	TIM3_CH2B	TIM6_CHB	LPUART0_RTS	VC2_OUT	TCLK_OUT
PB02	LPTIM0_TOG	PCA_ECI	LPUART1_TXD	TIM4_CHA	TIM1_BK	TIM0_BK	TIM2_BK
PB03	SPI0_SCK	TIM0_CHB	TIM1_GATE	TIM3_CH0A	LPTIM0_GATE	XTL_OUT	XTH_OUT
PB04	SPI0_MISO	PCA_CH0	TIM2_BK	UART0_CTS	TIM2_GATE	TIM3_CH0B	LPTIM0_ETR
PB05	SPI0_MOSI	-	TIM1_BK	PCA_CH1	LPTIM0_GATE	PCNT_S0	UART0_RTS
PB06	I2C0_SCL	UART0_TXD	TIM1_CHB	TIM0_CHA	LPTIM0_ETR	TIM3_CH0A	LPTIM0_TOG
PB07	I2C0_SDA	UART0_RXD	TIM2_CHB	LPUART1_CTS	TIM0_CHB	LPTIM0_TOGN	PCNT_S1
PB08	I2C0_SCL	TIM1_CHA	-	TIM2_CHA	TIM0_GATE	TIM3_CH2A	UART0_TXD
PB09	I2C0_SDA	IR_OUT	SPI1_CS	TIM2_CHA	-	TIM2_CHB	UART0_RXD
PB10	I2C1_SCL	SPI1_SCK	TIM1_CHA	LPUART0_TXD	TIM3_CH1A	LPUART1_RTS	UART1_RTS
PB11	I2C1_SDA	TIM1_CHB	LPUART0_RXD	TIM2_GATE	TIM6_CHA	LPUART1_CTS	UART1_CTS
PB12	SPI1_CS	TIM3_BK	LPUART0_TXD	TIM0_BK	-	LPUART0_RTS	TIM6_CHA

Px_SEL	1	2	3	4	5	6	7
PB13	SPI1_SCK	I2C1_SCL	TIM3_CH0B	LPUART0_CTS	TIM1_CHA	TIM1_GATE	TIM6_CHB
PB14	SPI1_MISO	I2C1_SDA	TIM3_CH1B	TIM0_CHA	RTC_1HZ	LPUART0_RTS	TIM1_BK
PB15	SPI1_MOSI	TIM3_CH2B	TIM0_CHB	TIM0_GATE	-	-	LPUART1_RXD
PC00	LPTIM0_GATE	PCNT_S0	UART1_CTS	UART2_RTS	-	-	-
PC01	LPTIM0_TOG	TIM5_CHB	UART1_RTS	PCNT_S0FO	-	UART2_CTS	-
PC02	SPI1_MISO	LPTIM0_TOGN	PCNT_S1	UART2_RXD	-	-	-
PC03	SPI1_MOSI	LPTIM0_ETR	LPTIM0_TOGN	PCNT_S1FO	UART2_TXD	-	-
PC04	LPUART0_TXD	TIM2_ETR	IR_OUT	VC2_OUT	-	-	-
PC05	LPUART0_RXD	TIM6_CHB	PCA_CH4	-	-	-	-
PC06	PCA_CH0	TIM4_CHA	TIM2_CHA	LPTIM1_GATE	-	UART3_RXD	-
PC07	PCA_CH1	TIM5_CHA	TIM2_CHB	LPTIM1_ETR	-	UART3_TXD	-
PC08	PCA_CH2	TIM6_CHA	TIM2_ETR	LPTIM1_TOG	-	UART3_CTS	-
PC09	PCA_CH3	TIM4_CHB	TIM1_ETR	LPTIM1_TOGN	-	UART3_RTS	-
PC10	LPUART1_TXD	LPUART0_TXD	PCA_CH2	-	-	-	-
PC11	LPUART1_RXD	LPUART0_RXD	PCA_CH3	PCNT_S0FO	-	-	-
PC12	LPUART0_TXD	LPUART1_TXD	PCA_CH4	PCNT_S1FO	-	-	-
PC13	-	RTC_1HZ	TIM3_CH1B	-	-	-	-
PC14	-	-	-	-	-	-	-
PC15	-	-	-	-	-	-	-
PD00	-	SPI1_CS	-	-	-	-	-
PD01	-	SPI1_SCK	-	-	-	-	-
PD02	PCA_ECI	LPUART0_RTS	TIM1_ETR	-	-	-	-
PD03	UART1_CTS	SPI1_MISO	LPTIM1_TOG	-	-	-	-
PD04	UART1_RTS	SPI1_MOSI	LPTIM1_TOGN	-	-	-	-
PD08	LPUART0_TXD	-	-	-	-	-	-
PD09	LPUART0_RXD	-	-	-	-	-	-
PD10	LPUART0_TXD	-	-	-	-	-	-
PD11	LPUART0_CTS	-	-	-	-	-	-
PE02	PCA_ECI	-	-	-	-	-	-
PE03	PCA_CH0	-	-	-	-	-	-
PE04	PCA_CH1	-	-	-	-	-	-

Px_SEL	1	2	3	4	5	6	7
PE05	PCA_CH2	-	-	-	-	-	-
PE11	TIM3_CH1A	-	-	-	-	-	-
PE12	TIM3_CH2B	SPI0_CS	UART3_CTS	-	-	-	-
PE13	TIM3_CH2A	SPI0_SCK	UART3_RTS	-	-	-	-
PE14	TIM3_CH0B	SPI0_MISO	UART3_RXD	-	-	-	-
PF00	I2C0_SDA	CTRIM_ETRTOG	UART1_TXD	-	-	-	-
PF01	I2C0_SCL	TIM4_CHB	UART1_RXD	-	-	-	-
PF04	-	-	-	-	-	-	-
PF05	-	-	-	-	-	-	-
PF06	I2C1_SCL	LPUART1_CTS	UART0_CTS	-	-	-	-
PF07	I2C1_SDA	LPUART1_RTS	UART0_RTS	-	-	-	-
PF11							

3.3 Module Signal Description

Table 3-3 Module signal description

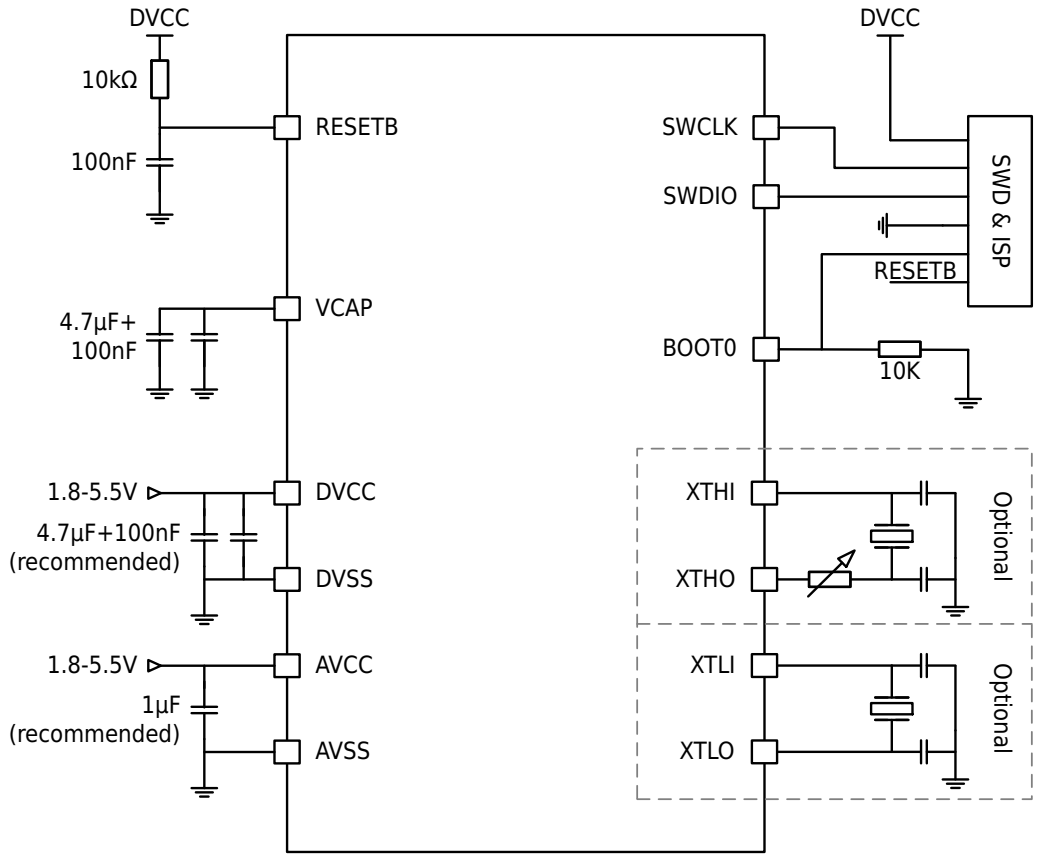
Modules	Pin name	Description
Power supply	DVCC	Digital power supply
	AVCC	Analog power
	DVSS	Digitally
	AVSS	Analog ground
	VCAP	LDO core power supply output (only for internal circuit use, external voltage stabilizing capacitor required)
ISP	BOOT0	When reset, BOOT0 (PF11) pin is high level, the chip works in ISP programming mode, and Flash can be programmed through ISP protocol. When reset, BOOT0 (PF11) pin is low level, the chip works in user mode, the chip executes the program code in the Flash, and the Flash can be programmed through the SWD protocol.
ADC	AINx (x=0~22, 24~25)	ADC input channel
	EXVREF	ADC external reference voltage
VC	VCINx (x=0~15)	VC input 0-15
	VCx_OUT (x=0~2)	VC0 ~ 2 comparison output
LVD	LVDINx (x=0~2)	Voltage detection input 0~ 2
	LVD_OUT	Voltage detection output
OPA	OPA_INN	OPA negative input
	OPA_INP	OPA positive input
	OPA_OUTx (x=0~4)	OPA output
LCD	COMx (x=0~7)	LCD common output
	SEGy (y=0~39, 44~47, 49~51)	LCD segment output
	VLCDx (x=1~3, H)	External resistance mode, external capacitor mode uses pins
UART	UARTx_TXD (x=0~3)	UART data transmitter
	UARTx_RXD (x=0~3)	UART data receiver
	UARTx_CTS (x=0~3)	UART send Hardware flow control
	UARTx_RTS (x=0~3)	UART Receive Hardware flow control
LPUART	LPUARTx_TXD (x=0~1)	LPUART data transmitter
	LPUARTx_RXD (x=0~1)	LPUART data receiver
	LPUARTx_CTS (x=0~1)	LPUART send Hardware flow control
	LPUARTx_RTS (x=0~1)	LPUART Receive Hardware flow control

Modules	Pin name	Description
SPI	SPIx_MISO (x=0~1)	SPI module host input and slave output data signal
	SPIx_MOSI (x=0~1)	SPI module master output slave input data signal
	SPIx_SCK (x=0~1)	SPI module clock signal
	SPIx_CS (x=0~1)	SPI chip select
I2C	I2Cx_SDA (x=0~1)	I2C module data signal
	I2Cx_SCL (x=0~1)	I2C module clock signal
General Timer TIM0~2	TIMx_CHA (x=0~2)	Timer capture input compare output A
	TIMx_CHB (x=0~2)	Timer's capture input compare output B
	TIMx_ETR (x=0~2)	Timer's external count input signal
	TIMx_GATE (x=0~2)	Timer gate signal
General Timer (TIM3)	TIM3_CHyA (y=0~2)	Timer capture input compare output A
	TIM3_CHyB (y=0~2)	Timer's capture input compare output B
	TIM3_ETR	Timer's external count input signal
	TIM3_GATE	Timer gate signal
Low Power Timer LPTIM	LPTIMx_TOG (x=0~1)	LPTimer's flipped output signal
	LPTIMx_TOGN (x=0~1)	LPTimer's flip output reverse signal
	LPTIMx_ETR (x=0~1)	LPTimer's external count input signal
	LPTIMx_GATE (x=0~1)	Gating signal of LPTimer
Programmable counting array PCA	PCA_ECI	External clock input signal
	PCA_CHx (x=0~4)	Capture input/comparison output/PWM output 0~4
PCNT	PCNT_Sx (x=0~1)	PCNT pulse count input 0~1
	PCNT_SxFO (x=0~1)	S0~1 pulse signal after shaping can be used for debugging and observation
Advanced Timer	TIMx_CHA (x=4~6)	Advanced Timer4~6 compare output/capture input A
	TIMx_CHB (x=4~6)	Advanced Timer4~6 compare output/capture input B

Note

The IO port is reset to the input high impedance state, and the sleep mode and deep sleep mode maintain the previous port state.

4 Typical Application Circuit Diagram



Note

- AVCC and DVCC voltage must be the same.
- Each power supply needs a decoupling capacitor, which should be as close as possible to the corresponding power supply pin.

5 Electrical Specifications

5.1 Testing Conditions

Unless otherwise specified, all voltages are based on VSS.

5.1.1 Minimum and Maximum Values

Unless otherwise specified, all minimum and maximum values will be in the worst environment through the test.

The notes at the bottom of each table indicate data obtained through comprehensive evaluation, design simulation and/or process characteristics, and will not be tested on the production line.

5.1.2 Typical Value

Unless otherwise specified, typical data is based on T_A=25℃ and VCC=3.3V. These data are only used for design guidance and not tested.

5.2 Absolute Maximum Ratings

If the load on the device exceeds the value given in the "Absolute Maximum Ratings" list, it may cause permanent damage to the device. This only gives the maximum load that can be withstood, and does not mean that the functional operation of the device under this condition is correct. Long-term operation of the device under the maximum condition will affect the reliability of the device.

Table 5-1 Voltage characteristics

Symbol	Description	Min	Max	Unit
VCC-VSS	External main supply voltage (includes AVCC and DVCC)(1)	-0.3	6.0	V
V_{IN}	Input voltage on other pins(2)(3)	VSS-0.3	VCC+0.3	V
|ΔVCCx|	Voltage difference between different power supply pins	-	50	mV
|VSSx-VSS|	Voltage difference between different ground pins	-	50	mV

Note

1. All power (DVCC, AVCC) and ground (DVSS, AVSS) pins must always be connected to the external power supply system within the allowable range.
2. $I_{INJ\ (PIN)}$ must not exceed its limit, which means that V_{IN} does not exceed its maximum value. If it cannot be guaranteed that V_{IN} does not exceed its maximum value, it is also necessary to ensure that the external limit $I_{INJ(PIN)}$ does not exceed its maximum value. When V_{IN}>VCC, there is a forward injection current; when V_{IN}<VSS, there is a reverse injection current.
3. The I/O input voltage with ADC analog input channel must be between VSS and VCC, otherwise it will affect the ADC conversion accuracy.

Table 5-2 Current Characteristics

Symbol	Description	Max(1)	Unit
I_{VCC}	The total current (supply current) through the DVCC/AVCC power cord(1)	100	mA
I_{VSS}	The total current through the VSS ground wire (outflow current)(1)	100	mA
I_{IO}	Output sink current on any I/O and control pin	25	mA
	Output current on any I/O and control pin	-25	mA
$I_{INJ(PIN)}$(2)(3)	Injection current of RESETB pin	±5	mA
	Injection current of XTHI pin of XTH and XTLI pin of XTL	±5	mA
	Injection current of other pins(4)	±5	mA
$\sum I_{INJ(PIN)}$(2)	Total injection current on all I/O and control pins(4)	±25	mA

Note

1. All power (DVCC, AVCC) and ground (DVSS, AVSS) pins must always be connected to the external power supply system within the allowable range.
2. $I_{INJ\ (PIN)}$ must not exceed its limit, which means that V_{IN} does not exceed its maximum value. If it cannot be guaranteed that V_{IN} does not exceed its maximum value, it is also necessary to ensure that the external limit $I_{INJ(PIN)}$ does not exceed its maximum value. When V_{IN}>VCC, there is a forward injection current; when V_{IN}<VSS, there is a reverse injection current.
3. The reverse injection current will interfere with the analog performance of the device.
4. When several I/O ports have injection current at the same time, the maximum value of $\sum I_{INJ(PIN)}$ is the sum of the instantaneous absolute value of the forward injection current and the reverse injection current. This result is based on the characteristics of the maximum $\Sigma I_{INJ(PIN)}$ on the 4 I/O ports of the device.

Table 5-3 temperature characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-65~+150	℃
T_J	Maximum junction temperature	105	°C

5.3 Operating Conditions

5.3.1 General Operating Conditions

Table 5-4 General Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK0}	Internal APB0 clock frequency	-	0	48	MHz

Symbol	Parameter	Conditions	Min	Max	Unit
f_{PCLK1}	Internal APB1 clock frequency	-	0	48	MHz
DVCC	Working voltage of digital part	-	1.8	5.5	V
AVCC(1)	Analog part working voltage	Must be the same as DVCC(2)	1.8	5.5	V
T_A	Ambient temperature(3)	Maximum power consumption	-40	85	°C
		Low power consumption(4)	-40	105	°C
T_J	Junction temperature range	-	-40	105	°C

Note

1. When using an ADC, see ADC Electrical Specifications.
2. It is recommended to use the same power supply for DVCC and AVCC, allowing a maximum of 300mV difference between DVCC and AVCC during power-up and normal operation.
3. T_A(max) is applicable to P_D(max). When P_D<P_D(max), the ambient temperature T_A is allowed to be higher than T_A(max) as long as the junction temperature T_J does not exceed T_J(max). For more description, see Packaging Thermal Resistance Coefficient.
4. In a state of lower power dissipation, as long as T_J does not exceed T_{Jmax} , T_A can be extended to this range.

5.3.2 VCAP External Capacitor

The stability of the main regulator is achieved by connecting an external capacitor, C_{EXT}, to the VCAP pin. The specified values of C_{EXT} are detailed in the following table.

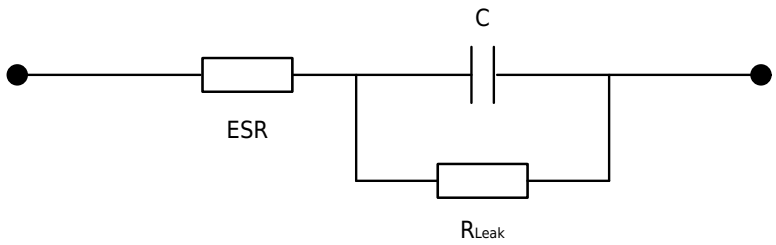


Figure 5-1 External capacitor C_{EXT}

Note

ESR is the equivalent series resistance.

Table 5-5 VCAP Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
C_{EXT}(1)	external capacitor value	-	2.2	10	μF
ESR	ESR of External Capacitance	-	-	100	mΩ

Note

1. The data is based on the assessment results and is not tested in production.

5.3.3 Working Conditions at Power-up and Power-down

Table 5-6 Working conditions at power-up and power-down(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{Vcc_r}	VCC rising rate	-	0	5	V/μs
t_{Vcc_f}	VCC falling rate	-	0	5	V/μs

Note

1. The data is based on the assessment results and is not tested in production.

5.3.4 Embedded Reset and LVD Module Features

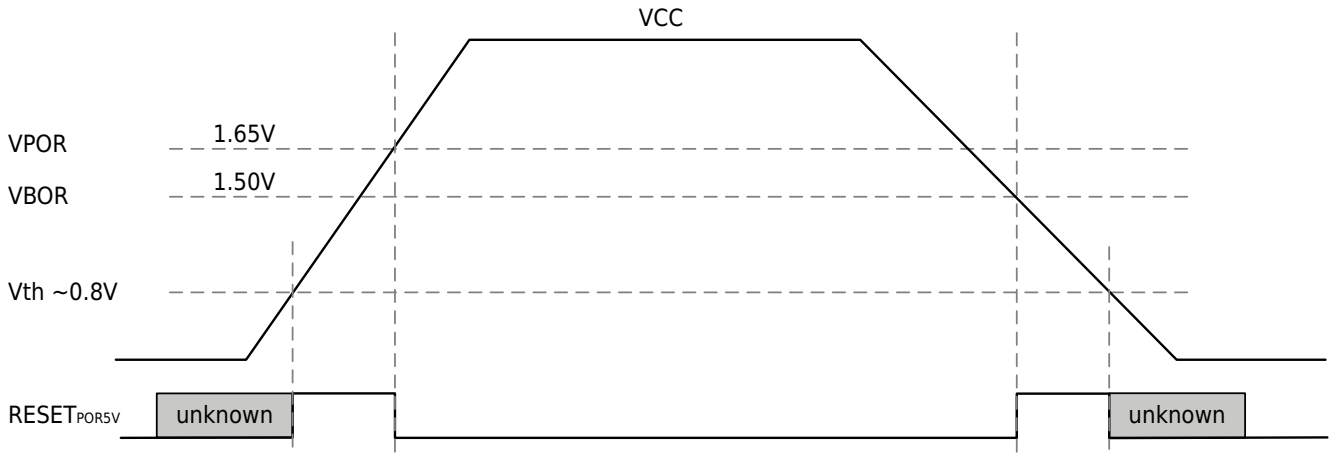


Figure 5-2 POR/Brown Out Diagram

Table 5-7 POR/Brown Out(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VPOR	POR release voltage (power-on process)	-	1.49	1.65	1.75	V
VBOR	BOR detection voltage (power-down process)	-	1.45	1.50	1.55	V

Note

1. Resulted from comprehensive evaluation, not tested in production.

Table 5-8 LVD module characteristics

Symbol	Parame-ter	Conditions	Min	Typ	Max	Unit
V_{ex}	External input voltage range	-	0	-	VCC	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{level}	Detection threshold	LVD_CR.VTDS=0b0000	1.70	1.80	1.90	V
		LVD_CR.VTDS=0b0001(1)	1.80	1.90	2.00	
		LVD_CR.VTDS=0b0010(1)	1.90	2.00	2.10	
		LVD_CR.VTDS=0b0011(1)	2.00	2.10	2.20	
		LVD_CR.VTDS=0b0100(1)	2.10	2.20	2.30	
		LVD_CR.VTDS=0b0101(1)	2.20	2.30	2.40	
		LVD_CR.VTDS=0b0110(1)	2.30	2.40	2.55	
		LVD_CR.VTDS=0b0111(1)	2.35	2.50	2.65	
		LVD_CR.VTDS=0b1000	2.45	2.60	2.75	
		LVD_CR.VTDS=0b1001(1)	2.55	2.70	2.85	
		LVD_CR.VTDS=0b1010(1)	2.65	2.80	2.95	
		LVD_CR.VTDS=0b1011(1)	2.75	2.90	3.05	
		LVD_CR.VTDS=0b1100(1)	2.85	3.00	3.15	
		LVD_CR.VTDS=0b1101(1)	2.95	3.10	3.25	
		LVD_CR.VTDS=0b1110(1)	3.05	3.20	3.35	
		LVD_CR.VTDS=0b1111	3.15	3.30	3.45	
I_{comp}	Power consumption	-	-	0.12	-	μA
$T_{response}$	Response time	Choose to detect the GPIO pin voltage, VCC=3.3V, LVD_CR.VTDS= 0b1000, the detection voltage changes from (V_{level}+100mV) to (V_{level}-100mV), the change slope is $2 \times 10^5 V/\mu s$	-	90	-	μs
T_{setup}	Establishment time	Choose to detect the GPIO pin voltage, VCC=3.3V, LVD_CR.VTDS=0b1000, the detection voltage is 100mV lower than V_{level}	-	400	-	μs
V_{hys}	Hysteresis voltage	-	-	40	-	mV
T_{filter}	Filter time	LVD_debounce=0b000	-	7	-	μs
		LVD_debounce=0b001	-	14	-	
		LVD_debounce=0b010	-	28	-	

Symbol	Parame-ter	Conditions	Min	Typ	Max	Unit
T_{filter}	Filter time	LVD_debounce=0b011	-	112	-	µs
		LVD_debounce=0b100	-	450	-	
		LVD_debounce=0b101	-	1800	-	
		LVD_debounce=0b110	-	7200	-	
		LVD_debounce=0b111	-	28800	-	

Note

1. The data is based on the assessment results and is not tested in production.

5.3.5 Built-in Reference Voltage

Table 5-9 Built-in reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REF25}^{(2)}$	Internal 2.5V Ref-erence Voltage	Room tempera-ture 25°C 3.3V	2.475	2.5	2.525	V
$V_{REF25}^{(1)(2)}$	Internal 2.5V Ref-erence Voltage	-40~85°C 2.8~5.5V	2.455	2.5	2.545	V
V_{REF15}	Internal 1.5V Ref-erence Voltage	Room tempera-ture 25°C 3.3V	1.485	1.5	1.515	V
$V_{REF15}^{(1)}$	Internal 1.5V Ref-erence Voltage	-40~85°C 1.8~5.5V	1.473	1.5	1.527	V
$T_{Coeff}^{(3)}$	Internal 2.5V 1.5V temperature coefficient	-40~85°C	-	-	120	ppm/°C
$T_{stable(BGR)}$	BGR stable time	Room tempera-ture 25°C 3.3V	-	20	-	µs

Note

1. The data is based on the assessment results and is not tested in production.
2. The 2.5V gear can only be selected when the power supply voltage exceeds 2.8V, otherwise it may cause the system to malfunction.
3. Guaranteed by design, not tested in production.

5.3.6 Supply Current Characteristics

Current consumption is a comprehensive index of multiple parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, product software configura-tion, operating frequency, I/O pin flip rate, and program in memory The location in and executed code, etc.

The microcontroller is in the following conditions:

- All I/O pins are in input mode and connected to a static level-VCC or VSS (no load).
- All peripherals are turned off, unless otherwise specified.

- The access time of the flash memory is adjusted to the frequency of f_{HCLK} (0 wait cycle for 0~24MHz, 1 wait cycle for 24~48MHz).
- When the peripheral is turned on: $f_{PCLK0} = f_{HCLK}$, $f_{PCLK1} = f_{HCLK}$.

Table 5-10 Operating Current Characteristics

Symbol	Parameter	Conditions			Typ(1)(3)	Max(2)(3)	Unit
I_{DD} (Run in RAM)	All peripherals clock ON, Run while(1) in RAM	V_{CAP}=1.5V V_{CC}=3.3V T_A=2xC	RCH clock source	4M	701.6	-	µA
				8M	1264	-	
				16M	2352.1	-	
				22.12M	3215.6	-	
				24M Flash Wait=0	3465.3	-	
			RC48M clock source	4M	707.6	-	
				6M	976.5	-	
				32M Flash Wait=1	6687.4	-	
				48M Flash Wait=1	6715.6	-	
			PLL RCH4M to xxM clock source	32M Flash Wait=1	4915.8	-	
				48M Flash Wait=1	7272.8	-	
	All peripherals clock OFF, Run while(1) in RAM	V_{CAP}=1.5V V_{CC}=3.3V T_A=2xC	RCH clock source	4M	402.2	-	µA
				8M	665	-	
				16M	1159.6	-	
				22.12M	1552.2	-	
				24M Flash Wait=0	1664.8	-	
			RC48M clock source	4M	406.4	-	
				6M	527.2	-	
				32M Flash Wait=1	3118.1	-	
				48M Flash Wait=1	3130.8	-	
			PLL RCH4M to xxM clock source	32M Flash Wait=1	2531.5	-	
				48M Flash Wait=1	3701.8	-	
IDD (Run CoreMark)	All peripherals clock OFF, Run CoreMark in Flash	V_{CAP}=1.5V V_{CC}=3.3V T_A=2xC	RCH clock source	4M	846	-	µA
				8M	1369	-	
				16M	1732	-	
				22.12M	2248	-	
				24M Flash Wait=0	2409	-	
			RC48M clock source	4M	847	-	
				6M	1157	-	
				32M Flash Wait=1	2479	-	
				48M Flash Wait=1	3558	-	

Symbol	Parameter	Conditions			Typ(1)(3)	Max(2)(3)	Unit
			PLL RCH4M to xxM clock source	16M	2016	-	
				24M Flash Wait=0	2767	-	
				32M Flash Wait=1	2772	-	
				48M Flash Wait=1	3958	-	
I_{DD} (Sleep mode)	All peripherals clock ON	V_{CAP}=1.5V V_{CC}=1.8~5.5V T_A=-40-85℃	RCH clock source	4M	508.4	646	μA
				8M	901.5	1127	
				16M	1652.4	2045	
				22.12M	2250.7	2779	
				24M Flash Wait=0	2422.3	2990	
			RC48M clock source	4M	513.4	641	
				6M	698.8	867	
				32M Flash Wait=1	4623.9	5757	
				48M Flash Wait=1	4643.1	5787	
			PLL RCH4M to xxM clock source	32M Flash Wait=1	3539.3	4362	
				48M Flash Wait=1	5194.7	6412	
	All peripherals clock OFF	V_{CAP}=1.5V V_{CC}=1.8~5.5V T_A=-40-85℃	RCH clock source	4M	208.1	285	μA
				8M	300.7	399	
				16M	456.3	588	
				22.12M	589.1	754	
				24M Flash Wait=0	622.4	795	
			RC48M clock source	4M	210.5	284	
				6M	247.1	327	
				32M Flash Wait=1	1055.3	1302	
				48M Flash Wait=1	1059	1301	
			PLL RCH12M to xxM clock source	32M Flash Wait=1	1155	1444	
				48M Flash Wait=1	1634.2	2039	
I_{DD} (Run mode)	All peripherals clock ON, Run while(1) in Flash	V_{CAP}=1.5V V_{CC}=1.8~5.5V T_A=-40-85℃	RCH clock source	4M	940	1215	μA
				8M	1748.1	2240	
				16M	2314.9	2870	
				22.12M	3126.3	3869	
				24M Flash Wait=0	3360.5	4155	
			RC48M clock source	4M	947.6	1204	
				6M	1336.4	1698	
				32M Flash Wait=1	5997	7409	
				48M Flash Wait=1	6022.2	7450	

Symbol	Parameter	Conditions			Typ(1)(3)	Max(2)(3)	Unit
I_{DD} (Run mode)			PLL RCH4M to xxM clock source	32M Flash Wait=1	4496.4	5513	
				48M Flash Wait=1	6571.9	8057	
	All peripherals clock OFF, Run while(1) in Flash	V_{CAP}=1.5V V_{CC}=1.8~5.5V T_A=-40-85℃	RCH clock source	4M	640.1	855	μA
				8M	1148.5	1523	
				16M	1122.4	1442	
				22.12M	1466.6	1874	
				24M Flash Wait=0	1564.5	1995	
			RC48M clock source	4M	645.8	847	
				6M	886.4	1165	
				32M Flash Wait=1	2440	3009	
				48M Flash Wait=1	2450	3060	
			PLL RCH12M to xxM clock source	32M Flash Wait=1	2116.8	2651	
				48M Flash Wait=1	3018.2	3770	
I_{DD} (LP Run)	All peripherals clock ON, Run while(1) in Flash	V_{CAP}=1.5V V_{CC}=1.8~5.5V T_A=-40-85℃	RCL clock source(4)	-	112.2	158	μA
			XTL clock source(4)	Driver=1	111.8	157	
	All peripherals clock OFF, Run while(1) in Flash	V_{CAP}=1.5V V_{CC}=1.8~5.5V T_A=-40-85℃	RCL clock source(4)	-	109.4	155	
			XTL clock source(4)	Driver=1	109.4	154	
I_{DD} (LP Sleep)	All peripherals clock ON,	V_{CAP}=1.5V V_{CC}=1.8~5.5V T_A=-40-85℃	RCL clock source(4)	-	84.9	121	μA
			XTL clock source(4)	Driver=1	84.9	120	
	All peripherals clock OFF,	V_{CAP}=1.5V V_{CC}=1.8~5.5V T_A=-40-85℃	RCL clock source(4)	-	82	117	
			XTL clock source(4)	Driver=1	82.4	117	
I_{DD} (Deep-Sleep)	All peripherals clock OFF	V_{CAP}=1.5V V_{CC}=1.8~5.5V T_A=-40-85℃	-	NO CLK	0.8	10.8	μA
	All peripherals clock OFF		-	RCL(4)	1.2	11	
	All peripherals clock OFF		-	XTL(4)	1.5	11.2	
	Other peripherals clock OFF		-	RCL(4)+WDT	1.3	11.1	
	Other peripherals clock OFF		-	RCL(4)+LVD	1.3	11.1	
	Other peripherals clock OFF		-	RCL(4)+RTC	1.3	11.1	
	Other peripherals clock OFF		-	RCL(4)+LPT	1.3	11.1	
	Other peripherals clock OFF		-	RCL(4)+WDT +LVD	1.4	11.2	

Symbol	Parameter	Conditions			Typ(1)(3)	Max(2)(3)	Unit
I_{DD} (Deep-Sleep)	Other peripherals clock OFF	V_{CAP}=1.5V V_{CC}=1.8~5.5V T_A=-40-85℃	-	XTL(4)+WDT	1.5	11.3	μA
	Other peripherals clock OFF		-	XTL(4)+LVD	1.5	11.3	
	Other peripherals clock OFF		-	XTL(4)+RTC	1.5	11.3	
	Other peripherals clock OFF		-	XTL(4)+LPT	1.5	11.3	
	Other peripherals clock OFF		-	XTL(4)+WDT +LVD	1.6	11.4	

Note

1. If there are no other specified conditions, the value of this Typ is measured at 25℃ & V_{CC}=3.3V.
2. If there are no other specified conditions, the value of Max is the maximum value in the range of V_{CC}=1.8-5.5V & Temperature=-40-85℃.
3. The data is based on the assessment results and is not tested in production.
4. The RCL and XTL clock tests use a frequency of 32.768kHz.

5.3.7 Time to Wake-up from Low Power Mode

The wake-up time is measured during the wake-up phase of the RCH oscillator. The clock source used when waking up depends on the current operating mode:

- Sleep mode: clock source is RCH oscillator
- RCH oscillator when entering deep sleep

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{wu}(1)	Sleep mode wake-up time	-	-	1.8	-	μs
	Deep sleep wake-up time	F_{MCLK} = 4MHz	-	13.0	-	μs
		F_{MCLK} = 8MHz	-	10.5	-	μs
		F_{MCLK} = 16MHz	-	9.4	-	μs
		F_{MCLK} = 24MHz	-	10.3	-	μs

Note

1. Guaranteed by design, not tested in production.
2. The wake-up time is measured from the start of the wake-up event to the user program reading the first instruction.

5.3.8 External Timer Characteristics

5.3.8.1 External Input High-speed Clock

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{XTH_ext}	User external clock frequency(1)	-	0	8	32	MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{XTHH}	Input pin high level voltage(1)	-	0.7VCC	-	VCC	V
V_{XTHL}	Input pin low voltage(1)	-	VSS	-	0.3VCC	V
$T_{r(XTH)}$	Rise time(1)	-	-	-	20	ns
$T_{f(XTH)}$	Falling time(1)	-	-	-	20	ns
$T_{w(XTH)}$	Enter high or low time(1)	-	16	-	-	ns
$C_{in(XTH)}$	Input capacitive reactance(1)	-	-	5	-	pF
Duty	Duty Cycle(1)	-	40	-	60	%
I_L	Input leakage current(1)	-	-	-	±1	μA

Note

1. Guaranteed by design, not tested in production.

5.3.8.2 External Input Low-speed Clock

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{XTL_ext}	User external clock frequency(1)	-	0	32.768	1000	kHz
V_{XTLH}	Input pin high level voltage(1)	-	0.7VCC	-	VCC	V
V_{XTLL}	Input pin low voltage(1)	-	VSS	-	0.3VCC	V
$T_{r(XTL)}$	Rise time(1)	-	-	-	50	ns
$T_{f(XTL)}$	Falling time(1)	-	-	-	50	ns
$T_{w(XTL)}$	Enter high or low time(1)	-	450	-	-	ns
$C_{in(XTL)}$	Input capacitive reactance(1)	-	-	5	-	pF
Duty	Duty Cycle(1)	-	30	-	70	%
I_L	Input leakage current(1)	-	-	-	±1	μA

Note

1. Guaranteed by design, not tested in production.

5.3.8.3 High-speed External Clock XTH

The high-speed external clock (XTH) can be generated using a 8~32MHz crystal/ceramic resonator oscillator. The information given in this section is based on the results obtained through comprehensive characteristic evaluation using the typical external components listed in the table below. In the application, the resonator and load capacitor must be as close as possible to the oscillator pin to reduce output distortion and settling time at startup. For detailed parameters (frequency, packaging, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

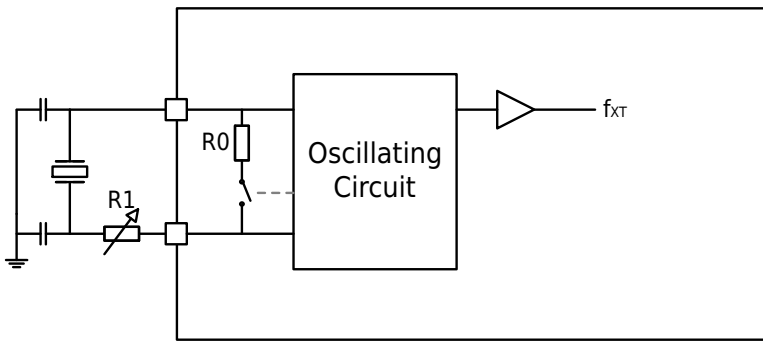
Table 5-14 External XTH crystal oscillator[1][2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CLK}	Oscillation frequency	-	8	-	32	MHz
ESR_{CLK}	Supported crystal oscillator ESR range	32MHz	-	-	60	Ω
		24MHz	-	-	80	
		16MHz	-	-	100	
		8MHz	-	-	120	
C_{LX}[3]	Load capacitance	Configure as required by the crystal manufacturer	4	12	20	pF
Duty	Duty ratio	-	40	50	60	%
I_{dd}[4]	Current	XTH_CR[3:0]=0b1111	-	1000	-	μA
		XTH_CR[3:0]=0b1110	-	600	-	
		XTH_CR[3:0]=0b1010	-	370	-	
		XTH_CR[3:0]=0b0110	-	300	-	
		XTH_CR[3:0]=0b0010	-	160	-	
g_m	transconductance	XTH_CR[3:0]=0b1111	-	11.75	-	mA/V
		XTH_CR[3:0]=0b1110 (32MHz, 24MHz recommended value)	-	6.34	-	
		XTH_CR[3:0]=0b1101	-	4.38	-	
		XTH_CR[3:0]=0b1100	-	3.38	-	
		XTH_CR[3:0]=0b1011	-	7.41	-	
		XTH_CR[3:0]=0b1010 (16MHz recommended value)	-	4.01	-	
		XTH_CR[3:0]=0b1001	-	2.77	-	
		XTH_CR[3:0]=0b1000	-	2.14	-	
		XTH_CR[3:0]=0b0111	-	5.59	-	
		XTH_CR[3:0]=0b0110 (12MHz recommended value)	-	3.01	-	
		XTH_CR[3:0]=0b0101	-	2.08	-	
		XTH_CR[3:0]=0b0100	-	1.60	-	
		XTH_CR[3:0]=0b0011	-	2.50	-	
		XTH_CR[3:0]=0b0010 (8MHz recommended value)	-	1.30	-	
		XTH_CR[3:0]=0b0001	-	0.93	-	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
g_m	transconduc-tance	XTH_CR[3:0]=0b0000	-	0.72	-	mA/V
T_{start} (5)	Start time	32MHz, CL=16pF @XTH_CR[3:0]=0b1110	-	500	-	µs
		8MHz, CL=16pF @XTH_CR[3:0]=0b0010	-	2	-	ms

Note

1. The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.
2. Resulted from comprehensive evaluation, not tested in production.
3. C_{LX} refers to the two pin load capacitors C_{L1} and C_{L2} of XTAL. For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors designed for high-frequency applications, and select a crystal or resonator that meets the requirements. Usually C_{L1} and C_{L2} have the same parameters. Crystal manufacturers usually specify the load capacitance as a serial combination of C_{L1} and C_{L2}. When selecting C_{L1} and C_{L2}, it should be based on parameters such as the frequency of the crystal oscillator and ESR, and the capacitive reactance of the PCB and MCU pins should be taken into consideration.
4. The current varies with the choice of frequency and drive capability. The higher the frequency, the stronger the driving capability and the greater the current consumption.
5. T_{start} is the start-up time, which is the time from the software enabling XTH to start measuring until a stable 32MHz/8MHz oscillation is obtained. This value is measured using a standard crystal resonator with the *XTH_CR[5:4]=0b10 setting.* It may vary greatly depending on the crystal manufacturer and model.



Note

- The matching capacitor of the crystal *configured* in accordance with the requirements of the crystal manufacturer's technical manual.

  If the crystal manufacturer gives the value of the load capacitor, the matching capacitor should be twice the value of the load capacitor given by the crystal manufacturer.

  If the crystal manufacturer gives the capacitance value of the matching capacitor, you can directly use the capacitance value of the matching capacitor given by the crystal manufacturer.
- The feedback resistor R0 has been integrated in the chip.
- The damping resistor R1 is optional. Its resistance value depends on the crystal characteristics and is 0Ω by default.

5.3.8.4 Low-speed External Clock XTL

The low-speed external clock (XTL) can be generated using a 32.768kHz crystal/ceramic resonator oscillator. The information given in this section is based on typical external components and the results obtained through comprehensive characteristic evaluation. In the application, the resonator and load capacitor must be as close as possible to the oscillator pin to reduce output distortion and settling time at startup. For detailed parameters (frequency, packaging, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

Table 5-15 External XTL crystal oscillator(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CLK}	Oscillation frequency	-	-	32.768	-	kHz
ESR_{CLK}	Supported crystal oscillator ESR range	-	-	-	60	kΩ
C_{LX}(2)	Load capacitance	Configure as required by the crystal manufacturer.	8	12	20	pF
DC_{ACLK}	Duty ratio	-	30	50	70	%
I_{dd}(3)	Current	XTL_CR[3:0]=0b1111	-	1330	-	nA
		XTL_CR[3:0]=0b1011	-	1230	-	
		XTL_CR[3:0]=0b0111	-	1140	-	
		XTL_CR[3:0]=0b0011	-	1050	-	
		XTL_CR[3:0]=0b1110	-	630	-	
		XTL_CR[3:0]=0b1010 (recommended value)	-	580	-	
		XTL_CR[3:0]=0b0110	-	530	-	
		XTL_CR[3:0]=0b0010	-	490	-	
g_m	transconductance	XTL_CR[3:0]=0b1111	-	14.64	-	μA/V
		XTL_CR[3:0]=0b1011	-	13.17	-	
		XTL_CR[3:0]=0b0111	-	11.67	-	
		XTL_CR[3:0]=0b0011	-	10.15	-	
		XTL_CR[3:0]=0b1110	-	7.37	-	
		XTL_CR[3:0]=0b1010 (recommended value)	-	6.62	-	
		XTL_CR[3:0]=0b0110	-	5.87	-	
		XTL_CR[3:0]=0b0010	-	5.10	-	
T_{start}(4)	Start time	ESR=30kΩ C_L=12pF XTL_CR[3:0]=0b1010	-	2000	-	ms

Note

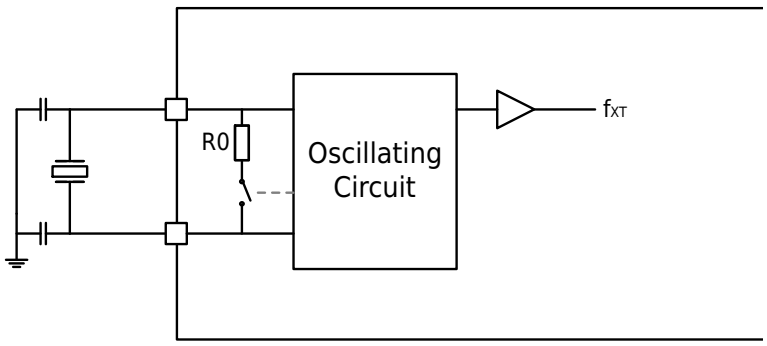
1. Resulted from comprehensive evaluation, not tested in production.
2. C_{LX} refers to the load capacitance of the two pins of XTAL. Users are advised to select the capacitance of this capacitor according to the requirements of the crystal manufacturer.

   If the crystal manufacturer gives the value of the load capacitor, the matching capacitor should be twice the value of the load capacitor given by the crystal manufacturer.

   If the crystal manufacturer gives the capacitance value of the matching capacitor, you can directly use the capacitance value of the matching capacitor given by the crystal manufacturer.

   example:

   - When the crystal manufacturer gives the load capacitance of the crystal as 8pF, the capacitance of the matching capacitor should be 16pF. Considering the distributed capacitance between the PCB and MCU pins, it is recommended to choose a matching capacitor with a capacitance of 15pF or 12pF.
   - The crystal manufacturer gives the matching capacitance of the crystal as 12pF, the matching capacitance should be 12pF. Considering the distributed capacitance between the PCB and MCU pins, it is recommended to choose a matching capacitor with a capacitance of 10pF or 8pF.
3. Choose a high-quality oscillator with a small ESR value (such as MSIV-TIN32.768kHz), and you can optimize the current consumption by adjusting the XTL_CR[3:0] setting value. Current consumption is proportional to the transconductance (g_m) provided by the circuit.
4. T_{start} is the start-up time, which is the time from the software enabling XTL to start measuring until a stable 32768Hz oscillation is obtained. This value is measured using a standard crystal resonator with XTL_CR[3:0]=0b1010 and XTL_CR[5:4]=0b11, and may vary greatly depending on the crystal manufacturer and model.



Note

- The matching capacitor of the crystal *configured* in accordance with the requirements of the crystal manufacturer's technical manual.

  If the crystal manufacturer gives the value of the load capacitor, the matching capacitor should be twice the value of the load capacitor given by the crystal manufacturer.

  If the crystal manufacturer gives the capacitance value of the matching capacitor, you can directly use the capacitance value of the matching capacitor given by the crystal manufacturer.
- The feedback resistor R0 has been integrated in the chip.

5.3.9 Internal Timer Characteristics

5.3.9.1 Internal High-speed Clock RC48M

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dev_{48}	RC48M oscillator accuracy	User trimming step for given VCC and T_A conditions	-	0.2	-	%
		VCC=1.8~5.5V T_{AMB}=-40~85°C F_{CLK48}=4/6MHz	-2.0(1)	-	+2.0(1)	
		VCC=1.8~5.5V T_{AMB}=-20~75°C F_{CLK48}=4/6MHz	-1.5(1)	-	+1.5(1)	
		VCC=1.8~5.5V T_{AMB}=-40~85°C F_{CLK48}=32/48MHz	-1.5(1)	-	+1.5(1)	
		VCC=1.8~5.5V T_{AMB}=-20~75°C F_{CLK48}=32/48MHz	-1.0(1)	-	+1.0(1)	
F_{CLK48}	Oscillation frequency	-	4.0	4.0 6.0 32.0 48.0	48.0	MHz
I_{CLK48}	Power consumption	F_{CLK48}=4MHz	-	54	-	µA
		F_{CLK48}=6MHz	-	60	-	
		F_{CLK48}=32MHz	-	181	-	
		F_{CLK48}=48MHz	-	235	-	
DC_{CLK48}(2)	Duty ratio	-	45	50	55	%
t_{su48}	Start-up time (from enable to start outputting clock)	F_{CLK48}=4MHz	-	18.2	-	µs
		F_{CLK48}=6MHz	-	16.6	-	
		F_{CLK48}=32MHz	-	10.9	-	
		F_{CLK48}=48MHz	-	10.4	-	

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.

5.3.9.2 Internal High-speed Clock RCH

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dev	RCH oscillator accuracy	User trimming step for given VCC and T_A conditions	-	0.25	-	%
		VCC=1.8~5.5V T_{AMB}=-40~85°C	-4.5(1)	-	+3.0(1)	%
F_{CLK}	Oscillation frequency	-	4.0	4.0 8.0 16.0 22.12 24.0	24.0	MHz
I_{CLK}	Power consumption	F_{MCLK}=4MHz	-	80	-	µA
		F_{MCLK}=8MHz	-	100	-	µA
		F_{MCLK}=16MHz	-	120	-	µA
		F_{MCLK}=24MHz	-	140	-	µA
DC_{CLK}(1)	Duty ratio	-	45	50	55	%

Note

1. Resulted from comprehensive evaluation, not tested in production.

5.3.9.3 Internal Low-speed Clock RCL

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dev	RCL oscillator accuracy	User trimming step for given VCC and T_A conditions	-	0.5	-	%
		VCC=1.8~5.5V T_{AMB}=-40~85°C	-5.0(1)	-	+3.0(1)	%
F_{CLK}	Oscillation frequency	VCC=3.3V T_{AMB}=25°C	38.2 32.5	38.4 32.768	38.6 33	kHz
T_{CLK}	Start time	-	-	150	-	µs
DC_{CLK}(1)	Duty ratio	-	25	50	75	%

Note

1. Resulted from comprehensive evaluation, not tested in production.

5.3.9.4 Internal Low-speed Clock RC10K

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V	Operation voltage	-	1.8	-	5.5	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dev(1)	oscillator accuracy	VCC=1.8~5.5V T_{AMB}=-20~50°C	-50	-	50	%
F_{CLK}	Oscillation frequency	VCC=3.3v T_{AMB}=25℃	-	10	-	kHz

Note

1. Resulted from comprehensive evaluation, not tested in production.

5.3.10 PLL Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Fin(1)	Input clock	-	4	4	24	MHz
Duty_in(1)	Input clock duty cycle	-	40	-	60	%
Fout	Output frequency	-	8	-	48	MHz
Duty_out(1)	Output duty cycle	-	48%	-	52%	-
Tlock(1)	Lock time	Input frequency 4MHz	-	100	200	μs
Iconsum	Power consumption	Output frequency 48MHz	-	450	-	μA

Note

1. Resulted from comprehensive evaluation, not tested in production.

5.3.11 Memory Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
EC_{FLASH}	Erase times	Regulator voltage=1.5V, T_{AMB}=25℃	20	-	-	kcycles
RET_{FLASH}	Data retention period	T_{AMB}=85℃, after 20 kcycles	20	-	-	Years
T_{b_prog}	Programming time (bytes)	-	22	-	30	μs
T_{w_prog}	Programming time (words)	-	40	-	52	μs
T_{p_erase}	Page erase time	-	2	-	3	ms
T_{m_erase}	Whole chip erase time	-	30	-	40	ms

5.3.12 ESD Characteristics

Using specific measurement methods, the chip is subjected to strength testing to determine its electrical sensitivity performance.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$VESD_{HBM}$(1)	ESD @ Human Body Mode	Ta=25°C, in compliance with ANSI/ESDA/JEDEC JS-001	-6	-	6	kV
$VESD_{CDM}$(1)	ESD @ Charge Device Mode	Ta=25°C, in compliance with ANSI/ESDA/JEDEC JS-002	-1.5	-	1.5	kV
$I_{latchup}$(1)	Latch up current	Ta=85°C, compliant with JESD78	-200	-	200	mA

Note

1. The data is based on the assessment results and is not tested in production.

5.3.13 I/O Port Characteristics

5.3.13.1 Output Characteristics-Ports

Table 5-23 Port output characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	IO pin outputs high level (low drive)	I_{IO}=3mA, VCC=3.3V	VCC-0.3	-	V
		I_{IO}=6mA, VCC=3.3V	VCC-0.7	-	V
V_{OL}	IO pin outputs low level (low drive)	I_{IO}=4mA, VCC=3.3V	-	VSS+0.3	V
		I_{IO}=8mA, VCC=3.3V	-	VSS+0.7	V
V_{OHD}	IO pin outputs high level (strong drive)	I_{IO}=6mA, VCC=3.3V	VCC-0.3	-	V
		I_{IO}=12mA, VCC=3.3V	VCC-0.7	-	V
V_{OLD}	IO pin outputs low level (strong drive)	I_{IO}=8mA, VCC=3.3V	-	VSS+0.3	V
		I_{IO}=16mA, VCC=3.3V	-	VSS+0.7	V

Note

1. Resulted from comprehensive evaluation, not tested in production.
2. The I_{IO} current of the device must always adhere to the absolute maximum ratings listed in Current Characteristics, and the sum of I_{IO} (I_{OH} and I_{OL} of the I/O port) must not exceed I_{Vcc}.

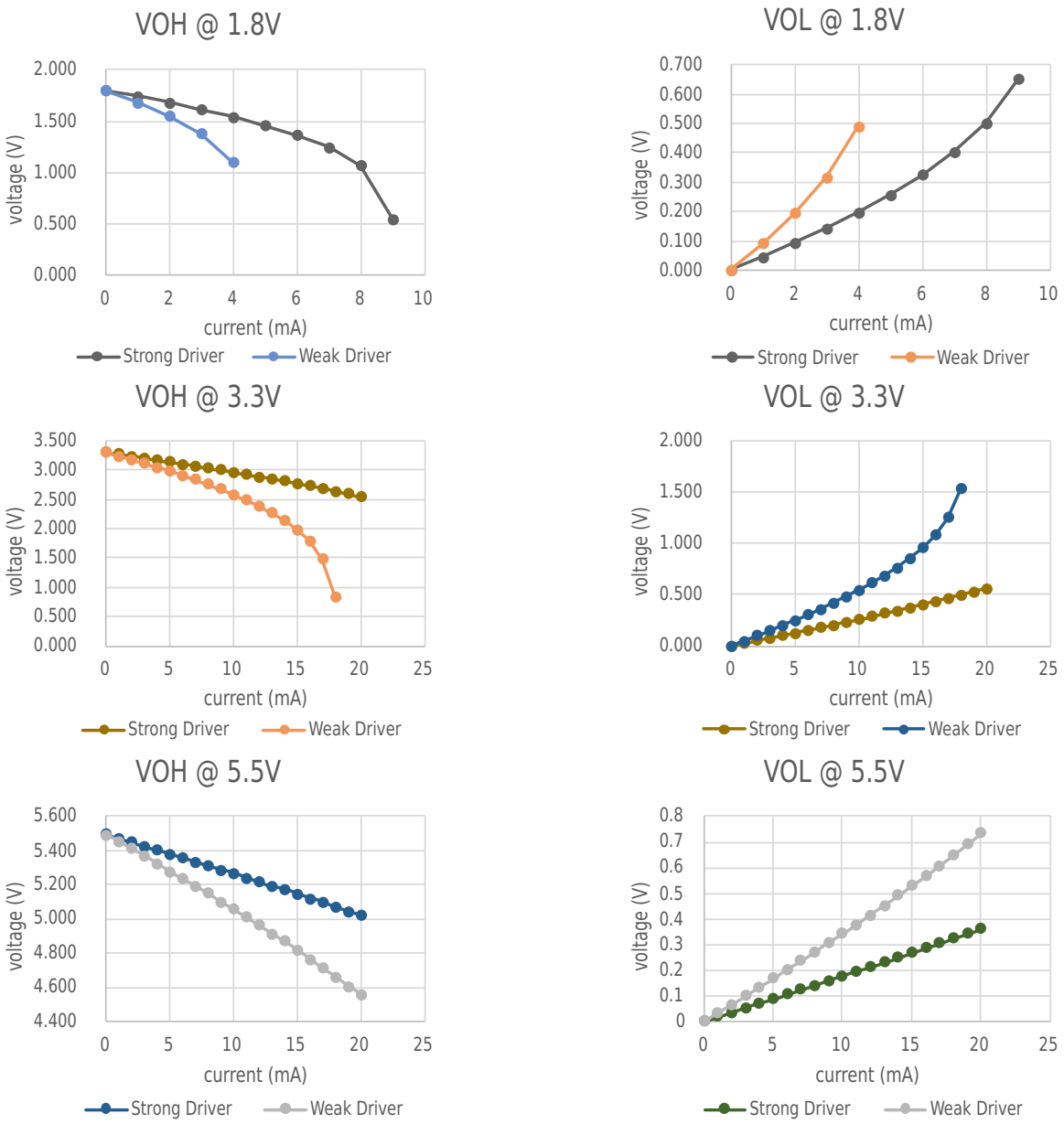


Figure 5-5 Output port VOH/VOL measured curve (typical value)

5.3.13.2 Input Characteristics-Ports PA/PB/PC/PD/PE/PF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}(1)	Positive-going input threshold voltage	VCC=1.8V	0.7VCC	-	-	V
		VCC=3.3V	0.7VCC	-	-	V
		VCC=5.5V	0.7VCC	-	-	V
V_{IL}(1)	Negative-going input threshold voltage	VCC=1.8V	-	-	0.3VCC	V
		VCC=3.3V	-	-	0.3VCC	V
		VCC=5.5V	-	-	0.3VCC	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{hys}	Input voltage hysteresis (V_{IH}-V_{IL})	VCC=1.8V	-	0.3	-	V
		VCC=3.3V	-	0.4	-	V
		VCC=5.5V	-	0.6	-	V
$R_{pullhigh}$	Pullup resistor	Pullup enabled VCC=3.3V	-	80	-	kΩ
$R_{pulllow}$	Pulldown resistor	Pulldown enabled VCC=3.3V	-	40	-	kΩ
C_{input}	Input capacitance	-	-	5	-	pF

Note

1. Resulted from comprehensive evaluation, not tested in production.

5.3.13.3 Port External Input Sampling Requirements-Timer Gate/Timer Clock

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{(cap)}$	Timer capture timing	Timer capture pulse width	-	0.5	-	µs
$t_{(clk)}$ (1)	Timer clock frequency applied to pin	Timer external clock input f_{HCLK}=4MHz	-	-	PCLK/2	MHz
$t_{(pca)}$ (1)	PCA clock frequency applied to pin	PCA external clock input f_{HCLK}=4MHz	-	-	PCLK/8	MHz

Note

1. Resulted from comprehensive evaluation, not tested in production.

5.3.13.4 Port Leakage Characteristics-Ports PA/PB/PC/PD/PE/PF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{lkg(Px.y)}$	Leakage current	$V_{(Px.y)}$ (1)(2)	-	±50	-	nA

Note

1. Port leakage is based on whether the corresponding port is connected to VSS or VCC.
2. The port must be set as an input port.

5.3.14 RESETB Pin Characteristics

The RESETB pin input driver uses CMOS technology, which is connected with a pull-up resistor that cannot be disconnected.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(RESETB)}$ (1)	Input low level voltage	-	-0.3	-	0.3VCC	V
$V_{IH(RESETB)}$ (1)	Input high level voltage	-	0.7VCC	-	VCC+0.3	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{hys(RESETB)}$	Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistance	$V_{IN}=V_{SS}$	-	80	-	kΩ
$V_{F(RESETB)}$(1)	Input filter pulse	-	-	-	2	ns
$V_{NF(RESETB)}$(1)	Input unfiltered pulse	-	10	-	-	ns

Note

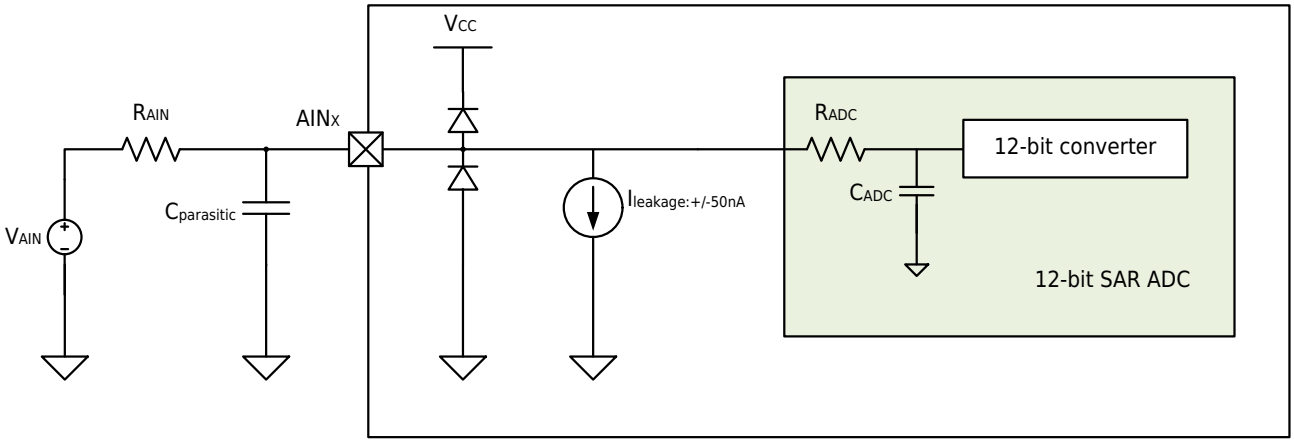
1. Guaranteed by design, not tested in production.

5.3.15 ADC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ADCIN}	Input voltage range	Single ended	0	-	V_{REF+}	V
V_{REF+}(1)	Positive reference voltage	-	1.5	-	AVCC	V
V_{REF-}	Negative reference voltage	-	-	AVSS	-	V
$DEV_{AVCC/3}$	AVCC/3 accuracy		-	±3	-	%
V_{INBUF}(1)	Input voltage range of the input buffer within which the accuracy is guaranteed	(AVCC-0.1V)<V_{REF+}	0.1	-	AVCC-0.1	V
		(AVCC-0.1V)≥V_{REF+}	0.1	-	V_{REF+}	
I_{ADC}(1)	Active current	reference generator on, input buffer on, f_S=200ksps	-	1.77	-	mA
		reference generator on, input buffer on, f_S=1Msps	-	2.10	-	
		reference generator off, input buffer off, f_S=1Msps	-	0.71	-	
C_{ADCIN}(1)	ADC input capacitance		-	16	-	pF
R_{ADC}(1)	ADC sampling switch impedance		-	1.5	-	kΩ
R_{AIN}(1)(3)	ADC external input resistor		-	-	100	kΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADCCLK}(1)	ADC clock Frequency	Range 1: 1.8V≤AVCC≤2.4V	0.2	-	4.8	MHz
		Range 2: 2.4V≤AVCC≤2.7V	0.2	-	12	
		Range 3: AVCC≥2.7V	0.2	-	24 (4)	
f_s(1)	Sampling rate	Range 3, V_{REF+}=AVCC	-	-	1	Msps
		Range 3, V_{REF+}=EXVREF (PB01)	-	-	0.9	
		Range 2, V_{REF+}=AVCC/EXVREF (PB01)	-	-	0.5	
		Range 1, V_{REF+}=AVCC/EXVREF (PB01)/internal 1.5V/ internal 2.5V	-	-	0.2 (5)	
$T_{ADCSTART}$	Startup time of reference generator and ADC core		-	20	-	µs
T_S	Sampling time	-	4	-	12	$1/f_{ADCCLK}$
$T_{ADCCONV}$	Conversion time			T_S+16		cycles
ENOB(1)	Effective Bits	V_{REF+}=AVCC=3.3V, T_A=25℃, f_S=1Msps	9.9	10.7	-	bits
		V_{REF+}=internal 1.5V, AVCC=3.3V, T_A=25℃, f_S=200ksps	9.1	9.8	-	
SNR(1)	Signal to Noise Ratio	V_{REF+}=AVCC=3.3V, T_A=25℃, f_S=1Msps	63.1	67.3	-	dB
		V_{REF+}=internal 1.5V, AVCC=3.3V, T_A=25℃, f_S=200ksps	56.9	60.6	-	
DNL(2)	Differential nonlinearity	V_{REF+}=AVCC=3.3V, T_A=25℃, f_S=500ksps	-1	-0.9/+1.3	+1.8	LSB
INL(2)	Integral non-linearity		-3.3	-2.2/+2.2	+3.3	
E_o(1)	Offset error		-	-1.2/+3.5	-	
E_g(1)	Gain error		-	-2.0/+3.4	-	
E_T(1)	Total unadjusted error		-	±5.4	-	

1. Guaranteed by design, not tested in production.
2. Resulted from comprehensive evaluation, not tested in production.
3. The typical application of ADC is shown in the figure below:



Under the condition of 0.5LSB sampling error accuracy requirement, the calculation formula of external input impedance is as follows:

$$R_{AIN} \leq \frac{T_S}{C_{ADC} *(N+1) * \ln (2)} - R_{ADC} = \frac{M}{f_{ADCCLK} * C_{ADC} *(N+1) * \ln (2)} - R_{ADC}$$

Where $T_s$is the sampling time, N is the number of ADC bits 12, f_{ADCCLK} is the ADC clock frequency, and M is the number of sampling cycles (the sampling time occupies M ADC clock cycles).

Register ADC_CR0[3:2] can set the relationship between f_{ADCCLK} and PCLK frequency f_{PCLK}, as shown in the following table:

Table 5-29 Relationship between ADC clock frequency f_{ADCCLK} and PCLK division ratio

ADC_CR0[3:2]	f_{PCLK}/f_{ADCCLK}
0b00	1
0b01	2
0b10	4
0b11	8

Register ADC_CR0[13:12] can set the number of sampling periods M, as shown in the following table:

Table 5-30 ADC Number of sampling cycles M

ADC_CR0 [13:12]	M
0b00	4
0b01	6
0b10	8
0b11	12

The following table shows the relationship between the ADC minimum sampling time T_S and the external resistor R_{AIN} under typical working conditions (M=12, sampling error 0.5LSB). For other special external input impedance values, the corresponding minimum sampling time requirements can also be calculated through the external input impedance calculation formula given above.

Table 5-31 Relationship between ADC minimum sampling time T_S and external resistor R_{AIN}

R_{AIN}(Ω)	Minimum sampling time T_S(ns)
10	218
47	223

$R_{AIN}(\Omega)$	Minimum sampling time T_S(ns)
68	226
100	231
150	238
220	248
330	264
470	284
680	314
1000	360
1500	433
2200	533
3300	692
4700	894
6800	1197
10000	1658
15000	2379

For the above typical applications, you should pay attention to:

- Try to minimize the parasitic capacitance $C_{parasitic}$ of the ADC input port AIN_x.
- In addition to considering the R_{AIN} value, if the internal resistance of the signal source V_{AIN} is large, it also needs to be considered.

4. For range 3, if V_{REF+}=EXVREF (PB01), the ADC maximum clock frequency needs to be reduced to 20MHz to ensure performance.
5. For range 1, if V_{REF+}=internal 2.5V, the lowest allowed AVCC voltage is 2.8V instead of 1.8V.

5.3.16 Temperature Sensor Characteristics

When the measurement channel of the ADC selects the output voltage of the temperature sensor, the current chip temperature can be calculated through the output result of the ADC and the calibration value stored in the Flash memory.

Table 5-32 Temperature sensor parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Temp Range	The operating junction temperature range of the temperature sensor	-	-40	-	105	°C
△Terror	Temperature error	-	-	±5	-	°C

5.3.17 VC Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{in}	Input voltage range	-		0	-	5.5	V
V_{com}	Input common mode range	-		0.2	-	VCC-0.2	V
V_{offset}	Input offset	0.8V≤V_{com}≤(AVCC-0.8V)	VCx_BIAS_SEL=0b00	-	±20	-	mV
			VCx_BIAS_SEL=0b01	-	±20	-	
			VCx_BIAS_SEL=0b10	-	±10	-	
			VCx_BIAS_SEL=0b11	-	±10	-	
		0.2V≤V_{com}≤0.8V or (AVCC-0.8V)≤V_{com}≤(AVCC-0.2V)	VCx_BIAS_SEL=0b00	-	±33	-	
			VCx_BIAS_SEL=0b01	-	±32	-	
			VCx_BIAS_SEL=0b10	-	±26	-	
			VCx_BIAS_SEL=0b11	-	±25	-	
I_{comp}	Comparator's current	VCx_BIAS_SEL=0b00 VCx_BIAS_SEL=0b01 VCx_BIAS_SEL=0b10 VCx_BIAS_SEL=0b11		-	0.23 0.46 9.1 18.2	-	µA
$T_{response}$	Comparator's response time when one input cross another	VCx_BIAS_SEL=0b00 VCx_BIAS_SEL=0b01 VCx_BIAS_SEL=0b10 VCx_BIAS_SEL=0b11		-	2500 1400 120 80	-	ns
T_{setup}	Comparator's setup time when ENABLE. Input signals unchanged.	-		-	360	-	ns
$V_{hysteresis}$	Comparator's hysteresis voltage	VCx_HYS_SEL=0b00 VCx_HYS_SEL=0b01 VCx_HYS_SEL=0b10 VCx_HYS_SEL=0b11		-	0 10 20 30	-	mV
R_{in}(1)	allowable source resistance of the input signal	VCx_HYS_SEL=0b00 VCx_HYS_SEL=0b01/0b10/0b11		-	-	100k 400	Ω
V_{off_DAC}	Comparator's inner DAC's offset	-		-	±40	-	mV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{warmup}	The waiting time after enabling the BGR	internal 1.5V/2.5V reference voltage	-	40	-	µs
		the temperature sensor is needed or VCx_BIAS_SEL=0b10/0b11	-	20	-	
T_{filter}	Digital filter time	VCx_CR[11:9]=0b000 VCx_CR[11:9]=0b001 VCx_CR[11:9]=0b010 VCx_CR[11:9]=0b011 VCx_CR[11:9]=0b100 VCx_CR[11:9]=0b101 VCx_CR[11:9]=0b110 VCx_CR[11:9]=0b111	-	7 14 28 112 450 1800 7200 28800	-	µs

Note

1. Guaranteed by design, not tested in production.

5.3.18 OPA Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{in}	Input voltage	-	0.2	-	AVCC-0.2	V
V_o(1)	The output voltage	-	0.2	-	AVCC-0.2	V
I_o(1)	Output current	-	-	-	0.3	mA
RL(1)	load resistance	-	5	-	-	kΩ
T_{start}(2)	Initialization time	V_{ip}=AVCC/2+50mV, V_{in}=AVCC/2-50mV I_{load}=300µA, CL=50pF	-	1	-	µs
V_{os}	Input offset voltage	V_{in}=AVCC/2, V_o=AVCC/2 I_{load}=300µA, Rs=50Ω	-	±6	-	mV
GBW	Unity gain bandwidth	V_{in}=AVCC/2, V_o=AVCC/2 I_{load}=300µA, CL=50pF	-	6.5	-	MHz
SR	Slew rate	I_{load}=300µA, CL=50pF	-	6	-	V/µs

Note

1. Guaranteed by design, not tested in production.
2. Need to set BGR_CR[0]= 0b1 at the same time.

5.3.19 LCD Controller Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LCD}(1)	Operating current	VCC=3.3V, internal resistance mode (high power consumption)	-	10	-	μA
		VCC=3.3V, internal resistance mode (medium power consumption)	-	7	-	μA
		VCC=3.3V, internal resistance mode (low power consumption)	-	3.5	-	μA
V_{LCDH}	LCD adjustable maximum voltage	-	-	-	VCC	V
V_{LCD3}	LCD maximum voltage	-	-	-	V_{LCDH}	V
V_{LCD2}	LCD 2/3 voltage	-	-	-	2/3 V_{LCDH}	V
V_{LCD1}	LCD 1/3 voltage	-	-	-	1/3 V_{LCDH}	V
V_{LCD0}	LCD minimum voltage	-	0	-	-	V
$\triangle V_{XX}$	LCD voltage deviation	T_A=-40~85℃	-	±5%	-	-

Note

1. The power consumption data is obtained by testing without an LCD screen, which only includes the power consumption of the LCD driver circuit itself, but does not include the power consumption of GPIO and other parts.

5.3.20 DAC Characteristics

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
V_{REF+}(1)	Positive reference voltage		1.5	-	AVCC	V
V_{REF-}	Negative reference voltage		-	AVSS	-	V
V_{DACOUT}(1)	Output voltage range	DAC buffer off (bypass buffer)	0	-	V_{REF+}	V
		DAC buffer on	0.2	-	V_{REF+}-0.2	

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
I_{DAC}	Active current	V_{REF+}=AVCC/ EXVREF (PB01)	-	9	-	μA
		V_{REF+}=internal 1.5V/2.5V	-	510	-	
R_O	Output resistance	DAC buffer off (bypass buffer)	-	100	-	kΩ
SR_{DAC}(1)	Sample rate	-	-	-	500	ksps
$t_{DACCONV}$(1)	Conversion time, variation of the input code = 1 LSB	settling error≤0.5*LSB, CL≤10pF, DAC buffer off (bypass buffer)	2	-	-	μs
		settling error≤0.5*LSB, CL≤50pF, DAC buffer on	2	-	-	
$t_{DACSETTLE}$	Setting time, transition between the lowest and the highest input codes	settling error≤0.5*LSB, CL≤10pF, DAC buffer off (bypass buffer)	-	9	-	μs
		settling error≤0.5*LSB, CL≤50pF, DAC buffer on	-	3	-	
SNR_{DAC}	Signal to Noise Ratio	DAC buffer on, R_L≥5kΩ	-	62	-	dB
$SNDR_{DAC}$	Signal to Noise and Distortion Ratio		-	59	-	dB
$SFDR_{DAC}$	Spurious Free Dynamic Range		-	67	-	dB
E_o(2)	Offset error at code 0x000	DAC buffer off (bypass buffer) , no R_L, AVCC=3.3V, T_A=25℃	-3.5	-2.5/+0.5	+1.4	LSB
E_g(2)	Gain error at code 0xFFF		-7.0	-3.5/+1.4	+3.1	LSB
DNL_{DAC}(2)	Differential nonlinearity		-1.5	-1.2/+0.7	+1.0	LSB
INL_{DAC}(2)	Integral non-linearity		-2.3	-1.8/+8.4	+10.1	LSB

Note

1. Guaranteed by design, not tested in production.
2. Resulted from comprehensive evaluation, not tested in production.

5.3.21 TIM Timer Characteristics

For details on the characteristics of the input and output multiplex function pins (output compare, input capture, external clock, PWM output), see the table below.

Table 5-37 Advanced Timer (ADVTIM) Features(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{res}	Timer to distinguish time	-	1	-	t_{TIMCLK}
		f_{TIMCLK}=48MHz	20.8	-	ns
f_{ext}	External clock frequency	-	0	$f_{TIMCLK/2}$	MHz
		f_{TIMCLK}=48MHz	0	24	MHz
Res_{Tim}	Timer resolution	-	-	16	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle	-	1	65536	t_{TIMCLK}
		f_{TIMCLK}=48MHz	0.0208	1363	μs

Note

1. Guaranteed by design, not tested in production.

Table 5-38 General timer features(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{res}	Timer to distinguish time	-	1	-	t_{TIMCLK}
		f_{TIMCLK}=48MHz	20.8	-	ns
f_{ext}	External clock frequency	-	0	$f_{TIMCLK/2}$	MHz
		f_{TIMCLK}=48MHz	0	24	MHz
Res_{Tim}	Timer resolution	-	-	16	Bit
		Mode 0 free counting	-	32	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle	-	1	65536	t_{TIMCLK}
		f_{TIMCLK}=48MHz	0.0208	-	μs

Note

1. Guaranteed by design, not tested in production.

Table 5-39 PCA Features(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{res}	Timer to distinguish time	-	1	-	t_{TIMCLK}
		f_{TIMCLK}=48MHz	20.8	-	ns
f_{ext}	External clock frequency	-	0	$f_{TIMCLK/8}$	MHz
		f_{TIMCLK}=48MHz	0	6	MHz
Res_{Tim}	Timer resolution	-	-	16	Bit

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle	-	1	65536	t_{TIMCLK}
		f_{TIMCLK}=48MHz	0.0208	1363	μs

Note

1. Guaranteed by design, not tested in production.

Table 5-40 Low Power Timer Features(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{res}	Timer to distinguish time	-	1	-	t_{TIMCLK}
		f_{TIMCLK}=48MHz	20.8	-	ns
f_{ext}	External clock frequency	-	0	$f_{TIMCLK/2}$	MHz
		f_{TIMCLK}=48MHz	0	24	MHz
Res_{Tim}	Timer resolution	-	-	16	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle	-	1	65536	t_{TIMCLK}
		f_{TIMCLK}=48MHz	0.0208	1363	μs

Note

1. Guaranteed by design, not tested in production.

Table 5-41 WDT Features(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{res}	WDT overflow time	f_{WDTCLK}=10kHz	1.6	52400	ms

Note

1. Guaranteed by design, not tested in production.

5.3.22 Communication Interface

5.3.22.1 I2C Characteristics

I2C interface characteristics are as follows:

Table 5-42 I2C interface characteristics(1)

Symbol	Parameter	Standard mode (100k)		Fast mode (400k)		Fast mode (1M)		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCLL}	SCL clock low time	4.7	-	1.25	-	0.5	-	μs
t_{SCLH}	SCL clock high time	4.0	-	0.6	-	0.26	-	μs
$t_{SU.SDA}$	SDA establishment time	250	-	100	-	50	-	ns

Symbol	Parameter	Standard mode (100k)		Fast mode (400k)		Fast mode (1M)		Unit
		Min	Max	Min	Max	Min	Max	
$t_{HD.SDA}$	SDA hold time	0	-	0	-	0	-	μs
$t_{HD.STA}$	Start condition hold time	2.5	-	0.625	-	0.25	-	μs
$t_{SU.STA}$	Repeated start condition establishment time	2.5	-	0.6	-	0.25	-	μs
$t_{SU.STO}$	Stop condition establishment time	0.25	-	0.25	-	0.25	-	μs
t_{BUF}	Bus idle (stop condition to start condition)	4.7	-	1.3	-	0.5	-	μs

Note

1. Guaranteed by design, not tested in production.

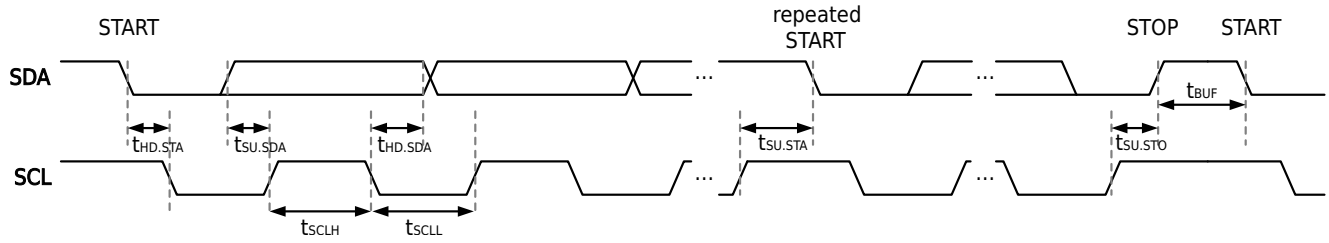


Figure 5-7 I2C Interface Timing

5.3.22.2 SPI Characteristics

Table 5-43 SPI Interface Features(1)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{c(SCK)}$	Serial clock period	Host mode	62.5	-	ns
		Slave mode f_{PCLK}=48MHz	125	-	ns
		Slave mode f_{PCLK}=16MHz	250	-	ns
$t_{w(SCKH)}$	High level time of serial clock	Host mode	0.5*$t_{c(SCK)}$	-	ns
		Slave mode	0.5*$t_{c(SCK)}$	-	ns
$t_{w(SCKL)}$	Low level time of serial clock	Host mode	0.5*$t_{c(SCK)}$	-	ns
		Slave mode	0.5*$t_{c(SCK)}$	-	ns
$t_{su(SSN)}$	Setup time selected by slave	Slave mode	0.5*$t_{c(SCK)}$	-	ns
$t_{h(SSN)}$	Hold time selected by slave	Slave mode	0.5*$t_{c(SCK)}$	-	ns

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(MO)}$	Effective time of host data output	f_{PCLK}=48MHz	-	3	ns
$t_{h(MO)}$	Hold time of host data output	f_{PCLK}=48MHz	2	-	ns
$t_{v(SO)}$	Effective time of slave data output	f_{PCLK}=48MHz	-	50	ns
$t_{h(SO)}$	Hold time of slave data output	f_{PCLK}=48MHz	30	-	ns
$t_{su(MI)}$	Setup time of host data input	-	10	-	ns
$t_{h(MI)}$	Hold time of host data input	-	2	-	ns
$t_{su(SI)}$	Setup time of slave data input	-	10	-	ns
$t_{h(SI)}$	Hold time of slave data input	-	2	-	ns

Note

1. Guaranteed by design, not tested in production.

The waveform and timing parameters of the SPI interface signal are as follows:

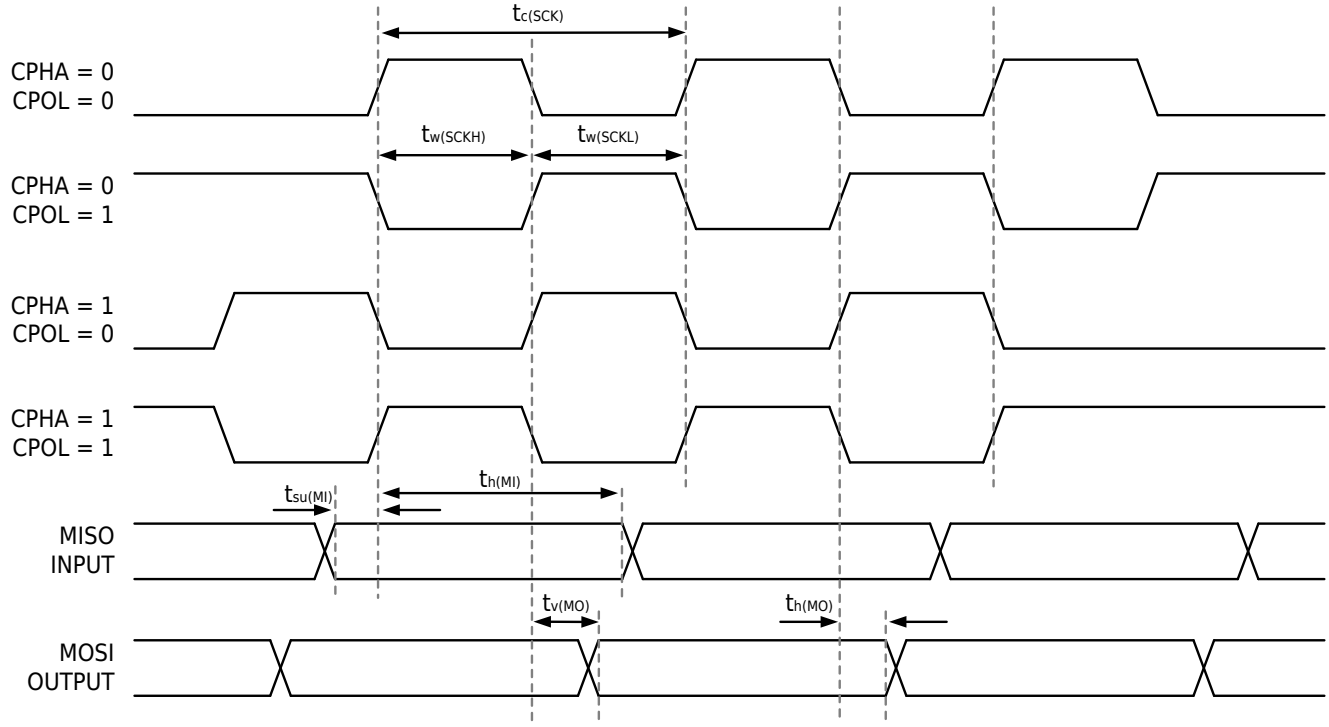


Figure 5-8 SPI Timing Diagram (Master mode)

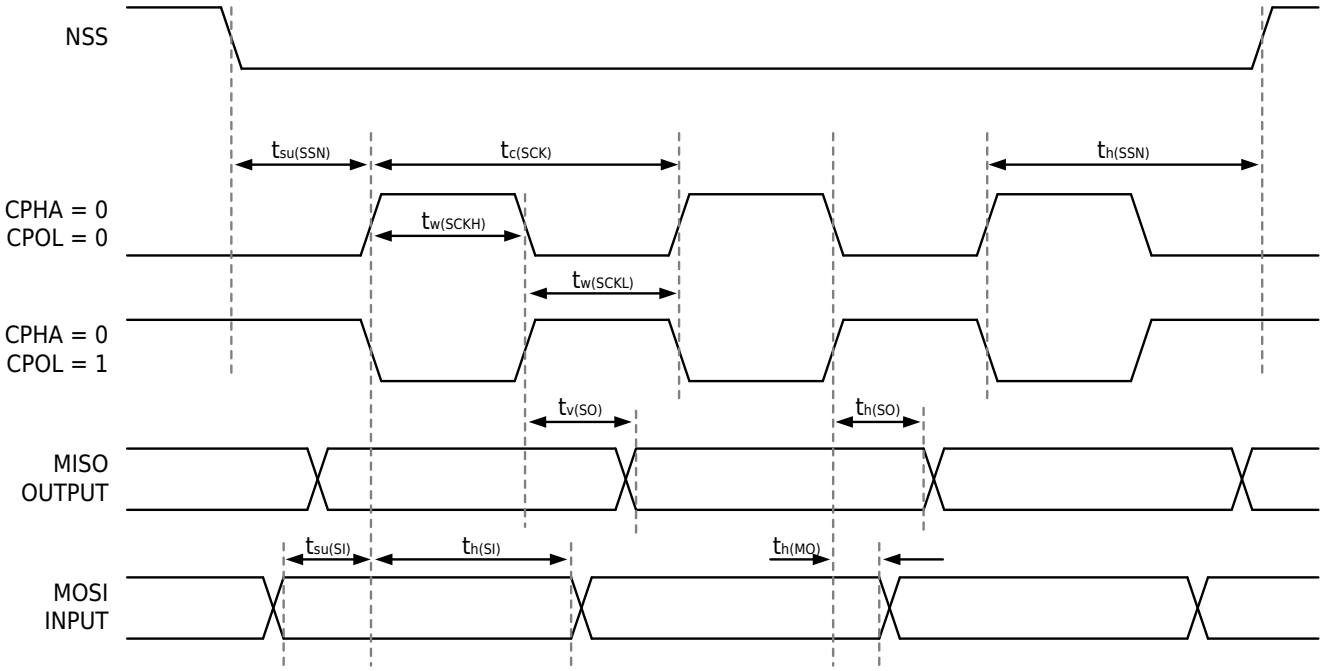


Figure 5-9 SPI timing diagram (slave mode CPHA=0)

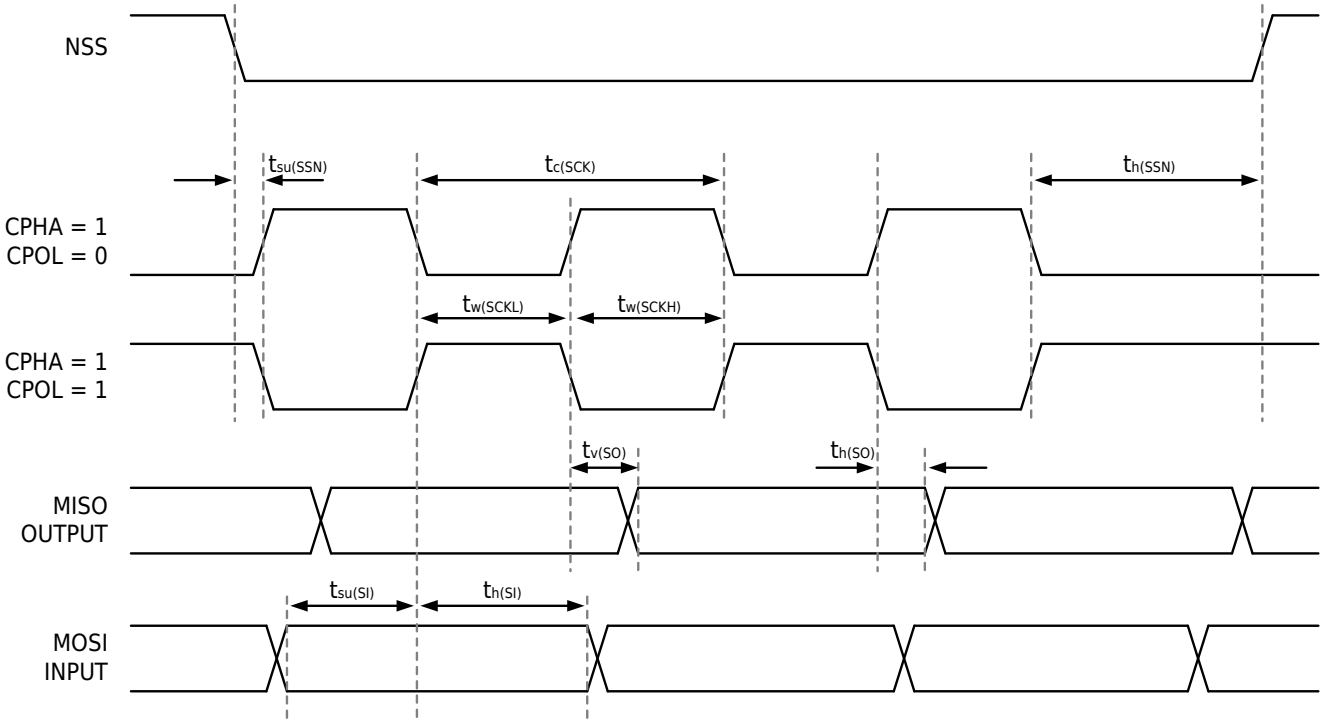
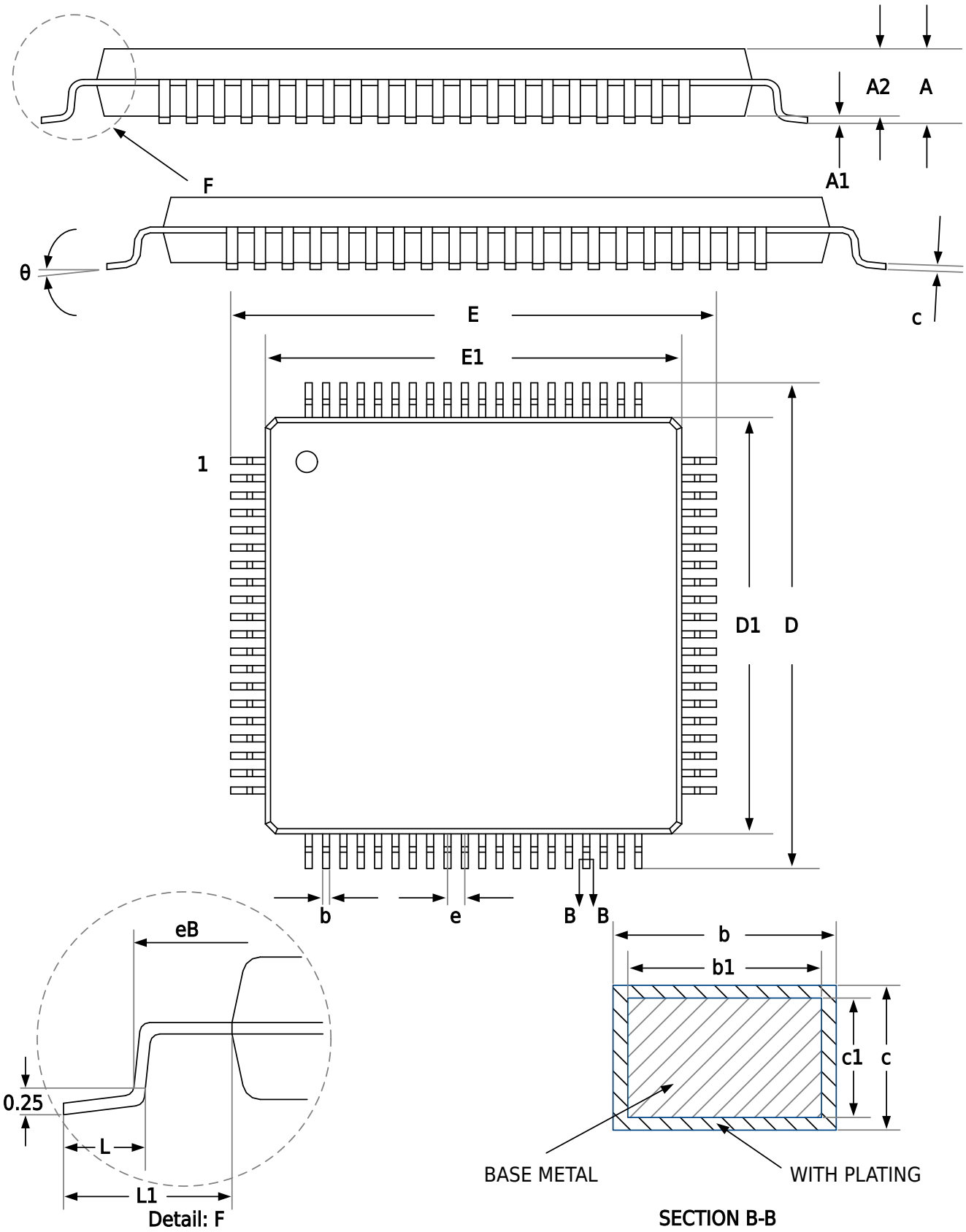


Figure 5-10 SPI timing diagram (slave mode CPHA=1)

6 Package Specifications

6.1 Package Dimensions

6.1.1 LQFP80 Package

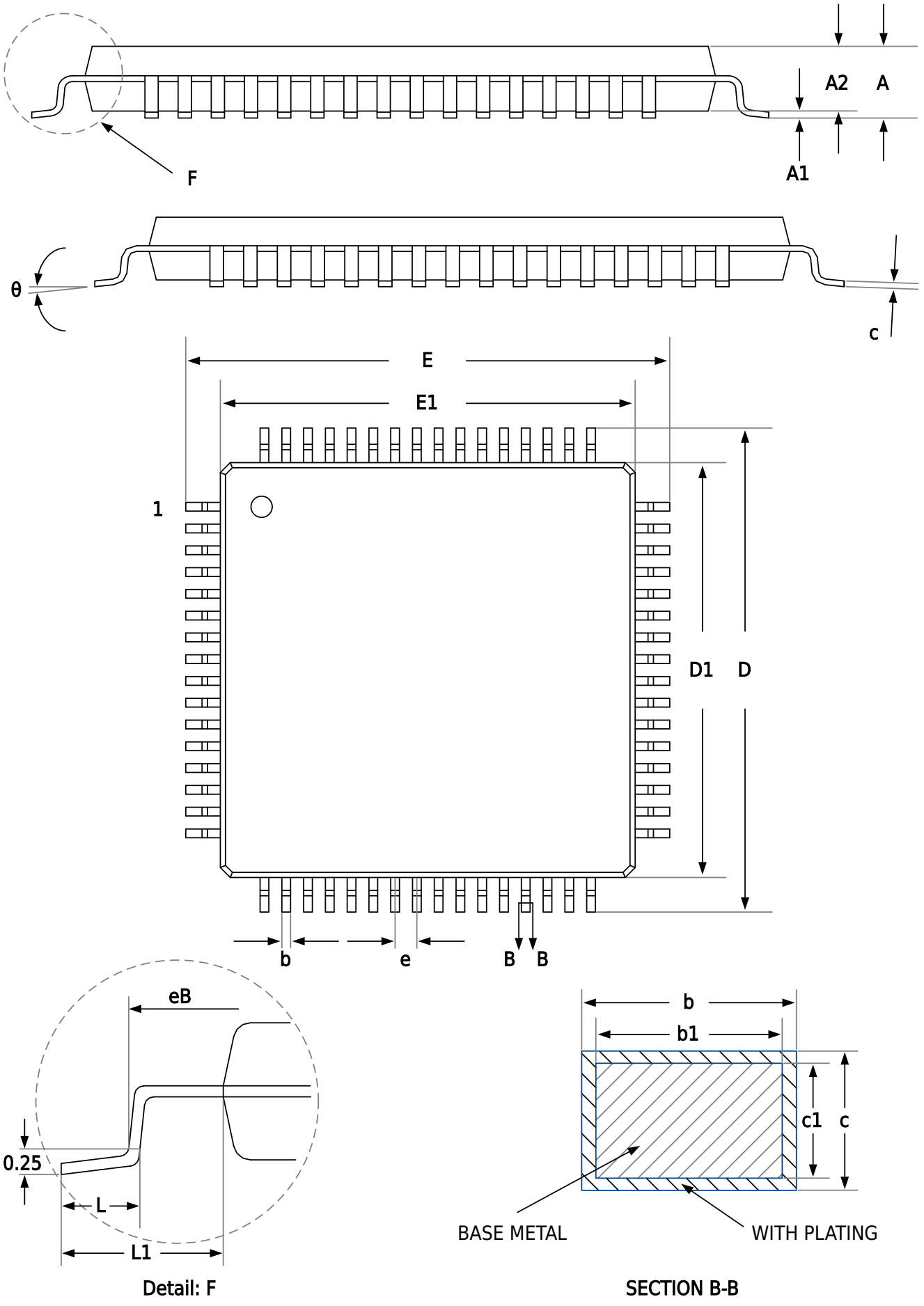


Symbol	12 x 12 Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	-	0.27
b1	0.17	0.20	0.23
c	0.09	-	0.20
c1	0.13BSC		
D	13.80	14.00	14.20
D1	11.90	12.00	12.10
E	13.80	14.00	14.20
E1	11.90	12.00	12.10
eB	13.05	-	13.25
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	-	7°

Note

Dimensions “D1” and “E1” do not include mold flash.

6.1.2 LQFP64 Package

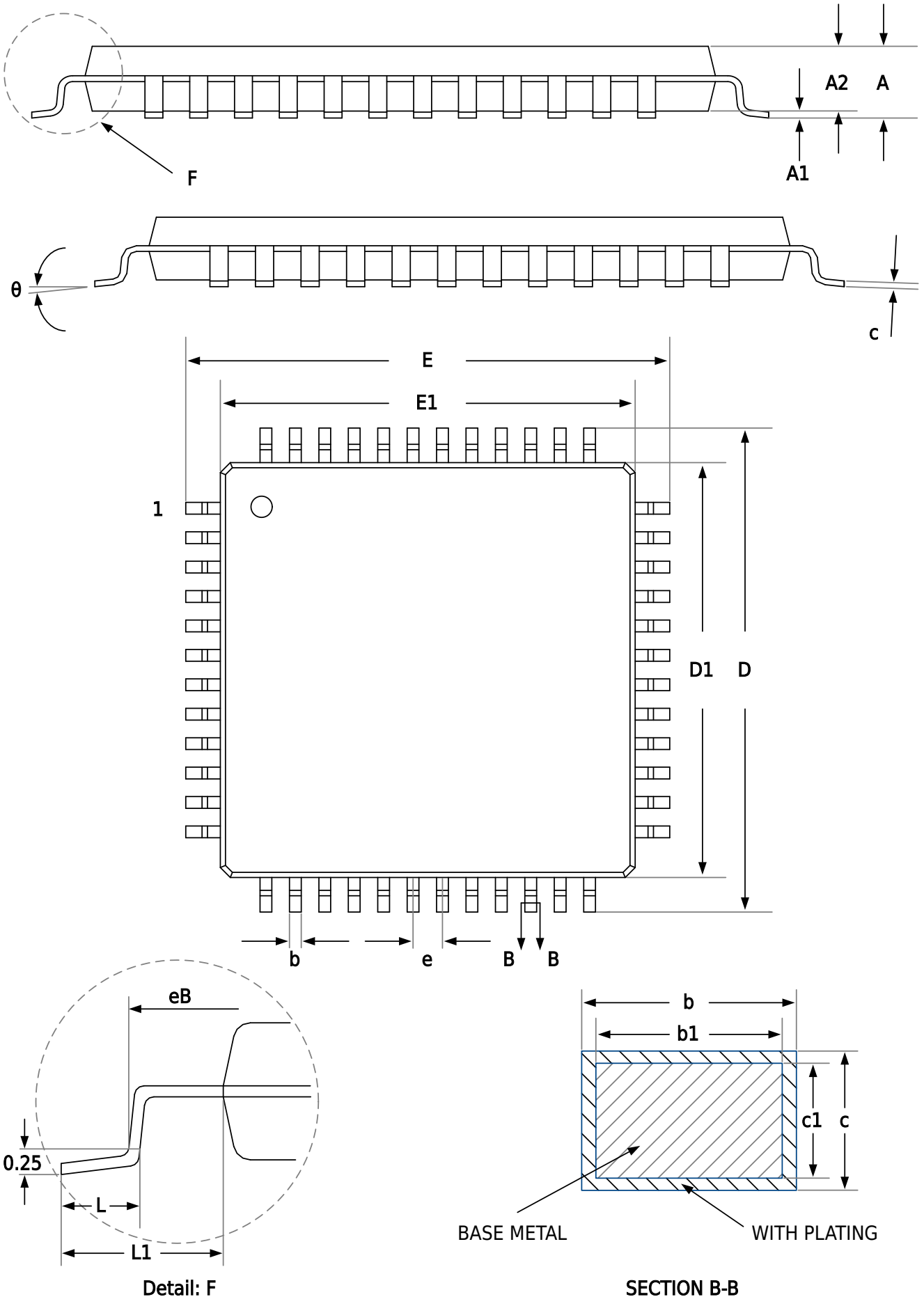


Symbol	LQFP64 (10x10)			LQFP64 (7x7)		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.60	-	-	1.60
A1	0.05	-	0.15	0.05	-	0.15
A2	1.35	1.40	1.45	1.35	1.40	1.45
b	0.17	-	0.27	0.16	-	0.25
b1	0.17	0.20	0.23	0.15	-	0.21
c	0.09	-	0.20	0.09	-	0.20
c1	0.13BSC			0.13BSC		
D	11.80	12.00	12.20	8.80	9.00	9.20
D1	9.90	10.00	10.10	6.90	7.00	7.10
E	11.80	12.00	12.20	8.80	9.00	9.20
E1	9.90	10.00	10.10	6.90	7.00	7.10
eB	11.05	-	11.25	8.10	-	8.25
e	0.50BSC			0.40BSC		
L	0.45	-	0.75	0.45	-	0.75
L1	1.00REF			1.00REF		
θ	0°	-	7°	0°	-	7°

Note

Dimensions “D1” and “E1” do not include mold flash.

6.1.3 LQFP48 Package

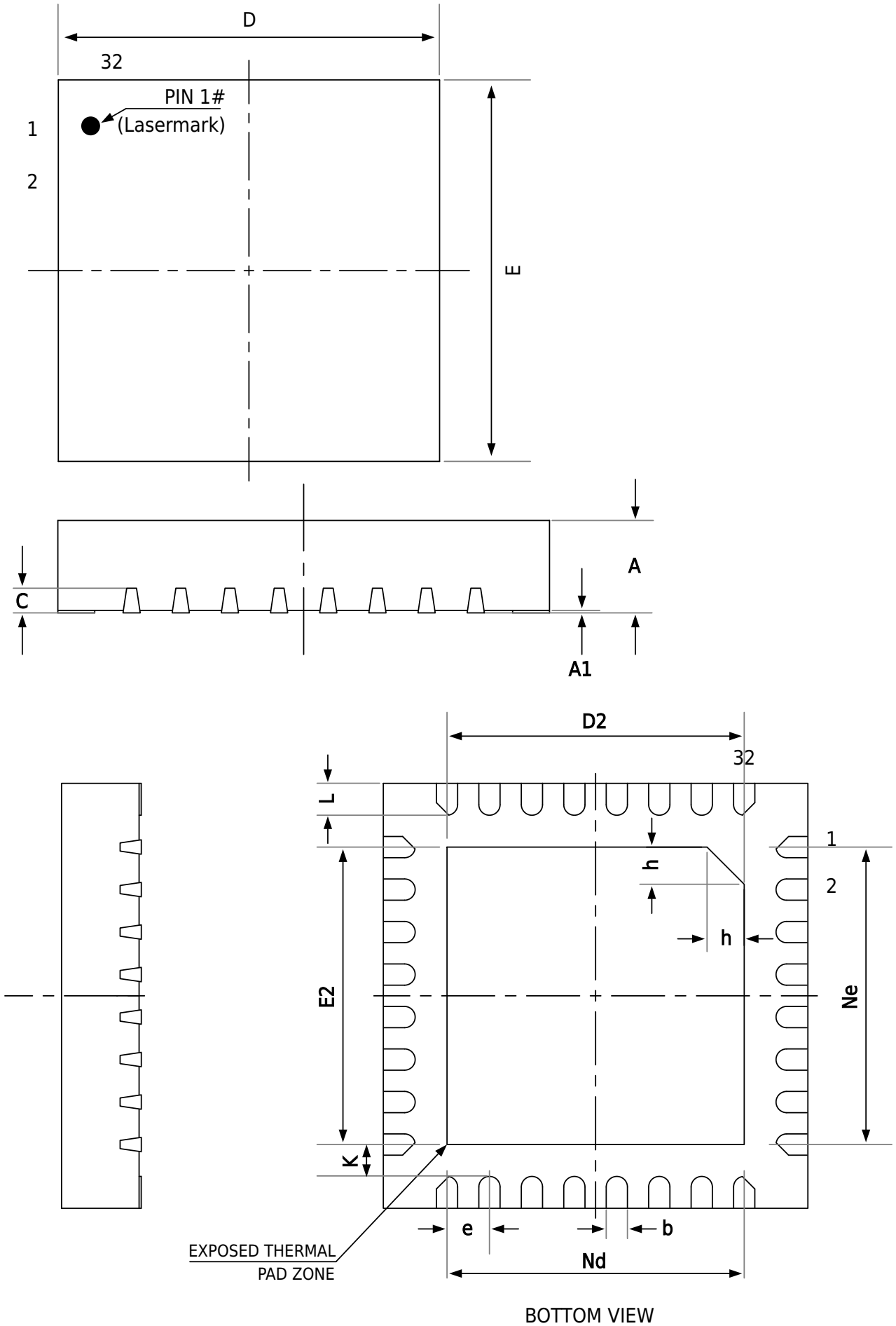


Symbol	7 x 7 Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	-	0.27
b1	0.17	0.20	0.23
c	0.09	-	0.20
c1	0.13BSC		
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.50BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0	-	7°

Note

Dimensions “D1” and “E1” do not include mold flash.

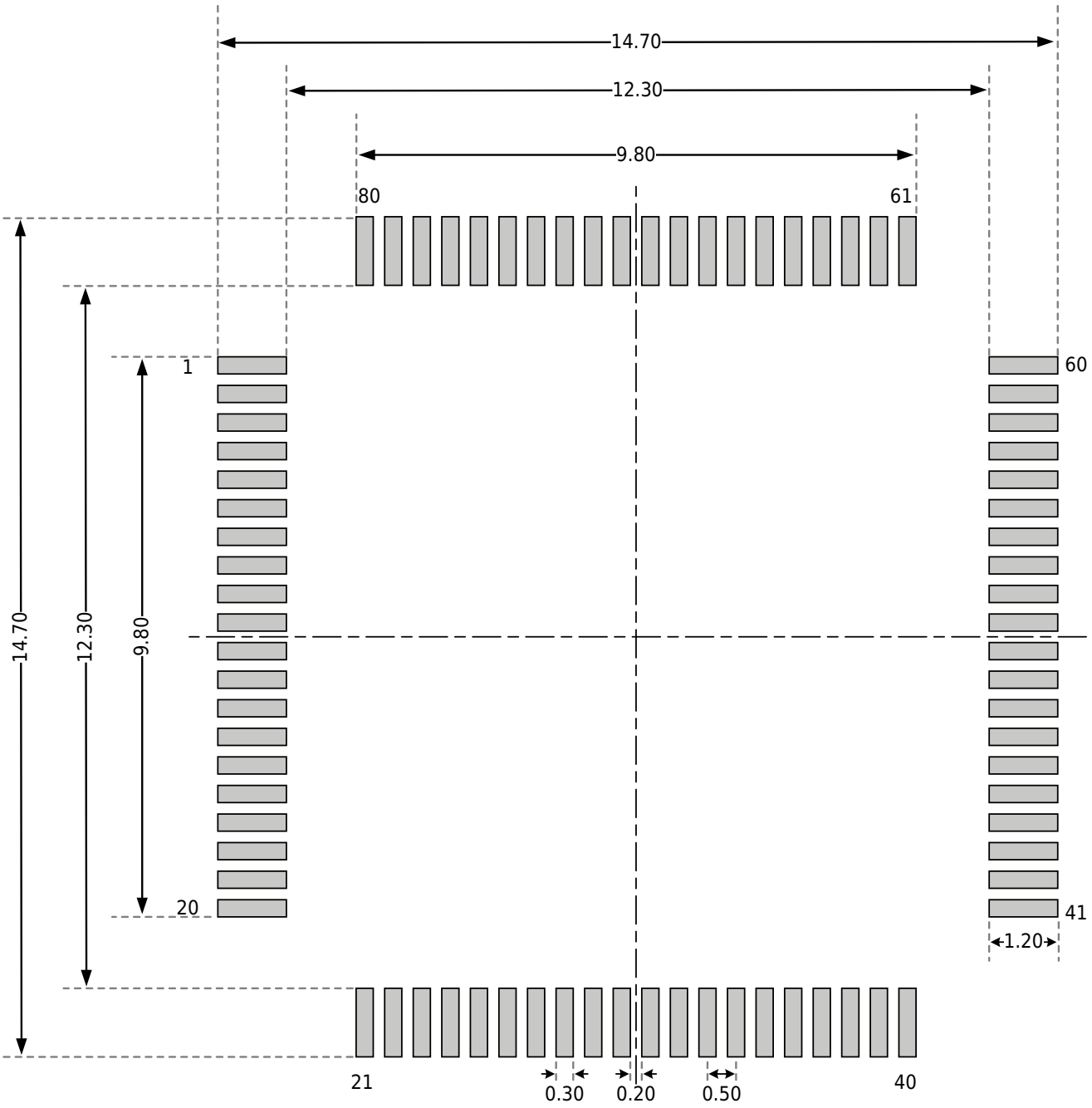
6.1.4 QFN32 Package



Symbol	4 x 4 Millimeter		
	Min	Nom	Max
A	-	-	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c		0.203REF	
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
e		0.40BSC	
Nd		2.80BSC	
E	3.90	4.00	4.10
E2	2.60	2.70	2.80
Ne		2.80BSC	
L	0.25	0.30	0.35
h	0.30	0.35	0.40
K		0.35REF	

6.2 PCB Land Pattern

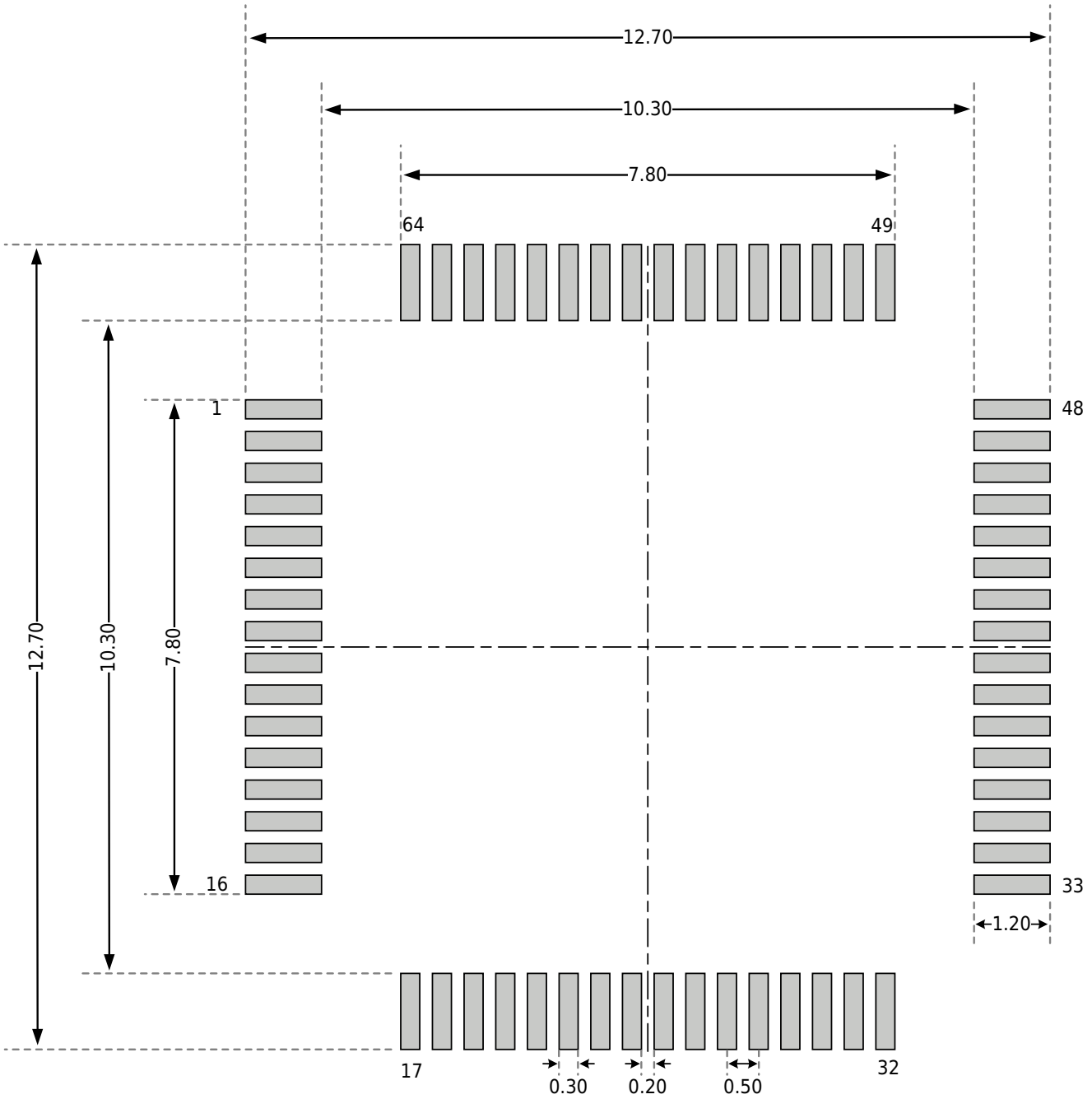
6.2.1 LQFP80 Package (12mm x 12mm)



Note

- Dimensions are in millimeters.
- Dimensions are for reference only.

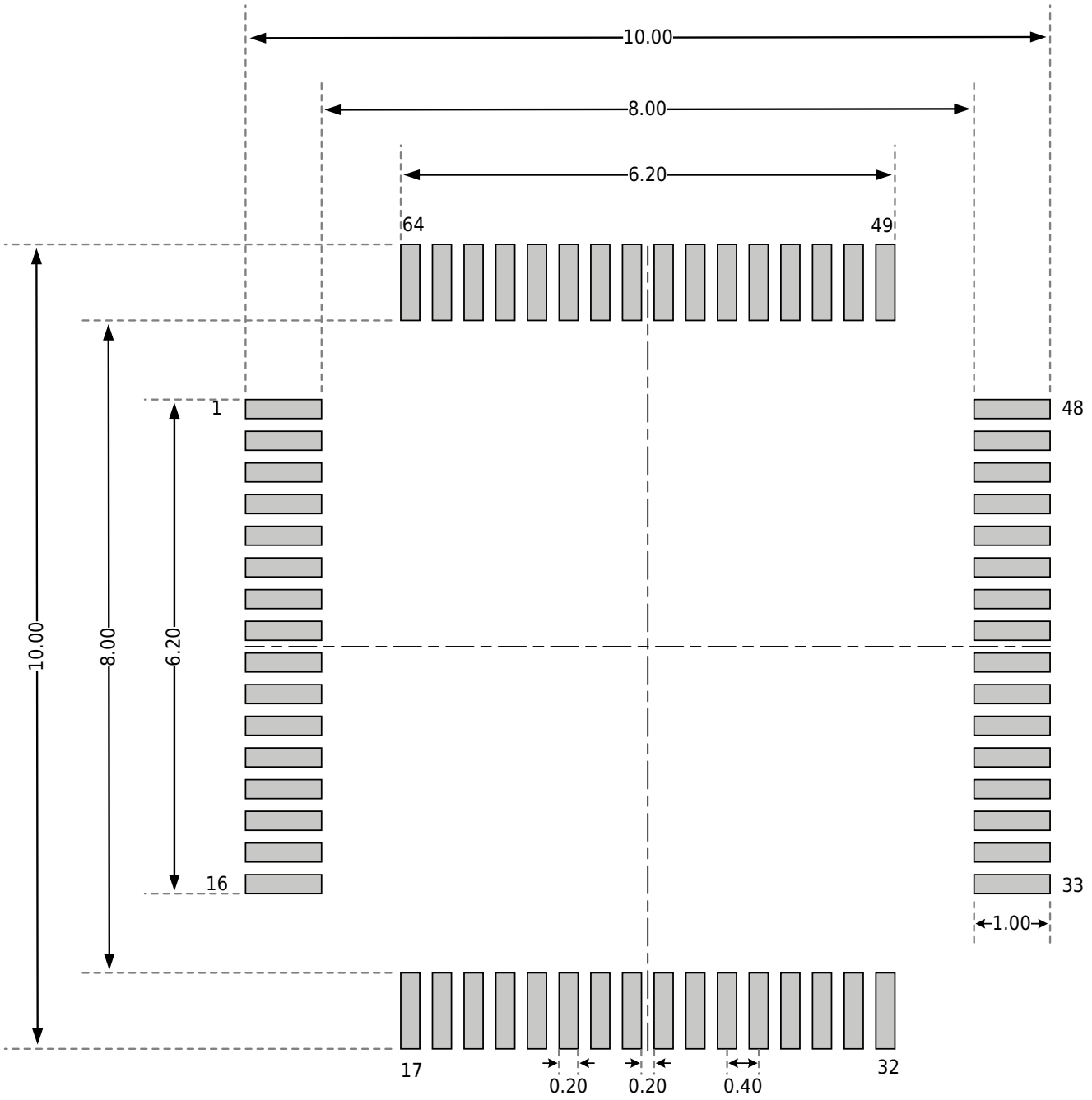
6.2.2 LQFP64 Package (10mm x 10mm)



Note

- Dimensions are in millimeters.
- Dimensions are for reference only.

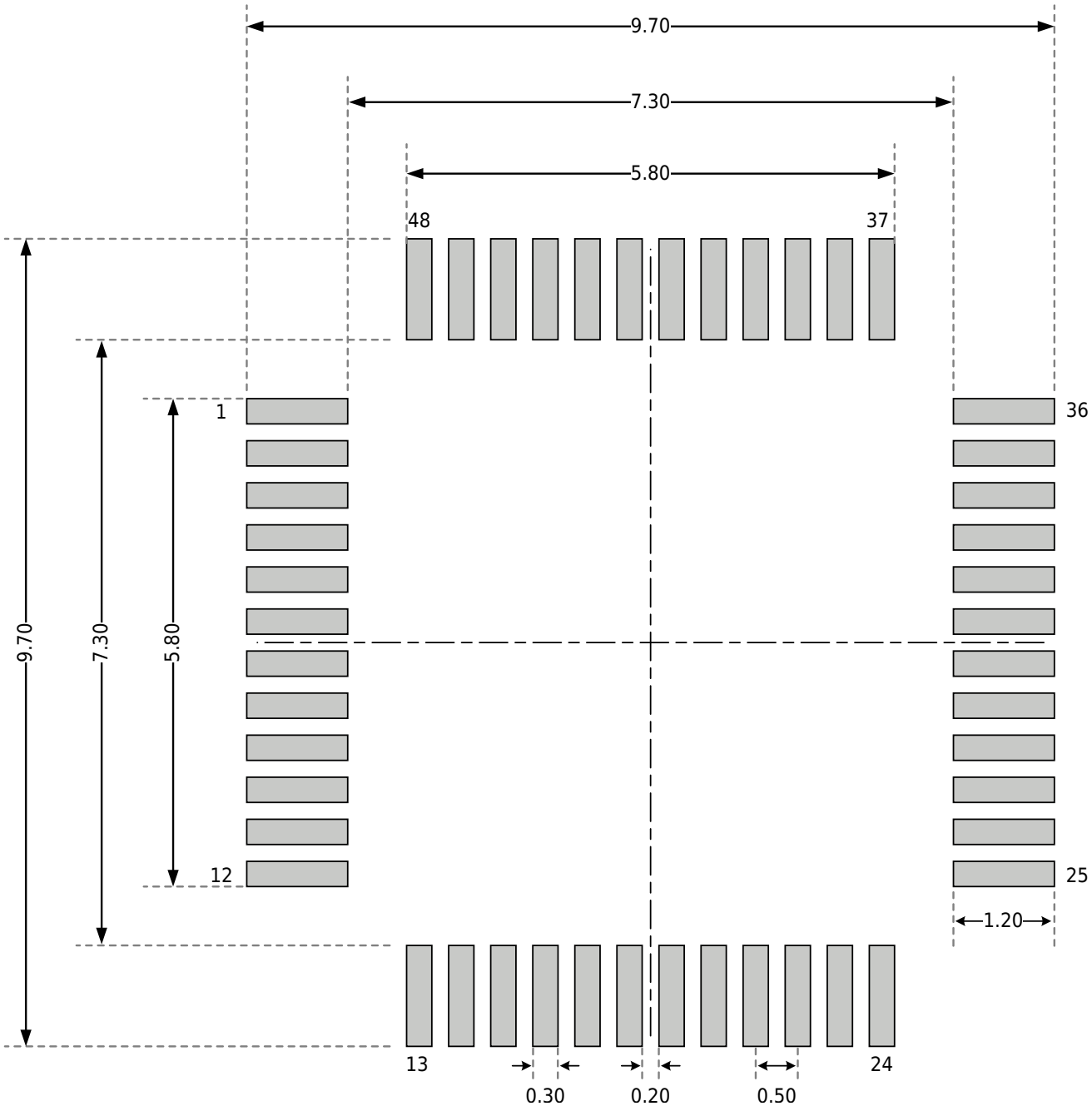
6.2.3 LQFP64 Package (7mm x 7mm)



Note

- Dimensions are in millimeters.
- Dimensions are for reference only.

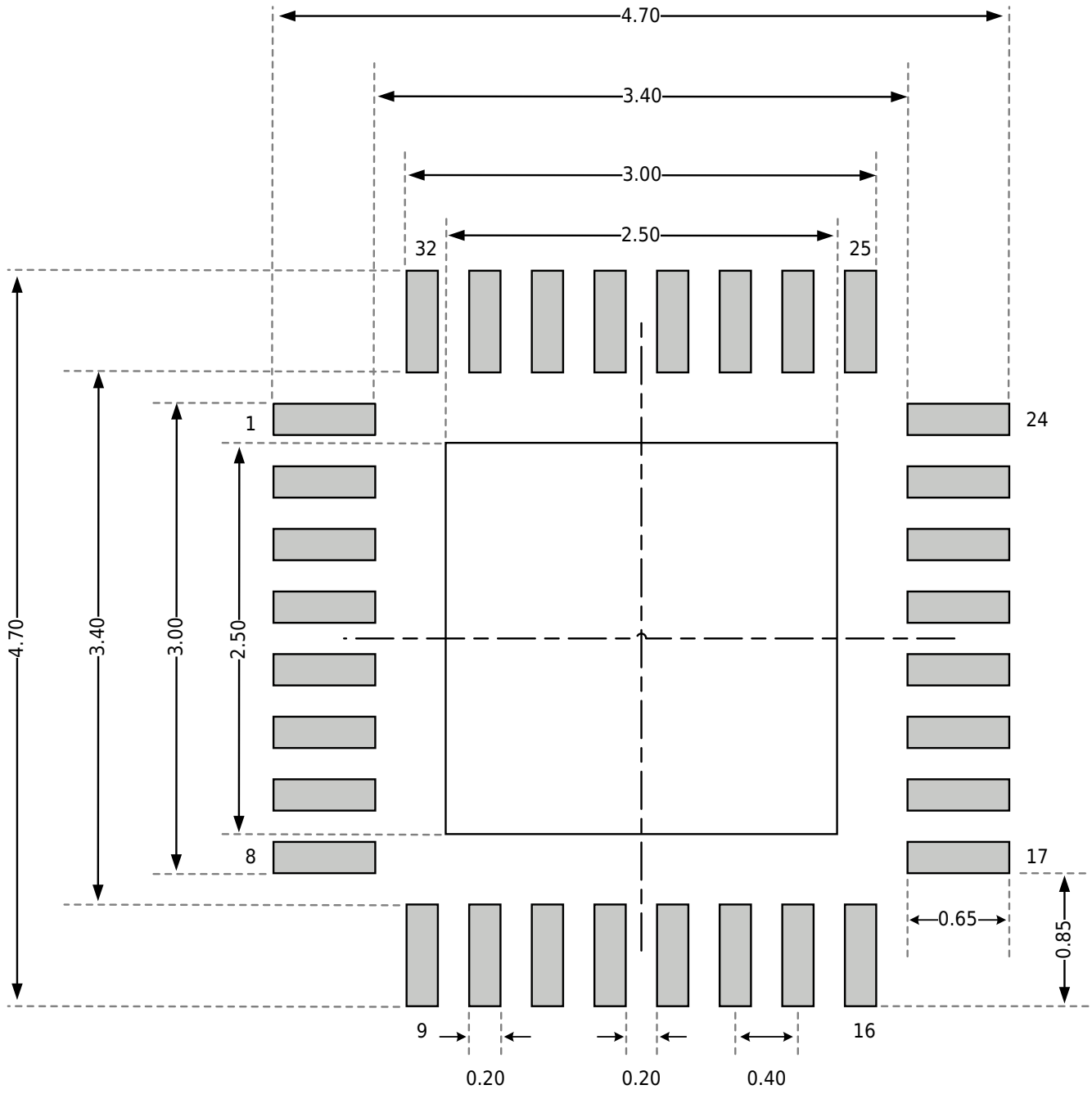
6.2.4 LQFP48 Package (7mm x 7mm)



Note

- Dimensions are in millimeters.
- Dimensions are for reference only.

6.2.5 QFN32 Package (4mm x 4mm)



Note

- Dimensions are in millimeters.
- Dimensions are for reference only.

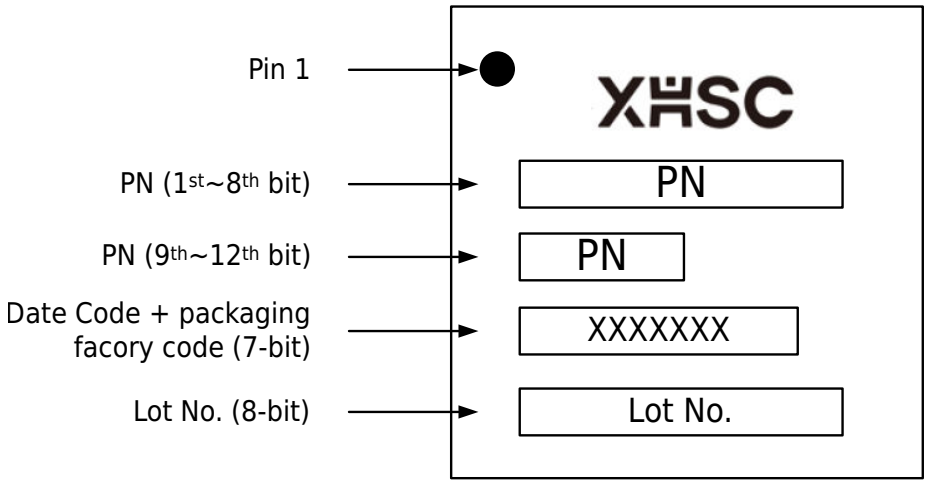
6.3 Package Marking

The position and information of Pin 1 printed on the front of each package are given below.

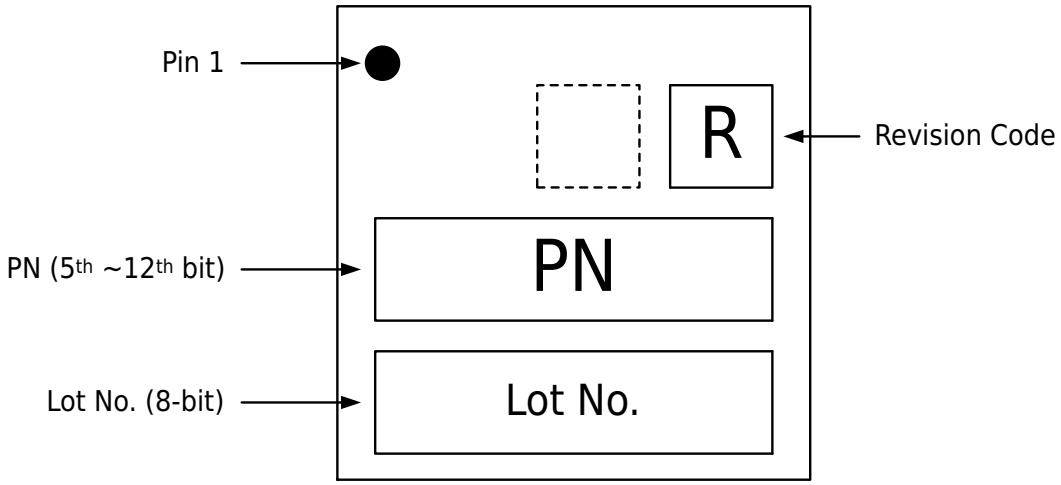
LQFP80 package (12mm x 12mm)

LQFP64 package (10mm x 10mm) / LQFP64 package (7mm x 7mm)

LQFP48 package (7mm x 7mm))



QFN32 package (4mm x 4mm)



Note

The blank boxes in the above figure indicate optional marks related to production, which are not explained in this section.

6.4 Packaging Thermal Resistance Coefficient

When the packaged chip is working at the specified working environment temperature, the junction temperature T_j (°C) on the chip surface can be calculated according to the following formula:

$T_j = T_{amb} + (P_D \times \theta_{JA})$

- T_{amb} refers to the working environment temperature when the packaged chip is working, the unit is ℃;
- θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, the unit is ℃/W;

- P_D is equal to the sum of internal power consumption of the chip and I/O power consumption P_{IO}, and the unit is W.

  $P_D = P_{INT} + P_{IO}$

  - P_{INT} is the internal power consumption of the chip, the product of Icc and Vcc of the product.
  - P_{IO} is the power consumption of all output IOs of the chip, and the calculation formula is: $P_{IO} = \Sigma(V_{OL} * I_{OL}) + \Sigma((VCC - V_{OH}) * I_{OH})$

When the chip is working at the specified working environment temperature, the junction temperature T_j of the chip surface cannot exceed the maximum allowable junction temperature T_J of the chip.

Table 6-5 Thermal resistance coefficient table for each package

Package Type and Size	Thermal Resistance Junction-ambient Value (θ_{JA})	Unit
LQFP80 12mm x 12mm / 0.5mm pitch	55 ± 10%	℃/W
LQFP64 10mm x 10mm / 0.5mm pitch	65 ± 10%	℃/W
LQFP64 7mm x 7mm / 0.4mm pitch	75 ± 10%	℃/W
LQFP48 7mm x 7mm / 0.5mm pitch	75 ± 10%	℃/W
QFN32 4mm x 4mm / 0.4mm pitch	51.61 ± 10%	℃/W

7 Ordering Information

Part Number		HC32L166MCTA-LQFP80	HC32L166KCTA-LQFP64	HC32L166KCTA-LQ64	HC32L166JCTA-LQ48	HC32L160FCUA-QFN32TR	HC32L166MATA-LQFP80	HC32L166KATA-LQFP64	HC32L166KATA-LQ64	HC32L166JATA-LQ48	HC32L160FAUA-QFN32TR
I/O		72	56	56	40	26	72	56	56	40	26
Memory	Flash	256KB	256KB	256KB	256KB	256KB	128KB	128KB	128KB	128KB	128KB
	RAM	32KB	32KB	32KB	32KB	32KB	16KB	16KB	16KB	16KB	16KB
Power supply voltages		1.8~5.5V	1.8~5.5V	1.8~5.5V	1.8~5.5V	1.8~5.5V	1.8~5.5V	1.8~5.5V	1.8~5.5V	1.8~5.5V	1.8~5.5V
Temp Range		-40~85℃	-40~85℃	-40~85℃	-40~85℃	-40~85℃	-40~85℃	-40~85℃	-40~85℃	-40~85℃	-40~85℃
DMAC		2ch	2ch	2ch	2ch	2ch	2ch	2ch	2ch	2ch	2ch
TIMER	General Timer	4	4	4	4	4	4	4	4	4	4
	Advanced Timer	3	3	3	3	3	3	3	3	3	3
	LPTimer	2	2	2	2	2	2	2	2	2	2
RTC		1	1	1	1	1	1	1	1	1	1
WDT		1	1	1	1	1	1	1	1	1	1
WWDT		1	1	1	1	1	1	1	1	1	1
Connectivity	UART	4	4	4	2	2	4	4	4	2	2
	LPUART	2	2	2	2	1	2	2	2	2	1
	I2C	2	2	2	2	2	2	2	2	2	2
	SPI	2	2	2	2	1	2	2	2	2	1
Analog	12-bit ADC	25ch	23ch	23ch	17ch	8ch	25ch	23ch	23ch	17ch	8ch
	12-bit DAC	1ch	1ch	1ch	1ch	1ch	1ch	1ch	1ch	1ch	1ch
	OPA	1	1	1	-	-	1	1	1	-	-
	VC	3	3	3	3	3	3	3	3	3	3
Display	LCD	4*47/6*45/8*43	4*40/6*38/8*36	4*40/6*38/8*36	4*26	-	4*47/6*45/8*43	4*40/6*38/8*36	4*40/6*38/8*36	4*26	-
LVD		1	1	1	1	1	1	1	1	1	1
CRC		√	√	√	√	√	√	√	√	√	√
Security	AES	√	√	√	√	√	√	√	√	√	√
Package Type		LQFP80(12*12mm)	LQFP64(10*10mm)	LQ64(7*7mm)	LQFP48(7*7mm)	QFN32(4*4mm)	LQFP80(12*12mm)	LQFP64(10*10mm)	LQ64(7*7mm)	LQFP48(7*7mm)	QFN32(4*4mm)
Packaging		Tray	Tray	Tray	Tray	Tape & Reel	Tray	Tray	Tray	Tray	Tape & Reel
Pitch		0.5mm	0.5mm	0.4mm	0.5mm	0.4mm	0.5mm	0.5mm	0.4mm	0.5mm	0.4mm

Before ordering, please contact the sales window for the latest mass production information.

Revision History

Document Version	release date	Modification Notes
Rev1.00	2024-04-22	First official release.
Rev1.01	2024-05-17	Added: 1. Added PF11 port to the port multiplexing table in the "Pin Function Description" section of the "Pin Configuration and Function" chapter. Revise: 1. In the "Product Features" section, the power consumption in sleep mode in ultra-low power performance was changed from "30μA/MHz@3V@24MHz" to "23μA/MHz@3V@48MHz"; 2. In the "Electrical Characteristics - Operating Conditions - ESD Characteristics" section, the maximum value of the VESDHBM parameter was changed from "4" to "6", and the minimum value was changed from "-" to "-6"; the minimum value of the VESDCDM parameter was changed from "-" to "-1.5"; the maximum value of the Ilatchup parameter was changed from "±200" to "200", and the minimum value was changed from "-" to "-200"; 3. The character "δ" in the description of the "Electrical Characteristics - Test Conditions" chapter was changed to "σ"; 4. The maximum value of the VCC-VSS parameter in the voltage characteristics table of "Electrical Characteristics - Absolute Maximum Ratings" was changed from "5.5" to "6.0"; 5. Revise the current data in I_{DD} (DeepSleep) in the "Electrical Characteristics - Operating Conditions - Supply Current Characteristics" section; 6. The minimum value of the Dev parameter in the "Electrical Characteristics - Operating Conditions - Internal Clock Source Characteristics - Internal Low-Speed Clock RC10K" section was changed from "50" to "-50". delete: 1. Deleted VC0_INN10 from the ANALOG description of PB00 in the Pin Function Description section of the "Pin Configuration and Functions" chapter.