1000 KSPS, 3.3 V – 4.8 V, ULTRA LOW POWER, 12-BIT SAR ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 12-Bit Resolution
- Low Power (XC2362A typical):
  2.40mW (3.3V, 1000KSPS)
  10.0mW (4.5V, 1000KSPS)
- Single 3.3 V to 4.8 V Supply Operation for XC2362A
- Fast Throughput Rate:
  1000 KSPS for XC2362A
- ±1.5LSB INL, ±1.5LSB DNL
- No Data Latency
- SPI/ MICROWIRE™ Compatible Serial Interface
- Guaranteed Operation from –40°C to 85°C
- 6-Pin SOT-23 Package
- Second-Source for LTC2362

DESCRIPTION

The XC2362A is a 12-bit, high speed, low power, and small-sized Successive-Approximation-Register (SAR) ADC. The supply current drops at lower sampling rates because the device automatically power down after conversion. The full-scale input of the XC2362A is 0V to VDD or VREF. This device can operate from a single 3.3 V to 4.8 V supply with a 1000 KSPS throughput.

The XC2362A is available in a 6-pin SOT-23 package and has an operating temperature range of -40°C to 85°C.

The XC2362A is a drop-in replacement for the LTC2362.

APPLICATIONS

- Communication Systems
- Data Acquisition Systems
- Handheld Portable Devices
- Uninterrupted Power Supplies
- Battery-Operated Systems
- Automotive

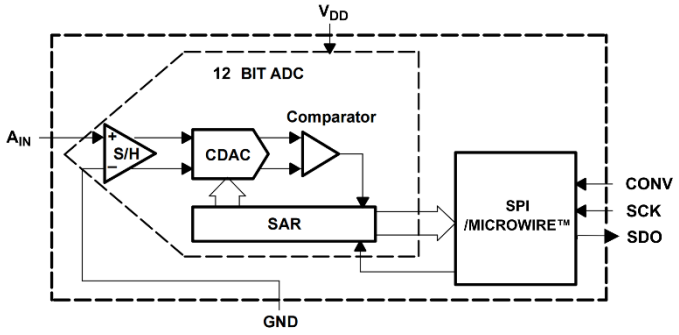


Figure 1. Functional Block Diagram

SPECIFICATIONS

At-40℃ to 85℃, f_{SAMPLE} = 1000 KSPS and f_{SCLK} = 20 MHz if 3.3 V ≤ V_{DD} ≤ 4.8 V. (unless otherwise noted)

PARAMETER	TEST CONDITIONS	XC2360A			XC2361A			XC2362A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SYSTEM PERFORMANCE											
Resolution			**12**			**12**			**12**		Bits
No missing codes		**12**			**12**			**12**			Bits
Integral linearity			**1.5**			**1.5**			**1.5**		LSB
Differential linearity			**1.5**			**1.5**			**1.5**		LSB
f_{SAMPLE} Throughput rate	3.3 V ≤ V_{DD} ≤ 4.8 V			**1000**			**1000**			**1000**	KSPS
SNR	f_{IN} = 100 kHz		**72.4**			**72.4**			**72.4**		dB
THD	f_{IN} = 100 kHz		**-84**			**-84**			**-84**		dB

XC2362A

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{DD} Supply current, normal operation	Digital inputs = 0 V or V_{DD}	f_{SAMPLE} = 1000 KSPS, f_{SCLK} = 20 MHz, V_{DD} = 3.3 V		**0.72**	**1.56**	mA
		f_{SAMPLE} = 1000 KSPS, f_{SCLK} = 20 MHz, V_{DD} = 4.5 V		**2.22**	**3.44**	
		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 3.3 V		**0.60**	**1.28**	
		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 4.5 V		**1.80**	**2.80**	
POWER DISSIPATION, XC2362A						
Normal operation		f_{SAMPLE} = 1000 KSPS, f_{SCLK} = 20 MHz, V_{DD} = 3.3 V		**2.40**	**5.15**	mW
		f_{SAMPLE} = 1000 KSPS, f_{SCLK} = 20 MHz, V_{DD} = 4.5 V		**10.0**	**15.5**	

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

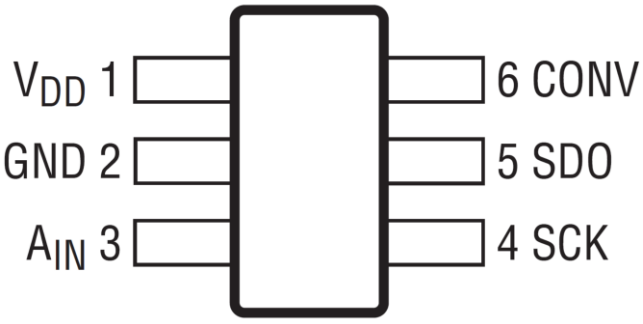


Figure 2. Pin Configuration

TERMINAL		DESCRIPTION
NAME	NO.	
V_{DD}	1	Power Supply Input.
GND	2	The ground return for the supply and signals.
A_{IN}	3	Analog Input. This signal can range from 0 V to V_{DD}.
SCK	4	Digital clock input. This clock directly controls the conversion and readout processes.
SDO	5	Digital data output. The output samples are clocked out of this pin on falling edges of the SCK pin.
CONV	6	Chip Select. On the falling edge of CONV, a conversion process begins.

TYPICAL CONNECTION

Figure 3 shows a typical connection diagram for the XC2362A. The 3.3 V supply should come from a stable power supply such as an LDO. The supply to XC2362A should be decoupled to the ground. A 1-µF and a 10-nF decoupling capacitor are required between the VDD and GND pins of the converter. Those capacitors should be placed as close as possible to the pins of the device. Always set the V_{DD} supply to be greater than or equal to the maximum input signal to avoid saturation of codes.

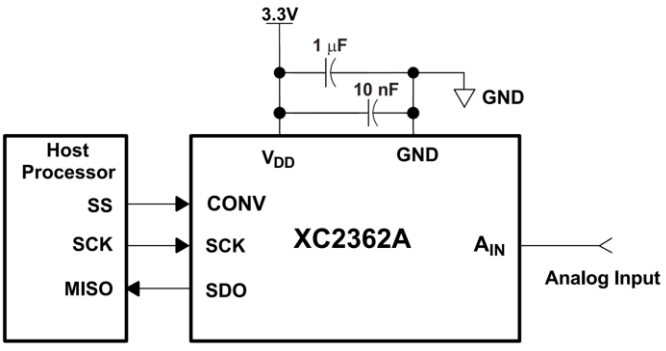


Figure 3. Typical Circuit Configuration

TIMING DIAGRAM

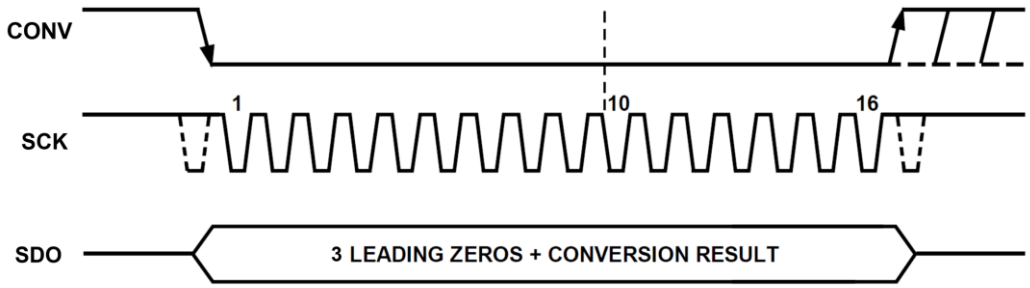


Figure 4. Timing Diagram

This is different from LTC2362 which outputs the conversion result through SDO immediately after the falling edge of the CONV. The XC2362A outputs a 12-bit conversion result from SDO after the fourth SCK falling edge after the CONV falling edge, after which the SDO enters a three-state and the conversion cycle ends. The XC2362A data word contains 3 leading zeros, followed by 12-bit data in MSB first format. Higher SCLK frequencies reduce the acquisition time and conversion time. This means the converters spend more time in auto power-down mode per conversion cycle.

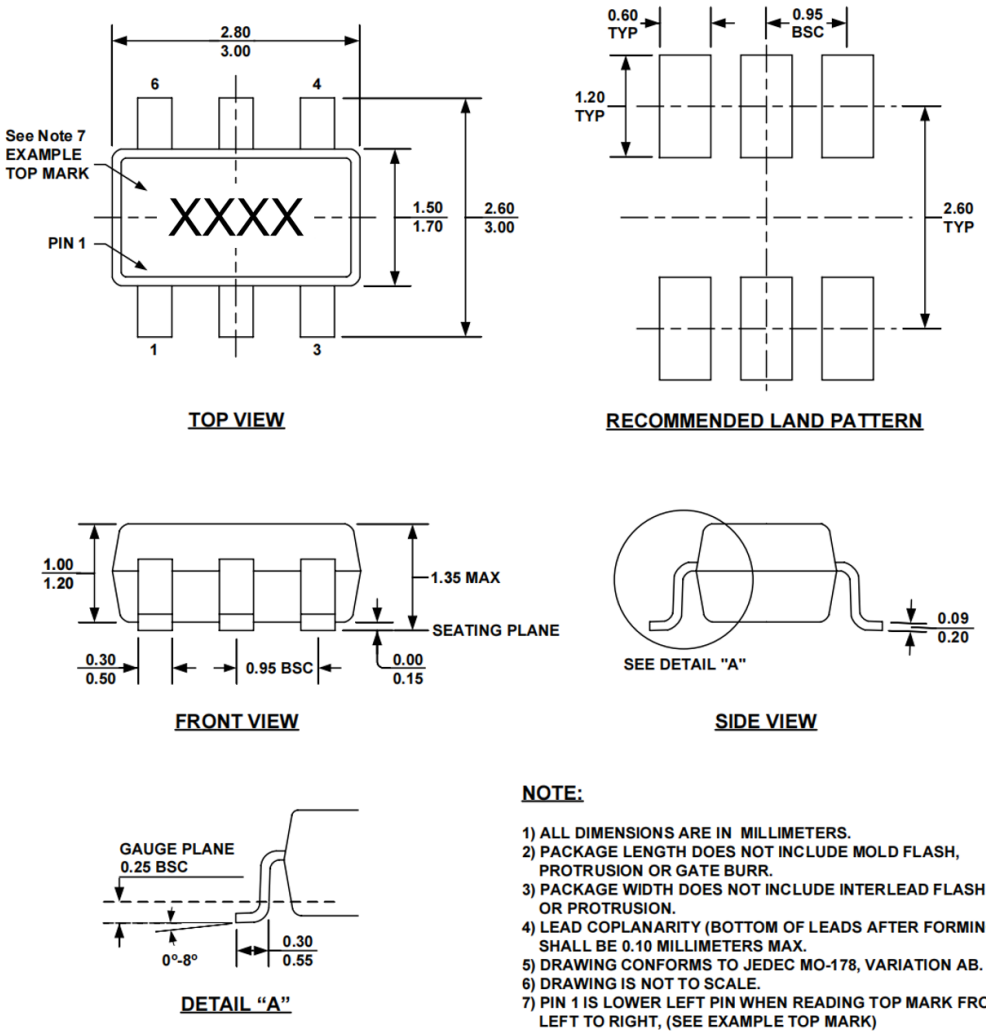
CONVERSION RESULT

The XC2362A outputs 12-bit data after 3 leading zeros, respectively. These codes are in straight binary format.

DESCRIPTION	ANALOG INPUT VOLTAGE	DIGITAL OUTPUT STRAIGHT BINARY	
		BINARY CODE	HEX CODE
XC2362A（12bit）			
Least Significant Bit (LSB)	V_{DD}/4096		
Full Scale	V_{DD} – 1LSB	1111 1111 1111	FFF
Mid Scale	V_{DD}/2	1000 0000 0000	800
Mid Scale – 1LSB	V_{DD}/2 – 1LSB	0111 1111 1111	7FF
Zero	0V	0000 0000 0000	000

There is no specific initialization requirement for these converters after power-on, but the first conversion might not yield a valid result. In order to set the converter in a known state, CONV should be toggled low then high after V_{DD} has stabilized during power-on. By doing this, the converter is placed in auto power-down mode, and the serial data output (SDO) is three-stated.

OUTLINE DIMENTIONS



NOTES

1. Unpacked ICs, tube-mounted ICs, etc. must be stored in a drying cabinet, and the humidity in the drying cabinet < 20% R.H.
2. After access, the components are stored in an electrostatic packaging protective bag.
3. Anti-static damage: the device is an electrostatic sensitive device, and sufficient anti-static measures should be taken during transmission, assembly and testing.
4. The user should conduct a visual inspection before use, and the bottom, side and surrounding of the circuit can be welded only if it is bright. If oxidation occurs, the circuit can be processed by means of oxidation, and the circuit must be soldered within 12 hours after processing.