IVCR1801 24V 4A Peak Source and 8A Peak Sink Single Channel Driver

1. Features

- 6-pin SOT-23
- 4A peak source and 8A peak sink drive current
- Wide VDD range up to 24V
- VDD operation from 4.5V to 20V with UVLO protection
- Dual inputs, either inverting or non-inverting input can be used. Unused input can be used as Enable or Disable control
- Ability to handle negative (-5V) input
- TTL and CMOS compatible input
- Low propagation delays (typical less than 20ns)
- Output held low when floating inputs
- Split output for independent turnon and turnoff speed adjustment
- Operating temperature range -40°C to 125°C

2. Applications

- Power Tools
- Motor Control
- AC/DC and DC/DC converters
- Server and Telecom rectifiers
- EV/HEV inverters and DC/DC converters
- PV boosters and inverters
- UPS
- Emerging Wide Band-Gap Power Devices

3. Description

The IVCR1801 is a 4A peak source and 8A peak sink drive single-channel, high-speed, low-side gate driver, capable of effectively and safely driving MOSFETs, IGBTs and emerging WBG power switches. Low propagation delay and compact SOT-23 package enable fast switching at hundreds of kHz. It is very suitable for server and telecom power supply's synchronous rectification driving, where synchronous MOSFET's dead time accuracy directly impacts converter's efficiency.

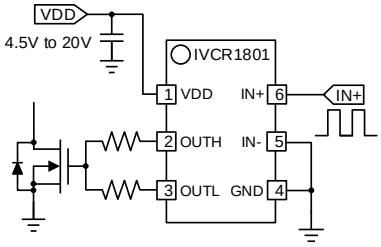
Wide VDD operating range from 4.5V to 20V enables effective driving with MOSFET or GaN power switches. Integrated UVLO protection ensures output held at low under abnormal conditions.

The independent inputs range from -5V to 24V ensure robust operation with undershoot or overshoot induced by parasitic inductances. The input thresholds are compatible with TTL input.

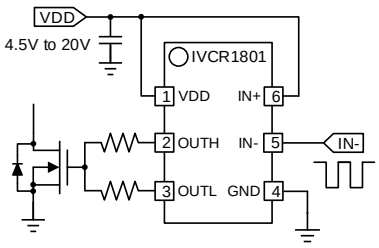
Device Information

PART NUMBER	PACKAGE	PACKING
IVCR1801SR	SOT-23-6	Tape and Reel

Typical Application Diagrams



Non-Inverting Input



Inverting Input

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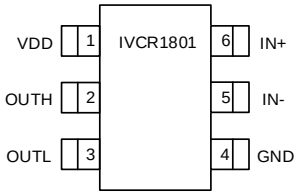
4. Pin Configuration and Functions

SOT-23-6 Top View



Pin Functions

PIN	NAME	I/O	DESCRIPTION
1	VDD	P	Positive bias supply
2	OUTH	O	Driver pull high output
3	OUTL	O	Driver pull low output
4	GND	G	Driver ground
5	IN-	I	Negative input
6	IN+	I	Positive input

Truth Table

VDD is higher than UVLO threshold.

IN+	IN-	OUTH/L
L or floating	X	L
X	H or floating	L
H	L	H

5. Specifications

5.1 Absolute Maximum Ratings

Over free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{DD}	Total supply voltage (reference to GND)	-0.3	24	V
OUTH	Gate driver output voltage		V_{DD}+0.3	V
OUTL	Gate driver output voltage	-0.3		V
IN+, IN-	Signal input voltage	-5.0	24	V
T_J	Junction temperature	-40	150	°C
T_{STG}	Storage temperature	-65	150	°C

(1) Operating beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended period may affect device reliability.

5.2 ESD Rating

		Value	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	+/-2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	+/-500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operation Conditions

		MIN	MAX	UNIT
V_{DD}	Total supply voltage	4.5	20	V
$V_{IN+, IN-}$	Signal input voltage	0	20	V
T_A	Operating ambient temperature range	-40	125	°C

5.4 Thermal Information

		Value	UNIT
$R_{\theta JA}$	Junction-to-Ambient thermal resistance	165	°C/W
$R_{\theta JB}$	Junction-to-Board thermal resistance	55	°C/W

5.5 Electrical Specifications

Unless otherwise noted, V_{DD} = 12 V, T_A = –40°C to 125°C
Currents are positive into and negative out of the specified terminal. Typical condition specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS CURRENT						
I_{DDoff}	Startup current	V_{DD}=3V, IN=0V		62		μA
I_{DDq}	Quiescent current	IN=0V		145		μA
UVLO						
V_{ON}	Under voltage thresholds	Rising threshold		3.8	4.2	V
V_{OFF}		Falling threshold	3.2	3.5		
INPUT (IN+, IN-)						
V_{INH}	Input rising threshold			2.0	2.4	V
V_{INL}	Input falling threshold		0.8	1.2		V
V_{INHYS}	Input hysteresis			0.8		V
V_{INNS}	Input negative voltage capability		-5			V
OUTPUTS (OUTH, OUTL)						
I_{OH}	Peak source current	C_{LOAD} =0.22uF, with external current limiting resistors, 1kHz switching frequency		4.0		A
I_{OL}	Peak sink current	C_{LOAD} =0.22uF, with external current limiting resistors, 1kHz switching frequency		8.0		A
V_{OH}	Output high voltage	I_{OUTH} = -10mA		V_{DD}-0.055	V_{DD}-0.12	V
V_{OL}	Output low voltage	I_{OUTL} = 10mA		0.0035	0.007	V
R_{OH}	Output pull-up resistance			5.5	12	Ω
R_{OL}	Output pull-down resistance			0.35	0.7	Ω
Timing						
TD_{rr}	Rising delay	Cload = 1.8nF		16	30	ns
TD_{ff}	Falling delay			16	30	
T_r	Rise time	Cload = 1.8nF		6		ns
T_f	Fall time			4.5		

6. Typical Characteristics

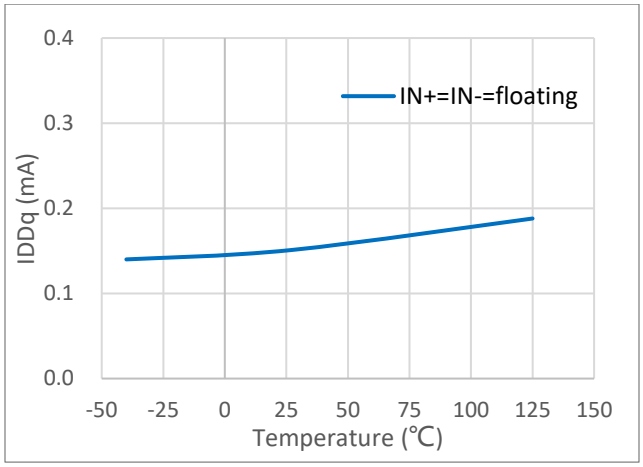


Figure 1. Quiescent Current IDDq vs Temperature

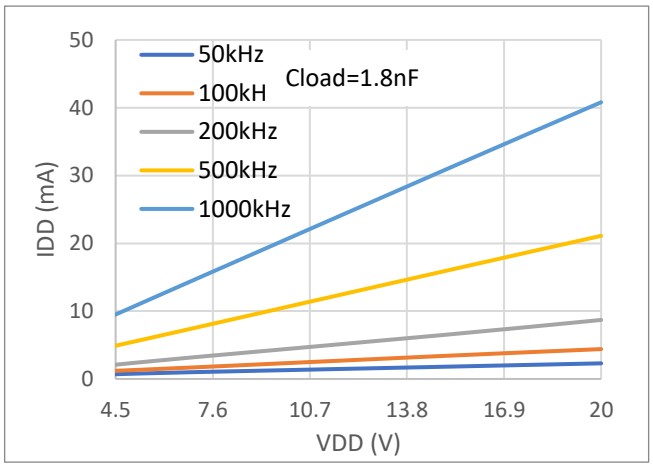


Figure 2. Operating Current IDD vs VDD

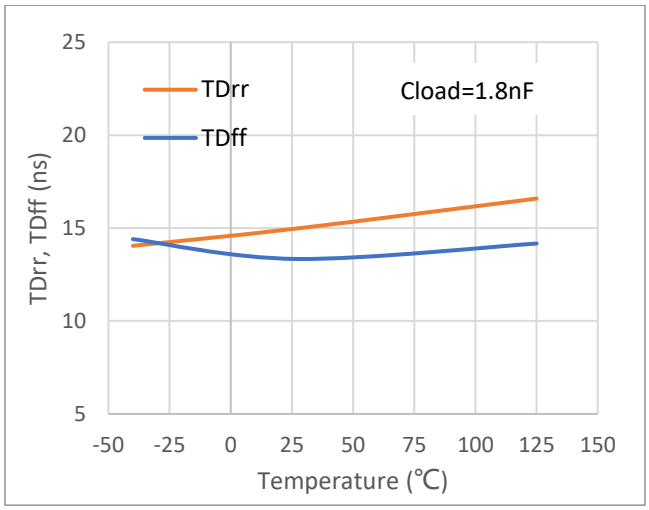


Figure 3. Propagation Delay vs Temperature

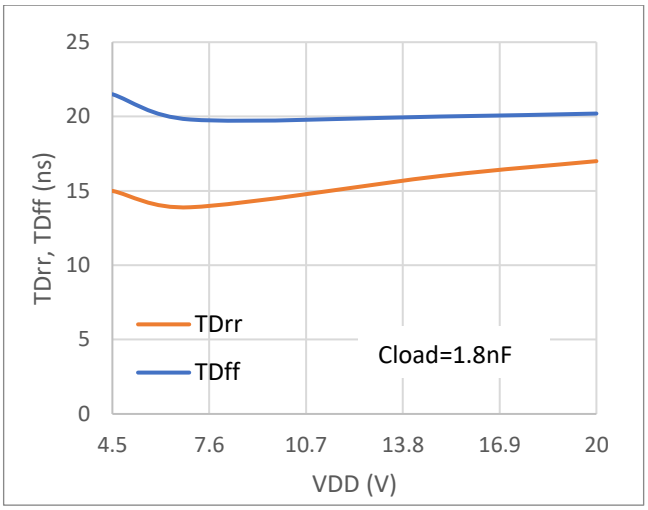


Figure 4. Propagation Delay vs VDD

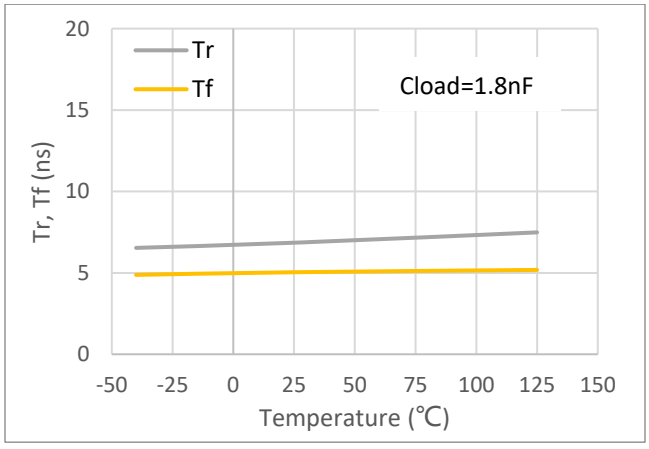


Figure 5. Rise Time and Fall time vs Temperature

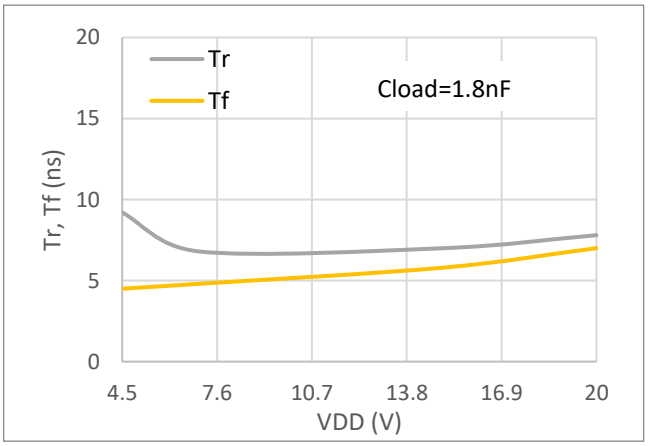


Figure 6. Rise Time and Fall time vs VDD

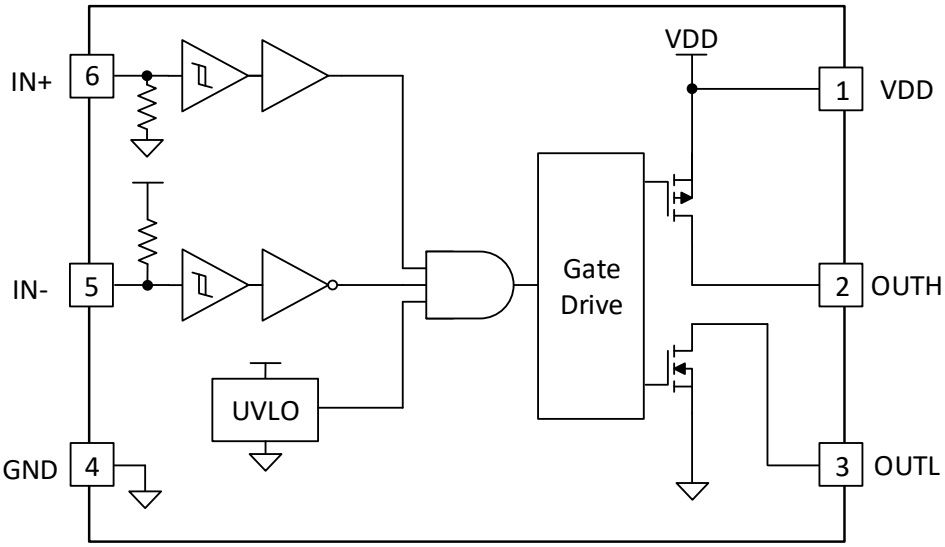
7. Detail Descriptions

IVCR1801 driver provides single-channel high-speed low-side gate drive. It features split outputs which make pull-up and pull-down capabilities independently adjustable.

7.1 Input Signal

IN+ is non-inverting logic gate driver input. IN- is inverting logic gate driver input. The input pins have a weak pull-up and pull-down. When left floating, outputs are pulled to GND. The input is a TTL and CMOS logic level with maximum 20V voltage tolerance.

Function Block Diagram



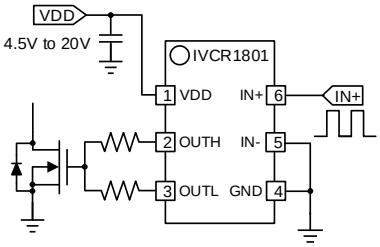
7.2 OUTH and OUTL

OUTH and OUTL are split outputs. OUTH consists of a hybrid pullup and OUTL consists an N-channel MOSFET for pulldown. Each output stage in IVCR1801 can supply 4A peak source and 8A peak sink current pulses. The output voltage swings between VDD and GND providing rail-to-rail operation. The presence of the MOSFET body diodes also offers voltage clamping paths to limit overshoot and undershoot. That means that in many cases, external Schottky diode clamps may not be necessary.

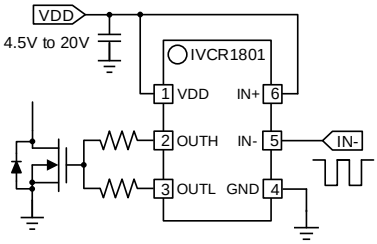
7.3 VDD and Under Voltage Protection

IVCR1801 maximum voltage rating is 24V. It is suitable for Si MOSFET, IGBT and SiC MOSFET gate drive. The driver has internal under voltage lockout (UVLO) protection feature. When VDD level is below UVLO threshold, this circuit holds the output LOW, regardless of the status of the inputs.

8. Application and Implementation

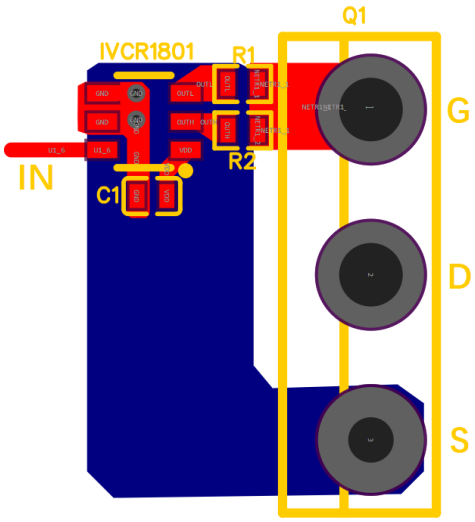


Using Non-Inverting Input



Using Inverting Input

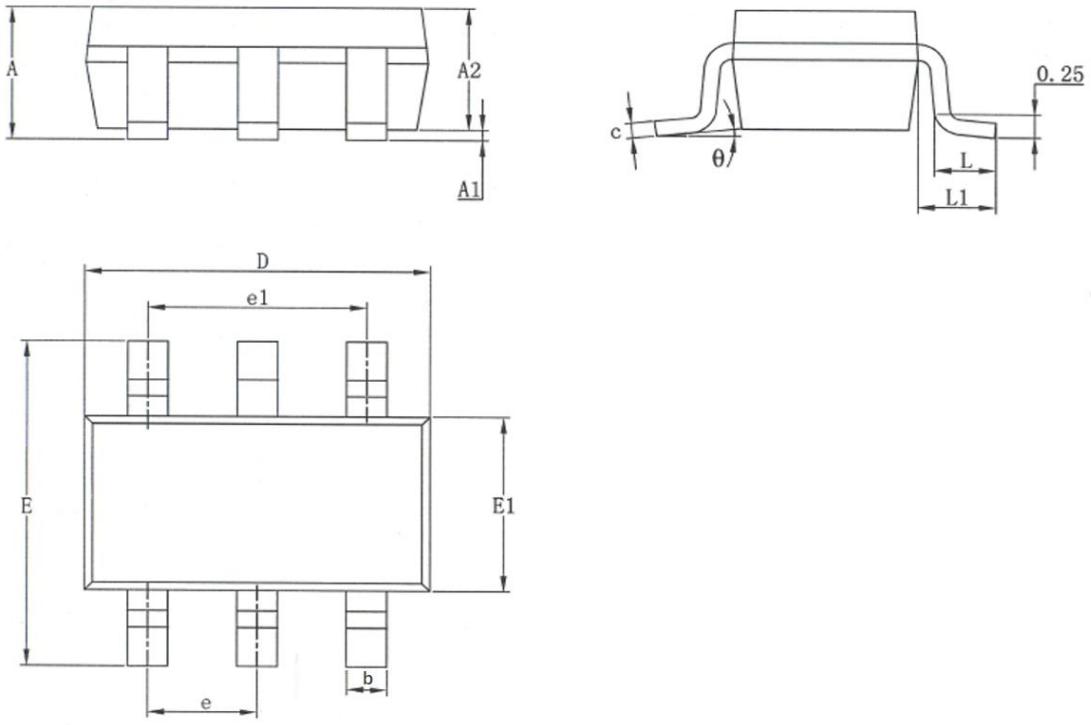
9. Layout



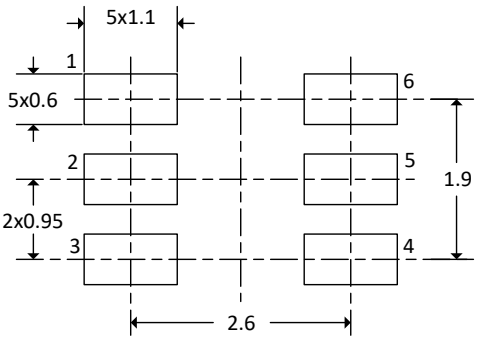
Layout Example for IVCR1801

10. Package Information

SOT-23-6 Package Dimensions



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.450	0.035	0.057
A1	0.000	0.150	0.000	0.006
A2	1.100		0.043	
b	0.300	0.500	0.012	0.020
c	0.080	0.220	0.003	0.009
D	2.750	3.050	0.108	0.120
E1	1.450	1.750	0.057	0.069
E	2.600	3.000	0.102	0.118
e	0.950		0.037	
e1	1.900		0.075	
L	0.300	0.600	0.012	0.024
L1	0.600		0.024	
θ	0.000	8.000	0.000	0.315



SOT-23-6 Recommended Soldering Dimensions