# Precision High Speed Fully Differential Amplifier

## Features

- Broad Power Supply Range: 3 V to 15 V
- Low Power: 4.6 mA
- High Bandwidth: 145 MHz
- High Slew Rate: 447 V/μs
- Low Input Offset Voltage:
  50 μV max (B grade)
  110 μV max from -40 °C to +125 °C (B grade)
- Low Input Offset Current: max 70 nA
- Low Noise: 2.9 $nV/\sqrt{Hz}$ , f = 100 kHz
- Wide Input Common-mode Range:
  $(-V_S) – 0.4$ V to $(+V_S) – 1$ V
- Wide Output Common Mode Control:
  $(-V_S) + 1$ V to $(+V_S) – 1$ V
- Rail-to-rail Output
- Low Harmonic Distortion:
  -133 dBc HD2 and -140 dBc HD3 at 1 kHz
- Fast Settling Time
  18-bit: 100 ns
  16-bit: 50 ns

## Applications

- Low Power Differential ADC Drivers
- Single-ended to Differential Converters
- Differential Buffers
- Medical Imaging
- Process Control
- Portable Electronics

## General Description

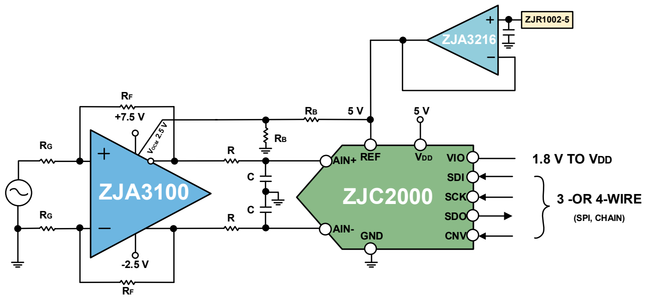
The ZJA3100 is a broadband fully differential amplifier. The gain of the amplifier is set by two pairs of matched resistors. The ZJA3100 is significant advancement over simple op amps for driving various differential input ADCs or for driving signals over long lines.

The ZJA3100 offers a -3 dB bandwidth of 145 MHz while consuming merely 4.6 mA supply current. It eliminates the need for a BALUN typically required by high performance high speed ADCs, achieving outstanding low frequency and dc accuracy in terms of input voltage and current offset. The common-mode level of the differential output is programmable by $V_{OCM}$ pin, with a wide range within 1 V to either rail, easily level shifting the input signals for driving single supply differential input ADCs. The combination of these features also makes ZJA3100 ideal driver for high performance SAR ADCs and Σ-Δ ADCs, which demands both DC precision and fast settling time for the large sampling cap of ADC.

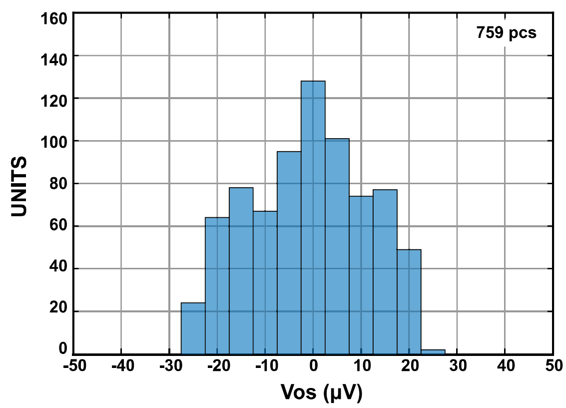
The ZJA3100 may serve as differential line driver for high speed signals over low cost twisted pair or coaxial cables. The wide supply range lends itself well to extensive general applications, such as analog or digital video signaling. The external feedback network can be optimized to boost the high frequency components of the signal in order to accommodate low pass filtering of the signal channel. The ZJA3100 yields significant cost saving, performance enhancement and area reduction over discrete line driver solutions.

ZJA3100 is available in both 8-lead SOIC, 8-lead MSOP and 16-lead QFN packages and specified over the extended industrial temperature range of -40 °C to +125 °C.

## Typical Application




## Typical Characteristics



## Table of Contents

## Version (Release D)[1]

### Revision History

**Feb. 2025 — Release D**

Updated Input Offset Voltage in Specifications table and Related Parts

**Dec. 2024 — Release C**

Added Typical Performance Characteristics

Updated Specifications

**Nov. 2024 — Release B**

Updated Outline Dimensions, Related Parts

**Sep. 2024**

Added Applications Information, Layout Guidelines, Layout Example

**May. 2024 — Release A**

**Dec. 2023 — Initial**

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## Pin Configurations and Function

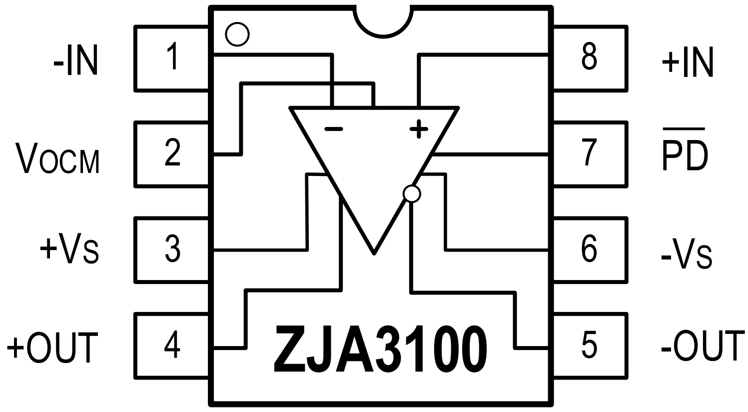


Figure 1. ZJA3100 Pin Configuration (8-lead SOIC and MSOP)

| Mnemonic | Pin No. | I/O[1] | Description |
|---|---|---|---|
| -IN | 1 | AI | Negative Input Summing Node. |
| $V_{OCM}$ | 2 | AI | Output Common-Mode Voltage. |
| $+V_S$ | 3 | P | Positive Supply Voltage. |
| +OUT | 4 | AO | Positive Output for Load Connection. |
| -OUT | 5 | AO | Negative Output for Load Connection. |
| $-V_S$ | 6 | P | Negative Supply Voltage. |
| $\overline{PD}$ | 7 | AI | Power Down Control.<br>$\overline{PD}$ = logic low = power off mode; $\overline{PD}$ = logic high = normal Operation. Normal operation is the default. It is recommended to add external resistor pulling up to positive power supply for best performances. |
| +IN | 8 | AI | Positive Input Summing Node. |

[1] AI: Analog Input; P: Power; AO: Analog Output.

  

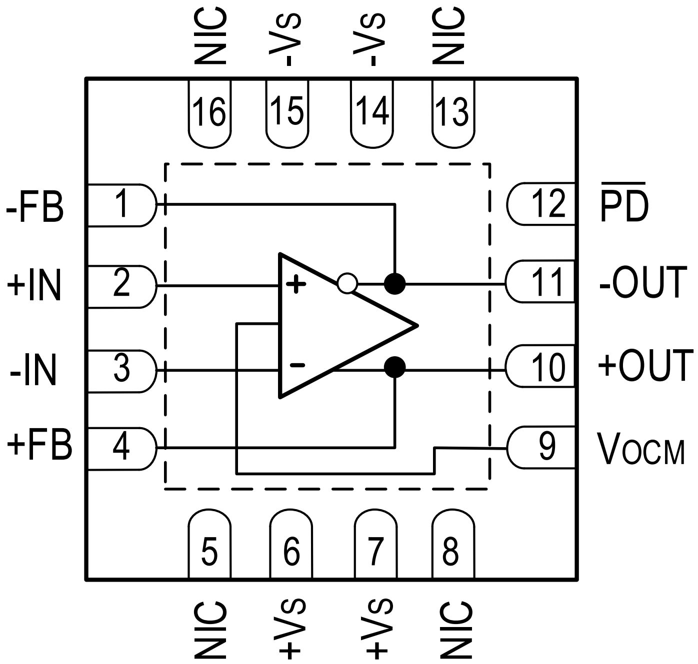


Figure 2. ZJA3100 Pin Configuration (16-lead QFN)

| Mnemonic | Pin No. | I/O[1] | Description |
|---|---|---|---|
| -FB | 1 | AO | Negative Output for Feedback Component Connection. |
| +IN | 2 | AI | Positive Input Summing Node. |
| -IN | 3 | AI | Negative Input Summing Node. |
| +FB | 4 | AO | Positive Output for Feedback Component Connection. |
| NIC | 5, 8, 13, 16 | -- | No Internal Connection. |
| $+V_S$ | 6,7 | P | Positive Supply Voltage. |
| $V_{OCM}$ | 9 | AI | Output Common-Mode Voltage. |
| +OUT | 10 | AO | Positive Output for Load Connection. |
| -OUT | 11 | AO | Negative Output for Load Connection. |
| $\overline{PD}$ | 12 | AI | Power Down Control.<br>$\overline{PD}$ = logic low = power off mode; $\overline{PD}$ = logic high = normal Operation. Normal operation is the default. It is recommended to add external resistor pulling up to positive power supply for best performances. |
| $-V_S$ | 14,15 | P | Negative Supply Voltage. |
| Exposed pad (EPAD) | | | Exposed Pad. Solder it to a heat-spreading power or ground plane. This pad is electrically isolated from the die, but must be connected to a power or ground plane and not floated. |

[1] AI: Analog Input; P: Power; AO: Analog Output.

  

## Absolute Maximum Ratings [1]

| Parameter | Rating |
|---|---|
| Supply Voltage | 15 V |
| Input Voltage | $\pm V_S$ |
| Operating Temperature Range | -40 °C to 125 °C |
| Storage Temperature Range | -65 °C to 150 °C |
| Junction Temperature Range | -65 °C to 150 °C |
| Max Reflow Temperature | 260 °C |
| Lead Temperature, Soldering (10 sec) | 300 °C |
| ESD Rating (ESD) [2] | |
| Human Body Model (HBM) [3] | 2 kV |
| Charge Device Model (CDM) [4] | 1.5 kV |

## Thermal Resistance [5]

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 8-lead SOIC | 158 | 43 | °C/W |
| 8-lead MSOP | 190 | 44 | °C/W |
| 16-lead QFN | 51 | 27 | °C/W |

[1] These ratings apply at 25 °C, unless otherwise noted.
Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

[2] Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

[3] ANSI/ESDA/JEDEC JS-001 Compliant

[4] ANSI/ESDA/JEDEC JS-002 Complaint

[5] $\theta_{JA}$ addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

## Specifications

### SUPPLY VOLTAGE ($V_S$ = ±5 V)

The ● denotes the specification which apply over the full operating temperature range, otherwise specifications are at $+V_S$ = 5 V, $-V_S$ = -5 V, $V_{OCM}$ = midsupply, G = 1, $R_F = R_G$ = 499 Ω, $R_{L,\,dm}$ =1 kΩ and $T_A$ = 25 °C, unless otherwise noted.

Positive Input ($+D_{IN}$) or Negative Input ($-D_{IN}$) to Differential Output Voltage ($V_{OUT,\,dm}$) Performance.

| Parameter | Symbol | Conditions | | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | | |
| Input Offset Voltage | $V_{OS}$ | B Grade | | | 20 | 50 | µV |
| | | | ● | | | 110 | µV |
| | | B Grade (QFN-16) | | | 25 | 120 | µV |
| | | | ● | | | 270 | µV |
| | | A Grade | | | 50 | 100 | µV |
| | | | ● | | | 500 | µV |
| | | A Grade (QFN-16) | | | 50 | 200 | µV |
| | | | ● | | | 500 | µV |
| Input Offset Voltage Drift | | | ● | | 0.5 | | µV/°C |
| Input Bias Current | | | | | 2 | 5.5 | µA |
| | | | ● | | | 25 | µA |
| Input Offset Current | | | | | 30 | 70 | nA |
| | | | ● | | | 300 | nA |
| Input Common-Mode Voltage ($V_{CM}$) Range | | | | $(-V_S)$ - 0.4 | | $(+V_S)$ - 1 | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = ±1 V | ● | 94 | | | dB |
| Open-Loop Gain | | Output Voltage ($V_{OUT}$) = ±4 V | | | | | dB |
| **DYNAMIC PERFORMANCE** | | | | | | | |
| -3 dB Small Signal Bandwidth | | $V_{OUT,\,dm}$ = 20 $mV_{P-P}$, G = 1 | | | 145 | | MHz |
| Bandwidth for 0.1 dB Flatness | | $V_{OUT,\,dm}$ = 20 $mV_{P-P}$, G = 1 | | | 19 | | MHz |
| Slew Rate | | $V_{OUT,\,dm}$ = 8 V step | | | 447 | | V/µs |
| Settling Time | $t_S$ | 16-bit | | | 50 | | ns |
| | | 18-bit | | | 100 | | ns |
| Output Overdrive Recovery | | G = 2, $V_{OUT,\,dm}$ = 10 $V_{P-P}$, triangular waveform | | | 30 | | ns |
| **OUTPUT CHARACTERISTICS** | | | | | | | |
| Output Voltage Swing [1] | | Load resistance ($R_L$) = 100 Ω for each single-ended output | | $(-V_S)$ + 0.9 | | $(+V_S)$ - 1 | V |
| | | | ● | $(-V_S)$ + 1.2 | | $(+V_S)$ - 1.4 | V |
| | | $R_L$ = 1 kΩ | | $(-V_S)$ + 0.2 | | $(+V_S)$ - 0.3 | V |
| | | | ● | $(-V_S)$ + 0.25 | | $(+V_S)$ - 0.4 | V |
| Short-Circuit Current | $I_{SC}$ | Sourcing | | | 82 | | mA |
| | | | ● | | 45 | | mA |
| | | Sinking | | | 89 | | mA |
| | | | ● | | 55 | | mA |

[1] Output voltage amplitude might vary with supply and temperature.

| Parameter | Symbol | Conditions | | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| **NOISE PERFORMANCE** | | | | | | | |
| Input Voltage Noise Differential | $e_n$ | f = 100 kHz | | | 2.9 | | $nV/\sqrt{Hz}$ |
| **$V_{OCM}$ PERFORMANCE** | | | | | | | |
| Input Voltage Noise Gain | | $\Delta V_{OUT,\,cm}/\Delta V_{OCM}$, $\Delta V_{OCM} = \pm 1$ V | | 0.99 | | 1.01 | V/V |
| **$V_{OCM}$ CHARACTERISTICS** | | | | | | | |
| Input Common-Mode Voltage Range | IVR | | | $(-V_S) + 1$ | | $(+V_S) - 1$ | V |
| Input Offset Voltage | $V_{OSI}$ | $V_{OS,\,cm} = V_{OUT,\,cm} / 2$;<br>$V_{DIN+} = V_{DIN-} = V_{OCM} = 0$ V | • | | 1 | 5 | mV |
| Input Bias Current | | | • | | 0.1 | 5 | μA |
| CMRR | | $\Delta V_{OS,\,dm}/\Delta V_{OCM}$, $\Delta V_{OCM} = \pm 1$ V | • | 86 | 96 | | dB |

## General Performance

| Parameter | Symbol | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **$\overline{PD}$ Pin** | | | | | | | |
| Input Voltage | | Logic threshold | • | 0.3 | 0.95 | 2 | V |
| $\overline{PD}$ Pin Bias Current | | | | | | | |
| Enable | | $\overline{PD}$ = 5 V | | | 1.7 | 5 | μA |
| Disable | | $\overline{PD}$ = 0 V | | -2 | -0.7 | | μA |
| **POWER SUPPLY** | | | | | | | |
| Operating Range | | | | 3 | | 15 | V |
| Quiescent Current | | | | | | | |
| Enabled | | | | | 4.6 | 4.9 | mA |
| | | | • | | | 7.3 | mA |
| Disabled | | | | | 45 | 60 | μA |
| | | | • | | | 80 | μA |
| Positive Power Supply Rejection Ratio (PSRR) | | $\Delta V_{OS,\,dm}/\Delta V_S$, $\Delta V_S = 1\ V_{P-P}$ | | 86 | 103 | | dB |
| **SPECIFIED TEMPERATURE RANGE** | | | | | | | |
| | | | | -40 | | 125 | °C |

## Typical Performance Characteristics

Unless otherwise stated, $T_A$ = 25 °C, $V_S$ = ±5 V, $R_L$ = 2 kΩ.

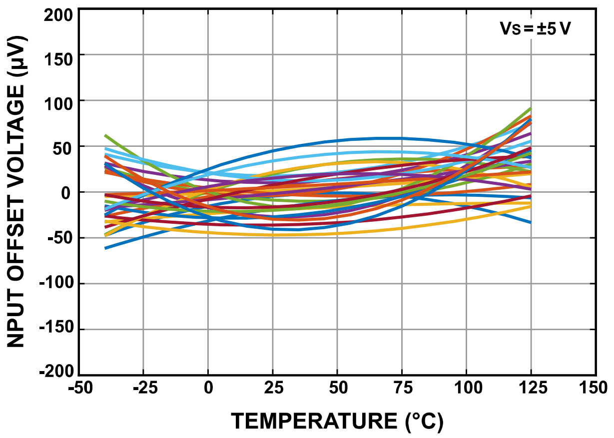


Figure 3. Input Offset Voltage vs. Temperature

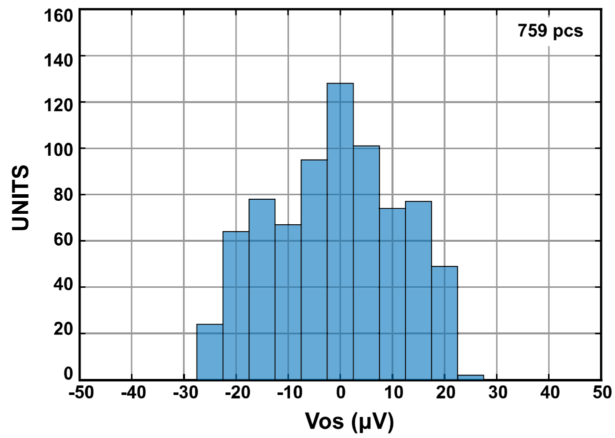


Figure 4. Input Offset Voltage Distribution

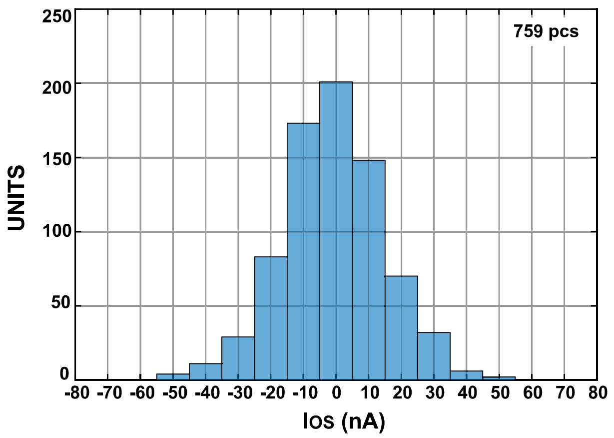


Figure 5. Input Offset Voltage Distribution

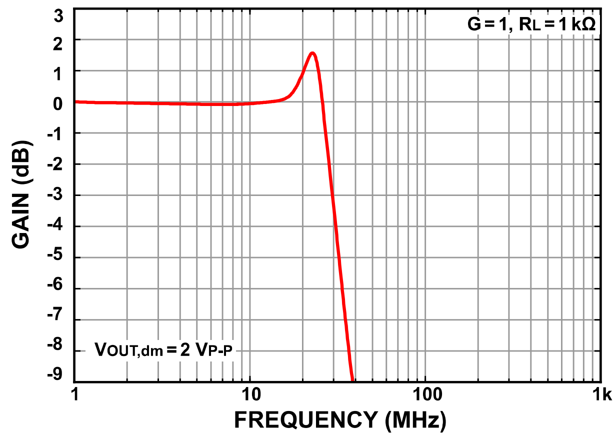


Figure 6. Large Signal Frequency Response

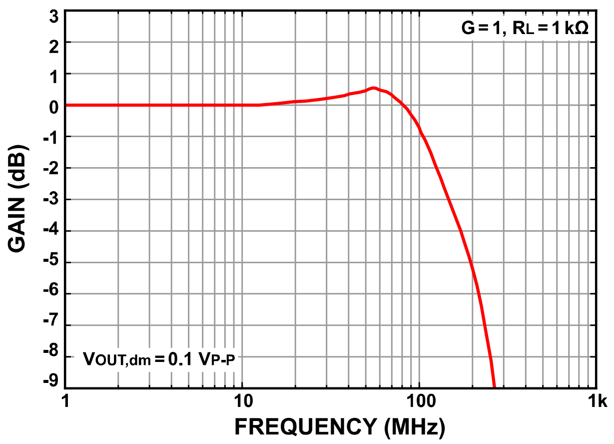


Figure 7. Small Signal Transient Response

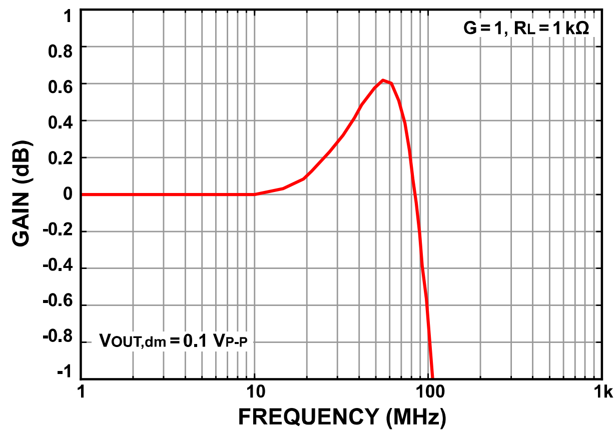


Figure 8. 0.1 dB Flatness Small Signal Frequency Response

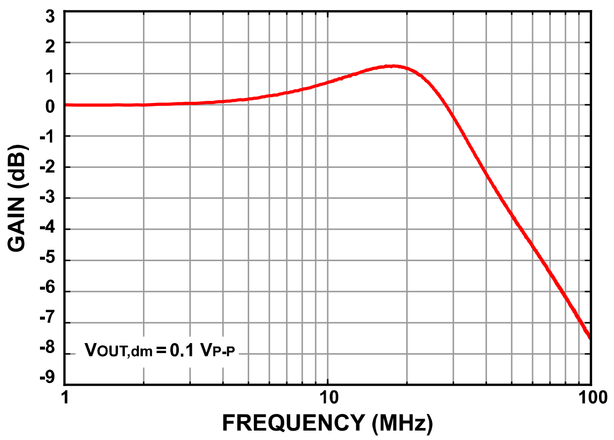


Figure 9. $V_{OCM}$ Small Signal Frequency Response

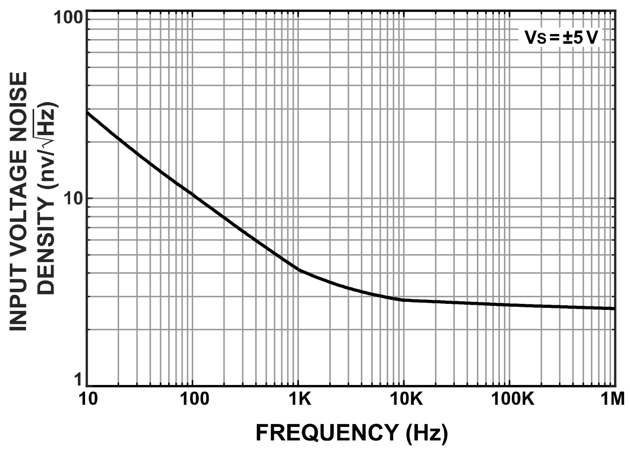


Figure 10. Voltage Noise Density

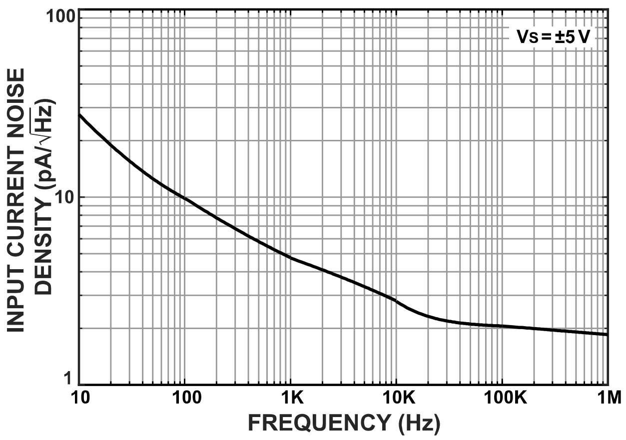


Figure 11. Current Noise Density

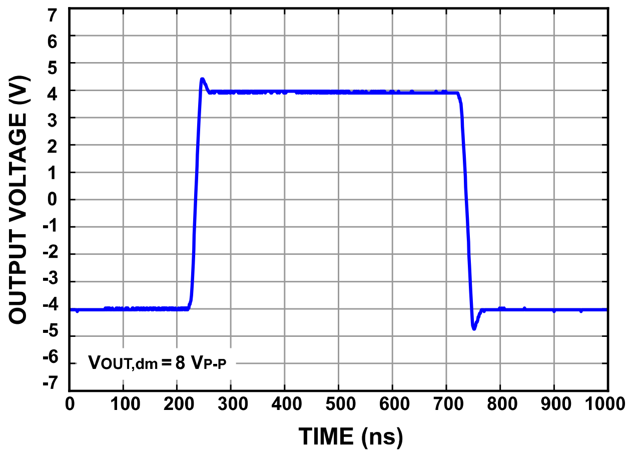


Figure 12. Large Signal Transient Response

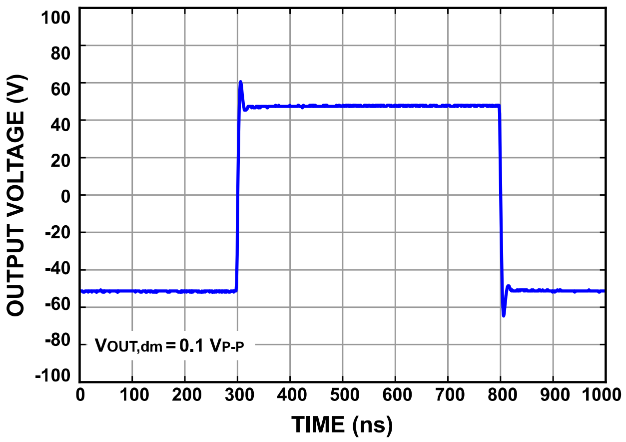


Figure 13. Small Signal Transient Response

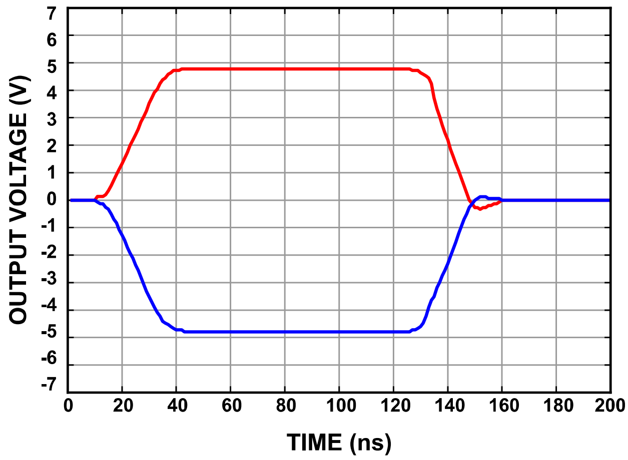


Figure 14. Overdrive Vs = 5 V Input = 5 $V_{P-P}$ G = 2

## Terminology and Application Assumptions

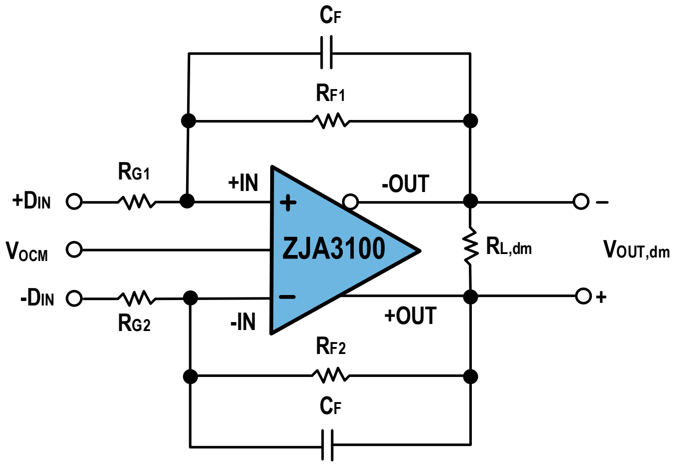


Figure 15. Circuit Definitions

Differential voltage refers to the difference between two node voltages. For example, the output differential voltage (or equivalently output differential-mode voltage) is defined as

$$V_{OUT,dm} = (V_{+OUT} - V_{-OUT}) \qquad \text{(E1)}$$

where $V_{+OUT}$ and $V_{-OUT}$ refer to the voltages at the +OUT and -OUT terminals with respect to a common reference.

Common-mode voltage refers to the average of two node voltages. The output common-mode voltage is defined as

$$V_{OUT,cm} = \frac{(V_{+OUT} + V_{-OUT})}{2} = V_{OCM} \qquad \text{(E2)}$$

By setting

$$\beta_1 = \frac{R_{G1}}{R_{F1} + R_{G1}}$$

$$\beta_2 = \frac{R_{G2}}{R_{F2} + R_{G2}}$$

The voltages at outputs under ideal assumptions:

$$V_{+OUT} = \frac{(+D_{IN})(1-\beta_1) - (-D_{IN})(1-\beta_2) + 2V_{OCM}\beta_1}{\beta_1+\beta_2} \qquad \text{(E3)}$$

$$V_{-OUT} = \frac{-[(+D_{IN})(1-\beta_1) - (-D_{IN})(1-\beta_2)] + 2V_{OCM}\beta_2}{\beta_1+\beta_2} \qquad \text{(E4)}$$

$$V_{OUT,dm} = \frac{2[(+D_{IN})(1-\beta_1) - (-D_{IN})(1-\beta_2)] + 2V_{OCM}(\beta_1-\beta_2)}{\beta_1+\beta_2} \qquad \text{(E5)}$$

For a balanced system where $R_{G1} = R_{G2} = R_G$ and $R_{F1} = R_{F2} = R_F$, the equations simplify to

$$\beta_1 = \beta_2 = \frac{R_G}{R_F + R_G}$$

  

Balance is a measure of how well differential signals are matched in amplitude and exactly 180° apart in phase. Balance is most easily determined by placing a well-matched resistor divider between the differential voltage nodes and comparing the magnitude of the signal at the midpoint of the divider with the magnitude of the differential signal (see Figure 16). By this definition, output balance is the magnitude of the output common-mode voltage divided by the magnitude of the output differential mode voltage:

$$Output\ Balance\ Error = \left|\frac{V_{OUT,cm}}{V_{OUT,dm}}\right|$$

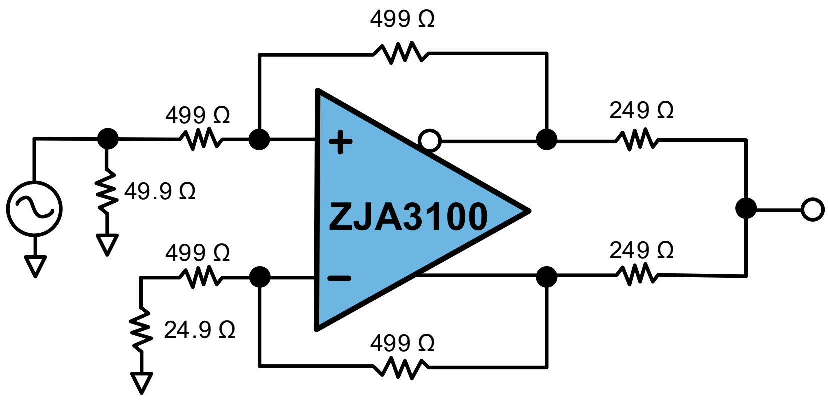


Figure 16. Test Circuit for Output Balance

Numerous common terms that are unique to this type of device exist.

- Fully differential amplifier (FDA). This term is restricted to devices offering what appears similar to a differential inverting op amp design element that requires an input resistor (not a high-impedance input) and includes a second internal control loop that sets the output average voltage ($V_{OUT,CM}$) to a set point.
- This second common-mode control loop interacts with the differential loop in certain configurations.
- The desired output signal at the two output pins is a differential signal that swings symmetrically around a common-mode voltage, which is the average voltage for the two outputs as defined above as $V_{OUT,CM}$.
- Single-ended to differential. The output must always be used differentially in an FDA; however, the source signal can be either a single-ended or a differential source with a variety of implementation details for either source. For an FDA operating in single-ended to differential, only one of the two input signals is applied to one of the input resistors.
- The common-mode control has limited bandwidth from the input $V_{OCM}$ pin to the common-mode output voltage. The internal loop bandwidth beyond the input $V_{OCM}$ buffer is a much wider bandwidth than the reported $V_{OCM}$ bandwidth but is not directly discernable. A very wide bandwidth in the internal $V_{OCM}$ loop is required to perform an effective and low-distortion single-ended to differential conversion.

Several features in the application of the ZJA3100 are not explicitly stated but are necessary for correct operation. These features are:

- Good power-supply decoupling is required. Often a larger capacitor (2.2 μF, typical) is used along with a high-frequency, 0.1 μF supply decoupling capacitor at the device supply pins. For single-supply operation, only the positive supply has these capacitors. Where a split supply is used, connect these capacitors to ground on both sides with the larger capacitor placed some distance from the package and shared among multiple channels of the ZJA3100, if used. A separate 0.1 μF capacitor must be provided to each device at the device power pins. With cascaded or multiple parallel channels, including ferrite beads from the larger capacitor to the local high-frequency decoupling capacitor is often useful. Linear regulator is recommended to be used as the power supply.
- Although often not stated, the power disable pin ($\overline{PD}$) is tied to the positive supply when only an enabled channel is desired.
- Virtually all ac characterization equipment expects a 50 Ω termination from the 50 Ω source and a 50 Ω, single-ended source impedance from the device outputs to the 50 Ω sensing termination. This condition is achieved in all characterizations (often with some insertion loss) but is not necessary for most applications. Matching impedance is most often required when transmitting over longer distances. Tight layouts from a source, through the ZJA3100, and to an ADC input do not require doubly-terminated lines or filter designs. The only exception is if the source requires a defined termination impedance for correct operation (for example, mixer outputs).
- The amplifier signal path is flexible for use as single- or split-supply operation. Most applications are intended to be single supply, but any split-supply design can be used as long as the total supply voltage across the ZJA3100, is within 15 V and the required input, output, and common-mode pin head rooms to each supply are taken into account. The $V_{OCM}$ pin cannot leave open and should be driven by a low impedance voltage source. Using a negative supply requires that $\overline{PD}$ be pulled down to below $\frac{[(+V_S)+(-V_S)]}{2}+0.7\ V$ to disable the amplifier.
- External element values are normally assumed to be accurate and matched. In an FDA, this assumption translates to equal feedback resistor values and a matched impedance from each input summing junction to either a signal source or a dc bias reference on each side of the inputs. Unbalancing these values introduces non-idealities in the signal path. For the signal path, imbalanced resistor ratios on the two sides create a common-mode to differential conversion. Furthermore, mismatched $R_F$ values and feedback ratios create additional differential output error terms from any common-mode dc or ac signal or noise terms. Using standard 1% resistor values is a typical approach and generally leads to some nominal feedback ratio mismatch. Modestly mismatched resistors or ratios do not by themselves degrade harmonic distortion. Where there is a meaningful common-mode noise or distortion coming in that gets converted to differential via an element or ratio mismatch. For the best dc precision, use 0.1% accuracy resistors that are readily available in E96 values (1% steps).

## Theory Of Operation

The ZJA3100 differs from conventional op amps in that it has two outputs whose voltages move in opposite directions. Like an op amp, it relies on high open-loop gain and negative feedback to force these outputs to the desired voltages. The ZJA3100 behaves much like a standard voltage feedback op amp and makes it easy to perform single-ended-to-differential conversion, common-mode level-shifting, and amplification of differential signals. Also like an op amp, the ZJA3100 has high input impedance and low output impedance.

Previous differential drivers, both discrete and integrated designs, have been based on using two independent amplifiers and two independent feedback loops, one to control each of the outputs. When these circuits are driven from a single-ended source, the resulting outputs are typically not well balanced.

Achieving a balanced output has typically required exceptional matching of the amplifiers and feedback networks.

DC common-mode level-shifting has also been difficult with previous differential drivers. Level-shifting has required the use of a third amplifier and feedback loop to control the output common-mode level. Sometimes the third amplifier has also been used to attempt to correct an inherently unbalanced circuit. Excellent performance over a wide frequency range has proven difficult with this approach.

The ZJA3100 uses two feedback loops to separately control the differential and common-mode output voltages. The differential feedback, set with external resistors, controls only the differential output voltage. The common-mode feedback controls only the common-mode output voltage. This architecture makes it easy to arbitrarily set the output common-mode level. It is forced, by internal common-mode feedback, to be equal to the voltage applied to the $V_{OCM}$ input, without affecting the differential output voltage.

The ZJA3100 architecture results in outputs that are very highly balanced over a wide frequency range without requiring tightly matched external components. The common-mode feedback loop forces the signal component of the output common-mode voltage to be zeroed. The result is nearly perfectly balanced differential outputs of identical amplitude and exactly 180° apart in phase.

# Applications Information

## Analyzing an Application Circuit

The ZJA3100 uses high open-loop gain and negative feedback to force its differential and common-mode output voltages in such a way as to minimize the differential and common-mode error voltages. The differential error voltage is defined as the voltage between the differential inputs labeled +IN and -IN in Figure 15. For most purposes, this voltage can be assumed to be zero. Similarly, the difference between the actual output common-mode voltage and the voltage applied to $V_{OCM}$ can also be assumed to be zero. Starting from these two assumptions, any application circuit can be analyzed.

## Setting the Closed-Loop Gain

Neglecting the capacitors $C_F$, the differential-mode gain of the circuit in Figure 15 can be determined to be described by

$$\left|\frac{V_{OUT,cm}}{V_{OUT,dm}}\right| = \frac{R_F}{R_G}$$

This assumes the input resistors, $R_G$, and feedback resistors, $R_F$, on each side are equal.

## Estimating the Output Noise Voltage

Similar to the case of a conventional op amp, the differential output errors (noise and offset voltages) can be estimated by multiplying the input referred terms, at +IN and -IN, by the circuit noise gain. The noise gain is defined as

$$G_N = 1 + \left(\frac{R_F}{R_G}\right)$$

To compute the total output referred noise for the circuit of Figure 15, consideration must also be given to the contribution of the Resistors $R_F$ and $R_G$. When the $R_F$ and $R_G$ terms are matched on each side and balanced, the total differential output noise is the root sum squared (RSS) of these separate terms. Using $G_N$, the total output noise is given as

$$e_o = \sqrt{(e_{ni}G_N)^2 + 2(i_n(R_F//R_G)G_N)^2 + 2(4kTR_F) + 2(4kTR_G G_N^2(\frac{R_F}{R_F+R_G})^2)}$$

Each resistor noise term is a 4kTR power (k is Boltzmann's constant $1.38 \times 10^{-23}$ J/K, $4kT = 1.6 \times 10^{-20}$ J at 290 K).

The first term is simply the differential input noise times the noise gain, the second term is the input current noise terms times the feedback resistor (and because there are two uncorrelated current noise terms, the power is two times one of them), and the last 2 terms are the output noise resulting from both the $R_F$ and $R_G$ resistors, at again twice the value for the output noise power of each side added together. Refer to Table 1 for the estimated output noise voltage densities at various closed-loop gains.

| Gain | $R_G$(Ω) | $R_F$(Ω) | Output Noise ZJA3100 Only | Output Noise ZJA3100 + $R_G$, $R_F$ |
|---|---|---|---|---|
| 1 | 499 | 499 | 5.8 nV/√Hz | 8.2 nV/√Hz |
| 2 | 499 | 1.0 k | 8.7 nV/√Hz | 13.4 nV/√Hz |
| 5 | 499 | 2.49 k | 17.4 nV/√Hz | 28.8 nV/√Hz |
| 10 | 499 | 4.99 k | 31.9 nV/√Hz | 54.5 nV/√Hz |

Table 1. ZJA3100 Output Noise at Different Gains

When using the ZJA3100 in gain configurations where $R_F/R_G$ of one feedback network is unequal to $R_F/R_G$ of the other network, there is a differential output noise due to input-referred voltage in the $V_{OCM}$ circuitry. The output noise is defined in terms of the following feedback terms (refer to Figure 15), $\beta_1$ for -OUT to +IN loop, and $\beta_2$ for +OUT to −IN loop. With these defined,

$$V_{nOUT,dm} = \left[(\beta_1 - \beta_2)G_N V_{nIN,V}\right] = 2V_{nIN,V_{OCM}}\left[\frac{\beta_1 - \beta_2}{\beta_1 + \beta_2}\right]$$

where $V_{nOUT,dm}$ is the output differential noise, and $V_{nIN,VOCM}$ is the input-referred voltage noise in $V_{OCM}$.

## The Impact of Mismatches in the Feedback Networks

As previously mentioned, even if the external feedback networks ($R_F/R_G$) are mismatched, the internal common-mode feedback loop still forces the outputs to remain balanced. The amplitudes of the signals at each output remain equal and 180° out of phase. The input-to-output differential-mode gain varies proportionately to the feedback mismatch, but the output balance is unaffected.

Ratio matching errors in the external resistors result in a degradation of the ability of the circuit to reject input common-mode signals, much the same as for a four-resistor difference amplifier made from a conventional op amp.

In addition, if the dc levels of the input and output common-mode voltages are different, matching errors result in a small differential-mode output offset voltage. For the G = 1 case, with a ground referenced input signal and the output common-mode level set for 2.5 V, an output offset of as much as 25 mV (1% of the difference in common-mode levels) can result if 1% tolerance resistors are used. Resistors of 1% tolerance result in a worst-case input CMRR of about 40 dB, worst-case differential mode output offset of 25 mV due to 2.5 V level-shift, and no significant degradation in output balance error.

For the best dc precision, use 0.1% accuracy resistors that are readily available in E96 values (1% steps).

## Calculating the Input Impedance of an Application

The effective input impedance of a circuit such as the one in Figure 15, at $+D_{IN}$ and $-D_{IN}$, depends on whether the amplifier is being driven by a single-ended or differential signal source. For balanced differential input signals, the input impedance ($R_{IN,\,dm}$) between the inputs ($+D_{IN}$ and $-D_{IN}$) is simply

$$R_{IN,dm} = 2R_G$$

In the case of a single-ended input signal (for example if $-D_{IN}$ is grounded and the input signal is applied to $+D_{IN}$) as shown in Figure 17. The $-D_{IN}$ is grounded, thus equation E4 is:

$$V_{-OUT} = \frac{-(+D_{IN})(1 - \beta_1)}{\beta_1 + \beta_2}$$

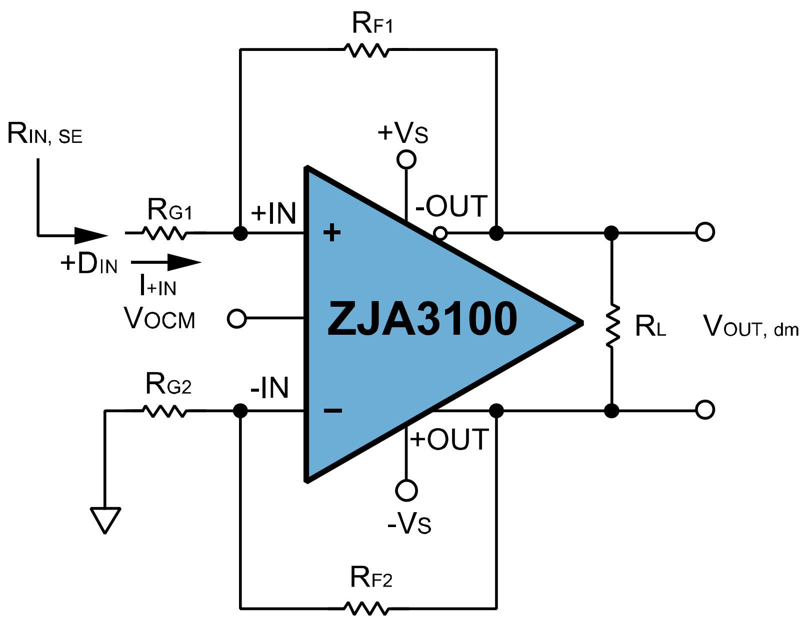


Figure 17. ZJA3100 with Unbalanced (Single-Ended) Input

The input impedance becomes

$$R_{IN,SE} = \frac{+D_{IN}}{I_{+IN}} = \frac{+D_{IN}}{(+D_{IN} - V_{-OUT}) \big/ (R_{G1} + R_{F1})} = R_{G1} \frac{\beta_1 + \beta_2}{\beta_1 (1 + \beta_2)}$$

For a balanced system where $R_{G1} = R_{G2} = R_G$ and $R_{F1} = R_{F2} = R_F$, the equations simplify to

$$R_{IN,SE} = \frac{R_G}{1 - \frac{R_F}{2(R_G + R_F)}} \qquad \text{(E6)}$$

The input impedance of the circuit is effectively higher than it would be for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistors $R_{G1}$ and $R_{G2}$.

## Input Common-mode Voltage Range

The input common-mode range at the summing nodes of the ZJA3100 is specified as ($-V_S$) – 0.4 V to ($+V_S$) – 1 V. By extending the input common-mode range down to ($-V_S$) – 0.4 V, the ZJA3100 is especially well suited to dc-coupled, single-ended-to-differential, and single-supply applications, such as ADC driving.

The ZJA3100 is optimized for level-shifting, ground-referenced input signals. For a single-ended input, this would imply, for example, that the voltage at $-D_{IN}$ in Figure 15 would be 0 V when the negative power supply voltage of the amplifier (at pin $-V_S$) is also set to 0 V.

## Setting the Output Common-mode Voltage

To ensure accurate control of the output common-mode level, the $V_{OCM}$ pin of the ZJA3100 should not be left open. An external low impedance voltage source, or resistor divider (made up of 10 kΩ resistors as shown in Figure 19), should be used. The output common-mode offset listed in the Specifications section assumes the $V_{OCM}$ input is driven by a low impedance voltage source.

  

## Driving a Capacitive Load

The capacitive load of an ADC or some other next-stage device is commonly required to be driven. However, a purely capacitive load can react with the pin and bond wire inductance of the ZJA3100, resulting in high frequency ringing in the pulse response. One way to minimize this effect is to place a small capacitor across each of the feedback resistors. The added capacitance should be small to avoid destabilizing the amplifier. An alternative technique is to place a small resistor in series with the outputs of the amplifier, as shown in Figure 18. Even when the small resistor is not required, good practice is to leave a place for them in a board layout (a 0 Ω value initially) for later adjustment in case the response appears unacceptable.

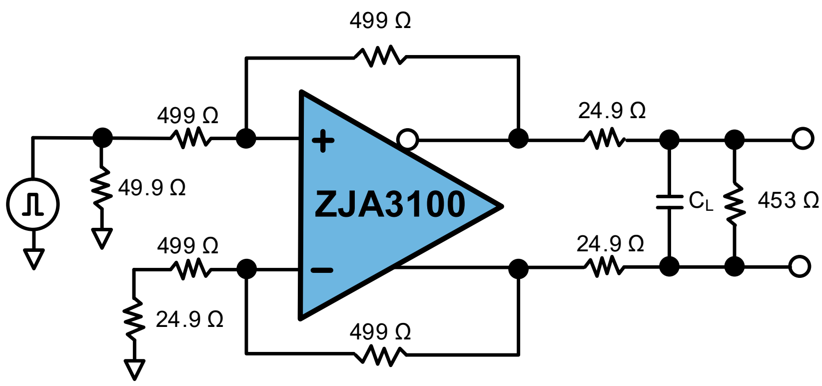


Figure 18. Test Circuit for Cap Load Drive

## Operating the Power Shutdown Feature

The wideband FDA requires external resistors for correct signal-path operation. When configured for the desired input impedance and gain setting with these external resistors, the amplifier can be controlled via the $\overline{PD}$ pin with a voltage threshold of

$$\frac{[(+V_S) + (-V_S)]}{2} + 0.7\ V$$

It can be turned off by asserting $\overline{PD}$ lower than the threshold. Disabling the amplifier shuts off the quiescent current and stops correct amplifier operation. The signal path is still present for the source signal through the external resistors, which provides poor signal isolation from the input to output in power-down mode.

An internal pullup resistor is provided on the $\overline{PD}$ pin so that ZJA3100's default state is power on. For applications simply requiring the device to be powered on when the supplies are present, tie the $\overline{PD}$ pin to the positive supply voltage.

## I/O Headroom Considerations

The starting point for most designs is to assign an output common-mode voltage for the ZJA3100. For accoupled signal paths, this voltage is often set to the midsupply voltage to retain the most available output swing around the voltage centered at the $V_{OCM}$ voltage. For dc-coupled designs, set this voltage with consideration to the required minimum headroom to the supplies. For precision ADC drivers, this output $V_{OCM}$ becomes the input $V_{CM}$ to the ADC. Often, $V_{CM}$ is set to $V_{REF}/2$ to center the differential input on the available input when precision ADCs are being driven.

From the target output $V_{OCM}$, the next step is to verify that the desired output differential peak-to-peak voltage ($V_{OPP}$) stays within the supplies. For any desired differential $V_{OPP}$, make sure that the absolute maximum voltage at the output pins swings within the supply rails minus the output headroom required for the rail-to-rail-output (RRO) device.

  

$$V_{Omax} = V_{OCM} + \frac{V_{OPP}}{4}$$

$$V_{Omin} = V_{OCM} - \frac{V_{OPP}}{4}$$

With the output headrooms confirmed, the input junctions must also stay within the operating range.

DC-coupled differential input designs must check the voltage divider from the source common-mode input voltage to the ZJA3100 $V_{OCM}$ setting. This result must be equal to an input $V_{ICM}$ within the specified range. If the source $V_{CM}$ can vary over some voltage range, validate this result over that range before proceeding.

For single-ended input to differential output designs, the $V_{ICM}$ is nominally at a voltage set by the external configuration with a small swing around the nominal value because of the common-mode loop. An ac-coupled, single-ended input to differential output design places an average input $V_{ICM}$ equal to the output $V_{OCM}$ for the FDA with an ac-coupled swing around the $V_{OCM}$ voltage following the input voltage. A dc-coupled, single-ended input to differential design gets a nominal input $V_{ICM}$ set by the source signal common-mode level and the $V_{OCM}$ output voltage with a small signal-related swing around the nominal $V_{ICM}$ voltage.

Taking a more complex example by using the ZJA3100 to attenuate a large bipolar input signal in a dc-coupled design for an ADC is shown in Figure 19. To remove the peaking for this low-noise gain design, the two $C_F$ elements and an input capacitor are added to shape the noise gain at high frequencies to a capacitive divider.

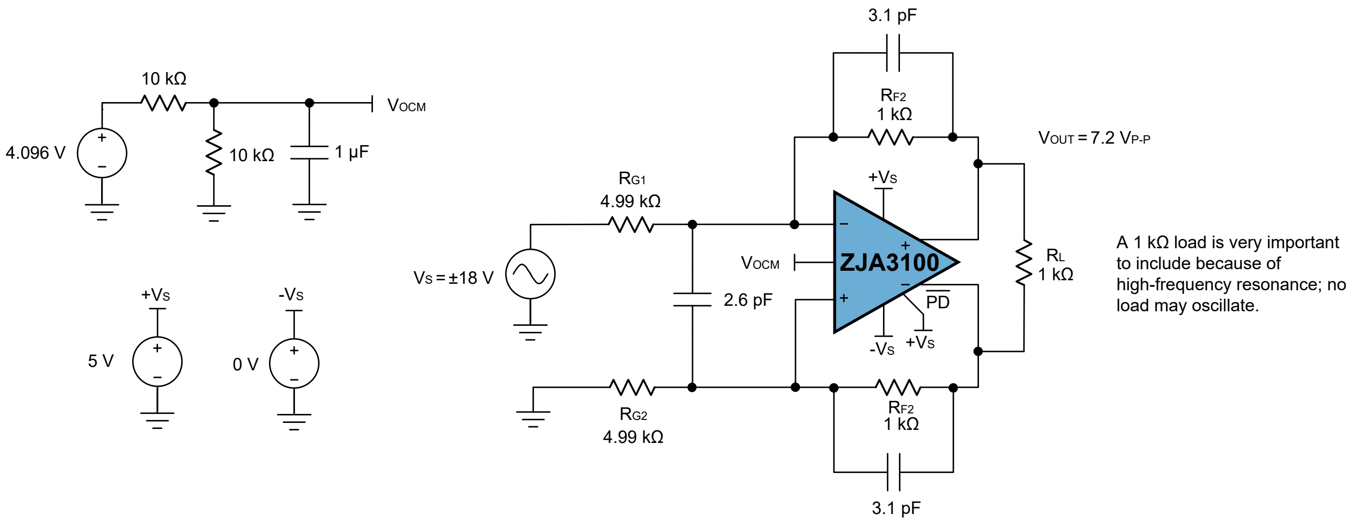


Figure 19. G = 0.2, DC-Coupled, Single-Ended to Differential Attenuator Design

In this example, the output $V_{OCM}$ is 4.096 V / 2, which equals 2.048 V and the source signal $V_{CM}$ is 0 V. These values set the nominal input pin $V_{ICM}$ to 2.048 V × 4.99 kΩ / (4.99 kΩ + 1 kΩ) = 1.71 V.

Applying a ±18 V input at the 4.99 kΩ input resistor produces a 7.2 $V_{P-P}$ differential output. That is, a ±1.8 V swing on the lower output side around the 2.048 V common-mode voltage. This 0.248 V to 3.84 V relative-to-ground swing at the output is well within the 0.2 V output headroom to the 5 V supply, but be careful if wide temperature range operation is required for the 0.25 V output to negative rail.

That output swing on the lower side produces an attenuated input common mode swing of (±1.8 V × (4.99 kΩ / (4.99 kΩ + 1 kΩ)) = ±1.5 V around the midscale input bias of 1.71 V. This 0.2 V to 3.2 V input common-mode swing is well within ZJA3100's -0.4 V to 4 V input range.

This ±18 V bipolar input signal is delivered to a SAR ADC with a 7.2 $V_{P-P}$ differential output with all I/O nodes operating in range using a single 5 V supply design. The source must sink the 2.048 V / 5.99 kΩ = 0.34 mA $V_{OCM}$ common-mode level-shifting current to take the input 0 V common-mode voltage up to the midscale 1.71 V $V_{ICM}$ operating voltage. Using the single-ended input impedance calculation by equation E6, the source must also drive an apparent input load of 5.44 kΩ.

Most designs do not run into an input range limit. However, using the approach shown in this section can allow a quick assessment of the input $V_{ICM}$ range under the intended full-scale output condition.

## Building Differential Filter

Creating an active first-order low-pass filter is easily accomplished by adding capacitors in the feedback loop, as shown in Figure 15. With balanced feedback, the transfer function is:

$$\frac{V_{OUT,dm}}{V_{IN,dm}} = \frac{R_F}{R_G} \times \frac{1}{1 + j2\pi f R_F C_F}$$

Multiple feedback (MFB) topology is used to create higher order filters and is easily adapted to fully-differential amplifiers as shown in Figure 20. A third-order filter is formed by adding $R_4$(s) and $C_3$ at the output.

Capacitors $C_2$ and $C_3$ can be placed differentially across the inputs and outputs as shown in solid lines. Alternatively, for better common-mode noise rejection, two capacitors of twice the value can be placed between each input or output and ground as shown in dashed lines.

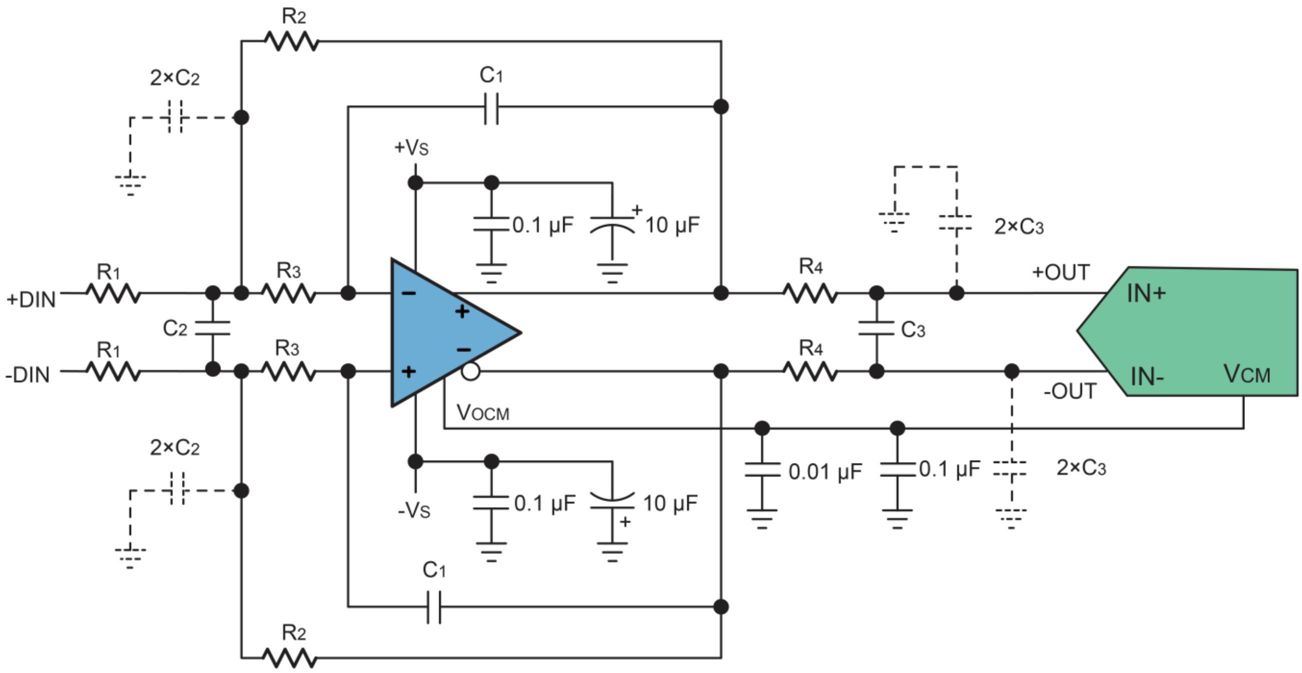


Figure 20. Third-Order Low-Pass Filter Driving an ADC

The transfer function for this filter circuit is:

$$\frac{V_{OUT,dm}}{V_{IN,dm}} = \left[ \frac{K}{-\left(\frac{f}{FSF \times f_c}\right)^2 + \frac{1}{Q}\frac{jf}{FSF \times f_c} + 1} \right] \times \frac{1}{1 + j2\pi f \times 2R_4C_3}$$

Where

$$K = \frac{R_2}{R_1}$$

$$FSF \times f_c = \frac{1}{2\pi\sqrt{2R_2R_3C_1C_2}}$$

$$Q = \frac{\sqrt{2R_2R_3C_1C_2}}{R_3C_1 + R_2C_1 + KR_3C_1}$$

K sets the pass-band gain, fc is the cutoff frequency of the filter, FSF is a frequency-scaling factor, and Q is the quality factor.

$$FSF = \sqrt{Re^2 + |Im|^2}$$

$$Q = \sqrt{Re^2 + |Im|^2/(2R_e)}$$

where Re is the real part, and Im is the imaginary part of the complex-pole pair. Setting $R_2 = R$, $R_3 = mR$, $C_1 = C$, and $C_2 = nC$, results in:

$$FSF \times f_c = \frac{1}{2\pi RC\sqrt{2nm}}$$

$$Q = \frac{\sqrt{2mn}}{1 + m(1 + K)}$$

It is easiest to start the design by choosing standard capacitor values for $C_1$ and $C_2$. This gives a value for n. Then determine if there is a value form that results in the required Q of the filter with the desired gain. If not, use another capacitor combination and try again. Once a suitable combination of m and n are found, use the value for C to calculate R based on the desired fc. It may take a few tries to obtain reasonable component values.

$R_4$ and $C_3$ are chosen to set the real pole in a third-order filter. Care should be exercised with setting this pole. Typically, $R_4$ is a low value (normally smaller than 100 Ω) and, at frequencies above the pole frequency, the series combination with $C_3$ loads the amplifier. The extra loading causes additional distortion in the amplifier's output. To avoid this, place the real pole at a higher frequency than the cutoff frequency of the complex pole pair.

If board space is not a constraint, multiple resistors or capacitors can be connected in series or parallel to achieve the desired calculated value.

To minimize noise in the filter design, consider using low-noise resistors like thin film, metal foil, or wire wound resistors.

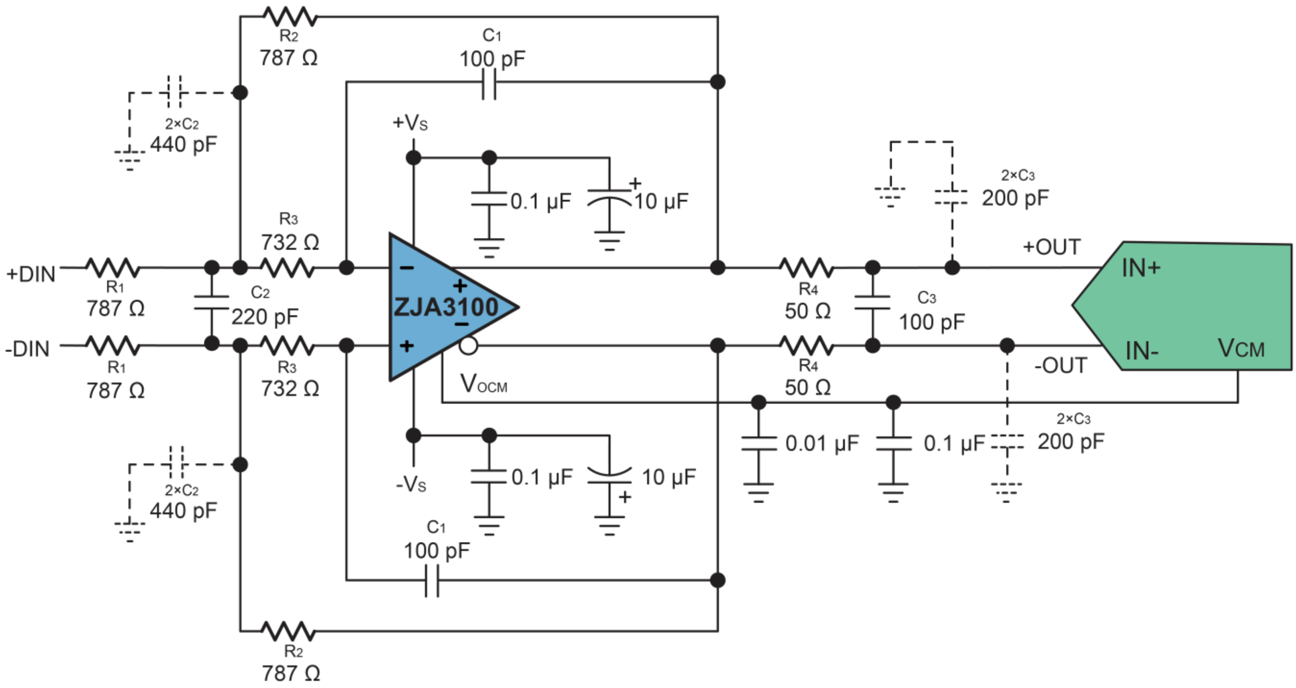


Figure 21. Third-Order 1 MHz Low-Pass Filter Example

Figure 21 shows a gain of 1, second-order Butterworth low-pass filter with corner frequency set at 1 MHz, and the real pole set by $R_4$ and $C_3$ at 15.9 MHz.

## Interfacing to High-Performance Precision ADCs

The ZJA3100 provides a simple interface to a wide variety of precision SAR and sigma-delta (Σ-Δ) ADCs. To deliver the exceptional distortion at the output pins, considerably wider bandwidth than what is typically required in the signal path to the ADC inputs is provided by the ZJA3100. This wide amplifier bandwidth provides the low broadband, closed-loop output impedance to supply the sampling glitches and to recover quickly for the best SFDR.

A particularly challenging task is to drive the high-frequency modulator sample rates for a precision Σ-Δ converter where the modulator frequency can be far higher than the final output data rate.

For SAR ADC drivers, noise, distortion, bandwidth, slew rate, and output drive capability are critical specifications. Since SAR ADCs are typically used in precision applications, the ZJA3100's precision performance, including offset voltage and its drift, is crucial for system performance. As demonstrated in Figure 22, the ZJC2000 (an 18-bit, 400 kSPS SAR ADC) combined with the ZJA3100 fully differential amplifier and the ZJM5400-4 delivers exceptional DC and AC performance across a wide temperature range of -40 °C to 125 °C.

  

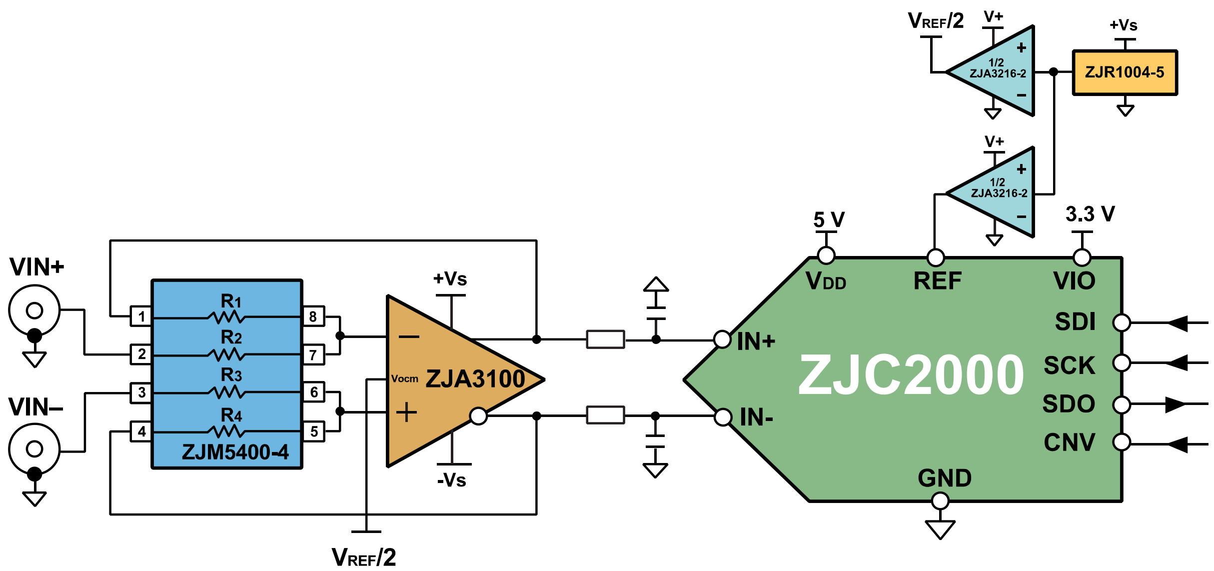


Figure 22. Using ZJA3100 with 18-bit SAR ADC ZJC2000

The ZJA3100 has also been verified to drive the ZJC2020, a 20-bit, 350 kSPS SAR ADC.

## Layout Guidelines

Similar to all high-speed devices, best system performance is achieved with close attention to board layout. General high-speed signal path layout suggestions include:

- Continuous ground planes are preferred for signal routing with matched impedance traces for longer runs; however, both ground and power planes must be opened up around the capacitive sensitive input and output device pins. When the signal goes to a resistor, parasitic capacitance becomes more of a band-limiting issue and less of a stability issue.
- Good high-frequency decoupling capacitors (0.1 μF) are required to a ground plane at the device power pins. Additional higher-value capacitors (2.2 μF) are also required but can be placed further from the device power pins and shared among devices. For best high-frequency decoupling, consider X2Y supply decoupling capacitors that offer a much higher self-resonance frequency over standard capacitors.
- Differential signal routing over any appreciable distance must use microstrip layout techniques with matched impedance traces.
- The input summing junctions are very sensitive to parasitic capacitance. Any $R_G$ elements must connect into the summing junction with minimal trace length to the device pin side of the resistor. The other side of the $R_G$ elements can have more trace length if needed to the source or to GND.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85 °C for 30 minutes is sufficient for most circumstances.

  

## Layout Example

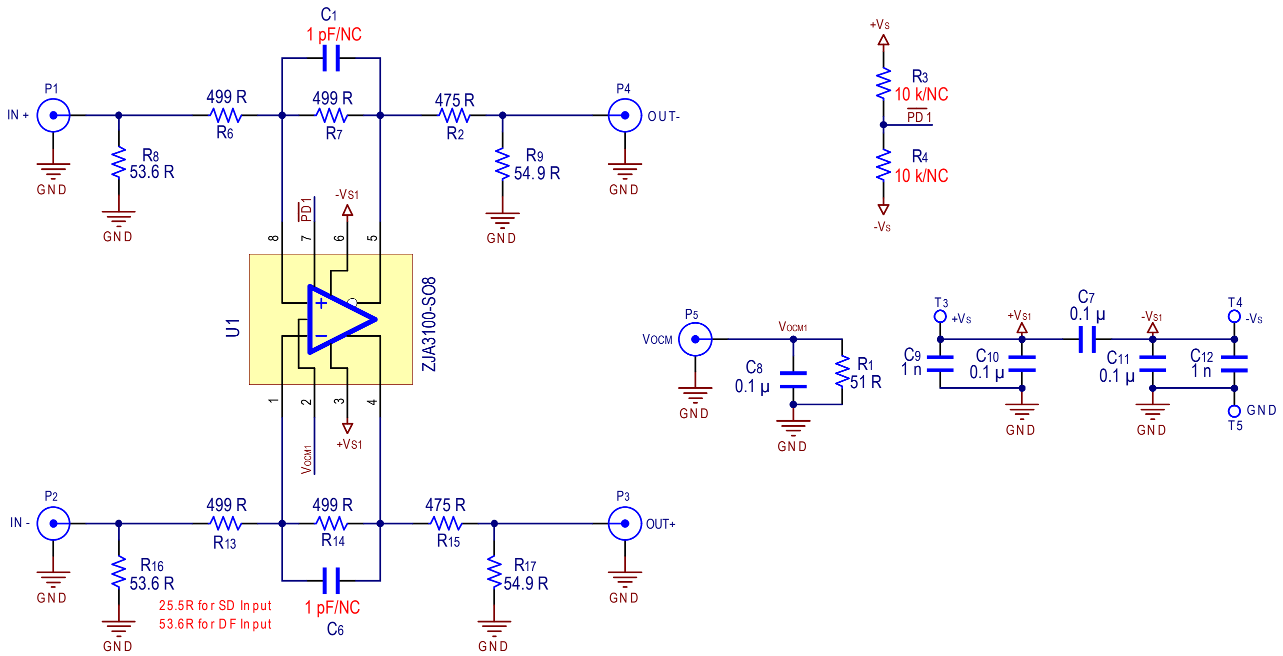


Figure 23. ZJA3100 Evaluation Board Schematic

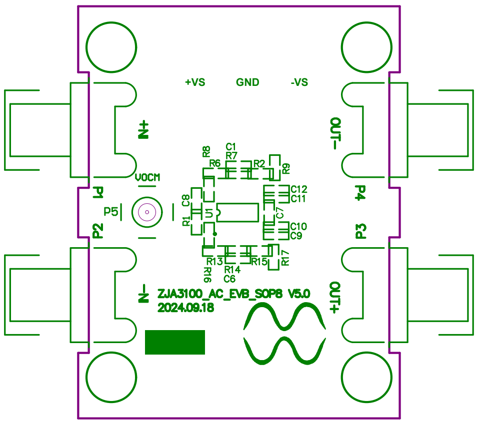


Figure 24. ZJA3100 Evaluation Board Top Silkscreen

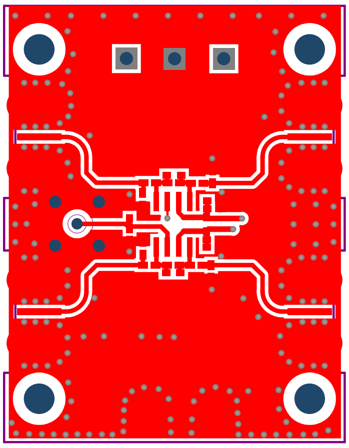

Figure 25. ZJA3100 Evaluation Board Layout (Top Layer)

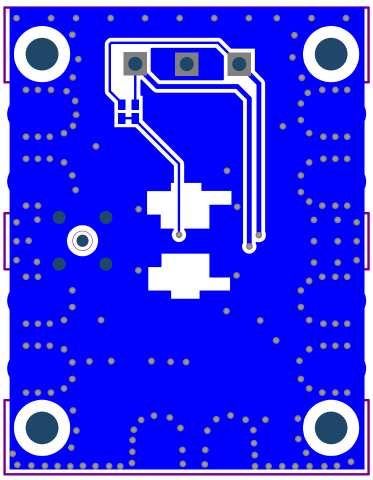

Figure 26. ZJA3100 Evaluation Board Layout (Bottom Layer)

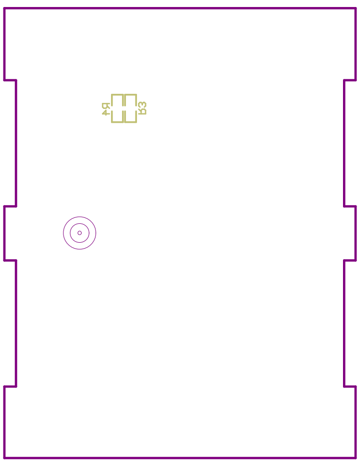

Figure 27. ZJA3100 Evaluation Board Bottom Silkscreen

## Outline Information

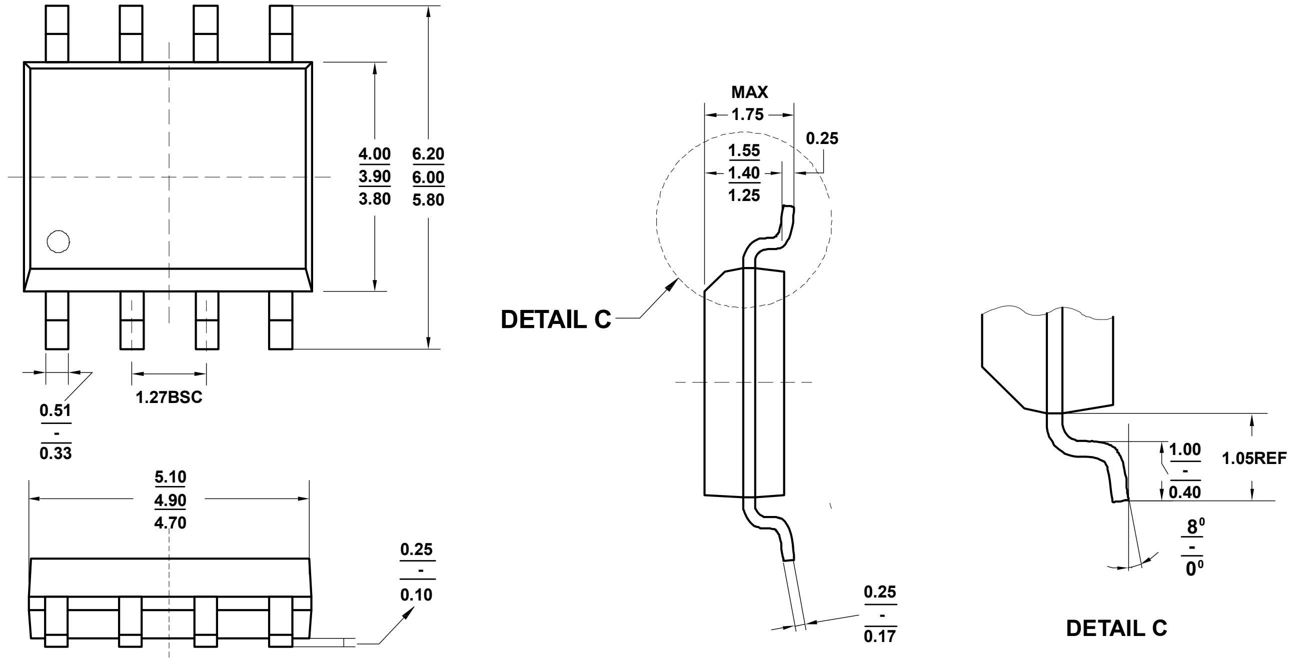


Figure 28. 8-Lead SOIC Package Dimensions shown in millimeters

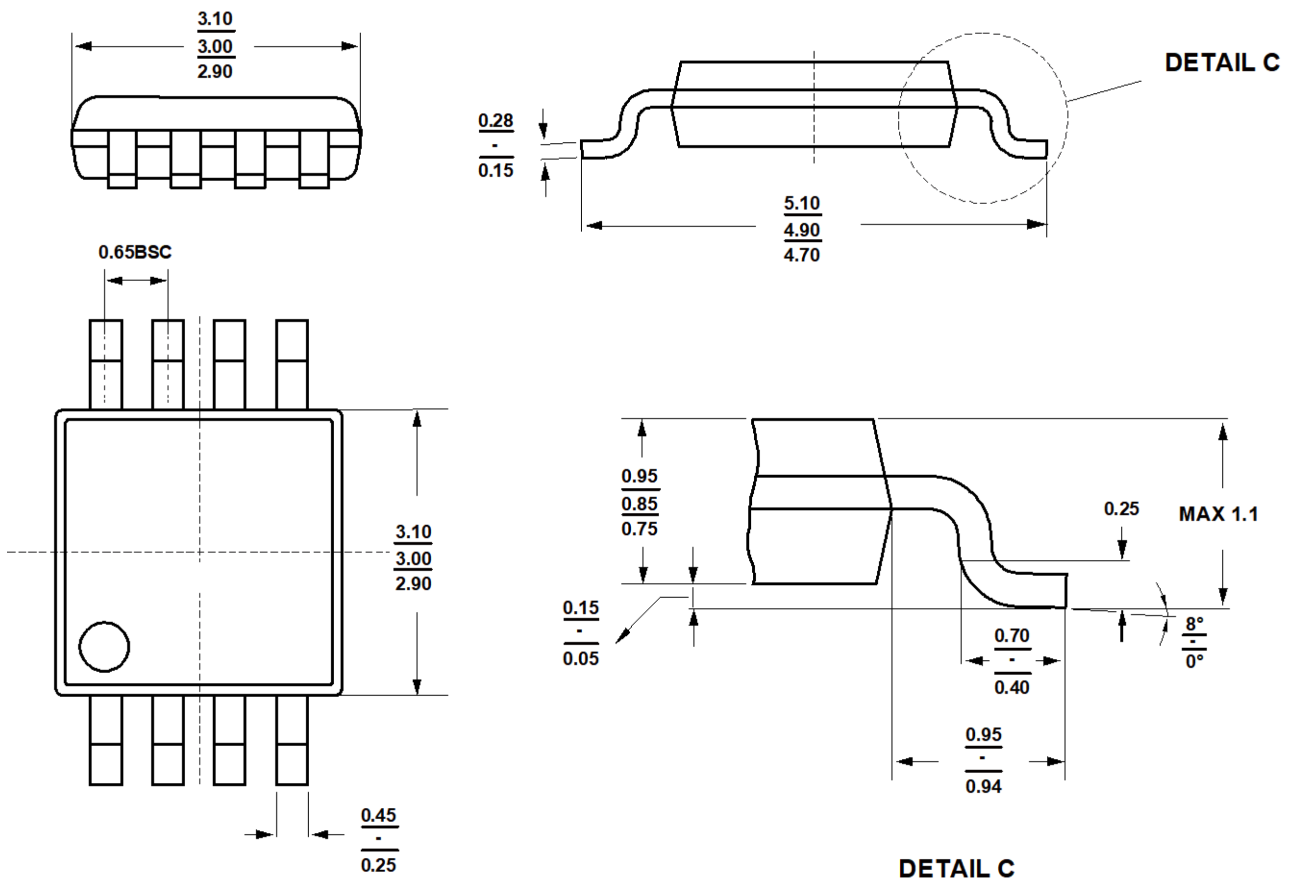


Figure 29. 8-Lead MSOP Package Dimensions shown in millimeters

  

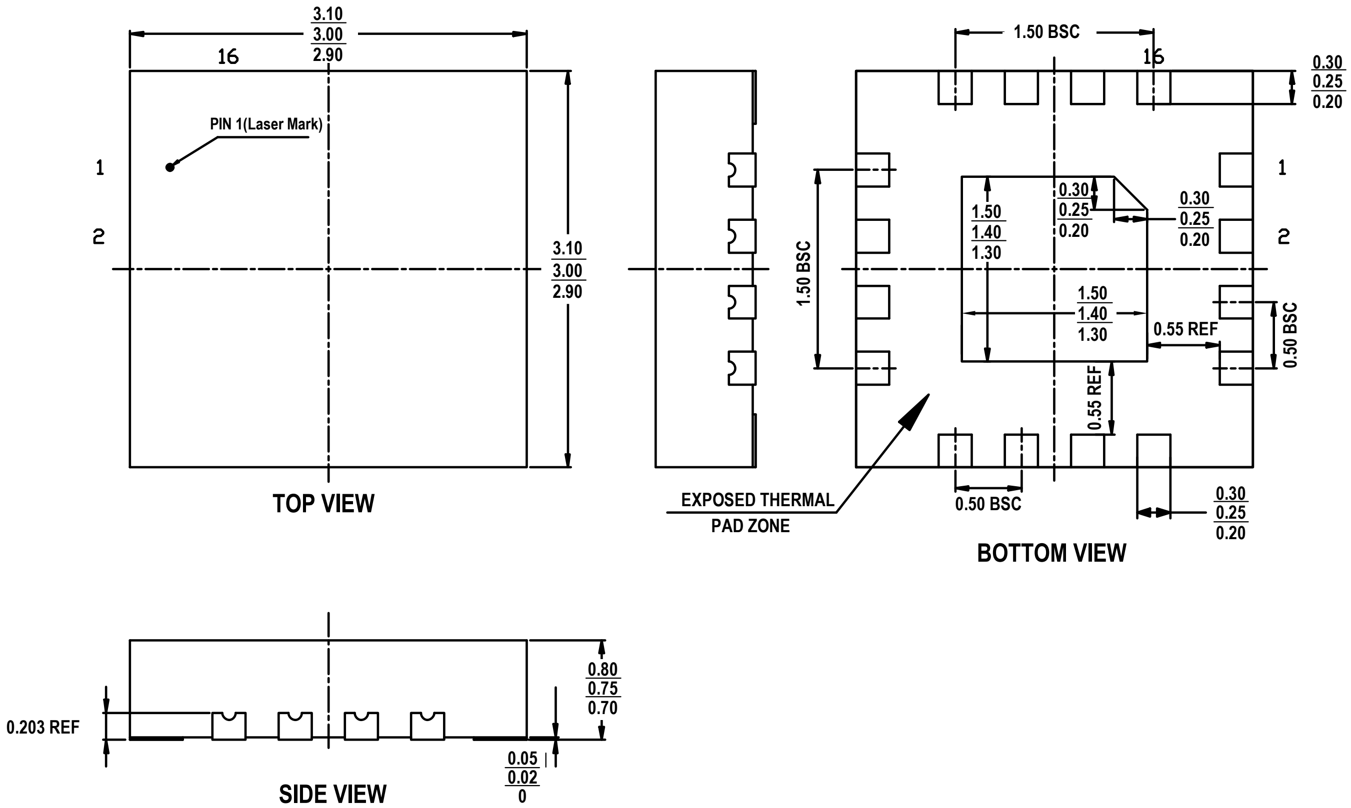


Figure 30. 16-Lead QFN Package Dimensions shown in millimeters

## Ordering Guide

<table>
<tr><th>Model</th><th>Orderable Device</th><th>Package</th><th>Vos (max) (μV)</th><th>Temperature Range (°C)</th><th>External Package</th></tr>
<tr><td rowspan="10">ZJA3100</td><td>ZJA3100BSABT</td><td rowspan="4">SOIC-8</td><td rowspan="2">50</td><td rowspan="10">-40 to +125</td><td>Tube</td></tr>
<tr><td>ZJA3100BSABR</td><td>13” Reel</td></tr>
<tr><td>ZJA3100ASABT</td><td rowspan="2">100</td><td>Tube</td></tr>
<tr><td>ZJA3100ASABR</td><td>13” Reel</td></tr>
<tr><td>ZJA3100BUABT</td><td rowspan="4">MSOP-8</td><td rowspan="2">50</td><td>Tube</td></tr>
<tr><td>ZJA3100BUABR</td><td>13” Reel</td></tr>
<tr><td>ZJA3100AUABT</td><td rowspan="2">100</td><td>Tube</td></tr>
<tr><td>ZJA3100AUABR</td><td>13” Reel</td></tr>
<tr><td>ZJA3100BTEBR</td><td rowspan="2">QFN-16</td><td>50</td><td rowspan="2">13” Reel</td></tr>
<tr><td>ZJA3100ATEBR</td><td>100</td></tr>
</table>

## Product Order Model

ZJXXXXX X X X X X Q1

- Q1: Automotive Grade
- External package: T=Tube; R=Reel
- Temperature range: A= -40°C to 125°C Automotive Grade 1; B= -40°C to 125°C; E= -40°C to 85°C
- Number of pins: R=3; K=5; T=6, A=8; B=10; D=14; E=16; P=20
- Package type: S=SOIC; U=MSOP, TSSOP, SOT (3 to 6 pins); T=DFN, QFN; K=SOT (8 pins)
- Grade: B grade is better than A grade
- Base: R=Voltage reference; A=Amplifier; C=Data Converter; G=Switches and Multiplexers, M=Others

## Related Parts

| Part Number | Description | Comments |
|---|---|---|
| **ADC** | | |
| ZJC2020 | 20-bit 350 kSPS SAR ADC | Fully differential input, SINAD 101.4 dB, THD -118 dB |
| ZJC2000/2010 | 18-bit 400 kSPS/200 kSPS SAR ADC | Fully differential input, SINAD 99.3 dB, THD -113 dB |
| ZJC2001/2011 | 16-bit 500 kSPS/250 kSPS SAR ADC | Fully differential input, SINAD 95.3 dB, THD -113 dB |
| ZJC2002/2012<br>ZJC2003/2013 | 16-bit 500 kSPS/250 kSPS SAR ADC | Pseudo-differential unipolar input, SINAD 91.7 dB, THD -105 dB<br>Pseudo-differential bipolar input, SINAD 91.7 dB, THD -105 dB |
| ZJC2004/2014<br>ZJC2005/2015 | 18-bit 400 kSPS/200 kSPS SAR ADC | Pseudo-differential unipolar input, SINAD 94.2 dB, THD -105 dB<br>Pseudo-differential bipolar input, SINAD 94.2 dB, THD -105 dB |
| ZJC2007/2017<br>ZJC2008/2018 | 14-bit 600 kSPS/300 kSPS SAR ADC | Pseudo-differential unipolar input, SINAD 85 dB, THD -105 dB<br>Pseudo-differential bipolar input, SINAD 85 dB, THD -105 dB |
| ZJC2009 | Small size, 12-bit 1 MSPS SAR ADC | Single-ended input, SOT23-6, 2.3 V to 5 V, SINAD 73 dB, THD -89 dB |
| ZJC2100/1-18<br>ZJC2100/1-16 | 18-bit 400 kSPS/200 kSPS 4-ch differential SAR ADC, SINAD 99.3 dB, THD -113 dB<br>16-bit 500 kSPS/250 kSPS 4-ch differential SAR ADC, SINAD 95.3 dB, THD -113 dB | |
| ZJC2102/3-18<br>ZJC2102/3-16<br>ZJC2102/3-14 | 18-bit 400 kSPS/200 kSPS 8-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB<br>16-bit 500 kSPS/250 kSPS 8-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB<br>14-bit 600 kSPS/300 kSPS 8-ch pseudo-differential SAR ADC, SINAD 85 dB, THD -105 dB | |
| ZJC2104/5-18<br>ZJC2104/5-16 | 18-bit 400 kSPS/200 kSPS 4-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB<br>16-bit 500 kSPS/250 kSPS 4-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB | |
| **DAC** | | |
| ZJC2541-18/16/14<br>ZJC2543-18/16/14 | 18/16/14-bit 1 MSPS single channel DAC with unipolar output | Power on reset to 0 V (ZJC2541) or $V_{REF}/2$ (ZJC2543), 1 nV-S glitch, SOIC-8, MSOP-10/8, DFN-10 packages |
| ZJC2542-18/16/14<br>ZJC2544-18/16/14 | 18/16/14-bit 1 MSPS single channel DAC with bipolar output | Power on reset to 0 V (ZJC2542) or $V_{REF}/2$ (ZJC2544), 1 nV-S glitch, SOIC-14, TSSOP-16, QFN 16 packages |
| **Amplifier** | | |
| ZJA3000-1/2/4<br>ZJA3001-1/2/4 | Single/Dual/Quad 36 V low bias current precision Op Amps | 3 MHz, 35 µV max Vos, 0.5 µV/°C max TCVos, 25 pA max Ibias, 1 mA/ch, input to V- (ZJA3000 only), RRO, 4.5 V to 36 V |
| ZJA3018-2<br>ZJA3008-2 | OVP ±75 V, 36 V, Low Power, High Precision Op Amp<br>36 V, Low Power, High Precision Op Amp | 1.3 MHz, 10 µV max Vos, 0.5 µV/°C max TCVos, 25 pA max Ibias, 0.5 mA/ch, OVP ±75 V (ZJA3018 only), RRO, 4.5 V to 36 V |
| ZJA3512-2 | Dual 36 V 7 MHz precision JFET Op Amps | 7 MHz, 35 V/µS, 50 µV max Vos, 1 µV/°C max TCVos, 2 mA/ch, RRO, 9 V to 36 V |
| ZJA3206/06/02-1/2 | Precision 24/11.6/5.3 MHz CMOS RRIO Op Amps | 24/11.6/5.3 MHz, RRIO, 30 µV max Vos, 1 µV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V |
| ZJA3600/1 | 36 V ultra-high precision in-amp | CMRR 105 dB min (G = 1), 25 pA max Ib, 25 µV max Vosi, ±2.4 V to ±18 V, -40 °C to 125 °C |
| ZJA3611, ZJA3609 | 36 V precision wider bandwidth precision in-amp (G ≥ 10) | CMRR 120 dB min (G = 10), 25 pA max Ibias, 25 µV max Vosi, 1.2 MHz BW (G = 10) |
| ZJA3676/7<br>ZJA3678/9 | Low power, G = 1 Single/Dual 36 V difference amplifier<br>Low power, G = 0.5/2 Single/Dual 36 V difference amplifier | Input protection to ±65 V, CMRR 104 dB min (G = 1), Vos 100 µV max, gain error 15 ppm max, 500 kHz BW (G = 1), 330 µA/channel, 2.7 V to 36 V |
| ZJA3669 | High Common-Mode Voltage Difference Amplifier | ±270 V CMV, 2.5 kV ESD, 96 dB min CMRR, 450 kHz BW, 4 V to 36 V, SOIC-8 |
| ZJA3100 | 15 V precision fully differential amplifier | 145 MHz, 447 V/µS, 50 nS to 16-bit, 50 µV max Vos, 4.6 mA Iq, SOIC/MSOP-8, QFN-16 |
| ZJA3236/26/22-2 | Low-cost 22/10/5 MHz CMOS RRIO Op Amps | 22/11/5 MHz, RRIO, 2 mV max Vos, 6 µV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V |
| ZJA3622/8 | 36 V low-cost precision in-amp | 0.5 nA max Ibias, 125 µV max Vosi, 625 kHz BW (G = 10), 3.3 mA Iq, ±2.4 V to ±18 V |
| **Voltage Reference** | | |
| ZJR1004 | 40 V supply precision voltage reference | $V_{OUT}$ = 2.048/2.5/3/3.3/4.096/5/10 V, 5 ppm/°C max drift -40 °C to 125 °C |
| ZJR1001/2<br>ZJR1003 | 5.5 V low power voltage reference (ZJR1001 with noise filter option) | $V_{OUT}$ = 2.048/2.5/3/3.3/4.096/5 V, 5 ppm/°C max drift -40 °C to 125 °C, ±0.05% initial error, 130 µA, ZJR1001/2 in SOT23-6, ZJR1003 in SOIC/MSOP-8 |
| ZJR1302 | 5.5 V low power compact precision voltage reference | $V_{OUT}$ = 2.048/2.5/3/3.3/4.096 V, 30 ppm/°C max drift -40 °C to 125 °C, 130 µA, SOT23-3 |
| **Switches and Multiplexers** | | |
| ZJG4438/4439 | 36 V fault protection 8:1/dual 4:1 multiplexer | Protection to ±50 V power on & off, latch-up immune, Ron 270 Ω, 14.8 pC, $t_{ON}$ 166 nS |
| ZJG4428/4429 | 36 V 8:1/dual 4:1 multiplexer | Latch-up immune, Ron 270 Ω, 14.8 pC charge injection, $t_{ON}$ 166 nS |
| **Quad Matching Resistor** | | |
| ZJM5400 | ±75 V precision match resistors | Mismatch < 100 ppm, 10k:10k:10k:10k, 100k:100k:100k:100k, 100k:10k:10k:100k, 1k:1k:1k:1k, 1M:1M:1M:1M, 5k:1k:1k:5k, 5k:1.25k:1.25k:5k, 9k:1k:1k:9k, ESD: 3.5 kV |