

Silicon Carbide Power MOSFET N-Channel Enhancement Mode

Features

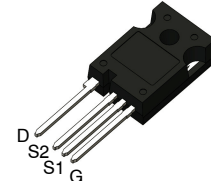
- C3M™ Silicon Carbide (SiC) MOSFET technology
- Optimized package with separate driver source pin
- 8mm of creepage distance between drain and source
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant

Typical Applications

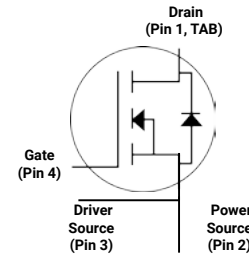
- EV chargers
- Server & Telecom PSU
- UPS
- Solar inverters
- SMPS
- DC/DC converters

Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency



TO-247-4L



ORDERING INFORMATION

HT52N650AKZ

$T_A = -40^\circ$ to 175° C for all packages

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			650	V	$T_c = 25^\circ\text{C}$	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+19		Transient	
Operational Gate-Source Voltage	V_{GSop}		-4/15			Static	Note 1
DC Continuous Drain Current	I_D			52	A	$V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}, T_J \leq 175^\circ\text{C}$	Fig. 19 Note 2
				35		$V_{GS} = 15\text{ V}, T_c = 100^\circ\text{C}, T_J \leq 175^\circ\text{C}$	
Pulsed Drain Current	I_{DM}			132		t_{Pmax} limited by T_{Jmax} $V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}$	Fig. 22
Power Dissipation	P_D			176	W	$T_c = 25^\circ\text{C}, T_J = 175^\circ\text{C}$	Fig. 20
Operating Junction and Storage Temperature	T_J, T_{stg}			-40 to +175	$^\circ\text{C}$		
Solder Temperature	T_L			260		According to JEDEC J-STD-020	
Mounting Torque	M_D			1 8.8	Nm lbf-in	M3 or 6-32 screw	

Note (1): Recommended turn-on gate voltage is 15V with $\pm 5\%$ regulation tolerance, see Application Note PRD-04814 for additional details

Note (2): Verified by design

Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Note
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.6	3.6	V	$V_{DS} = V_{GS}, I_D = 4.84 \text{ mA}$	Fig. 11
		—	2.2	—		$V_{DS} = V_{GS}, I_D = 4.84 \text{ mA}, T_J = 175^\circ\text{C}$	
Zero Gate Voltage Drain Current	I_{DSS}	—	1	50	μA	$V_{DS} = 650 \text{ V}, V_{GS} = 0 \text{ V}$	
Gate-Source Leakage Current	I_{GSS}	—	10	250	nA	$V_{GS} = 15 \text{ V}, V_{DS} = 0 \text{ V}$	
Drain-Source On-State Resistance	$R_{DS(on)}$	—	45	60	m Ω	$V_{GS} = 15 \text{ V}, I_D = 17.6 \text{ A}$	Fig. 4, 5, 6
		—	61	—		$V_{GS} = 15 \text{ V}, I_D = 17.6 \text{ A}, T_J = 175^\circ\text{C}$	
Transconductance	g_{fs}	—	12	—	S	$V_{DS} = 20 \text{ V}, I_{DS} = 17.6 \text{ A}$	Fig. 7
		—	11	—		$V_{DS} = 20 \text{ V}, I_{DS} = 17.6 \text{ A}, T_J = 175^\circ\text{C}$	
Input Capacitance	C_{iss}	—	1621	—	pF	$V_{GS} = 0 \text{ V}, V_{DS} = 0 \text{ V to } 600 \text{ V}$ $f = 1 \text{ Mhz}$ $V_{AC} = 25 \text{ mV}$	Fig. 17, 18
Output Capacitance	C_{oss}	—	101	—			
Reverse Transfer Capacitance	C_{rss}	—	8	—			
Effective Output Capacitance (Energy Related)	$C_{o(er)}$	—	126	—		$V_{GS} = 0 \text{ V}, V_{DS} = 0 \text{ V to } 400 \text{ V}$	Note 3
Effective Output Capacitance (Time Related)	$C_{o(tr)}$	—	178	—			
Output Capacitance Stored Energy	E_{oss}	—	20	—	μJ	$V_{DS} = 600 \text{ V}, f = 1 \text{ Mhz}$	Fig. 16
Turn-On Switching Energy (Body Diode)	E_{on}	—	57	—		$V_{DS} = 400 \text{ V}, V_{GS} = -4 \text{ V}/15 \text{ V}, I_D = 17.6 \text{ A},$ $R_{G(ext)} = 2.5 \Omega, L = 99 \mu\text{H}, T_J = 175^\circ\text{C}$ FWD = Internal Body Diode of MOSFET	Fig. 25
Turn Off Switching Energy (Body Diode)	E_{off}	—	14	—			
Turn-On Switching Energy (External Diode)	E_{on}	—	44	—			
Turn Off Switching Energy (External Diode)	E_{off}	—	14	—		$V_{DS} = 400 \text{ V}, V_{GS} = -4 \text{ V}/15 \text{ V}, I_D = 17.6 \text{ A},$ $R_{G(ext)} = 2.5 \Omega, L = 99 \mu\text{H}, T_J = 175^\circ\text{C}$ FWD = External SiC DIODE	
Turn-On Delay Time	$t_{d(on)}$	—	9	—	ns	$V_{DD} = 400 \text{ V}, V_{GS} = -4 \text{ V}/15 \text{ V}$ $I_D = 17.6 \text{ A}, R_{G(ext)} = 2.5 \Omega, L = 99 \mu\text{H}$ Timing relative to V_{DS} Inductive load	Fig. 26
Rise Time	t_r	—	12	—			
Turn-Off Delay Time	$t_{d(off)}$	—	18	—			
Fall Time	t_f	—	6	—			
Internal Gate Resistance	$R_{G(int)}$	—	3	—	Ω	$f = 1 \text{ MHz}, V_{AC} = 25 \text{ mV}$	
Gate to Source Charge	Q_{gs}	—	21	—	nC	$V_{DS} = 400 \text{ V}, V_{GS} = -4 \text{ V}/15 \text{ V}$ $I_D = 17.6 \text{ A}$ Per IEC60747-8-4 pg 21	Fig. 12
Gate to Drain Charge	Q_{gd}	—	18	—			
Total Gate Charge	Q_g	—	63	—			

Note:

³ $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

$C_{o(tr)}$, a lumped capacitance that gives same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Reverse Diode Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Notes
Diode Forward Voltage	V_F	4.8	—	V	$V_{GS} = -4\text{ V}, I_{SD} = 8.8\text{ A}, T_J = 25^\circ\text{C}$	Fig. 8, 9, 10
		4.2	—		$V_{GS} = -4\text{ V}, I_{SD} = 8.8\text{ A}, T_J = 175^\circ\text{C}$	
Continuous Diode Forward Current	I_S	—	29	A	$V_{GS} = -4\text{ V}, T_c = 25^\circ\text{C}$	
Diode Pulse Current	I_{SM}	—	132		$V_{GS} = -4\text{ V}$, pulse width t_p limited by $T_{j\max}$	
Reverse Recovery Time,	t_{rr}	13	—	ns	$V_{GS} = -4\text{ V}, I_{SD} = 17.6\text{ A}, V_R = 400\text{ V}$ $di_p/dt = 5215\text{ A}/\mu\text{s}, T_J = 175^\circ\text{C}$	
Reverse Recovery Charge	Q_{rr}	247	—	nC		
Peak Reverse Recovery Current	I_{RRM}	36	—	A		
Reverse Recovery Time,	t_{rr}	18	—	ns	$V_{GS} = -4\text{ V}, I_{SD} = 17.6\text{ A}, V_R = 400\text{ V}$ $di_p/dt = 1775\text{ A}/\mu\text{s}, T_J = 175^\circ\text{C}$	
Reverse Recovery Charge	Q_{rr}	171	—	nC		
Peak Reverse Recovery Current	I_{RRM}	16	—	A		

Thermal Characteristics

Parameter	Symbol	Typ.	Unit	Note
Thermal Resistance from Junction to Case	$R_{\theta JC}$	0.85	$^\circ\text{C}/\text{W}$	Fig. 21
Thermal Resistance From Junction to Ambient	$R_{\theta JA}$	40		

Typical Performance

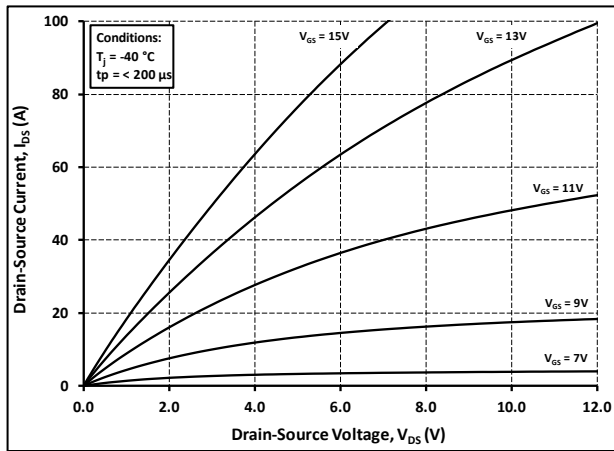


Figure 1. Output Characteristics $T_j = -40^{\circ}\text{C}$

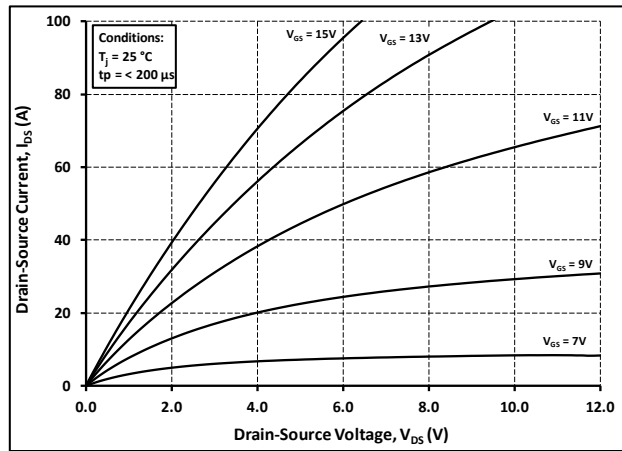


Figure 2. Output Characteristics $T_j = 25^{\circ}\text{C}$

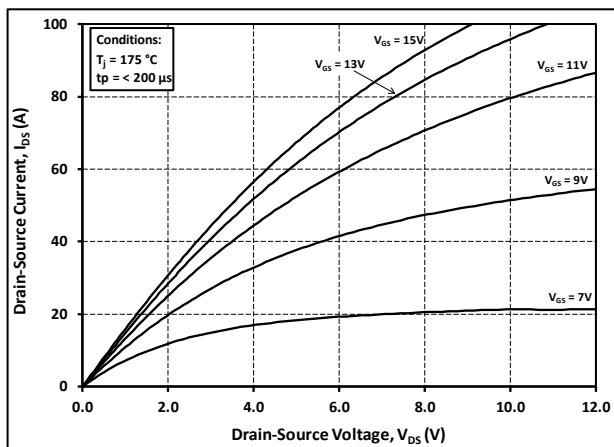


Figure 3. Output Characteristics $T_j = 175^{\circ}\text{C}$

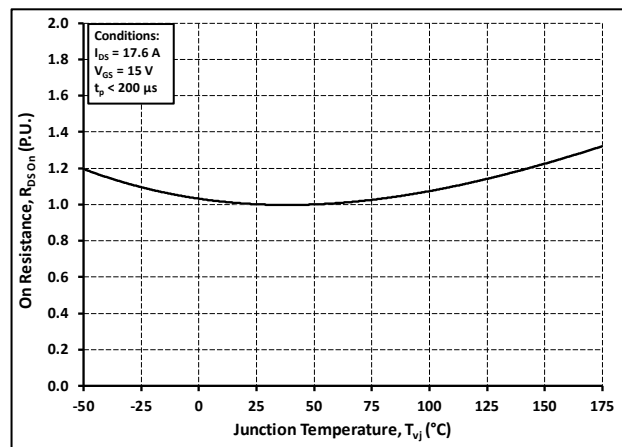


Figure 4. Normalized On-Resistance vs. Temperature

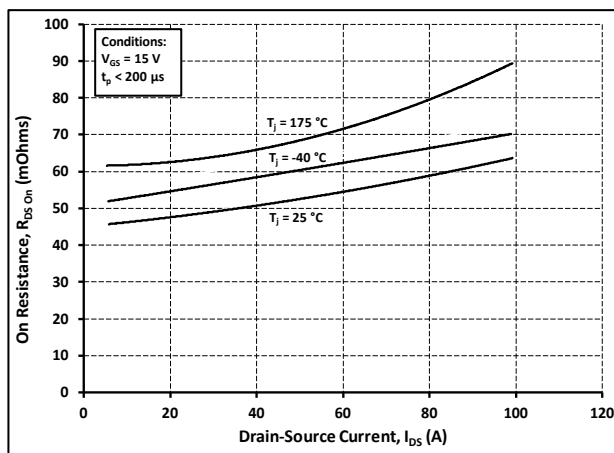


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

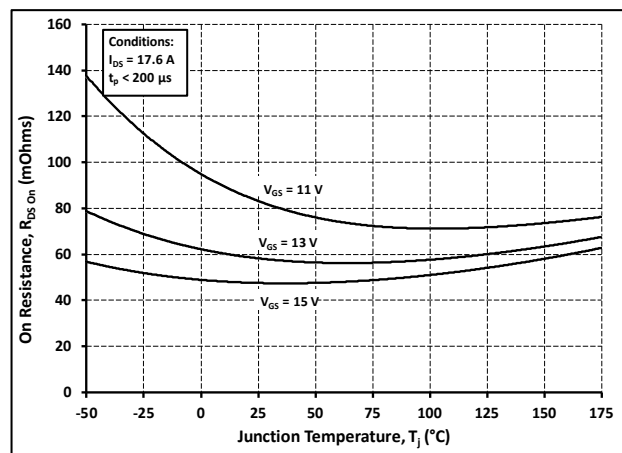


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

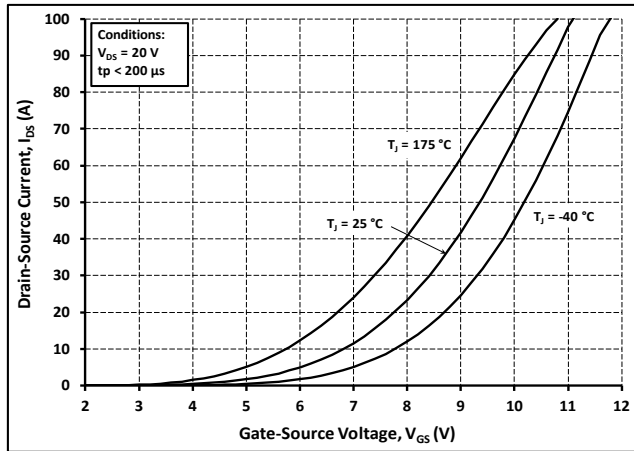


Figure 7. Transfer Characteristic for Various Junction Temperatures

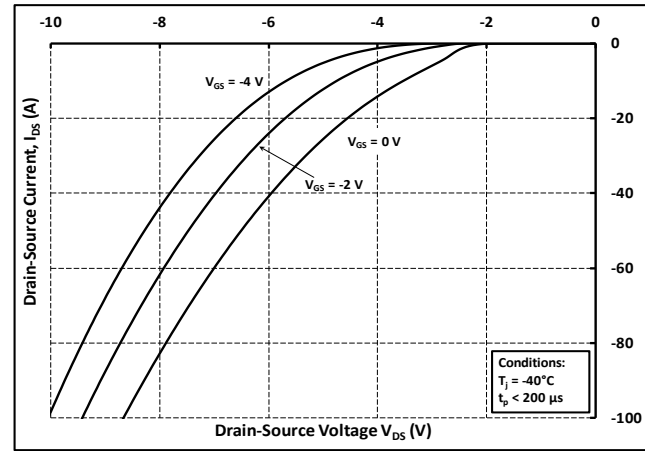


Figure 8. Body Diode Characteristic at -40 °C

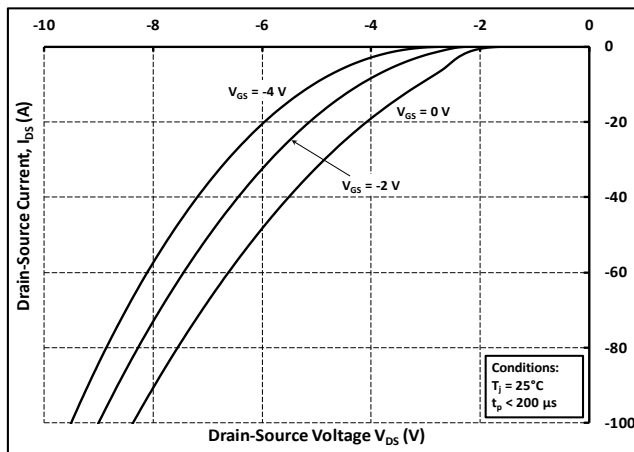


Figure 9. Body Diode Characteristic at 25 °C

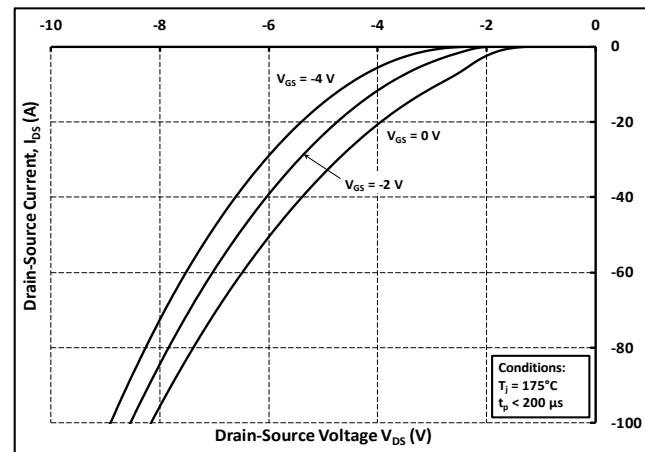


Figure 10. Body Diode Characteristic at 175 °C

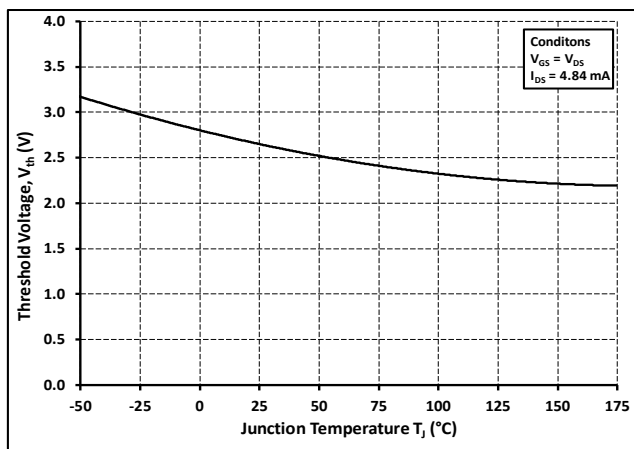


Figure 11. Threshold Voltage vs. Temperature

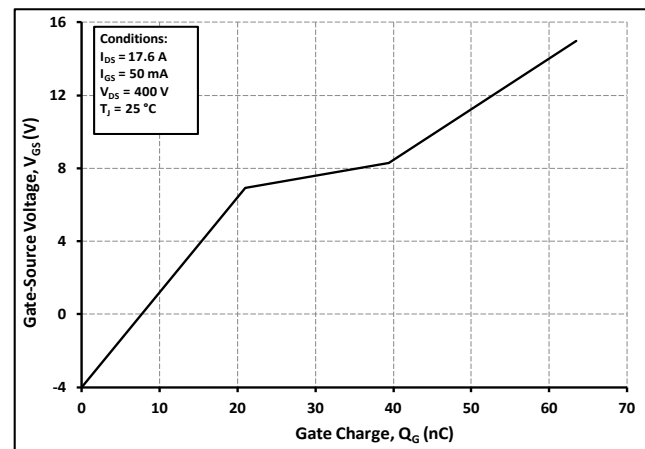


Figure 12. Gate Charge Characteristics

Typical Performance

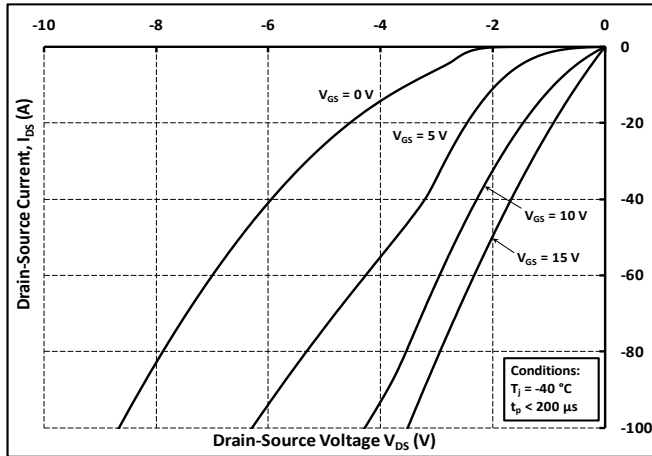


Figure 13. 3rd Quadrant Characteristic at -40°C

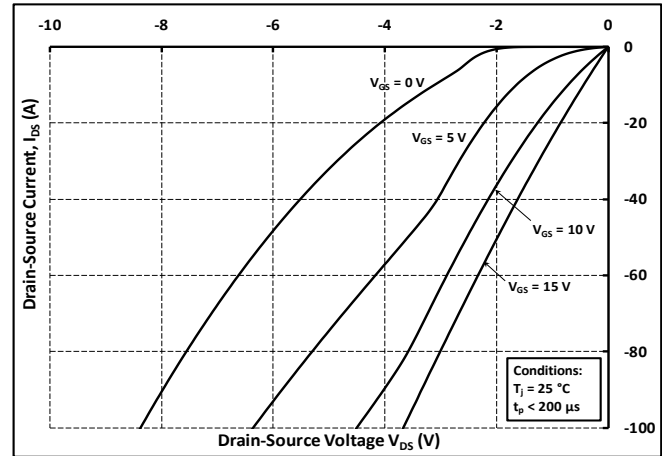


Figure 14. 3rd Quadrant Characteristic at 25°C

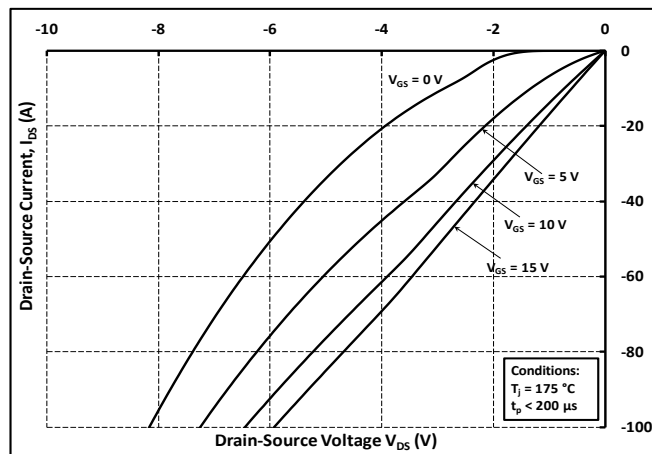


Figure 15. 3rd Quadrant Characteristic at 175°C

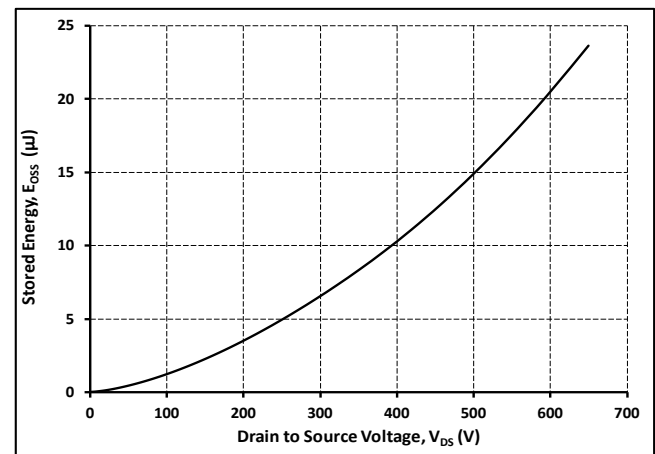


Figure 16. Output Capacitor Stored Energy

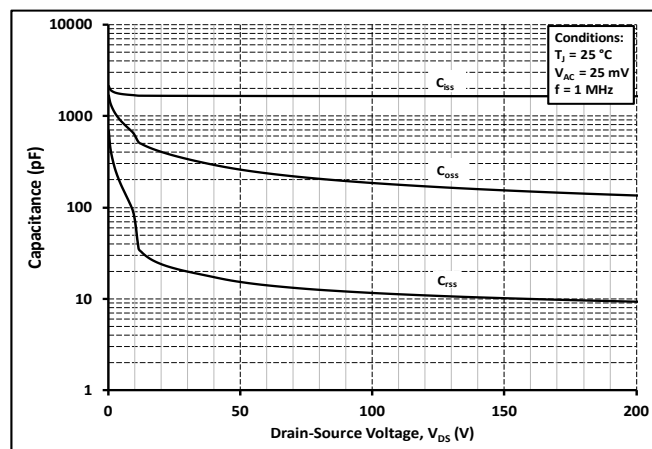


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

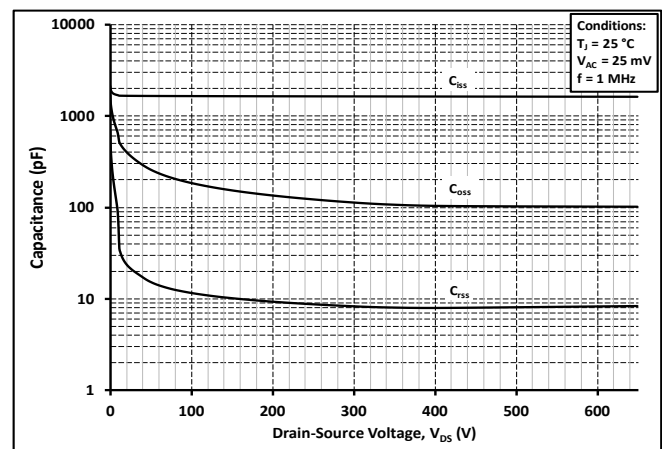


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 650V)

Typical Performance

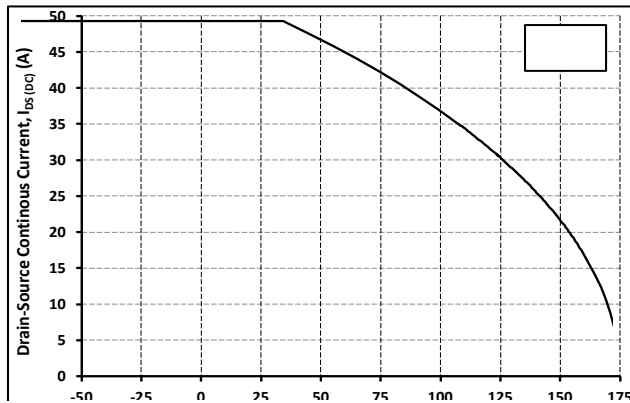


Figure 19. Continuous Drain Current Derating vs. Case Temperature

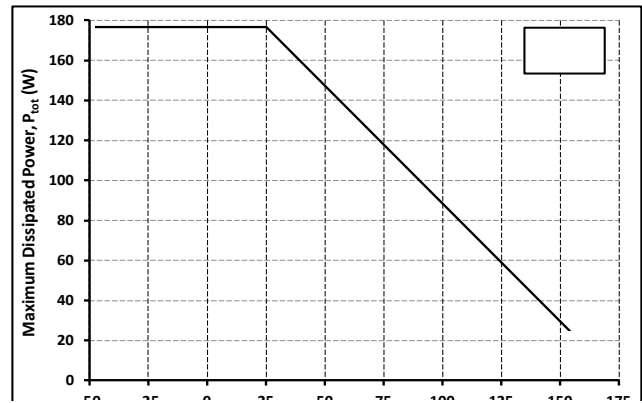


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

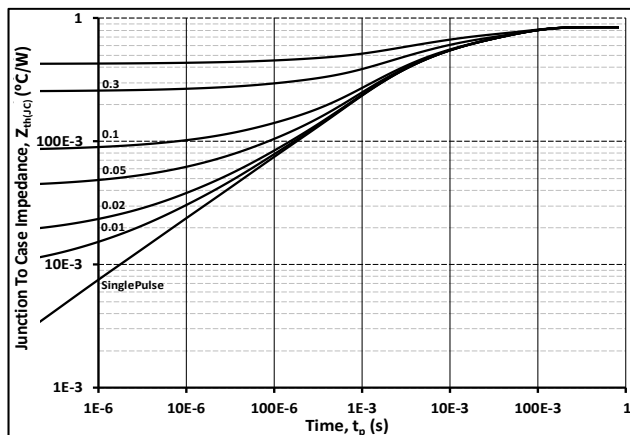


Figure 21. Transient Thermal Impedance (Junction - Case)

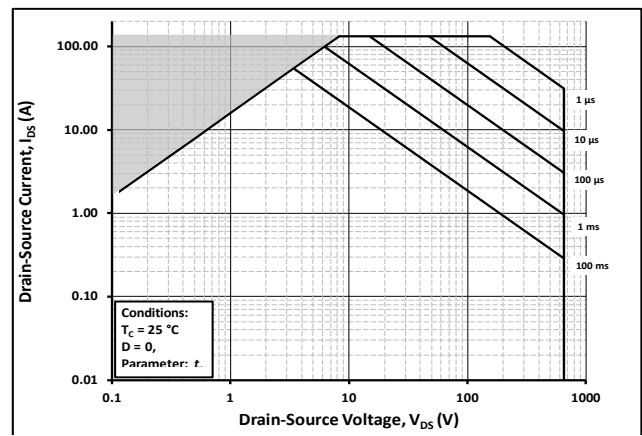


Figure 22. Safe Operating Area

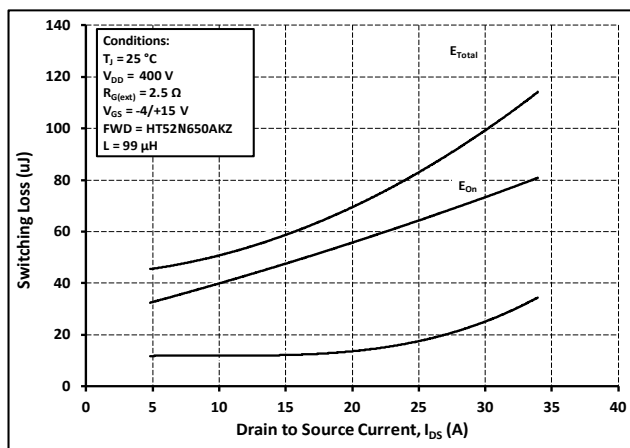


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 400V$)

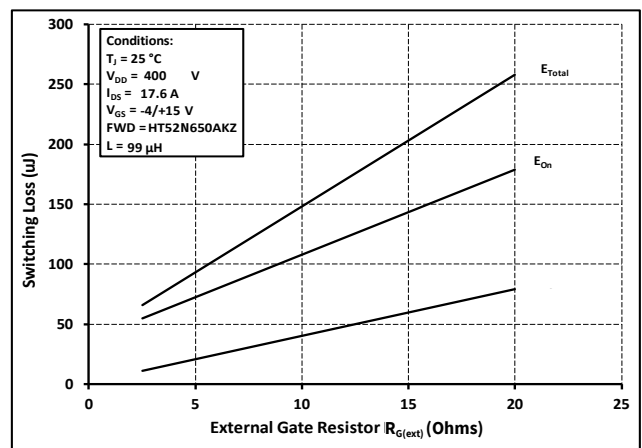


Figure 24. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

Typical Performance

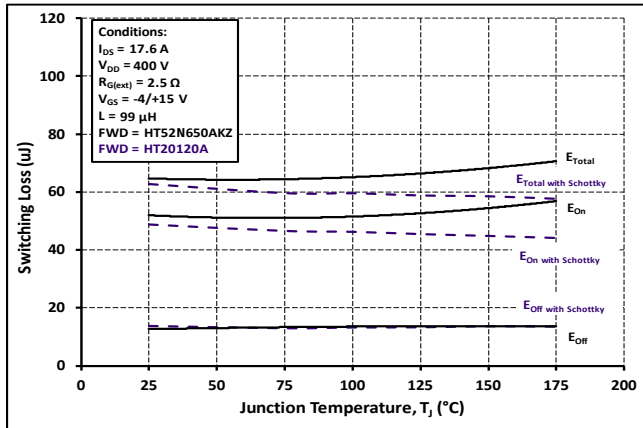


Figure 25. Clamped Inductive Switching Energy vs. Temperature

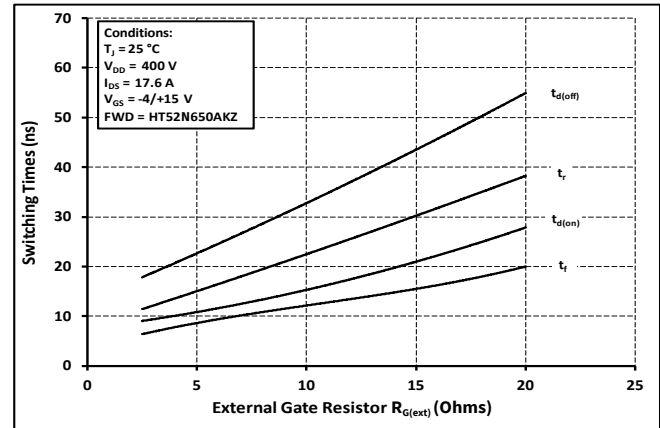


Figure 26. Switching Times vs. $R_{G(ext)}$

Test Circuit Schematic

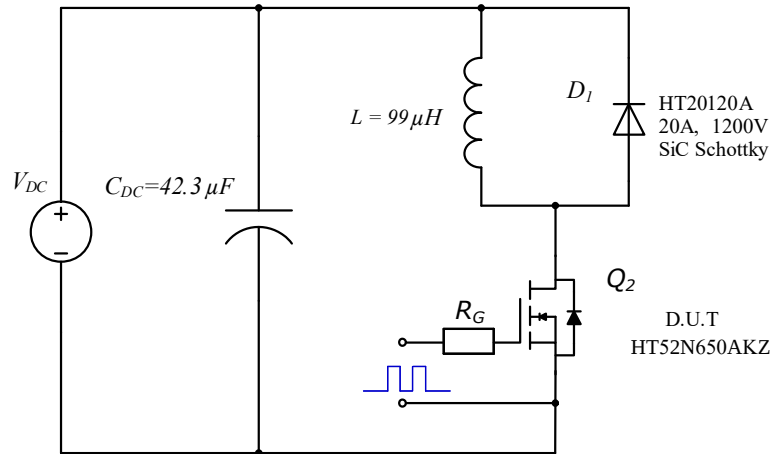


Figure 27. Clamped Inductive Switching Waveform Test Circuit

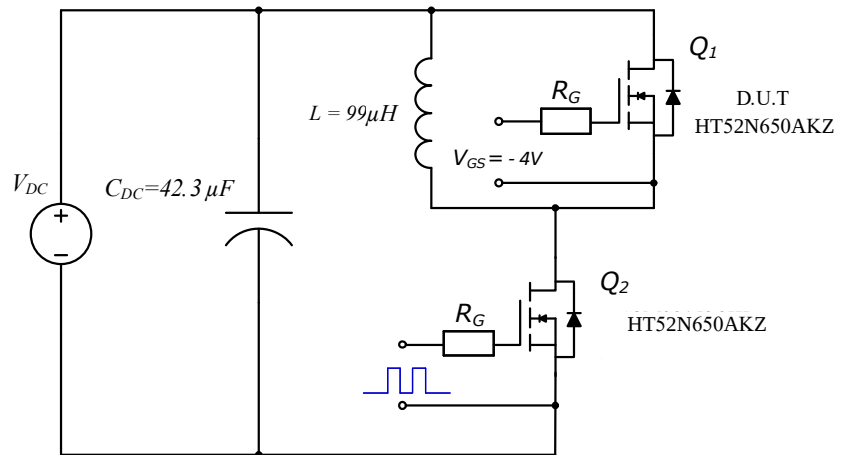
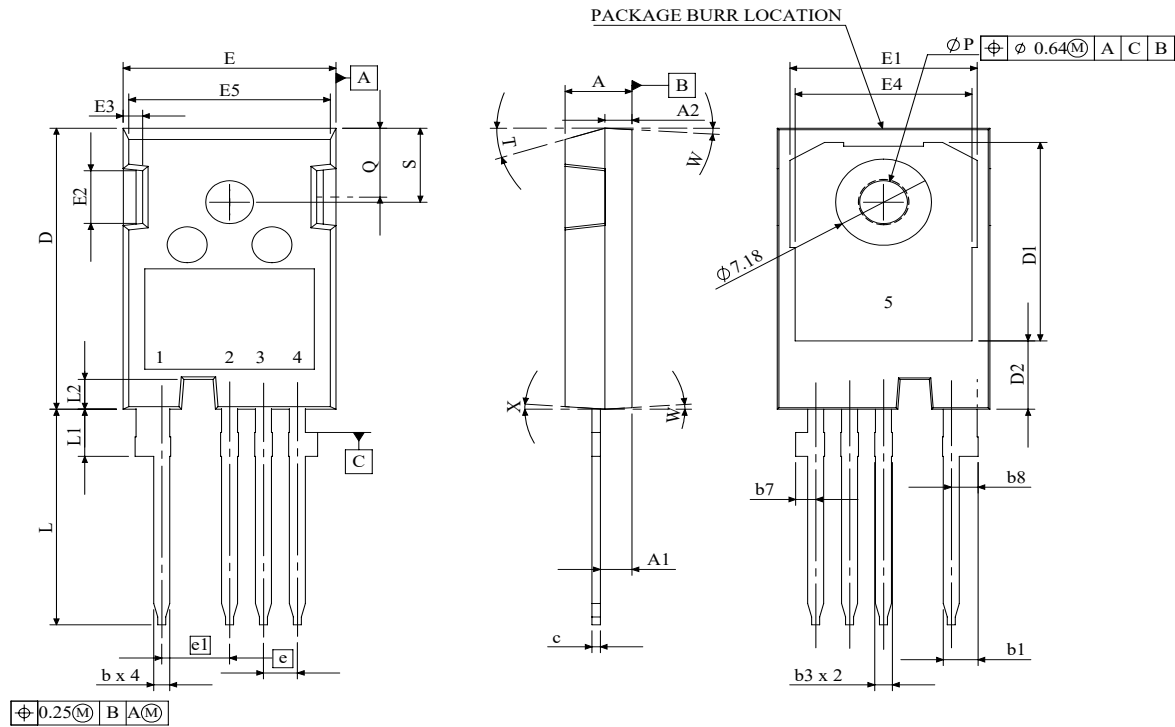


Figure 28. Body Diode Recovery Test Circuit

Package Dimensions

Package TO-247-4L



SYMBOL	MIN (mm)	MAX (mm)
A	4.83	5.21
A1	2.23	2.54
A2	1.91	2.16
b	1.07	1.33
b1	2.39	2.94
b3	1.07	1.60
b7	1.30	1.70
b8	1.80	2.20
c	0.55	0.68
D	23.30	23.63
D1	16.25	17.65
D2	5.55	5.95
E	15.75	16.13
E1	13.1	14.15
E2	3.68	5.10
E3	1.00	1.90
E4	12.38	13.43
E5	14.65	15.05
e1	5.08 BSC	
L	17.31	17.82
L1	3.97	4.37
L2	2.35	2.65
ϕP	3.51	3.65
Q	5.49	6.00
S	6.04	6.30
T	17.5° REF.	
W	3.5° REF.	
X	4° REF.	

1	DRAIN
2	SOURCE
3	DRIVER SOURCE
4	GATE
5	DRAIN

NOTE:

- ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
- BURR OR MOLD FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

Recommended Solder Pad Layout

