LM339-MIL Low-Power Low-Offset Voltage Quad Comparator

1 Features

- Wide Supply Voltage Range
- 2 to 36 V_{DC} or ±1 to ±18 V_{DC}
- Very-Low Supply Current Drain (0.8 mA) — Independent of Supply Voltage
- Low Input Biasing Current: 25 nA
- Low Input Offset Current: ±5 nA
- Offset Voltage: ±3 mV
- Input Common-Mode Voltage Range Includes GND
- Differential Input Voltage Range Equal to the Power Supply Voltage
- Low Output Saturation Voltage: 250 mV at 4 mA
- Output Voltage Compatible With TTL, DTL, ECL, MOS, and CMOS Logic Systems
- Advantages:
  - High-Precision Comparators
  - Reduced V_{OS} Drift Overtemperature
  - Eliminates Need for Dual Supplies
  - Allows Sensing Near GND
  - Compatible With All Forms of Logic
  - Power Drain Suitable for Battery Operation

2 Applications

- Limit Comparators
- Simple Analog-to-Digital Converters (ADCs)
- Pulse, Squarewave, and Time Delay Generators
- Wide Range VCO; MOS Clock Timers
- Multivibrators and High-Voltage Digital Logic Gates

3 Description

The LM339-MIL device consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV maximum for all four comparators. These comparators were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low-power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though they are operated from a single power supply voltage.

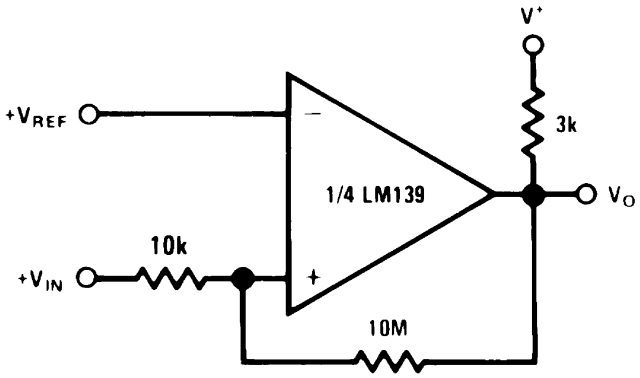
The LM339-MIL device was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the device directly interfaces with MOS logic where the low-power drain of the LM339-MIL is a distinct advantage over standard comparators.

Device Information(1)

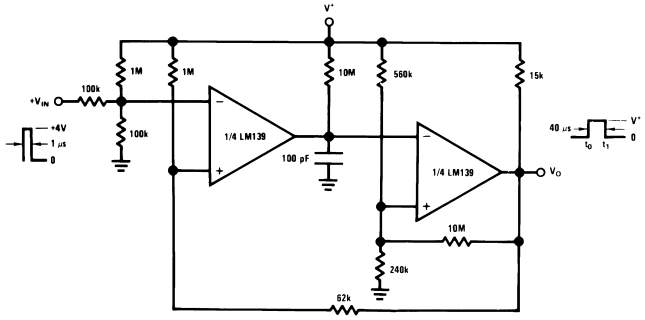
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM339-MIL	CDIP (14)	19.56 mm × 6.67 mm
	SOIC (14)	8.65 mm × 3.91 mm
	PDIP (14)	19.177 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Noninverting Comparator With Hysteresis



One-Shot Multivibrator With Input Lockout



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4 Revision History

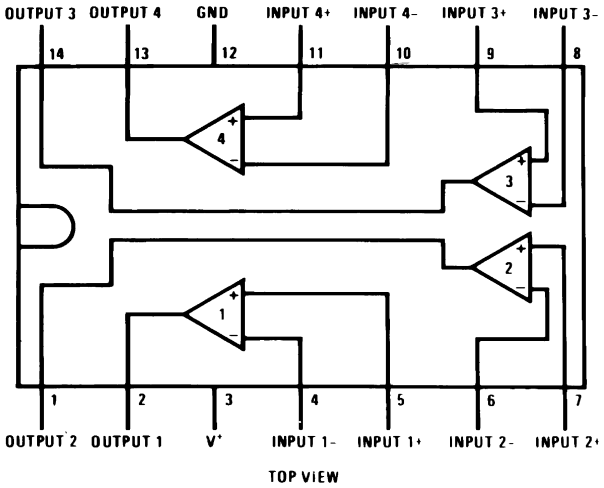
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2017	*	Initial release.

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5 Pin Configuration and Functions

J, D, and NFF Packages
14-Pin CDIP, SOIC, and PDIP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	OUTPUT2	O	Output, Channel 2
2	OUTPUT1	O	Output, Channel 1
3	V+	P	Positive Supply
4	INPUT1-	I	Inverting Input, Channel 1
5	INPUT1+	I	Noninverting Input, Channel 1
6	INPUT2-	I	Inverting Input, Channel 2
7	INPUT2+	I	Noninverting Input, Channel 2
8	INPUT3-	I	Inverting Input, Channel 3
9	INPUT3+	I	Noninverting Input, Channel 3
10	INPUT4-	I	Inverting Input, Channel 4
11	INPUT4+	I	Noninverting Input, Channel 4
12	GND	P	Ground
13	OUTPUT4	O	Output, Channel 4
14	OUTPUT3	O	Output, Channel 3

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6 Specifications

6.1 Absolute Maximum Ratings

See (1)(2)

		MIN	MAX	UNIT
Supply voltage, V+			36	V_{DC}
Differential input voltage(3)			36	
Input voltage		–0.3	36	
Input current (V_{IN} ≤ 0.3 V_{DC})(4)			50	mA
Power dissipation(5)	PDIP		1050	mW
	Cavity DIP		1190	
	SOIC package		760	
Output short-circuit to GND(6)			Continuous	
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Refer to RETS139X for military specifications.
(3) Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3 V_{DC} (or 0.3 V_{DC} below the magnitude of the negative power supply, if used) (at 25°C).
(4) This input current will only exist when the voltage at any of the input leads is driven negative. It is because of the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V_{DC} (at 25°C).
(5) For operating at high temperatures, the device must be derated based on a 125°C maximum junction temperature and a thermal resistance of 95°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The low bias dissipation and the *ON-OFF* characteristic of the outputs keeps the chip dissipation very small (P_D ≤ 100 mW), provided the output transistors are allowed to saturate.
(6) Short circuits from the output to V+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V+.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±600	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage, single	2	36	V
Supply voltage, dual	±1	±18	
Operating temperature	0	70	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM339-MIL			UNIT
		J (CDIP)	D (SOIC)	NFF (PDIP)	
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97.8	94.3	82.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.6	52.4	79	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	87.5	48.8	62.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	43.9	14.2	50.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	80.3	48.5	62	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	30.1	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

($V+ = 5\ V_{DC}$, $T_A = 25°C$, unless otherwise stated)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input offset voltage	At output switch point, $V_O \approx 1.4\ V_{DC}$, $R_S = 0\ \Omega$ with V+ from 5 V_{DC} to 30 V_{DC}; and over the full input common-mode range (0 V_{DC} to V+ −1.5 V_{DC}), at 25°C.		2	5	mV_{DC}
	At output switch point, $V_O \approx 1.4\ V_{DC}$, $R_S = 0\ \Omega$ with V+ from 5 V_{DC} to 30 V_{DC}; and over the full input common-mode range (0 V_{DC} to V+ −1.5 V_{DC}), at 25°C, 0°C ≤ T_A ≤ 70°C			9	
Input bias current(1)	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range, $V_{CM} = 0$ V		25	250	nA_{DC}
	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range, $V_{CM} = 0$ V, 0°C ≤ T_A ≤ 70°C			400	
Input offset current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0$ V		5	50	nA_{DC}
	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0$ V, 0°C ≤ T_A ≤ 70°C			150	
Input common-mode voltage range(2)	V+ = 30 V_{DC}	0		V+ − 1.5	V_{DC}
	V+ = 30 V_{DC}, 0°C ≤ T_A ≤ 70°C			$V^+ - 2$	
Supply current	$R_L = \infty$ on all comparators		0.8	2	mA_{DC}
	$R_L = \infty$, V+ = 36 V		1	2.5	mA_{DC}
Voltage gain	$R_L \geq 15\ k\Omega$, V+ = 15 V_{DC}, V_O = 1 V_{DC} to 11 V_{DC}	50	200		V/mV
Large signal response time	V_{IN} = TTL logic swing, V_{REF} = 1.4 V_{DC}, V_{RL} = 5 V_{DC}, R_L = 5.1 kΩ		300		ns
Response time(3)	V_{RL} = 5 V_{DC}, R_L = 5.1 kΩ		1.3		µs
Output sink current	$V_{IN(-)}$= 1 V_{DC}, $V_{IN(+)} = 0$, $V_O \leq 1.5\ V_{DC}$	6	16		mA_{DC}
Saturation voltage	$V_{IN(-)}$ = 1 V_{DC}, $V_{IN(+)} = 0$, $I_{SINK} \leq 4$ mA		250	400	mV_{DC}
	$V_{IN(-)}$ = 1 V_{DC}, $V_{IN(+)} = 0$, $I_{SINK} \leq 4$ mA, 0°C ≤ T_A ≤ 70°C			700	
Output leakage current	$V_{IN(+)}$ = 1 V_{DC},$V_{IN(-)} = 0$, V_O = 5 V_{DC}		0.1		nA_{DC}
	$V_{IN(+)}$ = 1 V_{DC}, $V_{IN(-)} = 0$, V_O = 30 V_{DC}, 0°C ≤ T_A ≤ 70°C			1	μA_{DC}
Differential input voltage(4)	Keep all V_{IN}s ≥ 0 V_{DC} (or V–, if used), 0°C ≤ T_A ≤ 70°C			36	V_{DC}

(1) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
(2) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V+ −1.5 V at 25°C, but either or both inputs can go to 30 V_{DC} without damage, independent of the magnitude of V+.
(3) The response time specified is a 100-mV input step with 5-mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.
(4) Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3 V_{DC} (or 0.3 V_{DC}below the magnitude of the negative power supply, if used) (at 25°C).

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6.6 Typical Characteristics

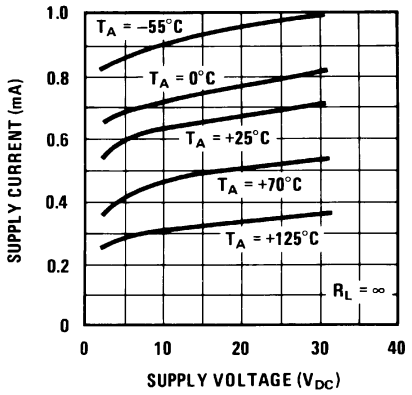


Figure 1. Supply Current

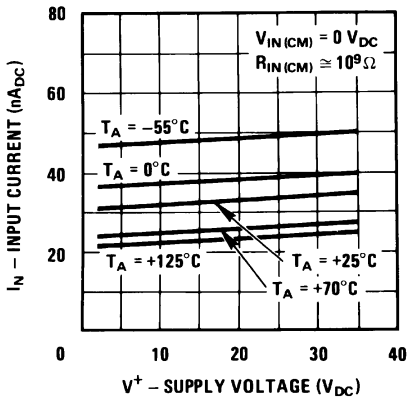


Figure 2. Input Current

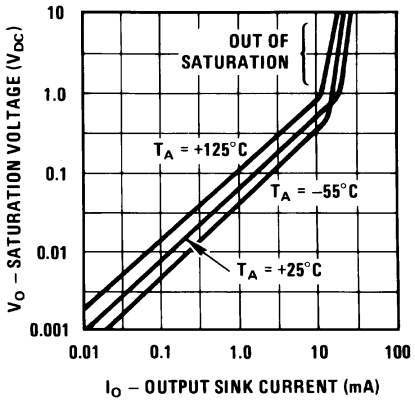


Figure 3. Output Saturation Voltage

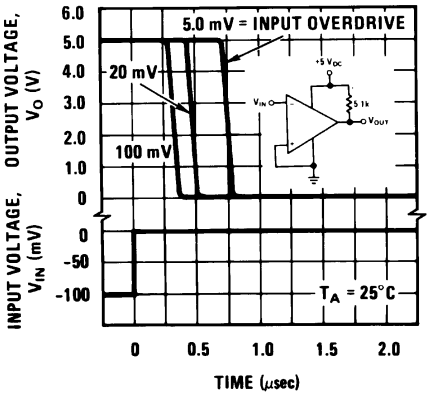


Figure 4. Response Time for Various Input Overdrives—Negative Transition

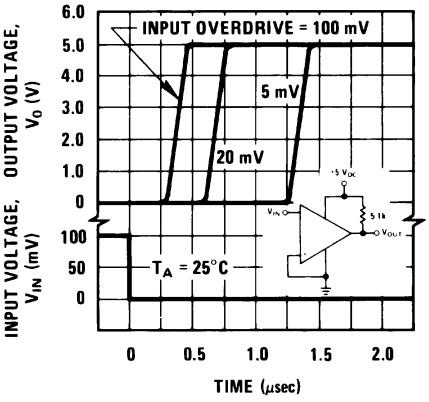


Figure 5. Response Time for Various Input Overdrives—Positive Transition

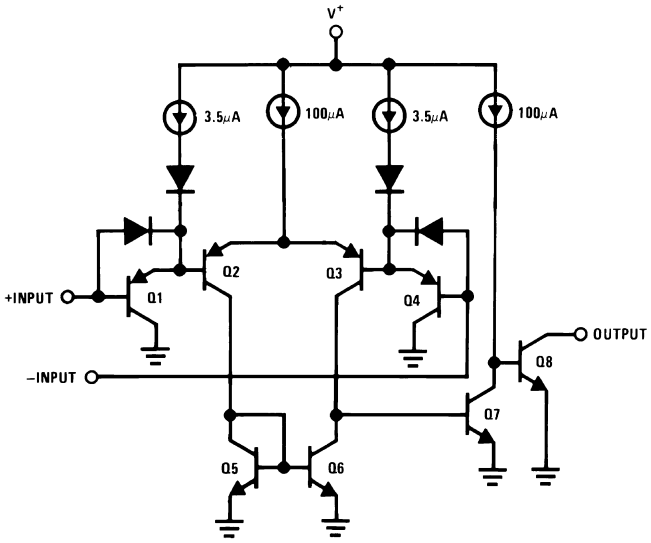
7 Detailed Description

7.1 Overview

The LM339-MIL device is a monolithic quad of independently functioning comparators designed to meet the requirements for a medium-speed, TTL-compatible comparator for industrial applications. Because no antisaturation clamps are used on the output, such as a Baker clamp or other active circuitry, the output leakage current in the OFF state is typically 0.1 nA. This OFF-state current level makes the device ideal for system applications where switching a node to ground while leaving it totally unaffected in the OFF state is desired. Other features include single supply, low-voltage operation with an input common mode range from ground up to approximately one volt below V_{CC} . The output is an uncommitted collector so it may be used with a pullup resistor and a separate output supply to give switching levels from any voltage up to 36 V down to a V CE SAT above ground (approximately 100 mV), sinking currents up to 16 mA. The open-collector output configuration allows the device to be used in wired-OR configurations, such as a window comparators.

The device can also be used as a single pole switch to ground, leaving the switched node unaffected while in the OFF state. Power dissipation with all four comparators in the OFF state is typically 4 mW from a single 5-V supply (1 mW/comparator).

7.2 Functional Block Diagram



7.3 Feature Description

The LM339-MIL device is a high-gain, wide bandwidth device which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs through stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Reducing the input resistors to < 10 kΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

The differential input voltage may be larger than V+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in the *Application and Implementation* section.

The output of the LM339-MIL device is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output ORing function. An output pullup resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage because of the magnitude of the voltage which is applied to the V+ pin. The output can also be used as a simple SPST switch to ground (when a pullup resistor is not used). The amount of current

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Feature Description (continued)

which the output device can sink is limited by the drive available (which is independent of V+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60-Ω R_{SAT} of the output transistor. The low offset voltage of the output transistor (4 mV) allows the output to clamp essentially to ground level for small load currents.

7.4 Device Functional Modes

A basic comparator circuit is used for converting analog signals to a digital output. The output is HIGH when the voltage on the noninverting (+IN) input is greater than the inverting (-IN) input. The output is LOW when the voltage on the noninverting (+IN) input is less than the inverting (-IN) input. The inverting input (-IN) is also commonly referred to as the reference, or VREF, input.

All pins of any unused comparators should be tied to the negative supply.

The bias network of the LM339-MIL device establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 V_{DC} to 30 V_{DC}.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM339-MIL device is specified for operation from 2 V to 36 V (±1 V to ±18 V) over the temperature range of 0°C to 70°C. While it may seem like a comparator has a well-defined and somewhat limited functionality as a *1-bit ADC*, a comparator is a versatile component which can be used for many functions.

8.2 Typical Application

8.2.1 Basic Comparator

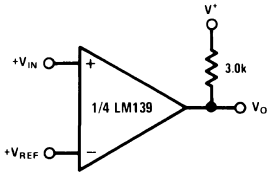


Figure 6. Basic Comparator Schematic

8.2.1.1 Design Requirements

The basic usage of a comparator is to indicate when a specific analog signal has exceeded some predefined threshold. In this application, the negative input is tied to a reference voltage, and the positive input is connected to the input signal. The output is pulled up with a resistor to the logic supply voltage, V+.

For an example application, the supply voltage is 5 V. The input signal varies between 1 V and 3 V. Specifically as an example, to know when the input exceeds 2.5 V, set the V_{REF} voltage to 2.5 V.

8.2.1.2 Application Curve

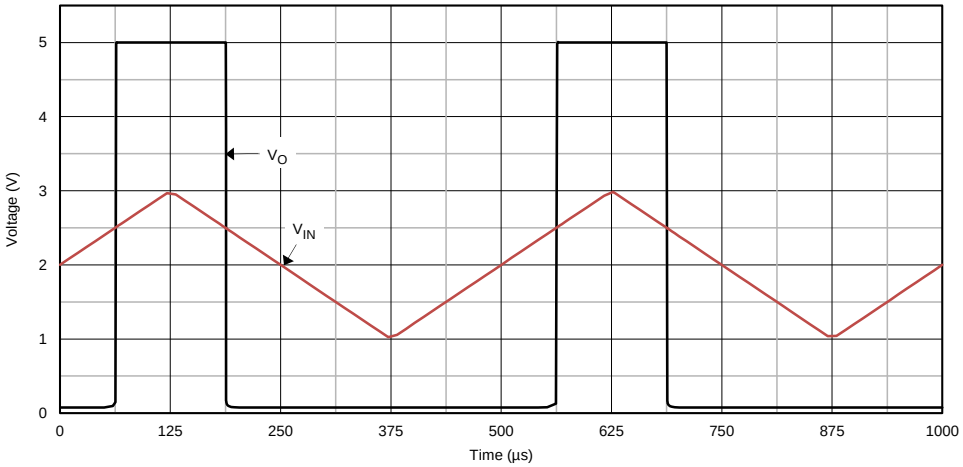


Figure 7. Basic Comparator Response

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8.3 System Examples

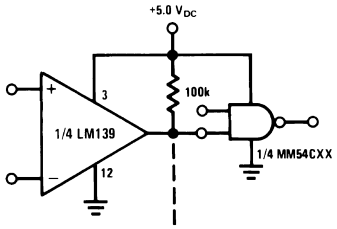


Figure 8. Driving CMOS ($V+ = 5\ V_{DC}$)

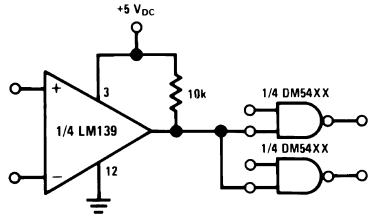


Figure 9. Driving TTL ($V+ = 5\ V_{DC}$)

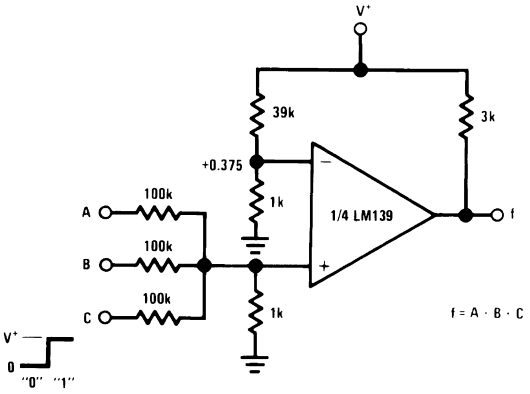


Figure 10. AND Gate ($V+ = 5\ V_{DC}$)

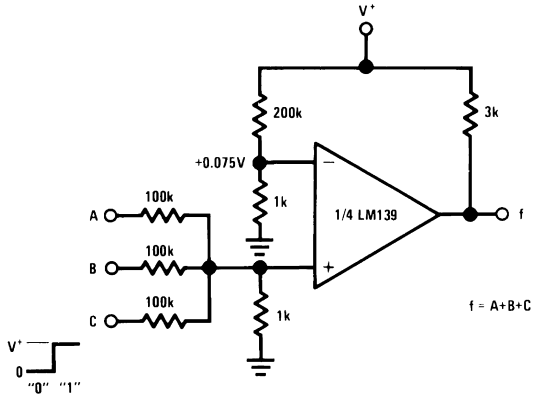


Figure 11. OR Gate ($V+ = 5\ V_{DC}$)

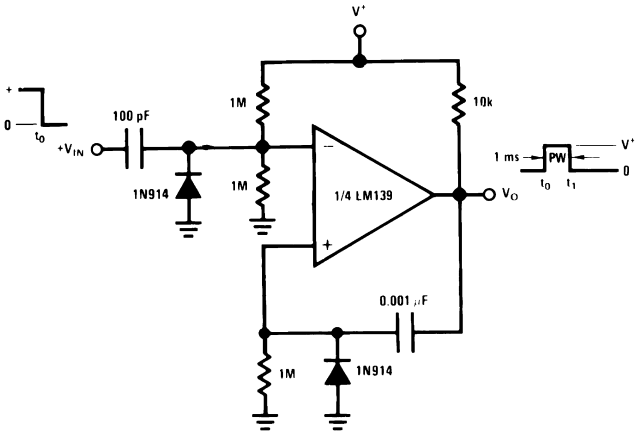


Figure 12. One-Shot Multivibrator ($V+= 15\ V_{DC}$)

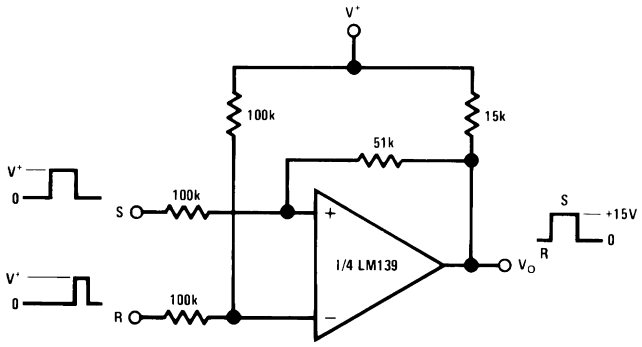


Figure 13. Bi-Stable Multivibrator ($V+= 15\ V_{DC}$)

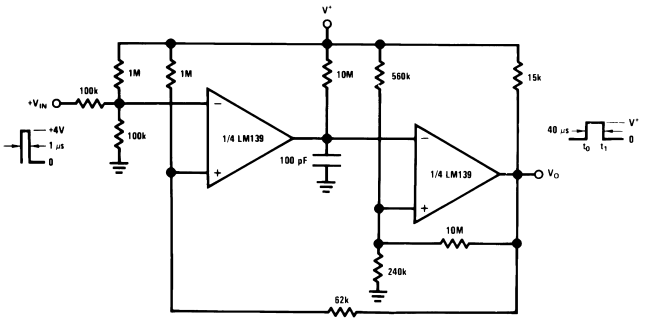


Figure 14. One-Shot Multivibrator With Input Lockout
(V+= 15 V_{DC})

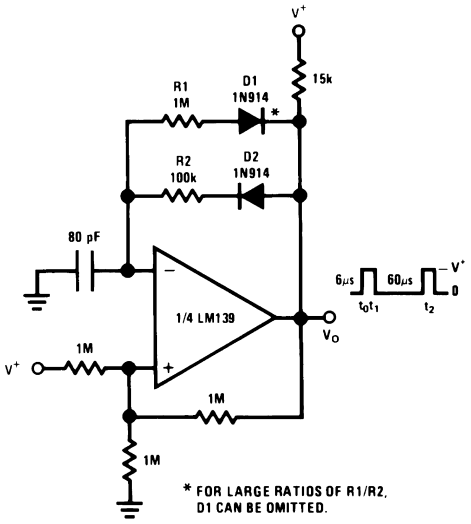


Figure 15. Pulse Generator
(V+= 15 V_{DC})

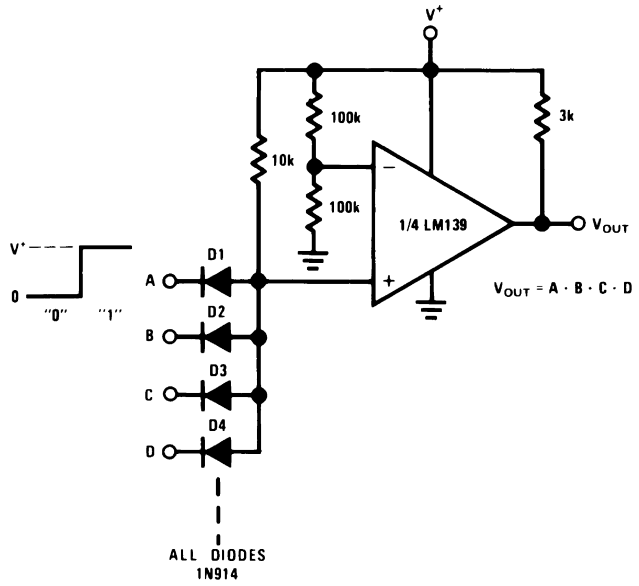


Figure 16. Large Fan-In AND Gate
(V+= 15 V_{DC})

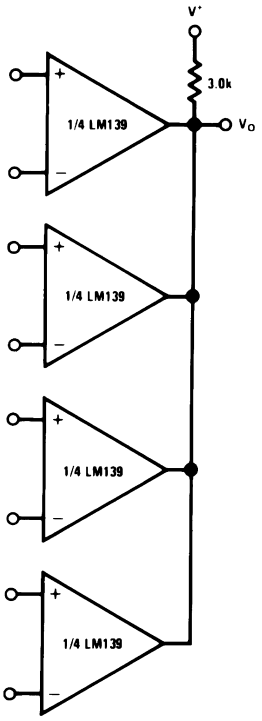


Figure 17. ORing the Outputs
(V+= 15 V_{DC})

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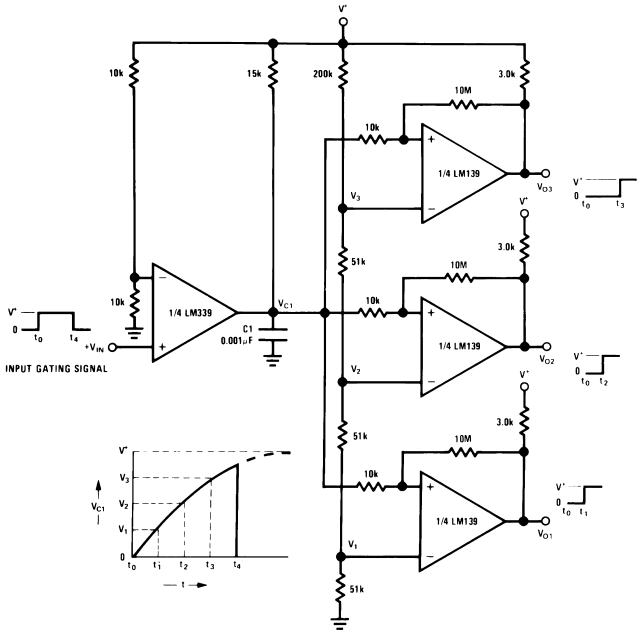


Figure 18. Time Delay Generator

(V+= 15 V_{DC})

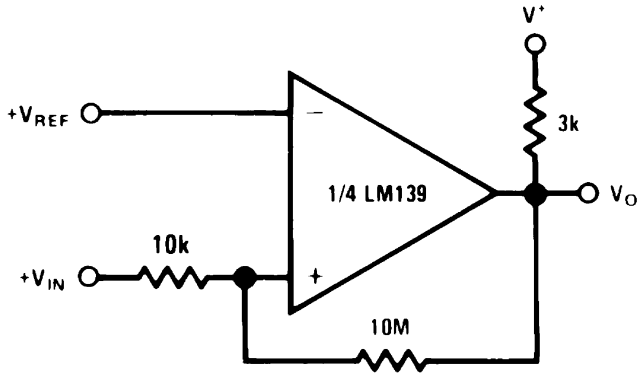


Figure 19. Noninverting Comparator with Hysteresis
(V+= 15 V_{DC})

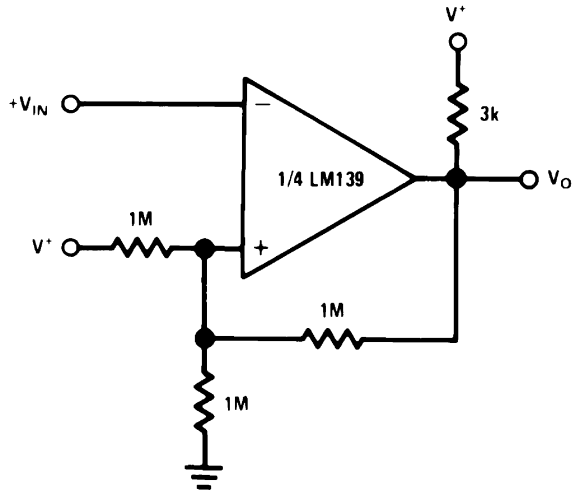


Figure 20. Inverting Comparator With Hysteresis
(V+= 15 V_{DC})

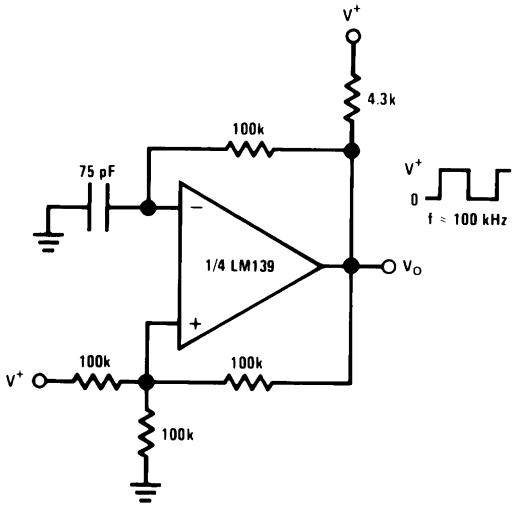


Figure 21. Squarewave Oscillator
(V+= 15 V_{DC})

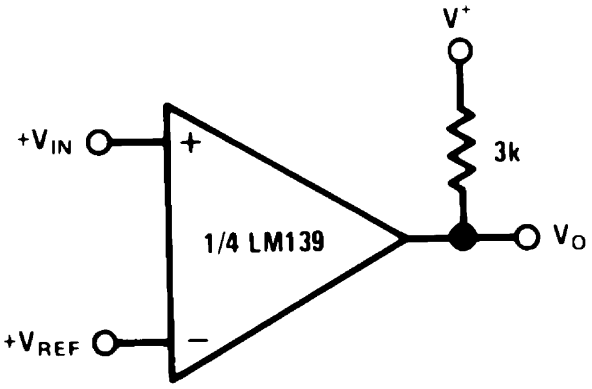


Figure 22. Basic Comparator
(V+= 15 V_{DC})

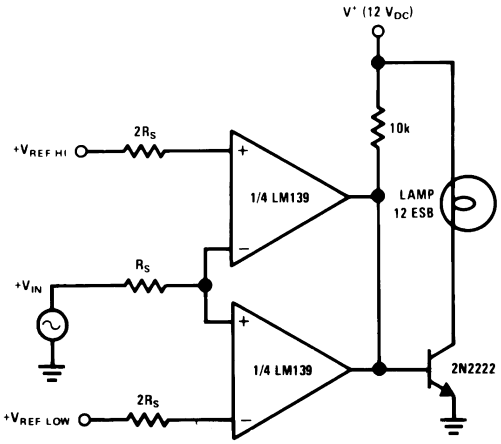


Figure 23. Limit Comparator
(V+= 15 V_{DC})

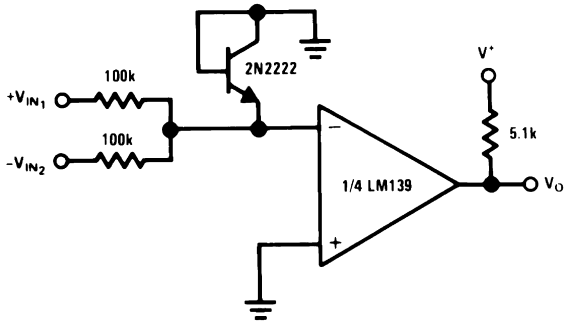
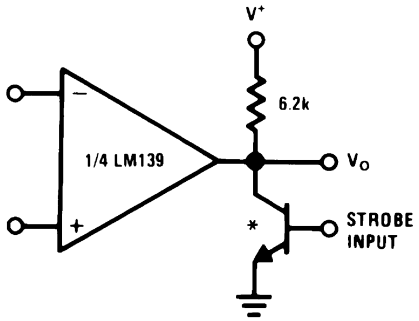


Figure 24. Comparing Input Voltages of Opposite Polarity
(V+= 15 V_{DC})



* Or open-collector logic gate without pullup resistor

Figure 25. Output Strobing
(V+= 15 V_{DC})

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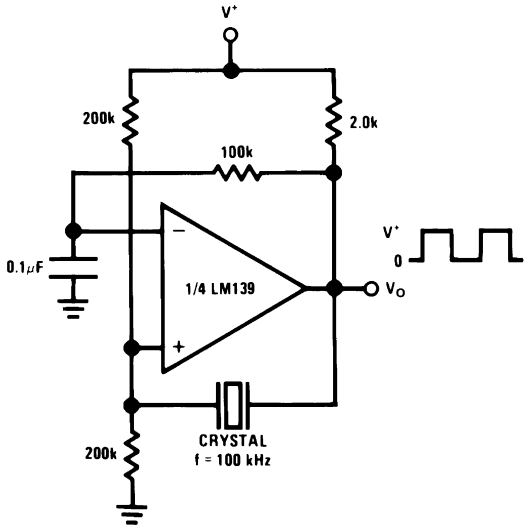


Figure 26. Crystal Controlled Oscillator

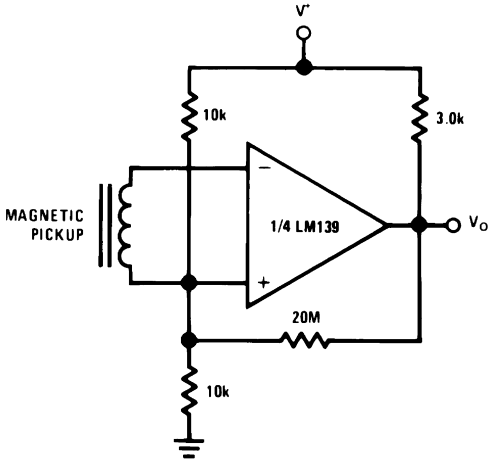
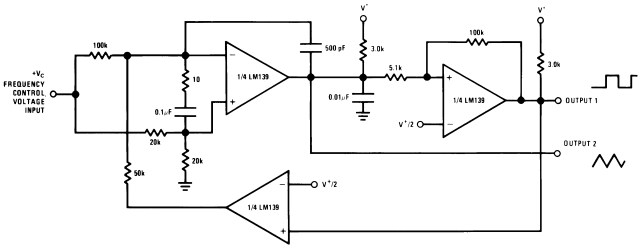


Figure 28. Transducer Amplifier
(V+= 15 V_{DC})

(V+= 15 V_{DC})



250 $mV_{DC} \leq V_C \leq +50\ V_{DC}$

700 Hz ≤ f_O ≤ 100 kHz

Figure 27. Two-Decade High-Frequency VCO
V+ = +30 V_{DC}

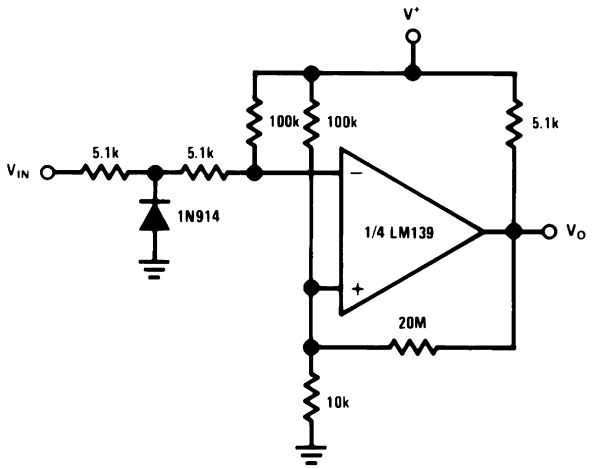


Figure 29. Zero Crossing Detector (Single Power Supply)
(V+= 15 V_{DC})

8.3.1 Split-Supply Applications

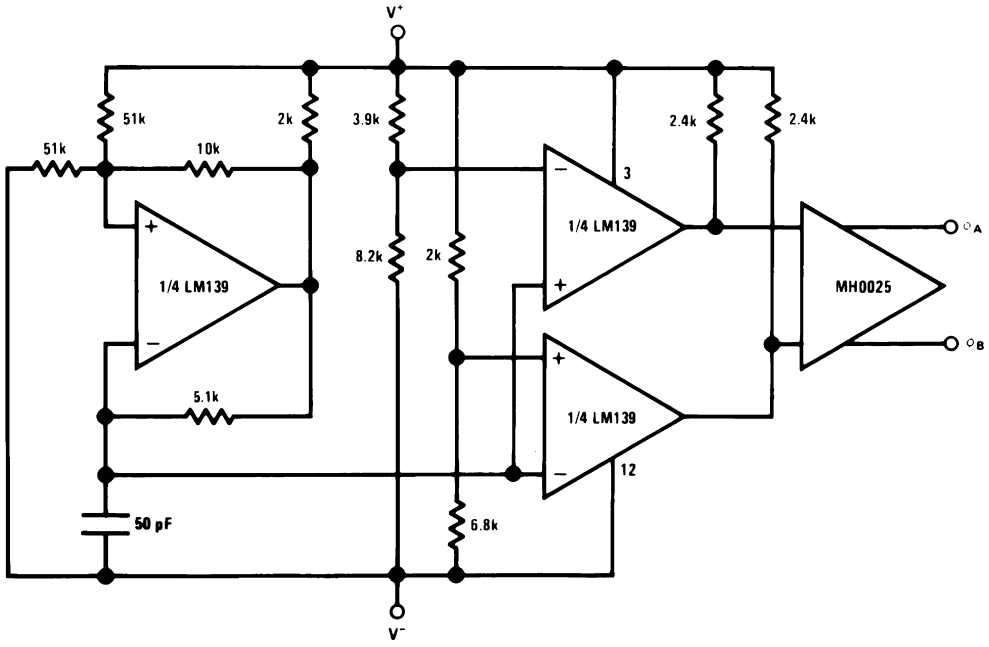


Figure 30. MOS Clock Driver
(V+ = +15 V_{DC} and V– = −15 V_{DC})

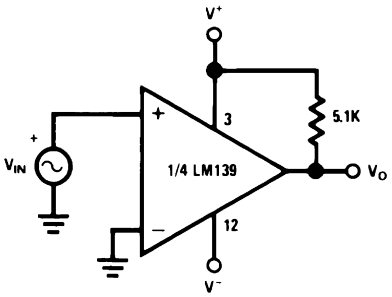


Figure 31. Zero Crossing Detector
(V+ = +15 V_{DC} and V– = −15 V_{DC})

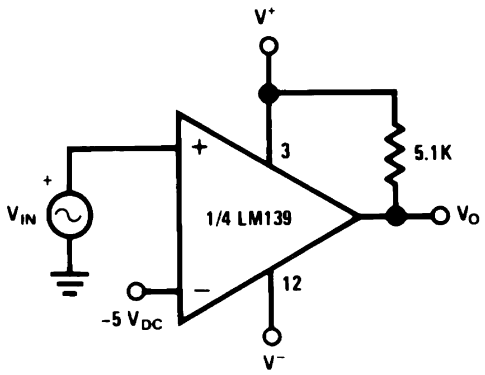


Figure 32. Comparator With a Negative Reference
(V+ = +15 V_{DC} and V– = −15 V_{DC})

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9 Power Supply Recommendations

Even in low-frequency applications, the device can have internal transients which are extremely quick. For this reason, bypassing the power supply with a 1-µF capacitor to ground will provide improved performance; the supply bypass capacitor should be placed as close as possible to the supply pin and have a solid connection to ground. The bypass capacitors should have a low ESR.

10 Layout

10.1 Layout Guidelines

Try to minimize parasitic impedances on the inputs to avoid oscillation. Any positive feedback used as hysteresis should place the feedback components as close as possible to the input pins. Ensure that the output pins do not couple to the inputs which can occur through capacitive coupling if the traces are too close and lead to oscillations on the output.

The optimum bypass capacitor placement is closest to the V+ and ground pins. Minimize the loop area formed by the bypass capacitor connection between V+ and ground. The ground pin should be connected to the PCB ground plane at the pin of the device. The feedback components should be placed as close to the device as possible minimizing strays.

10.2 Layout Example

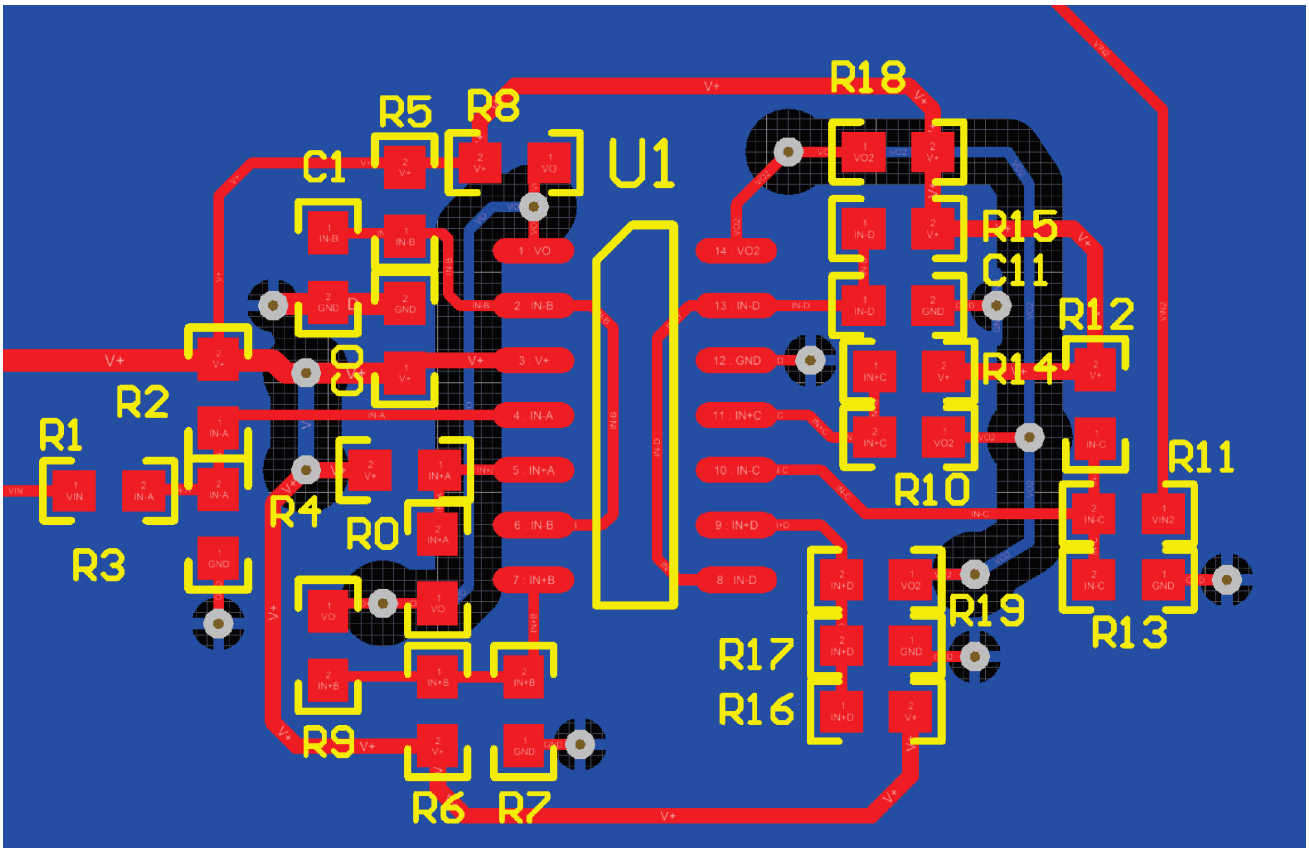


Figure 33. Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

Texas Instruments, *AN-74 LM139/LM239/LM339 A Quad of Independently Functioning Comparators* application report

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM339J	Active	Production	CDIP (J) | 14	25 | TUBE	No	Call TI	Level-1-NA-UNLIM	0 to 70	LM339J
LM339J.A	Active	Production	CDIP (J) | 14	25 | TUBE	-	Call TI	Call TI	0 to 70	LM339J

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

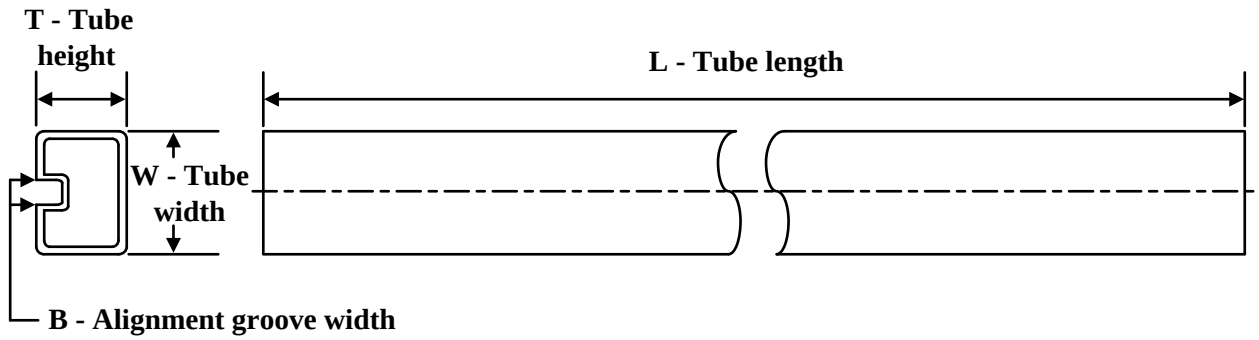
(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE



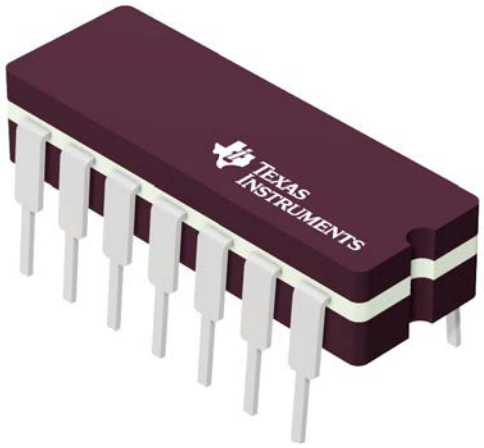
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM339J	J	CDIP	14	25	502	14	11938	4.32

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

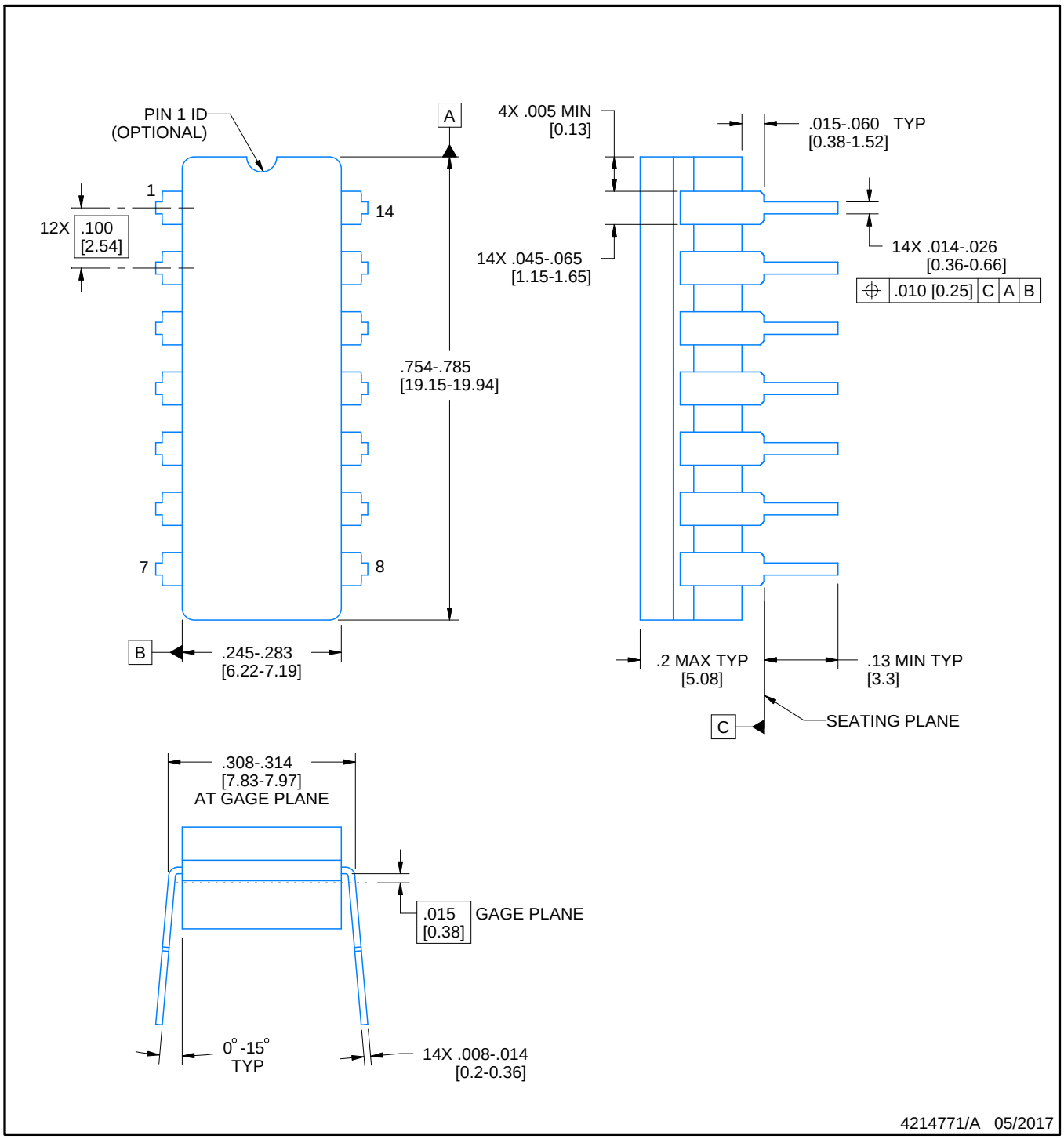


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

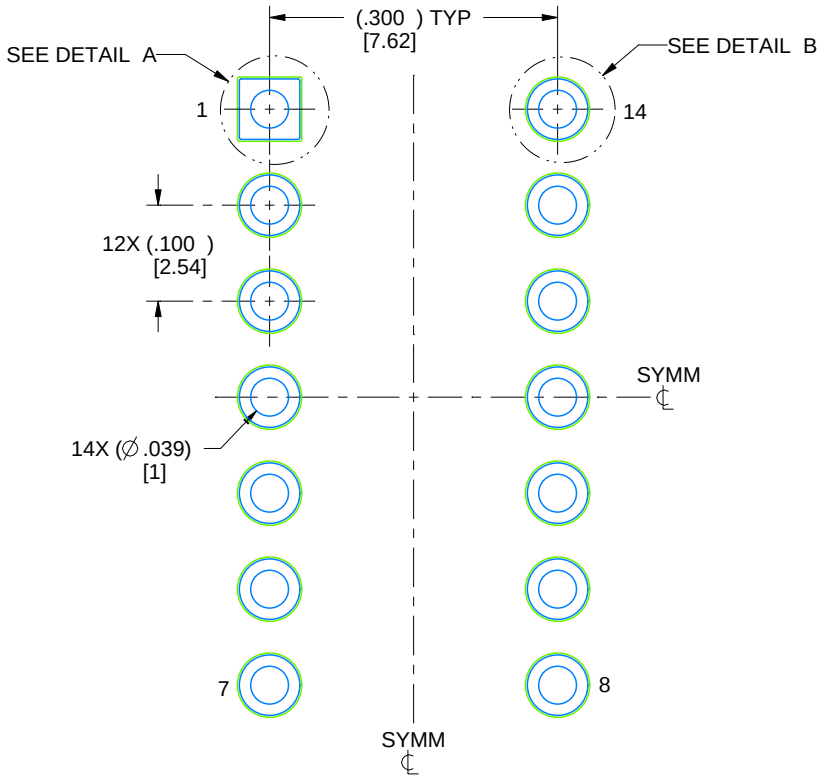
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

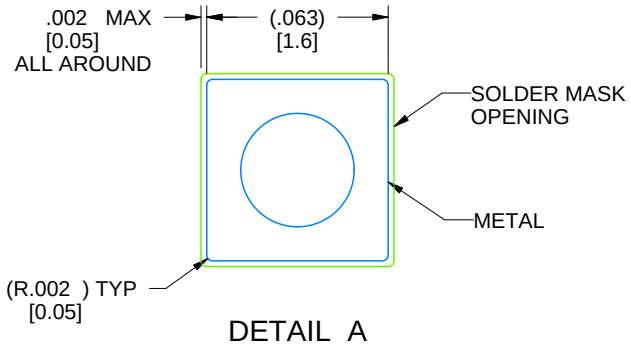
J0014A

CDIP - 5.08 mm max height

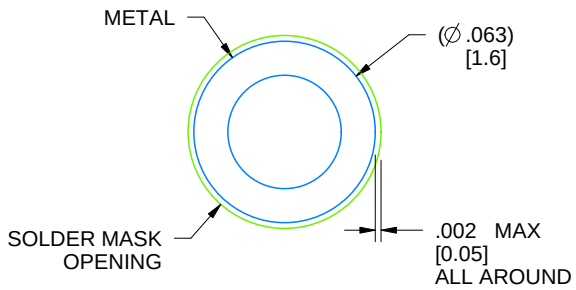
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

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