HX1302-S/HX1302-P Trickle-Charge Timekeeping Chip

FEATURES

Complete Management of All Timekeeping Functions

- Real-Time ClockCapable of Counting Seconds, Minutes, Hours, Date, Month, Day of the Week, and Year, with Leap-Year Compensation Valid Through 2100
- 31 x 8 Battery-Backed RAM for General-Purpose Use

Simplified Serial Port Connectivity with Most Microcontrollers

- Simple 3-Wire Interface for Easy Integration
- TTL-Compatible (VCC = 5V) for Seamless Communication
- Flexible Data Transfer Options: Single-Byte or Multiple-Byte (Burst Mode) for Clock or RAM Data Read/Write

Efficient Low-Power Operation Ensures Extended Battery Backup Time

- Full Operation within a Wide Voltage Range of 2.0V to 5.5V
- Ultra-Low Power Consumption, Less Than 300nA at 2.0V

Compact Footprint with 8-Pin DIP and 8-Pin SO Packages

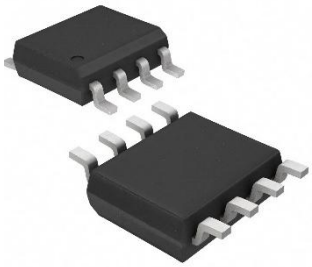
- Minimizes the Required Space for Easy Integration into Various Applications

Optional Industrial Temperature Range: -40°C to +85°C

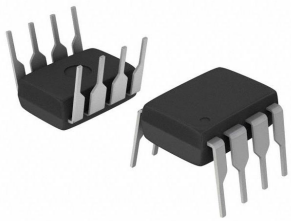
- Supports Operation in a Wide Range of Environments, Ensuring Reliable Performance

Recognition by Underwriters Laboratories® (UL)

- Ensures Compliance with Safety Standards for Reliable and Safe Operation

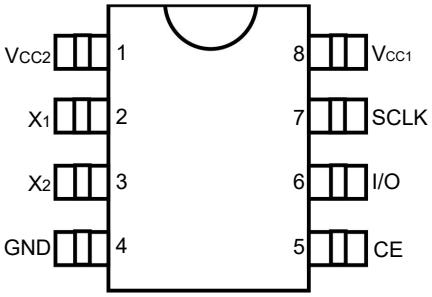


SOP-8

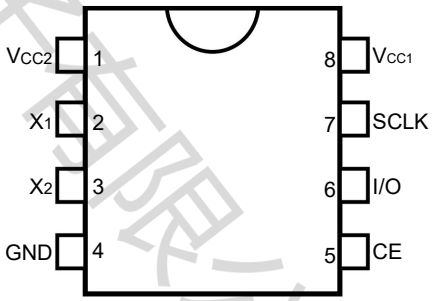


DIP-8

PIN CONFIGURATIONS



SOP-8



DIP-8

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	VCC2	Primary Power-Supply Pin in Dual Supply Configuration. VCC1 is connected to a backup source to maintain the time and date in the absence of primary power. The HX1302-S/HX1302-P operates from the larger of VCC1 or VCC2 . When VCC2 is greater than VCC1 + 0.2V, VCC2 powers the HX1302-S/HX1302-P. When VCC2 is less than VCC1 , VCC1 powers the HX1302-S/HX1302-P.
2	X1	Connections for Standard 32.768kHz Quartz Crystal. The internal oscillator is designed for operation with a crystal having a specified load capacitance of 6pF. For more information on crystal selection and crystal layout considerations, refer to Application Note 58: Crystal Considerations for Dallas Real-Time Clocks. The HX1302-S/HX1302-P can also be driven by an external 32.768kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.
3	X2	
4	GND	Ground
5	CE	Input. CE signal must be asserted high during a read or a write. This pin has an internal 40kΩ (typ) pulldown resistor to ground. Note: Previous data sheet revisions referred to CE as RST. The functionality of the pin has not changed.
6	I/O	Input/Push-Pull Output. The I/O pin is the bidirectional data pin for the 3-wire interface. This pin has an internal 40kΩ (typ) pulldown resistor to ground.
7	SCLK	Input. SCLK is used to synchronize data movement on the serial interface. This pin has an internal 40kΩ (typ) pulldown resistor to ground.
8	VCC1	Low-Power Operation in Single Supply and Battery-Operated Systems and Low-Power Battery Backup. In systems using the trickle charger, the rechargeable energy source is connected to this pin. UL recognized to ensure against reverse charging current when used with a lithium battery.

Product Information		
PART	**TEMP RANGE**	**PIN-PACKAGE**
HX1302-S	0°C to +70°C	SOP-8
HX1302-P	0°C to +70°C	DIP-8

DETAILED DESCRIPTION

The HX1302-S/HX1302-P trickle-charge timekeeping chip is equipped with a real-time clock/calendar system and 31 bytes of static RAM,
facilitating seamless communication with a microprocessor through a straightforward serial interface. This interface provides comprehensive information, encompassing seconds, minutes, hours, day, date, month, and year. The chip automatically adjusts for the varying number of days in each month, including leap-year corrections, ensuring accurate timekeeping.

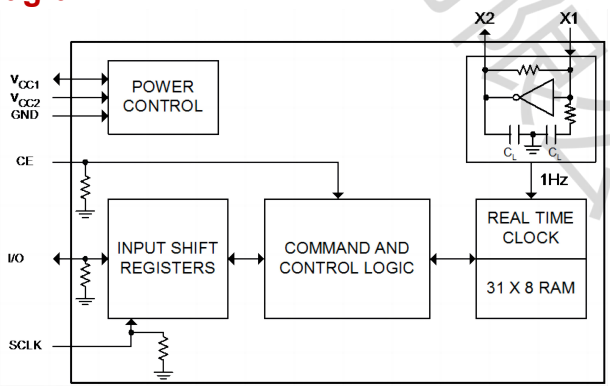
Moreover, the HX1302-S/HX1302-P offers flexibility in its time display format, operating in either 24-hour or 12-hour mode with an AM/PM indicator.
Communication with the HX1302-S/HX1302-P is straightforward, leveraging synchronous serial communication. Merely three wires - CE, I/O (data line), and SCLK (serial clock) - are required for seamless data exchange between the clock/RAM. Data transmission can occur either in single-byte increments or in bursts of up to 31 bytes. The HX1302-S/HX1302-P is designed to conserve power, maintaining data and clock information on minimal power consumption of less than 1μW.

The HX1302-S/HX1302-P builds upon its predecessor's fundamental timekeeping capabilities. It introduces added features such as dual power pins for both primary and backup power sources, a programmable trickle charger for VCC1, and an expanded seven-byte scratchpad memory.

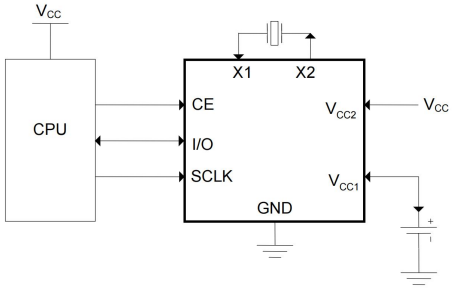
OPERATION

Fig 1 illustrates the core components of the serial timekeeper: a shift register, control logic, an oscillator, the real-time clock,and RAM. These elements work in tandem to ensure accurate and reliable timekeeping, making the HX1302-S/HX1302-P a robust and versatile solution for various applications.

Fig 1：Block Diagram

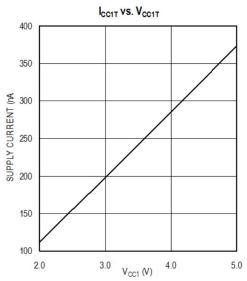


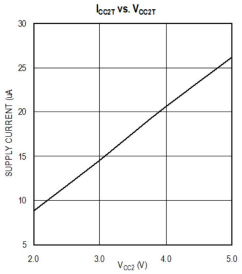
TYPICAL OPERATING CIRCUIT



TYPICAL OPERATING CHARACTERISTICS

(VCC = 3.3V, TA = +25°C, unless otherwise noted.)





OSCILLATOR CIRCUIT

The HX1302-S/HX1302-P relies on an external 32.768kHz crystal for its oscillator circuit, eliminating the need for any external resistors or capacitors.

Table 1 outlines the specific crystal parameters required for this application. A functional schematic of the oscillator circuit is depicted in Figure 1. Provided that a crystal with the specified characteristics is used, the startup time is typically less than a second.

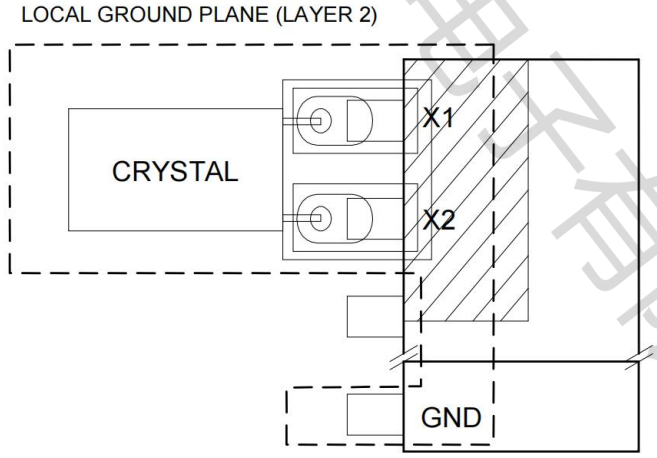
CLOCK ACCURACY

The precision of the clock is primarily determined by the accuracy of the crystal and how well the capacitive load of the oscillator circuit matches the capacitive load for which the crystal was calibrated. Additional errors may arise due to temperature-induced frequency drifts in the crystal. External circuit noise, if coupled into the oscillator circuit, can cause the clock to run faster. Figure demonstrates a typical PC board layout that effectively isolates the crystal and oscillator from such noise. For more detailed information, refer to Application Note 58: Crystal Considerations for Dallas Real-Time Clocks.

Table 1. Crystal Specifications

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	fO		32.768		kHz
Series Resistance	ESR			45	kΩ
Load Capacitance	CL		6		pF

Figure 2:Typical PC Board Layout for Crystal



NOTE: AVOID ROUTING SIGNALS IN THE CROSSHATCHED AREA (UPPER LEFT-HAND QUADRANT) OF THE PACKAGE UNLESS THERE IS A GROUND PLANE BETWEEN THE SIGNAL LINE AND THE PACKAGE.

COMMAND BYTE

Figure 3 illustrates the command byte, which initiates each data transfer. It is crucial that the Most Significant Bit (bit 7) is set to a logic 1. If it's a 0, writing to the HX1302-S/HX1302-P will be disabled. Bit 6 distinguishes between clock/calendar data (logic 0) and RAM data (logic 1). Bits 1 through 5 designate the specific registers for input or output, while the Least Significant Bit (bit 0) determines whether it's a write operation (input) for logic 0 or a read operation (output) for logic 1. Notably, the command byte is always input, commencing with the LSB (bit 0).

7	6	5	4	3	2	1	0
1	RAM $\overline{CK}$	A4	A3	A2	A1	A0	RD $\overline{WR}$

CE AND CLOCK CONTROL

Raising the CE input to a high state initiates all data transfers. CE serves dual purposes: first, it activates the control logic, enabling access to the shift register for the address/command sequence. Secondly, the CE signal serves as a means to terminate both single-byte and multiple-byte data transfers.

A clock cycle comprises a rising edge followed by a falling edge. For data inputs, the data must be stable during the rising edge of the clock, and data bits are outputted on the falling edge. If the CE input is low, all data transfer ceases, and the I/O pin transitions to a high-impedance state. Figure 4 illustrates the data transfer process. Upon

power-up, CE must remain at a logic 0 until VCC exceeds 2.0V. Additionally, SCLK must be set to a logic 0 before CE is driven to a logic 1 state.

DATA INPUT

After the eight SCLK cycles that input a write command byte, a data byte is inputted on the rising edge of the subsequent eight SCLK cycles. Any additional SCLK cycles that occur unintentionally are ignored. Data input begins with bit 0.

DATA OUTPUT

Following the eight SCLK cycles that input a read command byte, a data byte is outputted on the falling edge of the next eight SCLK cycles. Notably, the first data bit transmitted occurs on the first falling edge after the last bit of the command byte is written. If additional SCLK cycles occur unintentionally, the data bytes are retransmitted as long as CE remains high. This feature enables continuous burst mode reading. Additionally, the I/O pin is tristated on each rising edge of SCLK. Data output begins with bit 0.

BURST MODE

Burst mode can be activated for both clock/calendar and RAM registers by addressing location 31 decimal (address/command bits 1 through 5 set to logic 1). Similar to previous operations, bit 6 determines whether the target is the clock or RAM, while bit 0 specifies whether the operation is a read or a write. Notably, locations 9 through 31 in the Clock/Calendar Registers and location 31 in the RAM registers do not have any data storage capacity. When performing burst mode reads or writes, the process begins with bit 0 of address 0.

When writing to the clock registers in burst mode, it is imperative to write the first eight registers consecutively for the data to be successfully transferred. However, when writing to RAM in burst mode, it is not necessary to write all 31 bytes for the data to be transferred. Each byte that is written will be transferred to RAM regardless of whether all 31 bytes are written.

CLOCK/CALENDAR

To access the time and calendar information, you need to read the relevant register bytes. Table 3 provides a clear overview of the RTC registers. To set or initialize the time and calendar, you must write to the appropriate register bytes. Notably, the contents of these registers are stored in the binary-coded decimal (BCD) format.

The day-of-week register automatically increments at midnight. While the specific values for each day of the week are user-defined, they must be in sequential order (e.g., if 1 represents Sunday, then 2 represents Monday, and so on). Entering illogical time or date values may result in unpredictable behavior.

When reading or writing the time and date registers, secondary (user) buffers are employed to prevent errors during the internal register updates. Synchronization of the user buffers with the internal registers occurs on the rising edge of CE.

Writing to the seconds register resets the countdown chain. Write transfers are triggered on the falling edge of CE. To prevent rollover issues, it is crucial to write the remaining time and date registers within 1 second of resetting the countdown chain.

The HX1302-S/HX1302-P offers both 12-hour and 24-hour operation modes. Bit 7 of the hours register serves as the mode-select bit. When set to high, the 12-hour mode is activated. In 12-hour mode, bit 5 represents the AM/PM indicator, with logic high corresponding to PM. In 24-hour mode, bit 5 functions as the second 10-hour bit (representing hours 20 – 23). It is essential to re-initialize the hours data whenever the 12/24-hour bit is changed.

CLOCK HALT FLAG

Bit 7 of the seconds register functions as the clock halt (CH) flag. When set to logic 1, this flag halts the clock oscillator and puts the HX1302-S/HX1302-P into a low-power standby mode, reducing the current draw to below 100nA. Conversely, setting it to logic 0 resumes the clock operation. It's worth noting that the initial power-on state of this bit is not defined.

WRITE-PROTECT BIT

The write-protect bit occupies Bit 7 of the control register. The first seven bits (bits 0 to 6) are forcibly set to 0 and always read as 0. Before any write operation to the clock or RAM can be performed, Bit 7 must be set to 0. When set to high, the write-protect bit prevents any write operations to any other register. Similar to the clock halt flag, the initial power-on state of the write-protect bit is not defined. Therefore, it's crucial to clear the WP bit before attempting to write to the device.

TRICKLE-CHARGE REGISTER

This register regulates the trickle-charge characteristics of the HX1302-S/HX1302-P. The simplified schematic in Figure 5 illustrates the fundamental components of the trickle charger. The trickle-charge select (TCS) bits, spanning

from bits 4 to 7, govern the selection of the trickle charger. To prevent accidental activation, only the pattern 1010 enables the trickle charger; all other patterns disable it. By default, the HX1302-S/HX1302-P powers up with the trickle charger disabled.

The diode select (DS) bits, bits 2 and 3, determine whether one or two diodes are connected between VCC2 and VCC1. If DS is set to 01, one diode is selected, and if set to 10, two diodes are selected. If DS is set to 00 or 11, the trickle charger is independently disabled, regardless of the TCS setting.

The RS bits, bits 0 and 1, specify the resistor connected between VCC2 and VCC1. The selection of resistors and diodes is determined by the RS and DS bits as outlined in Table 2.

Table 2 : Trickle Charger Resistor and Diode Select

TCS BIT 7	TCS BIT 6	TCS BIT 5	TCS BIT 4	DS BIT 3	DS BIT 2	RS BIT 1	RS BIT 0	FUNCTION
X	X	X	X	X	X	0	0	Disabled
X	X	X	X	0	0	X	X	Disabled
X	X	X	X	1	1	X	X	Disabled
1	0	1	0	0	1	0	1	1 Diode, 2kΩ
1	0	1	0	0	1	1	0	1 Diode, 4kΩ
1	0	1	0	0	1	1	1	1 Diode, 8kΩ
1	0	1	0	1	0	0	1	2 Diodes, 2kΩ
1	0	1	0	1	0	1	0	2 Diodes, 4kΩ
1	0	1	0	1	0	1	1	2 Diodes, 8kΩ
0	1	0	1	1	1	0	0	Initial power-on state

Diode and resistor selection is determined by the user according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example. Assume that a system power supply of 5V is applied to VCC2 and a super cap is connected to VCC1. Also assume that the trickle charger has been enabled with one diode and resistor R1 between VCC2 and VCC1. The maximum current IMAX would therefore be calculated as follows:

$$IMAX = (5.0V - \text{diode drop}) / R1 \approx (5.0V - 0.7V) / 2k\Omega \approx 2.2mA$$

As the super cap charges, the voltage drop between VCC2 and VCC1 decreases and therefore the charge current decreases.

CLOCK/CALENDAR BURST MODE

The clock/calendar command byte initiates burst mode operation, enabling consecutive reads or writes of the first eight clock/calendar registers (see Table 3), commencing with bit 0 of address 0.

If the write-protect bit is set to high during a write clock/calendar burst mode, no data transfer will occur to any of the eight clock/calendar registers, including the control register. Additionally, the trickle charger remains inaccessible in burst mode.

At the commencement of a clock burst read, the current time is mirrored to a secondary set of registers. This allows for the reading of time information from these secondary registers while the clock continues to tick, eliminating the need to re-read the registers in case of an update to the main registers during a read operation.

RAM

The static RAM comprises 31 consecutive 8-byte registers, addressed sequentially within the RAM address space.

RAM BURST MODE

The RAM command byte triggers burst mode, permitting consecutive reads or writes of the 31 RAM registers (see Table 3), commencing with bit 0 of address 0.

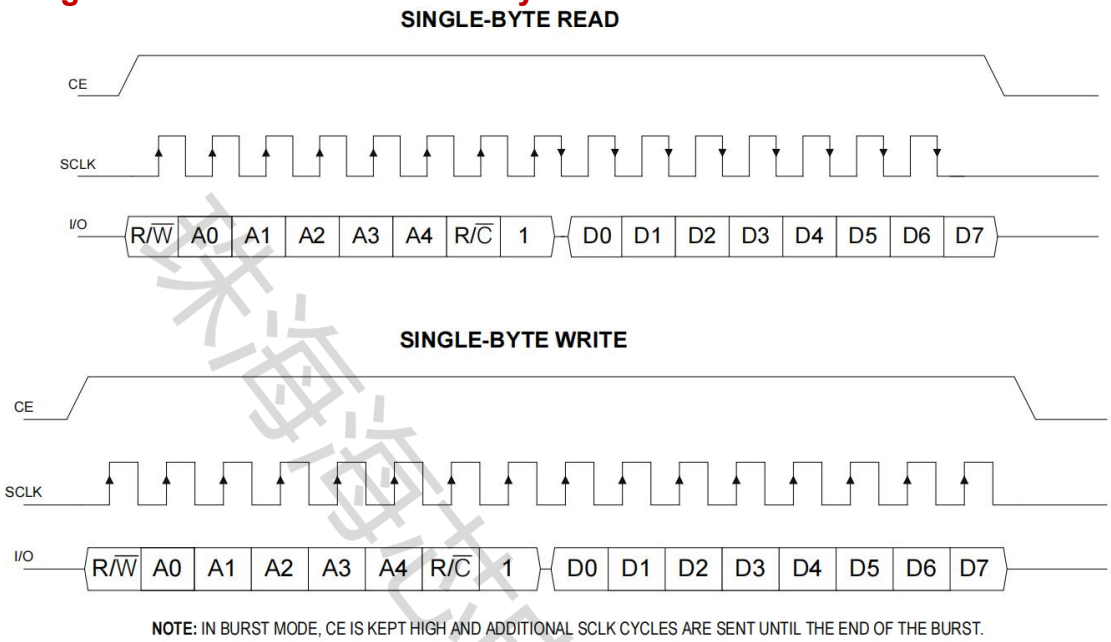
REGISTER SUMMARY

A comprehensive summary of the register data formats is presented in Table 3.

CRYSTAL SELECTION

A 32.768kHz crystal can be directly interfaced with the HX1302-S/HX1302-P via pins 2 and 3 (X1, X2). It is recommended to use a crystal with a specified load capacitance (CL) of 6pF. For detailed information on crystal selection and layout considerations, please refer to Application Note 58: Crystal Considerations for Dallas Real-Time Clocks.

Figure 4: Data Transfer Summary



NOTE: IN BURST MODE, CE IS KEPT HIGH AND ADDITIONAL SCLK CYCLES ARE SENT UNTIL THE END OF THE BURST.

Table 3. Register Address/Definition

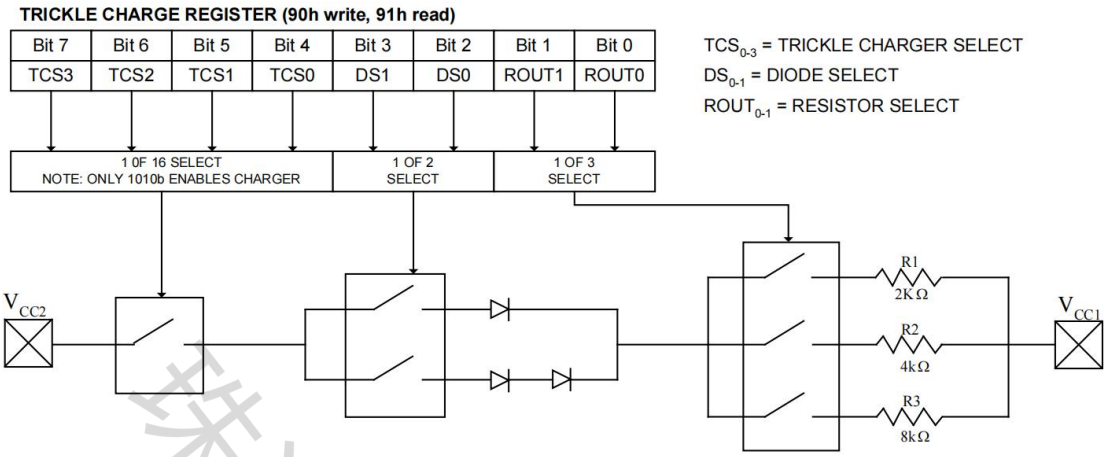
RTC										
READ	WRITE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RANGE
81h	80h	CH	10 Seconds			Seconds				00–59
83h	82h		10 Minutes			Minutes				00–59
85h	84h	12/$\overline{24}$	0	10	Hour	Hour				1–12/0–23
				$\overline{AM}$/PM						
87h	86h	0	0	10 Date		Date				1–31
89h	88h	0	0	0	10	Month				1–12
8Bh	8Ah	0	0	0	0	0	Day			1–7
8Dh	8Ch	10 Year				Year				00–99
8Fh	8Eh	WP	0	0	0	0	0	0	0	
91h	90h	TCS	TCS	TCS	TCS	DS	DS	RS	RS	

CLOCK BURST	
BFh	BEh

RAM			
C1h	C0h		00-FFh
C3h	C2h		00-FFh
C5h	C4h		00-FFh
⋮	⋮		⋮
FDh	FCh		00-FFh

RAM BURST	
FFh	FEh

Figure 5: Programmable Trickle Charger



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	UNITS
Voltage Range on Any Pin Relative to Ground	-0.5 to +7.0	V
Operating Temperature Range, Commercial	0 to +70	°C
Operating Temperature Range, Industrial (IND)	-40 to 85	°C
Storage Temperature Range	-55 to 125	°C
Soldering Temperature (leads, 10 seconds)	260	°C

RECOMMENDED DC OPERATING CONDITIONS TA = 0°C to +70°C or TA = -40°C to +85°C.[A]

PARAMETER	SYMBOL		CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage V_{CC1} , V_{CC2}	V_{CC1}, V_{CC2}		B,J	2.0	3.3	5.5	V
Logic 1 Input	VIH		B	2.0		VCC +	V
Logic 0 Input	VIL	VCC = 2.0V	B	-0.3		+0.3	V
		VCC = 5V		-0.3		+0.8	

DC ELECTRICAL CHARACTERISTICS TA = 0°C to +70°C or TA = -40°C to +85°C.[A]

PARAMETER	SYMBOL		CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage	ILI		E, M		85	500	µA
I/O Leakage	ILO		E, M		85	500	µA
Logic 1 Output (IOH = -0.4mA)	VOH	VCC = 2.0V	B	1.6			V
Logic 1 Output (IOH = -1.0mA)		VCC = 5V		2.4			
Logic 0 Output (IOL = 1.5mA)	VOL	VCC = 2.0V	B			0.4	V
Logic 0 Output (IOL = 4.0mA)		VCC = 5V				0.4	
Active Supply Current (Oscillator Enabled)	ICC1A	VCC1 = 2.0V	CH = 0			0.4	mA
		VCC1 = 5V	D,K			1.2	
Timekeeping Current (Oscillator Enabled)	ICC1T	VCC1 = 2.0V	CH = 0		0.2	0.3	µA
		VCC1 = 5V	C,K,M		0.45	1	
Standby Current (Oscillator Disabled)	ICC1S	VCC1 = 2.0V	CH = 1		1	100	nA
		VCC1 = 5V			1	100	
		IND	I,K,M		5	200	
Active Supply Current (Oscillator Enabled)	ICC2A	VCC2 = 2.0V	CH = 0			0.425	mA
		VCC2 = 5V	D,L			1.28	
Timekeeping Current (Oscillator Enabled)	ICC2T	VCC2 = 2.0V	CH = 0			25.3	µA

		VCC2 = 5V				81	
Standby Current (Oscillator Disabled)		VCC2 = 2.0V	CH = 1			25	
	ICC2S	VCC2 = 5V				80	μA
Trickle-Charge Resistors	R1				2		
	R2				4		kΩ
	R3				8		
Trickle-Charge Diode Voltage Drop	VTD				0.7		V

CAPACITANCE TA = +25°C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Capacitance	CI		10		pF
I/O Capacitance	CI/O		15		pF

AC ELECTRICAL CHARACTERISTICS TA = 0°C to +70°C or TA = -40°C to +85°C.[A]

PARAMETER	SYMBOL		CONDITIONS	MIN	TYP	MAX	UNITS
Data to CLK Setup	tDC	VCC = 2.0V	F	200			ns
		VCC = 5V		50			
CLK to Data Hold	tCDH	VCC = 2.0V	F	280			ns
		VCC = 5V		70			
CLK to Data Delay	tCDD	VCC = 2.0V	F,G,H			800	ns
		VCC = 5V				200	
CLK Low Time	tCL	VCC = 2.0V	F	1000			ns
		VCC = 5V		250			
CLK High Time	tCH	VCC = 2.0V	F	1000			ns
		VCC = 5V		250			
CLK Frequency	tCLK	VCC = 2.0V	F			0.5	MHz
		VCC = 5V		DC		2.0	
CLK Rise and Fall	tR, tF	VCC = 2.0V				2000	ns
		VCC = 5V				500	
CE to CLK Setup	tCC	VCC = 2.0V	F	4			μs
		VCC = 5V		1			
CLK to CE Hold	tCCH	VCC = 2.0V	F	240			ns
		VCC = 5V		60			
CE Inactive Time	tCWH	VCC = 2.0V	F	4			μs
		VCC = 5V		1			
CE to I/O High Impedance	tCDZ	VCC = 2.0V	F			280	ns
		VCC = 5V				70	
SCLK to I/O High Impedance	tCCZ	VCC = 2.0V	F			280	ns
		VCC = 5V				70	

Notes

A.Limits at -40°C are guaranteed by design and are not production tested.
B.All voltages are referenced to ground.
C.I_{CC1T} and I_{CC2T} are specified with I/O open, CE and SCLK set to a logic 0.
D.I_{CC1A} and I_{CC2A} are specified with the I/O pin open, CE high, SCLK = 2MHz at V_{CC} = 5V; SCLK = 500kHz, V_{CC} = 2.0V.
E.CE, SCLK, and I/O all have 40kΩ pulldown resistors to ground.
F.Measured at V_{IH} = 2.0V or V_{IL} = 0.8V and 10ns maximum rise and fall time.
G.Measured at V_{OH} = 2.4V or V_{OL} = 0.4V.
H.Load capacitance = 50pF.
I.I_{CC1S} and I_{CC2S} are specified with CE, I/O, and SCLK open.
J.V_{CC} = V_{CC2}, when V_{CC2} > V_{CC1} + 0.2V; V_{CC} = V_{CC1}, when V_{CC1} > V_{CC2}.
K.V_{CC2} = 0V.
L.V_{CC1} = 0V.

M.Typical values are at +25°C.

Figure 6: Timing Diagram: Read Data Transfer

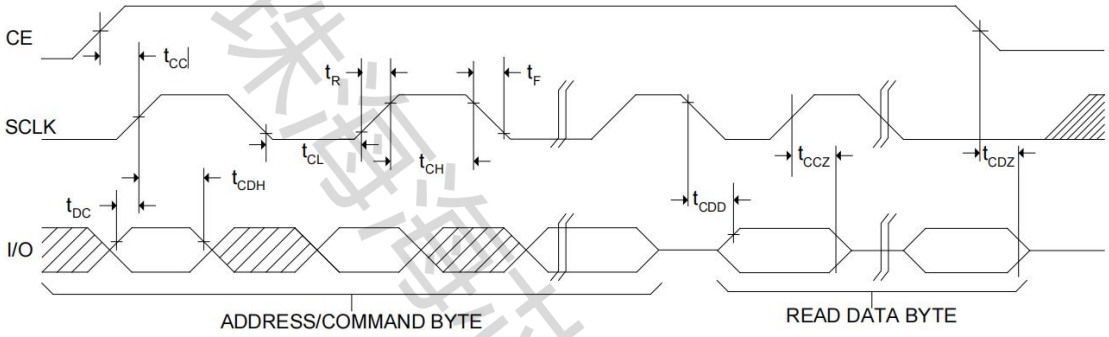
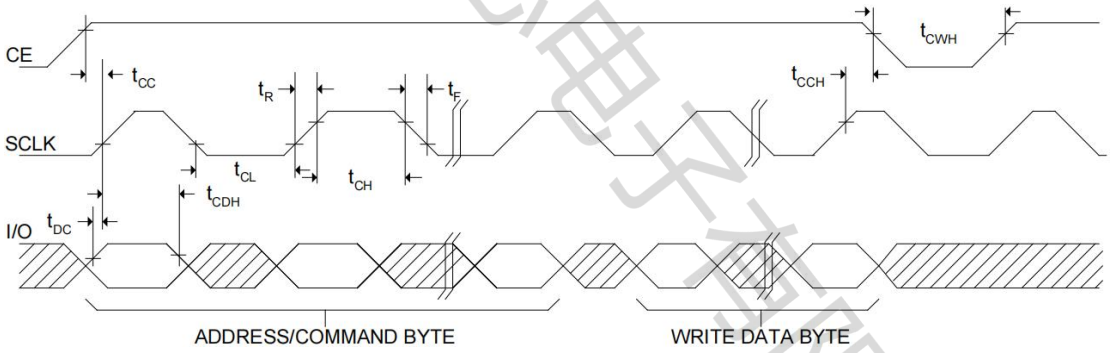


Figure 7: Timing Diagram: Write Data Transfer

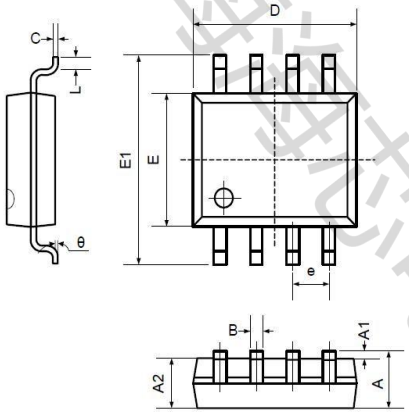


珠海海芯电子有限公司

Package Information

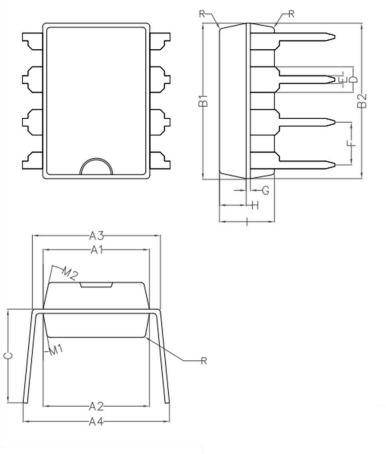
Part Number	Package Type	THETA-JA (°C/W)	THETA-JC (°C/W)	package	quantity
HX1302-S	SOP-8	170	40	Taping	2500
HX1302-P	DIP-8	110	40	Tube-mounted	50

SOP8 (Package Outline Dimensions)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

DIP8 (Package Outline Dimensions)



Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
I	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°

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