深圳市汉昇实业有限公司

HS19264G06A
规格书

	制作	审核	批准
汉昇			

版本：VER 1.0	

深圳市汉昇实业有限公司
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REVISION HISTORY:				
Revision	Date	Description	Written By	Approved By
1.0	2019-05-16	麦克斯 广东 深圳 技术支持加微信 扫一扫上面的二维码图案，加我微信		

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1.0 GENERAL SPECIFICATION

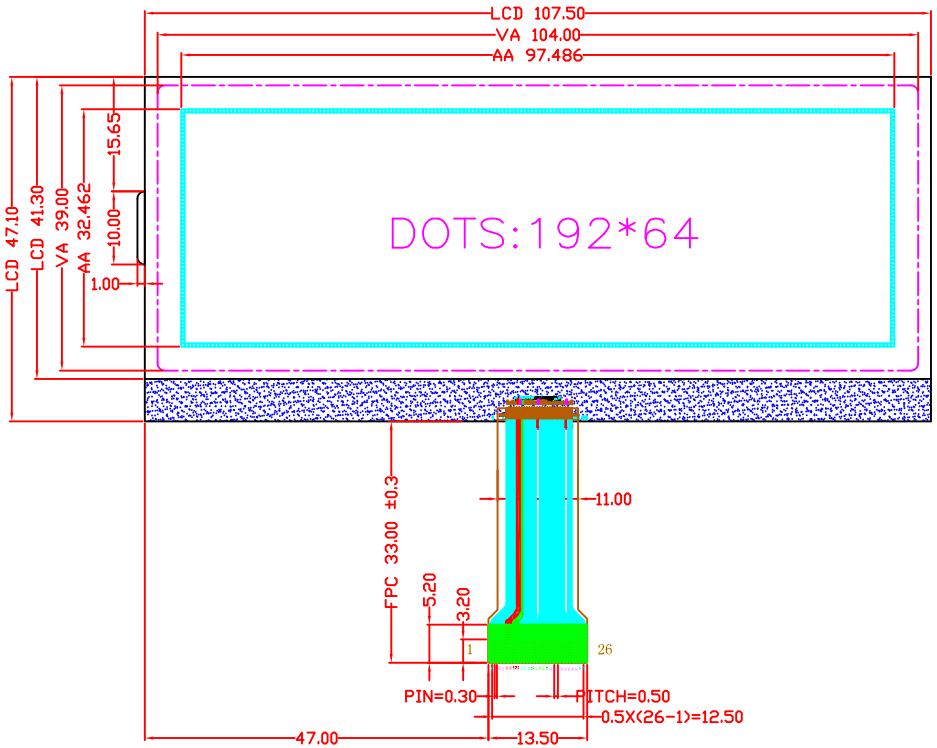
Item	Contents	Unit
LCD type	STN TRANSMISSIVE/NEGATIVE	-
Viewing direction	6:00	O'Clock
Module size (W×H×T)	1075<×47.1×6.1 (excluded FPC length)	mm
Viewing area (W×H)	10; 57×: 9.0	mm
Driver IC	ST7525	-
Number of dots	192×64	-
Backlight type	7LEDS White 2.9V 105mA	-
Interface type	Serial interface	-
Operating temperature	-20 ~ 70	ºC
Storage temperature	-30 ~ 80	ºC

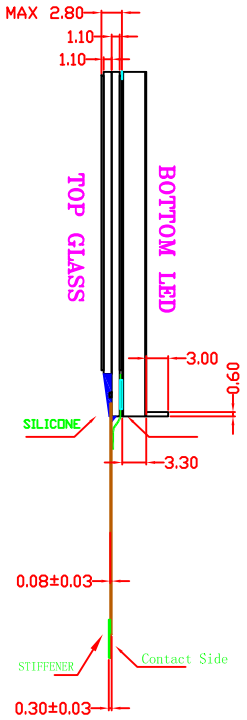
2.0 LCM NUMBERING SYSTEM

HS 19264 G06A
(1) (2) (3)

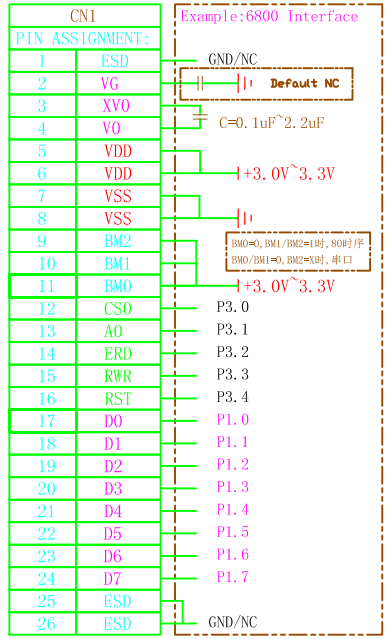
(1) ShenZhen HanshengIndustrail Co Ltd
(2) Number of dots
(3) Serial number

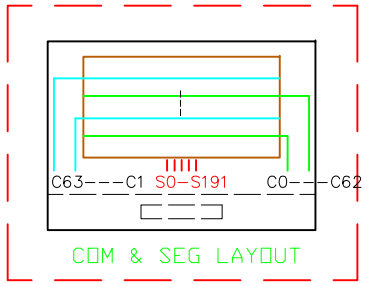
VER.	SYMBOL	AMENDMENT	SIGN	DATE
01	0			

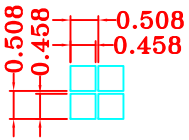




CN1	
PIN ASSIGNMENT:	
1	ESD
2	VG
3	XV0
4	V0
5	VDD
6	VDD
7	VSS
8	VSS
9	BM2
10	BM1
11	BM0
12	CS0
13	A0
14	ERD
15	RWR
16	RST
17	D0
18	D1
19	D2
20	D3
21	D4
22	D5
23	D6
24	D7
25	ESD
26	ESD

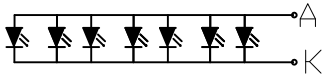






电路：**CIRCUIT DIAGRAM (LED** 1*7=3 **dies)**

电压电流：3.0V-15mA*7



NOTES:

1. DISPLAY TYPE: STN (BLUE)
2. OPERATING VOLTAGE: 12.0 V
3. OPERATING TEMPERATURE: −20°C~70°C
4. STORAGE TEMPERATURE: −30°C~80°C
5. DRIVE MODE: DUTY:1/64; BIAS:1/9
6. VIEWING DIRECTION: 6:00 O'CLOCK
7. POLARIZER TYPE: TRANSMISSIVE/NEGATIVE
8. CONNECTOR: COG/ST7525
9. CUSTOMER No.:
10. FREQUENCY 64HZ
11. Unassigned tolerances ±0.20.
12. (...)IS REFERENCE DIMENSION.

SHENZHEN HANSHENG INDUSTRAIL CO., LTD.

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DESIGNED BY:	HS19264G06A	VERSION: 1.0
CHECKED BY:		NO. 1 OF 2
APPROVED BY:		TOL:±0.2mmif not specity
		UNIT: MM
		DATE: 2020-09-29

4.0 INTERFACE PIN DESCRIPTION

Pin no.	Symbol	Function(parallel)		
1	ESD	the ESD Pin can connect To the Ground		
2	VG	VG is the LCD driving voltage for segment circuits at positive frame		
3	XV0	XV0 is the LCD driving voltage for common circuits at positive frame		
4	V0	V0 is the LCD driving voltage for common circuits at negative frame		
5 6	VDD	Power supply		
7 8	VSS	Ground		
9	BM2	BM0=1,BM1=0,BM2=1 IIC BM0=0,BM1=0,BM2=0 4SPI		
10	BM1	BM0=1,BM1=1,BM2=1 INTER6800		
11	RBM0	BM0=0,BM1=1,BM2=1 INTER8080		
12	CS0	This is the chip select signal. SPI-CS		
13	A0	This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or command.		
14	ERD	68:Read/Write control input pin. 80:Read enable input pin. .		
15	RWR	68:Read/Write control input pin. 80:Write enable input pin.		
16	RST	A reset pin.		
17	D2	Data Bus	Serial clock input	Serialclockinput
18	D1	Data Bus	Serial data input	Serialdatainput
19-24	D2-D7	Data Bus	IIC	SPI
25-26	ESD	The ESD Pin can connect To the Ground		

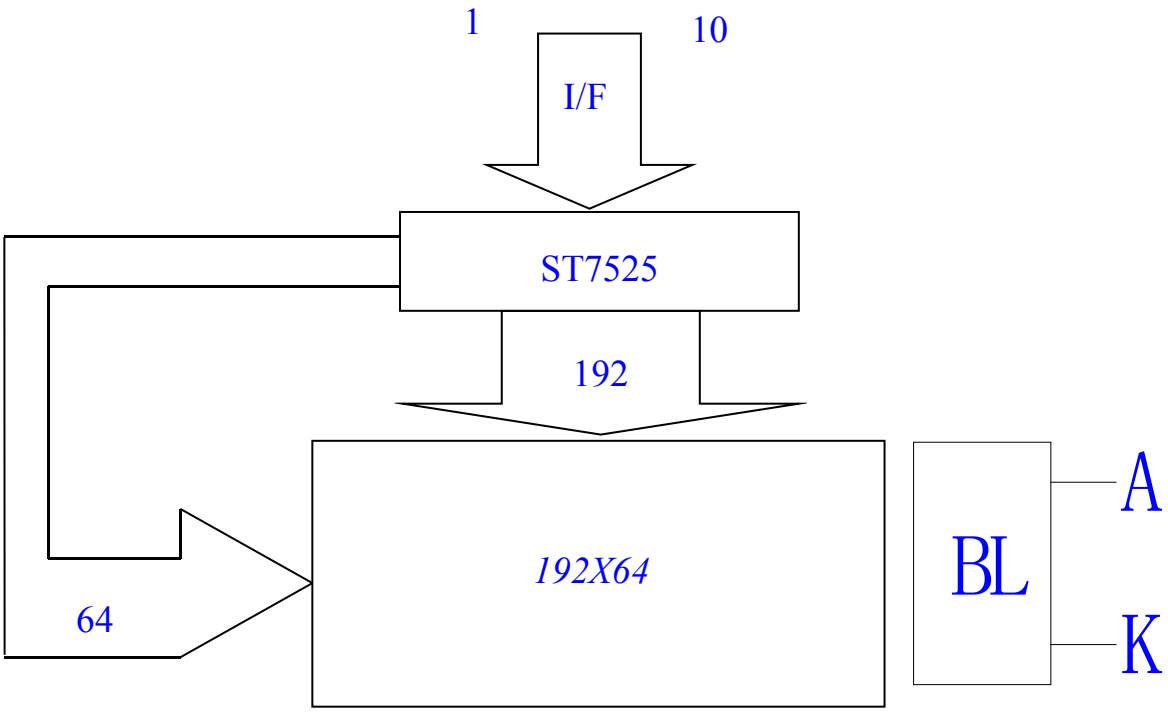
4-line SPI mode:

D0 and D4 must be connected together for SCL. D1 to D3 must be connected together for SDA

I2C interface :

D0 and D4 must be connected together for SCL. D1 to D3 must be connected together for SDA.

5.0 BLOCK DIAGRAM



6.0 OPERATING PRINCIPLE & DRIVING METHOD

COMMAND TABLE											
INSTRUCTION	A0	R/W (RWR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data to DDRAM
Read Data	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from DDRAM Only for parallel interface and I^2C
Read Status Byte (parallel interface)	0	1	ID0	MX	MY	WA	DE	0	0	0	Read status byte Only for parallel interface
			0	0	0	0	0	o	ID2	ID1	
Set Column Address LSB	0	0	0	0	0	0	CA3	CA2	CA1	CA0	Set column address of RAM
Set Column Address MSB	0	0	0	0	0	1	CA7	CA6	CA5	CA4	
Set Scroll Line	0	0	0	1	SL5	SL4	SL3	SL2	SL1	SL0	Specify line address for the 1st display line of DDRAM (vertical scrolling)
Set Page Address	0	0	1	0	1	1	PA3	PA2	PA1	PA0	Set page address of RAM
Set Contrast	0	0	1	0	0	0	0	0	0	1	2-byte instruction. Set Vop voltage
			EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	
Set Partial Screen Mode	0	0	1	0	0	0	0	1	0	PS	PS=1: Enable partial mode
Set RAM Address Control	0	0	1	0	0	0	1	AC2	AC1	AC0	Set column and page address behavior
Set Frame Rate	0	0	1	0	1	0	0	0	FR1	FR0	Set frame frequency
Set All Pixel ON	0	0	1	0	1	0	0	1	0	AP	Set all display segments on
Set Inverse Display	0	0	1	0	1	0	0	1	1	INV	Set inverse display
Set Display Enable	0	0	1	0	1	0	1	1	1	PD	PD=0: Chip is in power down mode
Scan Direction	0	0	1	1	0	0	0	MY	MX	0	Set COM and SEG scan direction
Software Reset	0	0	1	1	1	0	0	0	1	0	Set software reset
NOP	0	0	1	1	1	0	0	0	1	1	No operation
Set Bias	0	0	1	1	1	0	1	0	BR1	BR0	Set internal bias circuit
Set COM End	0	0	1	1	1	1	0	0	0	1	2-byte instruction. Set display duty
			--	--	CEN5	CEN4	CEN3	CEN2	CEN1	CEN0	
Partial Start Address	0	0	1	1	1	1	0	0	1	0	Set partial start for partial display screen
			--	--	DST5	DST 4	DST 3	DST 2	DST 1	DST 0	
Partial End Address	0	0	1	1	1	1	0	0	1	1	Set partial end for partial display screen
			--	--	DEN5	DEN4	DEN3	DEN2	DEN1	DEN0	
Test Control	0	0	1	1	1	1	0	0	0	0	Set test command table
			--	--	--	--	--	--	H1	H0	

Serial Read Command Table (Enabled only in 4 line SPI)										
INSTRUCTION	A0	R/W (RWR)	COMMAND BYTE							DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Read Status Byte	0	0	1	1	1	1	1	1	1	0	Read status byte
	0	1	ID0	MX	MY	WA	DE	0	0	0	
			0	0	0	0	0	0	ID2	ID1	
Read Data	0	0	1	1	1	1	1	1	1	1	Read data from DDRAM
	1	1	D7	D6	D5	D4	D3	D2	D1	D0	

Note: 1. Do not use instructions not listed in these tables (Command Table).

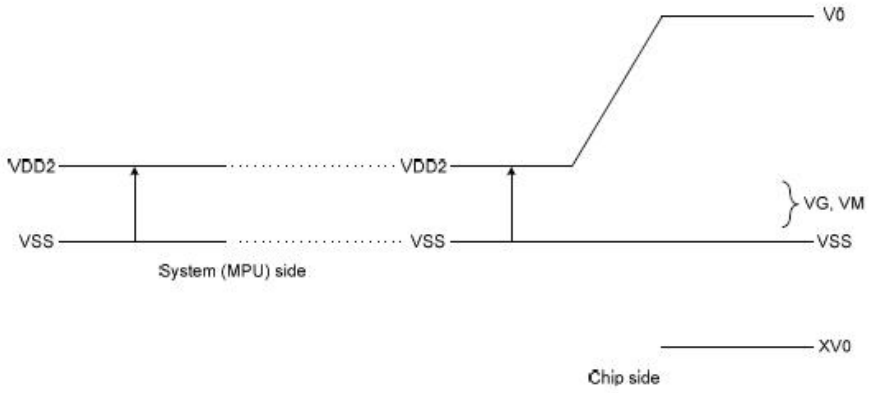
2. "--" = Disabled bit. It can be either logic 0 or 1.

7.0 ABSOLUTE MAXIMUM RATINGS

12. ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System; please refer to notes 1~ 4.

Parameter	Symbol	Conditions	Unit
Digital Power Supply Voltage	VDDI (VDD1)	-0.3 ~ 4.0	V
Analog Power Supply Voltage	VDDA (VDD2 & VDD3)	-0.3 ~ 4.0	V
LCD Power Supply Voltage	V0-XV0	-0.3 ~ 13.5	V
LCD Power Supply Voltage	VG	-0.3 ~ 4.0	V
Input Voltage	VIN	-0.3 ~ VDD1+0.3 *4	V
Operating Temperature	TOPR	-30 to +85	°C
Storage Temperature	TSTR	-55 to +125	°C



Notes

1. Insure the voltage levels of V0, VDDA, VG, VM, VSS and XV0 always match the correct relation while operating: V0 ≥ VDDA > VG > VM > VSS ≥ XV0
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.
3. Stresses exceed the Limiting Values listed above may cause permanent damage to IC. These values are stresses only. IC should be operated under DC/Timing Characteristics condition for normal operation. If this condition is not met, IC operation may be error and the reliability may be deteriorated.
4. VIN should be less than or equal to 3.6V (VIN≦3.6V).

8.0 ELECTRICAL CHARACTERISTICS

13. DC CHARACTERISTICS

VSS=VSS1=VSS2=VSS3=0V; Bare chip; Temp. = -30˚C to +85˚C; unless otherwise specified.

Item	Symbol	Condition		Rating			Unit	Applicable Pin
				Min.	Typ.	Max.		
Operating Voltage (1)	VDD1			1.65	—	3.6	V	VDD1
Operating Voltage (2)	VDD2 VDD3			2.4	—	3.6	V	VDD2 VDD3
LCD Power Supply Voltage	Vop			4.8	—	11.5	V	V0-XV0
Input High-Level Voltage	V_{IHC}			0.7 x VDD1	—	VDD1	V	MPU Interface
Input Low-Level Voltage	V_{ILC}			VSS1	—	0.3 x VDD1	V	MPU Interface
Output High-Level Voltage	V_{OHC}	I_{OUT}=1mA, VDD1=1.8V		0.8 x VDD1	—	VDD1	V	D[7:0]
Output Low-Level Voltage	V_{OLC}	I_{OUT}=-1mA, VDD1=1.8V		VSS1	—	0.2 x VDD1	V	D[7:0]
Input Leakage Current	I_{LI}			-1.0	—	1.0	μA	MPU Interface
LCD Driver ON Resistance	R_{ON}	Ta=25˚C Bias=1/9	Vop=10V, ΔV=1V	—	0.7	—	KΩ	COMx
			VG=2.2V, ΔV=0.22V	—	0.7	—	KΩ	SEGx
Frame Frequency	fFR	1/65 Duty, FR[1:0]=(0,0), Ta = 25℃		72	76	80	Hz	

Note:

- The LCD Output Voltage (Vop) range of the measurement environment is as follows:
  V0 to XV0 : 1uF
- The maximum possible Vop voltage that may be generated is dependent on voltage, temperature and panel loading.

Bare chip current consumption with internal power system:

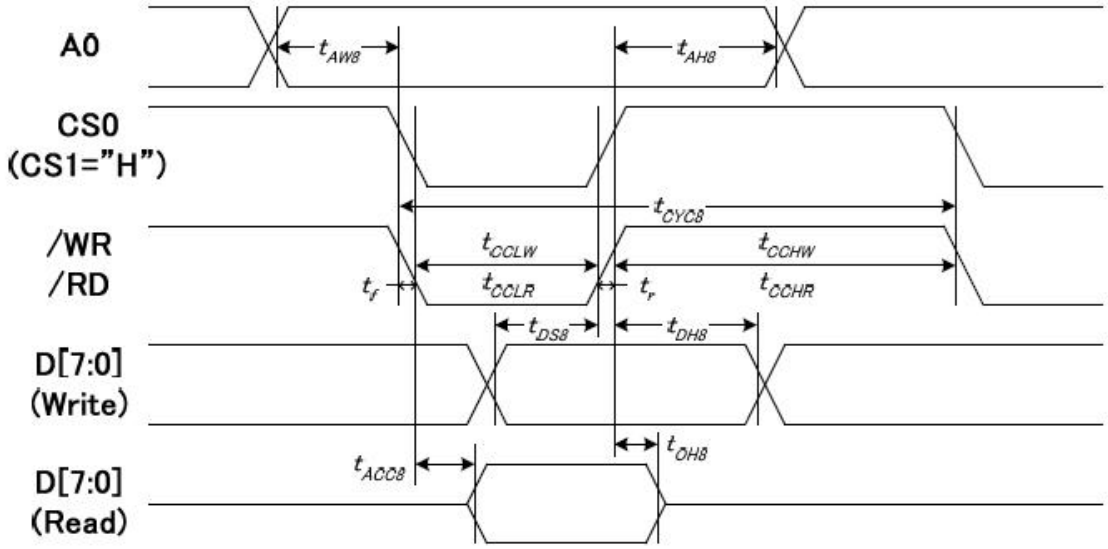
Test Pattern	Symbol	Condition	Rating			Unit	Note
			Min.	Typ.	Max.		
Display Pattern: SNOW (Static)	ISS	VDD1=VDD2=VDD3=3V, Vop=10V, Bias=1/9, Frame Rate=76Hz, Ta=25˚C	—	150	—	μA	
Power Down	ISS	VDD1=VDD2=VDD3=3V, Ta=25˚C	—	2	5	μA	

Note:

The Current Consumption is DC characteristics.

9.0 ELECTRO-OPTICAL CHARACTERISTICS

System Bus Read/Write Characteristics (For the 8080 Series MPU)



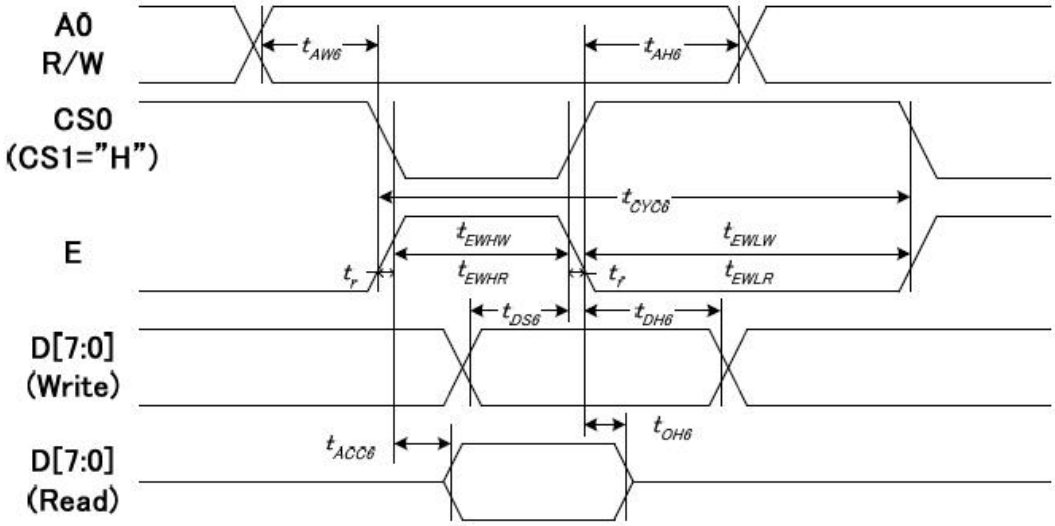
(VDD1 = 1.8V ~ 3.3V, Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		5	-	ns
Address hold time		tAH8		10	-	
System write cycle time	/WR	tCYC8		190	-	
Write L pulse width		tCCLW		80	-	
Write H pulse width		tCCHW		80	-	
Read L pulse width	/RD	tCCLR		100	-	
Read H pulse width		tCCHR		100	-	
Data setup time (Write)	D[7:0]	tDS8		60	-	
Write Data hold time (Write)		tDH8		5	-	

Note :

1. All timing is specified using 20% and 80% of VDD1 as the reference.
2. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≤ (tCYC8 – tCCLR – tCCHR) are specified.
3. tCCLW (tCCLR) is specified as the overlap between CS0 being "L" and /WR (/RD) being "L".

System Bus Read/Write Characteristics (For the 6800 Series MPU)



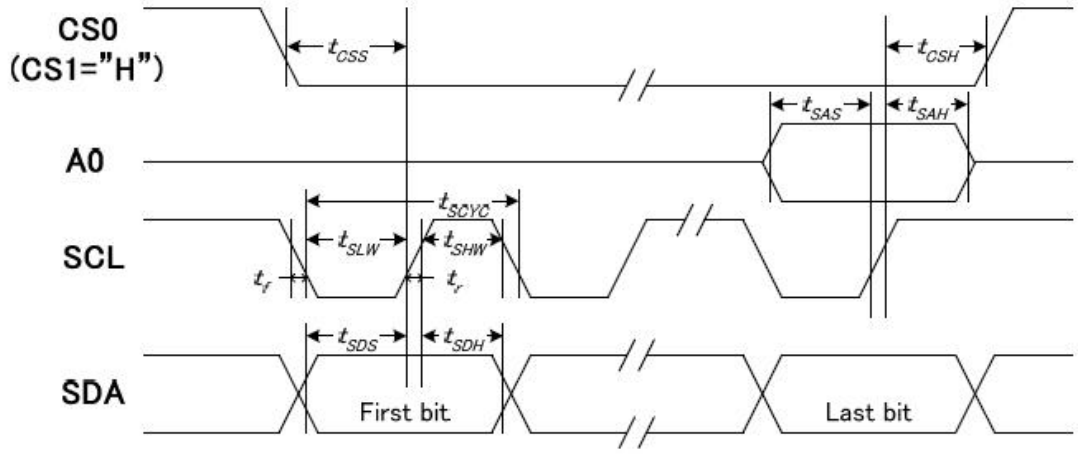
(VDD1 = 1.8V ~ 3.3V, Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Control setup time	A0	tAW6		5	-	ns
Control hold time	R/W	tAH6		10	-	
System cycle time	E	tCYC6		190	-	
Enable H pulse width (WRITE)		tEWHW		80	-	
Enable L pulse width (WRITE)		tEWLW		100	-	
Enable H pulse width (READ)		tEWHR		100	-	
Enable L pulse width (READ)		tEWLR		100	-	
Write data setup time	D[7:0]	tDS6		60	-	
Write data hold time		tDH6		5	-	

Note :

1. All timing is specified using 20% and 80% of VDD1 as the reference.
2. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≤ (tCYC6 – tEWLR – tEWHR) are specified.
3. tEWLW and tEWLR are specified as the overlap between CS0 being "L" and E being "H".

SERIAL INTERFACE (4-Line Interface)



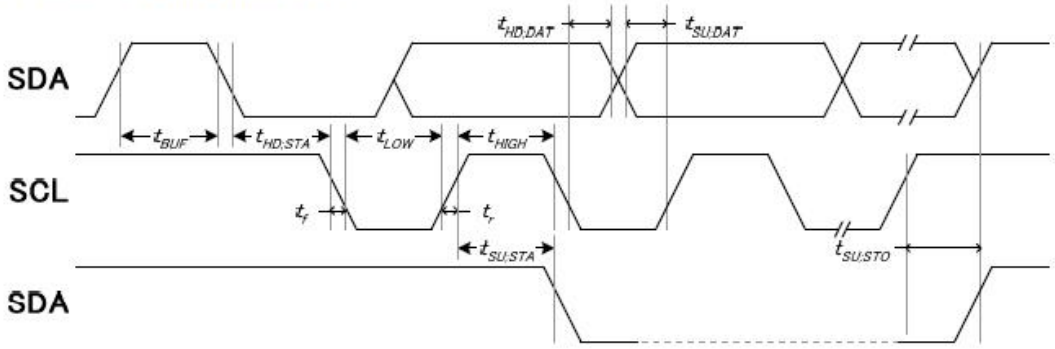
(VDD1 = 1.8V ~ 3.3V, Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		110	-	ns
SCL "H" pulse width		tSHW		40	-	
SCL "L" pulse width		tSLW		40	-	
Address setup time	A0	tSAS		10	-	
Address hold time		tSAH		10	-	
Data setup time	SDA	tSDS		20	-	
Data hold time		tSDH		10	-	
CS0 setup time	CS0	tCSS		20	-	
CS0 hold time		tCSH		10	-	

Note :

1. All timing is specified using 20% and 80% of VDD1 as the standard.
2. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

SERIAL INTERFACE (I²C Interface)



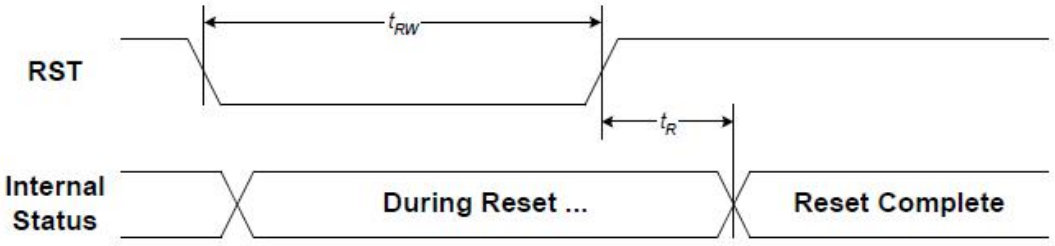
(VDD1 = 1.8V ~ 3.3V, Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
SCL clock frequency	SCL	fSCL		-	400	kHZ
SCL clock low period		tLOW		1.3	-	us
SCL clock high period		tHIGH		0.6	-	
Data set-up time	SDA	tSU;Data		0.1	-	
Data hold time		tHD;Data		0	0.9	
Setup time for a repeated START condition		tSU;STA		0.6	-	
Start condition hold time		tHD;STA		0.6	-	
Setup time for STOP condition		tSU;STO		0.6	-	
Bus free time between a STOP and START		tBUF		0.1	-	
Signal rise time	SCL SDA	tr		20+0.1Cb	300	ns
Signal fall time		tf		20+0.1Cb	300	
Capacitive load represented by each bus line		Cb		-	400	pF
Tolerable spike width on bus		tSW		-	50	ns

Note :

All timing is specified using 20% and 80% of VDD1 as the standard.

RESET TIMING

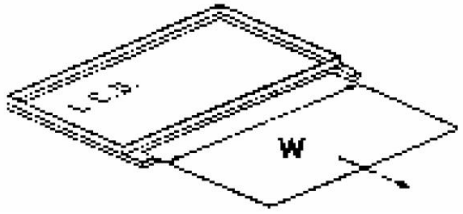


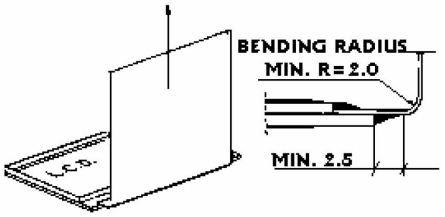
(VDD1 = 1.8V ~ 3.3V, Ta =25°C)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		-	1	ms
Reset "L" pulse width	tRW		1	-	

10.0 STANDARD SPECIFICATION FOR RELIABILITY

10.1 Standard specification of Reliability Test

No.	Test Item	Content of Test	Test Condition
1	High temperature operation	Endurance test applying the high storage temperature for a long time.	+70°C for 500Hrs
2	Low temperature operation	Endurance test applying the low storage temperature for a long time.	-20°C for 500Hrs
3	Low temperature storage	Endurance test applying the low storage temperature for a long time.	-30 °C for 500hrs
4	High temperature storage	Endurance test applying the low storage temperature for a long time.	+80 °C for 500hrs
5	Damp heat Operation	Endurance test applying the electric stress and temperature / humidity stress to the element for a long time.	+60 °C, 95%RH for 500Hrs
6	Thermal cycles operation	Endurance test applying the thermal shock operation for a long time.	Display on , 2h at -30°C ; shift from - 30°C to + 80°C with gradient of 3°C/min; 2 h at 80°C; shift from +80°C to - 30°C with gradient of 2°C/min , repeated 100 times.
7	Thermal shocks	Endurance test applying the thermal shock operation for a long time.	Display off, 1h at -30°C ; shift from - 30°C to + 80°C in 10 s max. 1 h at 80°C; shift from + 80°C to - 30°C in 10 s max. , repeated 100 times
8	Random vibrations	Endurance test applying the vibrations. for a long time when transportation	Test 3 axes during 8 hour/axe - from 5 to 200 Hz: Acc = 10G - from 200 to 500 Hz : Amplitude =5mm – from 5 to 12HZ. Scanning speed= 1 octave / min
9	ESD test	To check the immunity of display to ESD incurred during storage, handling, maintenance and assembly operation.	Discharge resistance = 2kΩ Discharge capacitance = 150pF Number of discharges = 3times Discharge interval = 3 sec Discharge voltage = ± 2 kV on COG connection interface.
10	FPC pull test	To verify the FPC/ glass connection resistance to pull forces applied to the FPC.	 Keeping the LCD fixed, pull the FPC/FFC with a force F= 40 N for cm width of FPC at glass connection.

11	FPC peel test	To verify the FPC/ glass connection resistance to peel forces applied to the FPC.	 Keeping the LCD fixed, pull the FPC/FFC according to the figure above with a force F= 10 N for cm width of FPC at glass connection. The minimum bending radius has to be 2 mm

Remarks:

1) For operation test, above specification is applicable when test pattern is changing during entire operation test.
2) Inspections after reliability tests are performed when the display temperature resumes back to room temperature.
3) It is a normal characteristic that some display abnormality can be seen during reliability test. If the display abnormality can resume back to normal condition at room temperature within 24hours, there is no permanent destruction over the display. The display still possesses its functionality after reliability tests.

10.2 Failure Judgment Criteria

After the reliability tests above, test sample shall be let return to room temperature and humidity for at least 4 hours before final tests are carried out.

Criterion Item	Failure Judgment Criteria
Electrical characteristic	Electrical short and open.
Mechanical characteristic	Out of mechanical specification
Optical characteristic	Out of the Appearance Standard

11.0 QUALITY ASSURANCE

11.1 Inspection Standard

Item	Contents
Objective	This product inspection standard is intended to provide an inspection guideline for the LCD or LCM products manufactured by the Company for automotive customer MM.
Scope	Applicable to the inspection criteria of dimension, appearance, functionality etc.for the LCD or LCM products supplied to the customer MM. Criteria not included in this Inspection Standard will be justified in accordance with any documents agreed upon otherwise.
Inspection Unit	An inspection unit is a unit of display under inspection. The unit for the dimension addressed in this inspection standard is referring to mm, unless otherwise specified.
Inspection System	1： Inspection system includes inspection during production inspection and outgoing product inspection. 2： Process inspection is the inspection for appearance and functionality of the products during the production process. 3： Outgoing inspection is the inspection for the finished products prior to the delivery, based on defined sampling plan.

Inspection Condition	1： Inspection equipments: Equipment and tools used for inspection, measuring and testing during the inspection process. 2：Inspection conditions are described as the following. Distance：40cm between the observer's eyes and the LCD. Viewing angle：according to main viewing direction（MVD）.

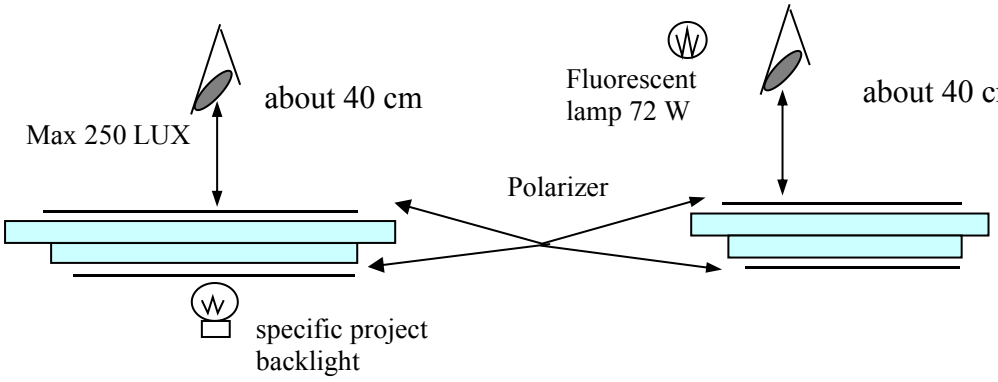


Fig 1
Trasflective or Transmissive LCD/LCM

Fig 2
Reflective LCD/LCM

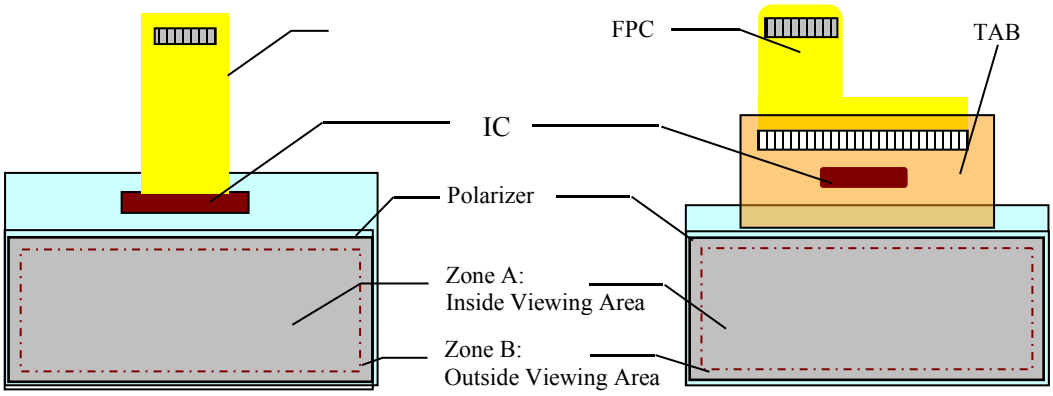
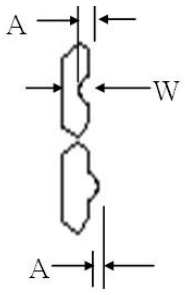
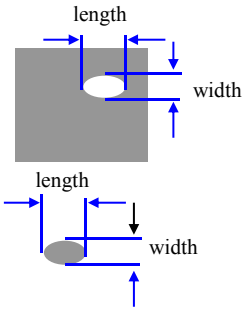


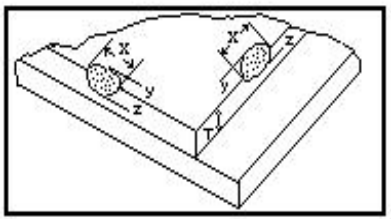
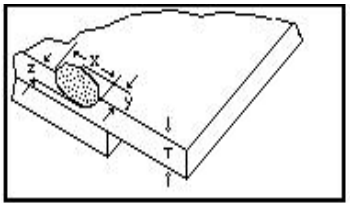
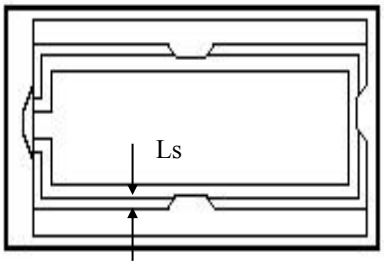
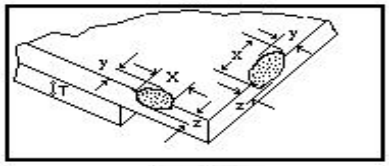
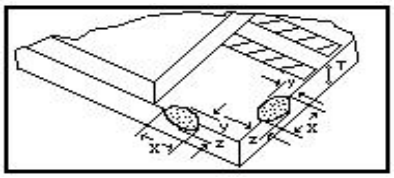
Fig 3
Product Configuration

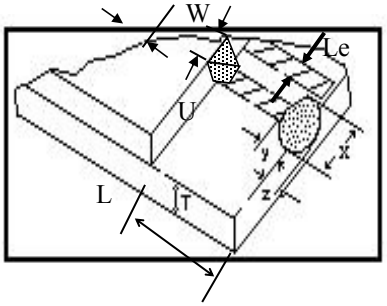
11.2 **Acceptance Criteria** (Zastron internal standard: JU-MM)

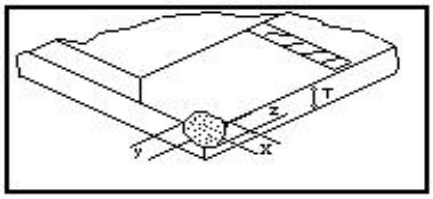
<table>
<tr><th>Inspection Item</th><th>Acceptance/Rejection Criteria</th><th>Defect Classification</th><th>Method</th><th>Applicable Zone</th></tr>
<tr><td>Functional</td><td>1. No display defect is not acceptable.
2. Abnormal display defect is not acceptable.
3. Missing segment and extra segment is not acceptable.
4. Dim contrast or dark contrast is not acceptable.
5. Current consumption (Idd MAX) shall not exceed the limit specified on the MI.
6. Wrong/reversed viewing angle is not acceptable.
7. Uneven contrast or stripe defect shall be in accordance with master sample. (Refer to specified limit sample if applicable)
8. Display character/ pattern shall be referred to the Test Instruction of the related models.</td><td>Major</td><td>Visual</td><td>A</td></tr>
<tr><td>Pattern Deformation</td><td> 

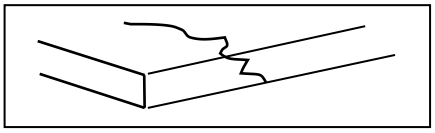
<table>
<tr><th>Size</th><th>Acceptable Number</th></tr>
<tr><td>A≤0.10 or A≤1/4W, whichever is less</td><td>1 per segment
3 per display</td></tr>
<tr><td>A>0.10 or A>1/4W, whichever is less</td><td>Unlimted</td></tr>
</table>
Note: Protrusion shall not cause bridging between adjacent segments</td><td>Major</td><td>Visual
Magnifier</td><td>A</td></tr>
<tr><td>Black or white spots (on pattern), pin hole</td><td> 

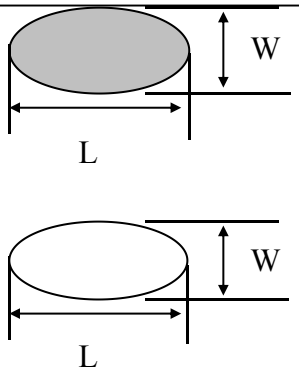
<table>
<tr><th>Size, d (mm)</th><th>Acceptable quantity</th></tr>
<tr><td>d ≤ 0.15</td><td>Unlimited</td></tr>
<tr><td>0.15 < d ≤ 0.25</td><td>1</td></tr>
<tr><td>d > 0.25</td><td>0</td></tr>
<tr><td colspan="2">d = (length + width) / 2</td></tr>
</table>
Note:
Number of spot shall not be more than 1 per each segment.
If 2 spots exist, the distance must be > 20mm between each other</td><td>Minor</td><td>Visual
Magnifier</td><td>A</td></tr>
</table>

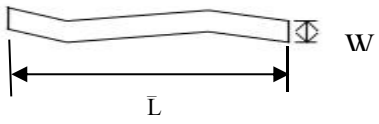
<table>
<tr>
<td>Chip-out</td>
<td>A. General chip-out (for glass edges and glass corner along perimeter seal)
  
 
<table>
<tr><td>X</td><td>Y</td><td>Z</td></tr>
<tr><td>⩽2.0</td><td>⩽1.5 or ⩽Ls, whichever is less</td><td>⩽1/2t</td></tr>
<tr><td>⩽2.0</td><td>⩽1.0 or ⩽Ls, whichever is less</td><td>⩽t</td></tr>
<tr><td colspan="3">X = length parallel with glass edge.
Y = width perpendicular with glass edge
Z = height of glass
t = single glass thickness</td></tr>
</table>
Note:
Chip out shall not reach the perimeter seal.</td>
<td>Minor</td>
<td>Visual Magnifier</td>
<td>B</td>
</tr>
<tr>
<td></td>
<td>B： Chip-out at terminal ledge or back of terminal ledge, but no exactly on terminal
 
 
<table>
<tr><td>X</td><td>Y</td><td>Z</td></tr>
<tr><td>≤2.0</td><td>≤1.5</td><td>≤1/2t</td></tr>
<tr><td>≤2.0</td><td>≤1.0</td><td>≤t</td></tr>
</table>
Note:
In the event that the distance between the chip-out location and the terminal is less than the width of ITO pad Le, the acceptance criteria of chip-out on terminal shall apply.</td>
<td>Minor</td>
<td>Visual Magnifier</td>
<td>B</td>
</tr>
</table>

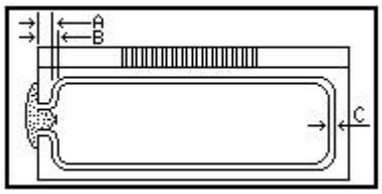
<table>
<tr><td></td><td>C：Chip-out and protuberance at terminals
 

<table>
<tr><th>W</th><th>U</th></tr>
<tr><td colspan="2">Meet the dimension tolerance of the drawing</td></tr>
</table>
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤0.5 Le
& not bridge two adjacent ITO pads.</td><td>≤0.2L or ≤2.0mm whichever is less</td><td>≤1/2t</td></tr>
</table>
Note:
Chip out and protuberance shall not co-exist on the same ITO pad.
Protuberance is not allowed if affect assembly.</td><td>Minor</td><td>Visual
Magni
fier</td><td>B</td></tr>
<tr><td></td><td>D：Chip-out at corner (ITO ledge)
 

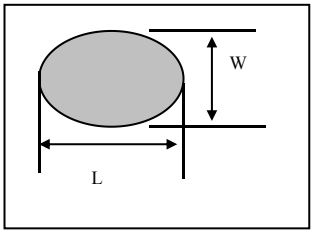
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤2.0</td><td>≤2.0</td><td>≤t</td></tr>
</table></td><td>Minor</td><td>Visual
Magni
fier</td><td>B</td></tr>
<tr><td>Crack line</td><td> 
Crack line is not acceptable.</td><td>Minor</td><td>Visual
Magni
fier</td><td>A &
B</td></tr>
<tr><td>Number of Chip-out</td><td>Maximum acceptable number of chip-out: 2 defects per LCD; 1 defect on ITO ledge.
Distance between chip-out: > 5mm.</td><td>Minor</td><td>Visual</td><td>B</td></tr>
</table>

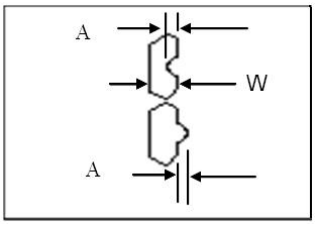
<table>
<tr>
<td>Black spot
White spot
Bubble
Foreign material
Dent</td>
<td> 

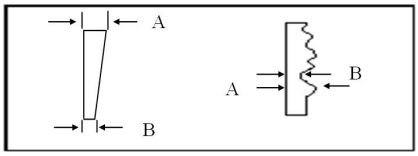
<table>
<tr><th>D</th><th>Acceptable Number</th></tr>
<tr><td>D≤0.15</td><td>Unlimited</td></tr>
<tr><td>0.15＜D≤0.25</td><td>1</td></tr>
<tr><td>D＞0.25</td><td>0</td></tr>
<tr><td colspan="2">Note: If 2 spots exist, the distance must be > 20mm between each other</td></tr>
</table>
D=（L+W）/2</td>
<td>Minor</td>
<td>Visual
Magni
fier</td>
<td>A</td>
</tr>
<tr>
<td>Scratch line
Dark line
Lint</td>
<td> 

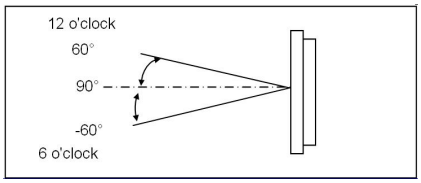
<table>
<tr><th>Length</th><th>Width</th><th>Acceptable Number</th></tr>
<tr><td>L≤3.0</td><td>W≤0.015</td><td>2</td></tr>
<tr><td>L≤1.5</td><td>W≤0.03</td><td>1</td></tr>
<tr><td></td><td>W＞0.03</td><td>0</td></tr>
</table>
Note: If 2 line defects co-exist, the distance must be > 20mm between each other</td>
<td>Minor</td>
<td>Visual
Magni
fier</td>
<td>A</td>
</tr>
<tr>
<td>Endseal</td>
<td> 

<table>
<tr><td>A：Length of end-sealant</td></tr>
<tr><td>B：Length of seal mouth</td></tr>
<tr><td>C：Perimeter seal width</td></tr>
</table>
1.Minimum amount of end-sealant filled, A> 1/3 B
2.Maximum amount of end-sealant shall not spread over to Zone A, Viewing Area (VA).
3.Dimension of end seal shall meet the dimension specified on the drawing.
4.Deformation of perimeter seal which result in perimeter seal becoming less than 1/3 C is not acceptable.</td>
<td>Minor</td>
<td>Visual
Magni
fier</td>
<td>A,B</td>
</tr>
<tr>
<td>Polarizer</td>
<td>Polarizer position shall meet the dimension tolerance indicated on the drawing</td>
<td>Minor</td>
<td>Visual</td>
<td>A,B</td>
</tr>
<tr>
<td>Background color</td>
<td>Background color shall not exceed the range of the limit sample. Obvious uneven coloration (rainbow) shall not be seen.</td>
<td>Minor</td>
<td>Visual</td>
<td>A</td>
</tr>
<tr>
<td rowspan="6">Ink printing</td>
<td>1. Pattern position on the display shall match the MI/drawing.</td>
<td>Major</td>
<td>Visual</td>
<td rowspan="6">A</td>
</tr>
<tr>
<td>2. Pattern appearance shall match the MI/drawing.</td>
<td>Major</td>
<td>Visual</td>
</tr>
<tr>
<td>3. Reverse printing is not acceptable.</td>
<td>Major</td>
<td>Visual</td>
</tr>
<tr>
<td>4. Printing color shall match the master sample.</td>
<td>Major</td>
<td>Visual</td>
</tr>
<tr>
<td>5. Insufficient ink, blur, missing pattern, broken pattern are not acceptable.</td>
<td>Major</td>
<td>Visual</td>
</tr>
<tr>
<td>6. Angle of the printed pattern, the dimension between the pattern and the glass edge shall meet the dimension on the drawing.</td>
<td>Major</td>
<td>Visual</td>
</tr>
</table>

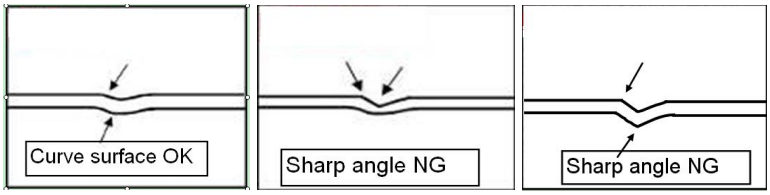
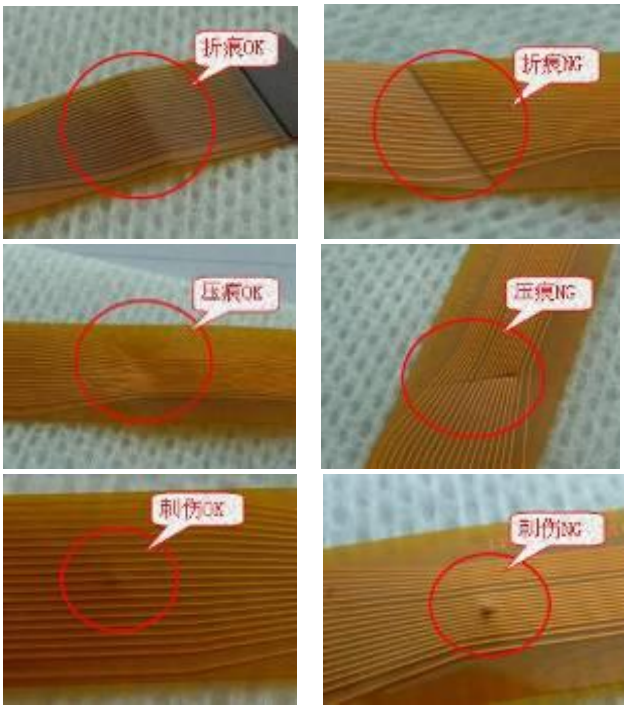
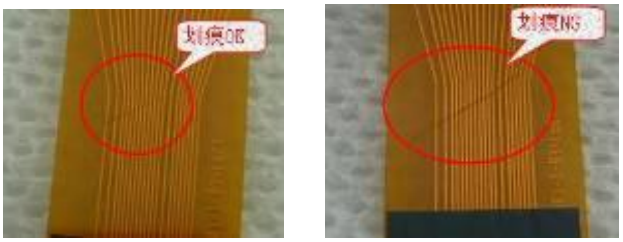
<table>
<tr><td></td><td>7. The printed patterns shall be free of stain, fingeprint and scratch.</td><td>Major</td><td>Visual
Magni
fier</td><td></td></tr>
<tr><td></td><td>8. Spot/pinhole on the pattern.
 

<table>
<tr><td>D</td><td>Acceptable Number</td></tr>
<tr><td>D≤0.15</td><td>Unlimited</td></tr>
<tr><td>0.15＜D≤0.25</td><td>1</td></tr>
<tr><td>D＞0.25</td><td>0</td></tr>
<tr><td colspan="2">Note:
If 2 spots exist, the distance must be > 20mm between each other</td></tr>
</table>
D=（L+W）/2</td><td>Major</td><td>Visual</td><td></td></tr>
<tr><td></td><td>9. Ink pattern deformation
 

Protrusion ≤0.10 or ≤1/4W, whichever is less,
Indentation ≤0.10 or ≤1/4W, whichever is less</td><td>Minor</td><td>Visual
Magni
fier</td><td>A</td></tr>
<tr><td></td><td>10. Ink line deformation
 

A-B≤0.15</td><td>Minor</td><td>Visual
Magni
fier</td><td>A</td></tr>
<tr><td></td><td>11. Pattern misalignment
 

Dimension must meet the requirement on the drawing
For 12 o'clock viewing angle product, light leakage between 90°to 60° shall not be seen.
For 6 o'clock viewing angle product, light leakage between 90°to -60° shall not be seen.</td><td>Minor</td><td>Visual</td><td>A</td></tr>
<tr><td>HSC
FPC
FFC</td><td>1. The outer dimension shall meet the MI/drawing.</td><td>Minor</td><td>Visual</td><td>B</td></tr>
</table>

	2. FPC、HSC、FFC、shall not have folding/stress/dented mark with sharp angle on the surface.  			
	4.Scratch on FPC、HSC、FFC、TAB shall not damage the PI layer and the conductive traces. 			
	5.Goldfinger of FPC、TAB、FFC shall be free of solder。			
	6.Goldfinger of FPC、TAB、FFC shall be max 5% of area of oxidization and corrosion. 	Major	Visual	B

Stiffening tape Identity Label Identity marking	1. The tape sticking position shall meet the requirement on the MI/drawing. 2. Missing label/tape/marking is not acceptable. 3. The format of identification (including date code and product code) shall meet the requirement (eg. label,color marking, inkjet printing) on the MI/drawing.	Minor	Visual	B
Metal bezel	1. Dimension and specification shall meet the requirment on the MI/drawing.	Major	Visual	B
	2.The lock tab of bezel shall not have wrong bending orientation, missing tab, or crack.	Minor		B
	3.Bezel shall be free of rust, twist, deformation,finger print,oil stain and unknown contamination.	Minor		B

12.0 PRECAUTIONS FOR USING LCD MODULE

12.1 Handing Precautions

12.1.1 The display panel is made of glass and polarizer. Do not subject it to mechanical shock by dropping or impact which may cause chipping especially on the edges.

12.1.2 Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead (glass, tweezers, etc.). The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

12.1.3 If the display surface becomes contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with Isopropyl alcohol or ethyl alcohol. Avoid using solvents like acetone (ketene), water, toluene, ethanol to clean the polarizer surface.

12.1.4 Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peel-off may occur with high temperature and high humidity.

12.1.5 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

12.1.6 Install the LCD Module by using the mounting holes. When mounting the LCD module make sure it is free of twisting, warping and distortion.

12.1.7 Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets, moisture condensation or a current flow in a high-humidity environment.

12.1.8 NC terminal should be open. Do not connect anything.

12.1.9 If the logic circuit power is off, do not apply the input signals.

12.1.10 Avoid contacting oil and fats.

12.1.11 Condensation on the surface and contact with terminals due to cold will damage, stain or dirty the polarizers. After products are tested at low temperature they must be warmed up in a container before coming is contacting with room temperature air.

12.1.12 Wipe off saliva or water drops immediately, contact with water over a long period of time may cause deformation or color fading.

12.2 Electro-Static Discharge Control

12.2.1 Since this module uses a CMOS LSI, the same careful attention should be paid to electrostatic discharge as for an ordinary CMOS IC.

12.2.2 Be sure to ground the body when handling the LCD modules. Tools required for assembling, such as soldering irons, must be properly grounded.

12.2.3 To reduce the amount of static electricity generated, do not conduct assembling and other work under dry conditions. To reduce the generation of static electricity, be careful that the air in the work is not too dried. A relative humidity of 50%-60% is recommended.

12.2.4 The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

12.2.5 When soldering the terminal of LCM, make certain the AC power source for the soldering iron does not leak.

12.3 Precaution for soldering to the LCM

12.3.1 Observe the following when soldering lead wire, connector cable and etc. to the LCD module.

- Soldering iron temperature: 300 ~ 350°C.
- Soldering time: ≤ 3 sec.
- Solder: eutectic solder.

Above is a recommended approach based on a 5mm distance between soldering point and pin contact point. Due to different solder composition, actual distance between soldering and contact point, and processing method, it is recommended that customer to study and fine tuning their soldering process parameters accordingly so that the temperature at pin-LCD contact point does not exceed 85°C during soldering..

12.3.2 If soldering flux is used, be sure to remove any remaining flux after finishing to soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended that you protect the LCD surface with a cover during soldering to prevent any damage due to flux spatters.

12.4 Precautions for Operation

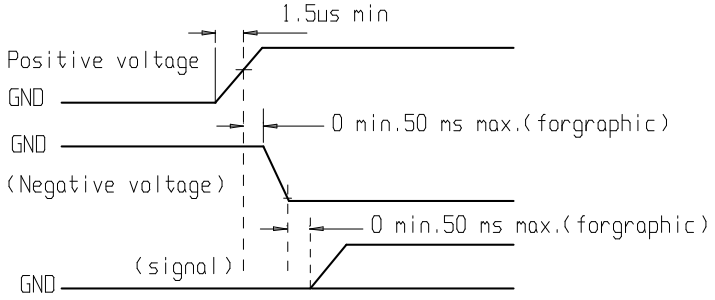
12.4.1 Viewing angle varies with the change of liquid crystal driving voltage (V_O). Adjust V_O to show the best contrast.

12.4.2 Driving the LCD in the voltage above the limit shortens its lifetime.

12.4.3 Response time is greatly delayed at temperature below the operating temperature range. However, it will recover when it returns to the specified temperature range.

12.4.4 If the display area is pushed hard during operation, the display will become abnormal. However, it will return to normal if it is turned off and then back on.

12.4.5 When turning the power on, input each signal after the positive/negative voltage becomes stable (below figure is a general illustration where typical value depends on individual product design).



12.5 Storage

12.5.1 When storing LCDs as spares for some years, the following precautions are necessary.

- Store them in a sealed polyethylene bag. If properly sealed, there is no need for desiccant.
- Store them in a dark place. Do not expose to sunlight or fluorescent light, keep the temperature between 0°C and 35°C.

12.5.2 Environmental conditions:

- Do not leave them for more than 168hrs. at 60°C.
- Should not be left for more than 48hrs. at -20°C.

12.6 Safety

12.6.1 It is recommended to crush damaged or unnecessary LCD into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.

12.6.2 If any liquid leaks out of a damaged glass cell and comes in contact with the hands, wash off thoroughly with soap and water.

13.0 MANUFACTURER CONTACT:

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