1. DESCRIPTION

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register.The circuit contains 46 equivalent gates and features parallel inputs,parallel outputs,right-shift and left-shift serial inputs,operating-mode-control inputs,and a direct overriding clear line.The register has four distinct modes of operation,
namely:

Inhibit clock (do nothing)

Shift right (in the direction QA toward QD)

Shift left (in the direction QD toward QA)

Parallel (broadside) load

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs,S0 and S1,high.The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input.During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low.Serial data for this mode is entered at the shift-right data input.When S0 is low and S1 is high,data shifts left synchronously and new data is entered at the shift -left serial input.

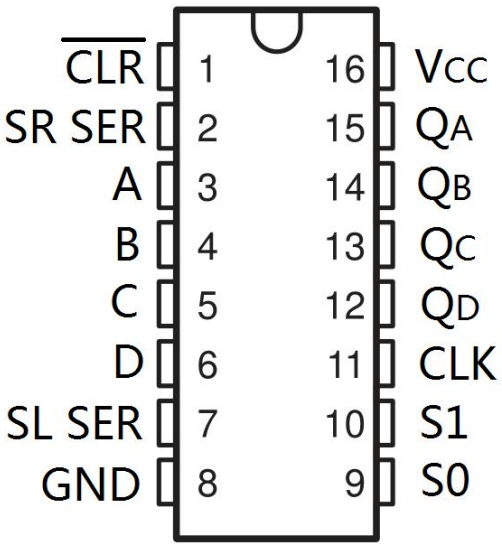
Clocking of the shift register is inhibited when both mode control inputs are low.

2. FEATURES

- Parallel Inputs and Outputs
- Four Operating Modes:
  - Synchronous Parallel Load
  - Right Shift
  - Left Shift
  - Do Nothing
- Positive Edge-Triggered Clocking
- Direct Overriding Clear

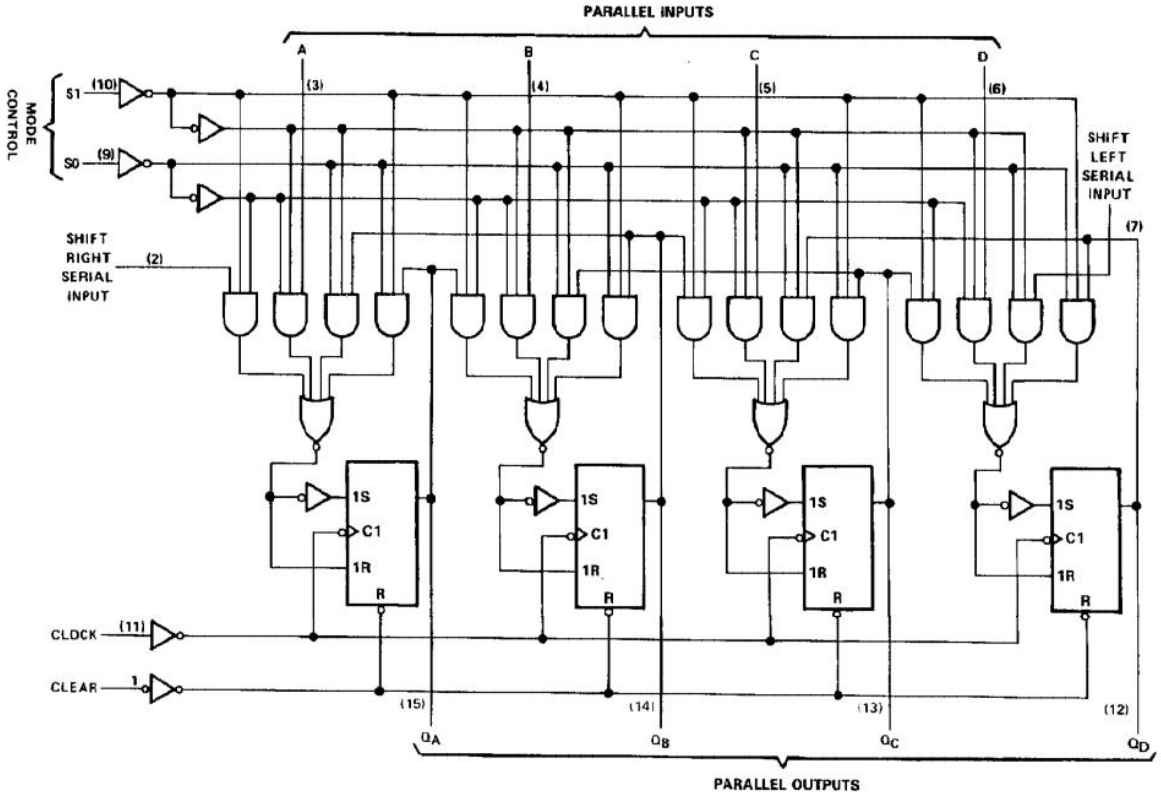
3. PIN CONFIGURATIONS

(TOP VIEW)

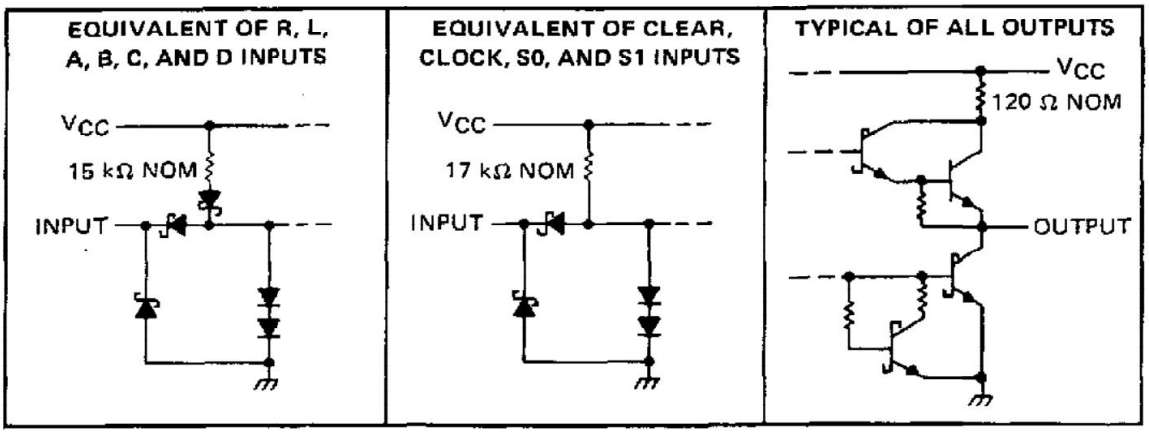


INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

4. LOGIC DIAGRAM



5. SCHEMATICS OF INPUTS AND OUTPUTS



6. ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTES)

Supply voltage, V_{CC} 7V

Input voltage, VI: 74LS194..... 7V

Operating free-air temperature range: DIP package..... 0°C to 70°C

Storage temperature range, Tstg..... −65°C to 150°C

7. RECOMMENDED OPERATING CONDITIONS

		74LS194			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.75	5	5.25	V
I_{OH}	High-level output current			−400	μA
I_{OL}	Low-level output current			8	mA
f_{clock}	Clock frequency	0		25	MHz
t_w	Width of any input pulse	20			ns
t_{su}	Clear inactive-state setup time	30			ns
	Load inactive-state setup time	20			ns
	Data setup time	25			ns
t_h	Data hold time	0			ns
T_A	Operating free-air temperature range	0		70	°C

8. ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR RANGE (UNLESS OTHERWISE NOTED)

PARAMETER		TEST CONDITIONS†		74LS194			UNIT
				MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} MAX	V_{IH} = 2 V, I_{OH} = −400 μA	2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} MAX	I_{OL} = 4 mA		0.25	0.4	V
			I_{OL} = 8 mA		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX			15	23	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

9. SWITCHING CHARACTERISTICS,VCC = 5 V, TA = 25℃

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 15 pF, R_L = 2 kΩ	25	36		MHz
t_{PHL}	Propagation delay time,high-to-low-level output from clear			19	30	ns
t_{PLH}	Propagation delay time,low-to-high-level output from clear			14	22	ns
t_{PHL}	Propagation delay time,high-to-low-level output from clear			17	26	ns

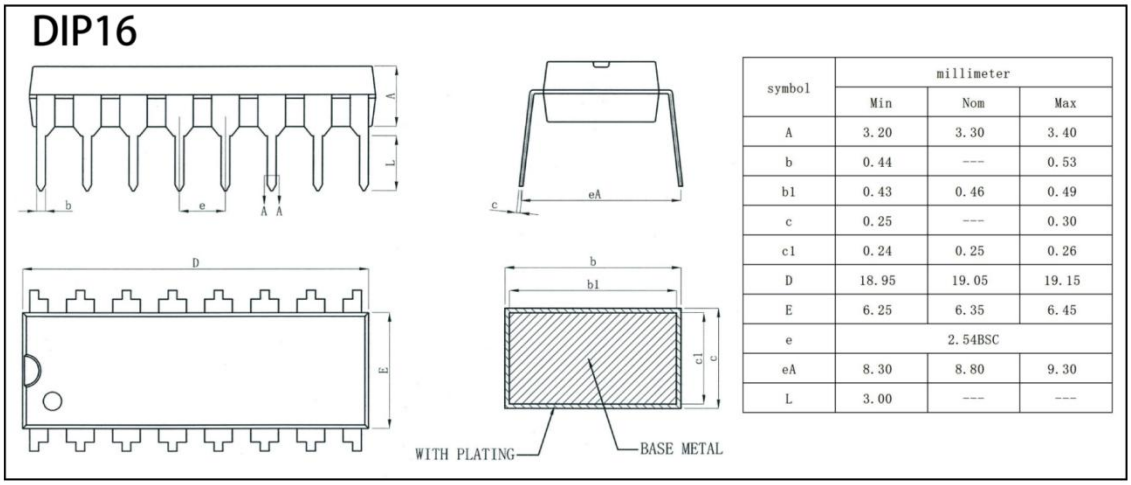
† t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

10. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XD74LS194	XD74LS194	DIP16	19.05 * 6.35	-0 to 70	MSL3	Tube 25	1000

11. DIMENSIONAL DRAWINGS



symbol	millimeter		
	Min	Nom	Max
A	3.20	3.30	3.40
b	0.44	---	0.53
b1	0.43	0.46	0.49
c	0.25	---	0.30
c1	0.24	0.25	0.26
D	18.95	19.05	19.15
E	6.25	6.35	6.45
e	2.54BSC		
eA	8.30	8.80	9.30
L	3.00	---	---