19-2786; Rev 1; 12/03

MAXIM

# 3.3V, 16-Bit, 200Msps High Dynamic Performance DAC with CMOS Inputs



## General Description

The MAX5885 is an advanced, 16-bit, 200Msps digital-to-analog converter (DAC) designed to meet the demanding performance requirements of signal synthesis applications found in wireless base stations and other communications applications. Operating from a single 3.3V supply, this DAC offers exceptional dynamic performance such as 77dBc spurious-free dynamic range (SFDR) at $f_{OUT}$ = 10MHz. The DAC supports update rates of 200Msps at a power dissipation of less than 200mW.

The MAX5885 utilizes a current-steering architecture, which supports a full-scale output current range of 2mA to 20mA, and allows a differential output voltage swing between 0.1$V_{P-P}$ and 1$V_{P-P}$.

The MAX5885 features an integrated 1.2V bandgap reference and control amplifier to ensure high accuracy and low noise performance. Additionally, a separate reference input pin enables the user to apply an external reference source for optimum flexibility and to improve gain accuracy.

The digital and clock inputs of the MAX5885 are designed for CMOS-compatible voltage levels. The MAX5885 is available in a 48-pin QFN package with an exposed paddle (EP) and is specified for the extended industrial temperature range (-40°C to +85°C).

Refer to the MAX5883 and MAX5884 data sheets for pin-compatible 12- and 14-bit versions of the MAX5885. For LVDS high-speed versions, refer to the MAX5886/MAX5887/MAX5888 data sheet.

## Applications

Base Stations: Single/Multicarrier UMTS, CDMA, GSM

Communications: LMDS, MMDS, Point-to-Point Microwave

Digital Signal Synthesis

Automated Test Equipment (ATE)

Instrumentation

## Features

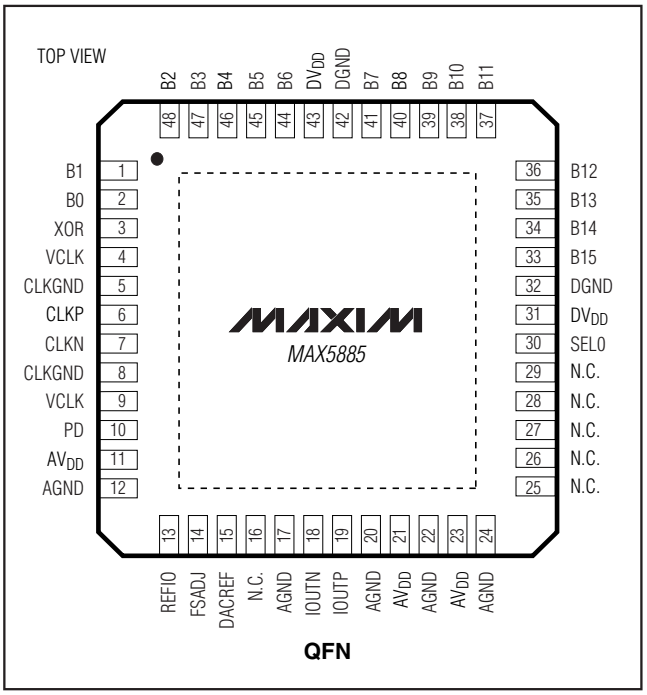
- **200Msps Output Update Rate**
- **Single 3.3V Supply Operation**
- **Excellent SFDR and IMD Performance**
  **SFDR = 77dBc at $f_{OUT}$ = 10MHz (to Nyquist)**
  **IMD = -88dBc at $f_{OUT}$ = 10MHz**
  **ACLR = 74dB at $f_{OUT}$ = 30.72MHz**
- **2mA to 20mA Full-Scale Output Current**
- **CMOS-Compatible Digital and Clock Inputs**
- **On-Chip 1.2V Bandgap Reference**
- **Low Power Dissipation**
- **48-Pin QFN-EP Package**

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX5885EGM | -40°C to +85°C | 48 QFN-EP* |

**EP = Exposed paddle.*

## Pin Configuration






**For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.**

# 3.3V, 16-Bit, 200Msps High Dynamic Performance DAC with CMOS Inputs

## ABSOLUTE MAXIMUM RATINGS

$AV_{DD}$, $DV_{DD}$, VCLK to AGND .....-0.3V to +3.9V
$AV_{DD}$, $DV_{DD}$, VCLK to DGND .....-0.3V to +3.9V
$AV_{DD}$, $DV_{DD}$, VCLK to CLKGND .....-0.3V to +3.9V
AGND, CLKGND to DGND.....-0.3V to +0.3V
DACREF, REFIO, FSADJ to AGND.....-0.3V to $AV_{DD}$ + 0.3V
IOUTP, IOUTN to AGND.....-1V to $AV_{DD}$ + 0.3V
CLKP, CLKN to CLKGND.....-0.3V to VCLK + 0.3V
B0–B15, SEL0, PD, XOR to DGND.....-0.3V to $DV_{DD}$ + 0.3V

Continuous Power Dissipation ($T_A$ = +70°C)
48-Pin QFN (derate 27mW/°C above +70°C).....2162.2mW
Thermal Resistance ($\theta_{JA}$) .....+37°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($AV_{DD}$ = $DV_{DD}$ = VCLK = 3.3V, AGND = DGND = CLKGND = 0V, external reference, $V_{REFIO}$ = 1.25V, $R_L$ = 50Ω, $I_{OUT}$ = 20mA, $f_{CLK}$ = 200Msps, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. ≥+25°C guaranteed by production test, <+25°C guaranteed by design and characterization. Typical values are at $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **STATIC PERFORMANCE** | | | | | | | |
| Resolution | | | | | 16 | | Bits |
| Integral Nonlinearity | INL | Measured differentially | | | ±0.006 | | %FS |
| Differential Nonlinearity | DNL | Measured differentially | | | ±0.003 | | %FS |
| Offset Error | OS | | | -0.025 | ±0.003 | +0.025 | %FS |
| Offset Drift | | | | | ±50 | | ppm/°C |
| Full-Scale Gain Error | $GE_{FS}$ | External reference, $T_A$ ≥ +25°C | | -3.5 | | +1.3 | %FS |
| Gain Drift | | Internal reference | | | ±100 | | ppm/°C |
| | | External reference | | | ±50 | | |
| Full-Scale Output Current | $I_{OUT}$ | (Note 1) | | 2 | | 20 | mA |
| Min Output Voltage | | Single ended | | | -0.5 | | V |
| Max Output Voltage | | Single ended | | | 1.1 | | V |
| Output Resistance | $R_{OUT}$ | | | | 1 | | MΩ |
| Output Capacitance | $C_{OUT}$ | | | | 5 | | pF |
| **DYNAMIC PERFORMANCE** | | | | | | | |
| Output Update Rate | $f_{CLK}$ | | | 1 | | 200 | Msps |
| Noise Spectral Density | | $f_{CLK}$ = 100MHz | $f_{OUT}$ = 16MHz, -12dB FS | | -155 | | dB FS/ Hz |
| | | $f_{CLK}$ = 200MHz | $f_{OUT}$ = 80MHz, -12dB FS | | -148 | | |
| Spurious-Free Dynamic Range to Nyquist | SFDR | $f_{CLK}$ = 100MHz | $f_{OUT}$ = 1MHz, 0dB FS | | 88 | | dBc |
| | | | $f_{OUT}$ = 1MHz, -6dB FS | | 83 | | |
| | | | $f_{OUT}$ = 1MHz, -12dB FS | | 80 | | |

## ELECTRICAL CHARACTERISTICS (continued)

($AV_{DD}$ = $DV_{DD}$ = VCLK = 3.3V, AGND = DGND = CLKGND = 0V, external reference, $V_{REFIO}$ = 1.25V, $R_L$ = 50Ω, $I_{OUT}$ = 20mA, $f_{CLK}$ = 200Msps, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. ≥+25°C guaranteed by production test, <+25°C guaranteed by design and characterization. Typical values are at $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Spurious-Free Dynamic Range to Nyquist | SFDR | $f_{CLK}$ = 100MHz | $f_{OUT}$ = 10MHz, -12dB FS | | 77 | | dBc |
| | | | $f_{OUT}$ = 30MHz, -12dB FS | | 73 | | |
| | | $f_{CLK}$ = 200MHz | $f_{OUT}$ = 10MHz, -12dB FS | | 72 | | |
| | | | $f_{OUT}$ = 16MHz, -12dB FS, $T_A$ ≥+25°C | 68 | 76 | | |
| | | | $f_{OUT}$ = 30MHz, -12dB FS | | 71 | | |
| | | | $f_{OUT}$ = 50MHz, -12dB FS | | 71 | | |
| Two-Tone IMD | TTIMD | $f_{CLK}$ = 100MHz | $f_{OUT1}$ = 9MHz, -6dB FS | | -88 | | dBc |
| | | | $f_{OUT2}$ = 10MHz, -6dB FS | | | | |
| | | $f_{CLK}$ = 200MHz | $f_{OUT1}$ = 29MHz, -6dB FS | | -74 | | |
| | | | $f_{OUT2}$ = 30MHz, -6dB FS | | | | |
| Four-Tone IMD, 1MHz Frequency Spacing, GSM Model | FTIMD | $f_{CLK}$ = 150MHz | $f_{OUT}$ = 31.99MHz, -12dB FS | | -82 | | dBc |
| Adjacent Channel Leakage Power Ratio, 4.1MHz Bandwidth, WCDMA Model | ACLR | $f_{CLK}$ = 184.32MHz | $f_{OUT}$ = 30.72MHz | | 74 | | dB |
| Output Bandwidth | $BW_{-1dB}$ | (Note 2) | | | 450 | | MHz |
| **REFERENCE** | | | | | | | |
| Internal Reference Voltage Range | $V_{REFIO}$ | | | 1.1 | 1.21 | 1.34 | V |
| Reference Input Compliance Range | $V_{REFIOCR}$ | | | 0.125 | | 1.25 | V |
| Reference Input Resistance | $R_{REFIO}$ | | | | 10 | | kΩ |
| Reference Voltage Drift | $TCO_{REF}$ | | | | ±50 | | ppm/°C |
| **ANALOG OUTPUT TIMING** | | | | | | | |
| Output Fall Time | $t_{FALL}$ | 90% to 10% (Note 3) | | | 375 | | ps |
| Output Rise Time | $t_{RISE}$ | 10% to 90% (Note 3) | | | 375 | | ps |
| Output Voltage Settling Time | $t_{SETTLE}$ | Output settles to 0.025% FS (Note 3) | | | 11 | | ns |
| Output Propagation Delay | $t_{PD}$ | (Note 3) | | | 1.8 | | ns |
| Glitch Energy | | | | | 1 | | pV-s |
| Output Noise | $N_{OUT}$ | $I_{OUT}$ = 2mA | | | 30 | | pA/√Hz |
| | | $I_{OUT}$ = 20mA | | | 30 | | |
| **TIMING CHARACTERISTICS** | | | | | | | |
| Data to Clock Setup Time | $t_{SETUP}$ | Referenced to rising edge of clock (Note 4) | | 0.4 | | | ns |
| Data to Clock Hold Time | $t_{HOLD}$ | Referenced to rising edge of clock (Note 4) | | 1.25 | | | ns |

# 3.3V, 16-Bit, 200Msps High Dynamic Performance DAC with CMOS Inputs

## ELECTRICAL CHARACTERISTICS (continued)

($AV_{DD}$ = $DV_{DD}$ = VCLK = 3.3V, AGND = DGND = CLKGND = 0V, external reference, $V_{REFIO}$ = 1.25V, $R_L$ = 50Ω, $I_{OUT}$ = 20mA, $f_{CLK}$ = 200Msps, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. ≥+25°C guaranteed by production test, <+25°C guaranteed by design and characterization. Typical values are at $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Data Latency | | | | 3.5 | | Clock cycles |
| Minimum Clock Pulse Width High | $t_{CH}$ | CLKP, CLKN | | 1.5 | | ns |
| Minimum Clock Pulse Width Low | $t_{CL}$ | CLKP, CLKN | | 1.5 | | ns |
| **CMOS LOGIC INPUTS (B0–B15, PD, SEL0, XOR)** | | | | | | |
| Input Logic High | $V_{IH}$ | | 0.7 x $DV_{DD}$ | | | V |
| Input Logic Low | $V_{IL}$ | | | | 0.3 x $DV_{DD}$ | V |
| Input Leakage Current | $I_{IN}$ | | -15 | | +15 | µA |
| Input Capacitance | $C_{IN}$ | | | 5 | | pF |
| **CLOCK INPUTS (CLKP, CLKN)** | | | | | | |
| Differential Input Voltage Swing | $V_{CLK}$ | Sine wave | | ≥1.5 | | $V_{P-P}$ |
| | | Square wave | | ≥0.5 | | |
| Differential Input Slew Rate | $SR_{CLK}$ | (Note 5) | | >100 | | V/µs |
| Common-Mode Voltage Range | $V_{COM}$ | | | 1.5 ±20% | | V |
| Input Resistance | $R_{CLK}$ | | | 5 | | kΩ |
| Input Capacitance | $C_{CLK}$ | | | 5 | | pF |
| **POWER SUPPLIES** | | | | | | |
| Analog Supply Voltage Range | $AV_{DD}$ | | 3.135 | 3.3 | 3.465 | V |
| Digital Supply Voltage Range | $DV_{DD}$ | | 3.135 | 3.3 | 3.465 | V |
| Clock Supply Voltage Range | $V_{CLK}$ | | 3.135 | 3.3 | 3.465 | V |
| Analog Supply Current | $I_{AVDD}$ | $f_{CLK}$ = 100Msps, $f_{OUT}$ = 1MHz | | 27 | | mA |
| | | Power-down | | 0.3 | | |
| Digital Supply Current | $I_{DVDD}$ | $f_{CLK}$ = 100Msps, $f_{OUT}$ = 1MHz | | 8.5 | | mA |
| | | Power-down | | 10 | | µA |
| Clock Supply Current | $I_{VCLK}$ | $f_{CLK}$ = 100Msps, $f_{OUT}$ = 1MHz | | 5.5 | | mA |
| | | Power-down | | 10 | | µA |
| Power Dissipation | $P_{DISS}$ | $f_{CLK}$ = 100Msps, $f_{OUT}$ = 1MHz | | 135 | | mW |
| | | Power-down | | 1 | | |
| Power-Supply Rejection Ratio | PSRR | $AV_{DD}$ = VCLK = $DV_{DD}$ = 3.3V ±5% (Note 5) | -0.1 | | +0.1 | %FS/V |

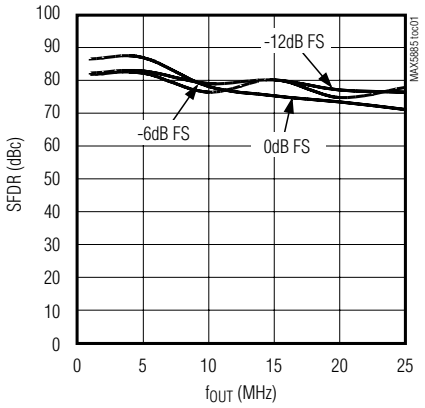
**Note 1:** Nominal full-scale current $I_{OUT} = 32 \times I_{REF}$.
**Note 2:** This parameter does not include update-rate depending effects of sin(x)/x filtering inherent in the MAX5885.
**Note 3:** Parameter measured single ended into a 50Ω termination resistor.
**Note 4:** Parameter guaranteed by design.
**Note 5:** Parameter defined as the change in midscale output caused by a ±5% variation in the nominal supply voltage.

# 3.3V, 16-Bit, 200Msps High Dynamic Performance DAC with CMOS Inputs

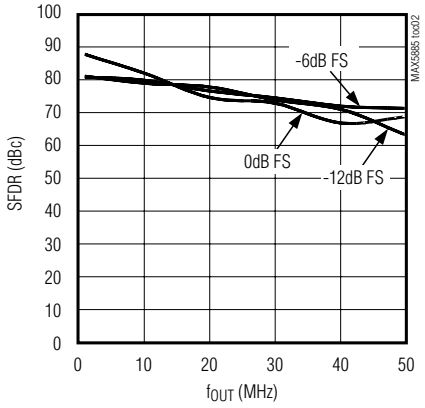
## Typical Operating Characteristics

($AV_{DD}$ = $DV_{DD}$ = VCLK = 3.3V, external reference, $V_{REFIO}$ = 1.25V, $R_L$ = 50Ω, $I_{OUT}$ = 20mA, $T_A$ = +25°C, unless otherwise noted.)

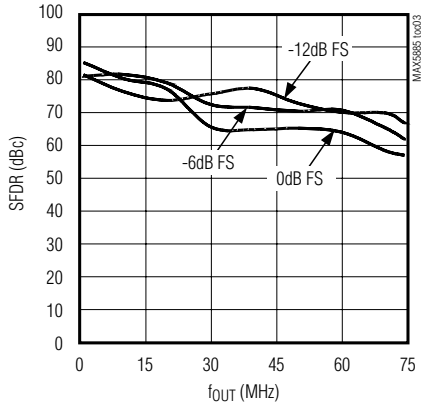
**SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY ($f_{CLK}$ = 50MHz)**



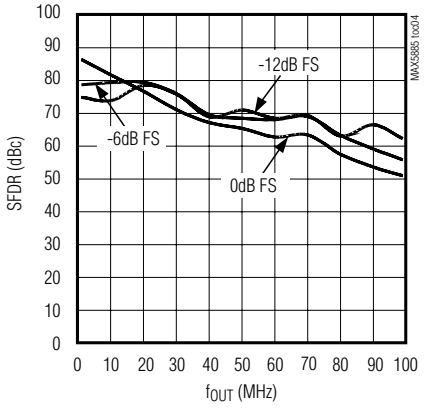

**SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY ($f_{CLK}$ = 100MHz)**



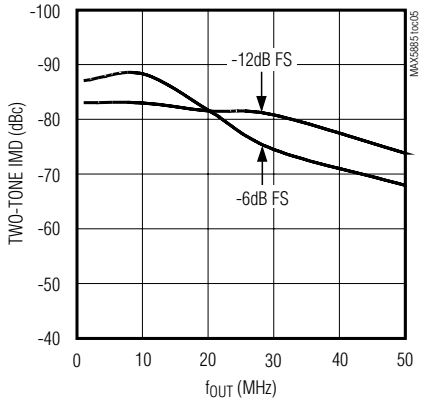

**SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY ($f_{CLK}$ = 150MHz)**



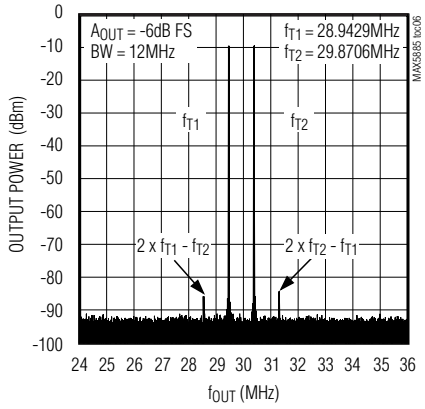

**SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY ($f_{CLK}$ = 200MHz)**



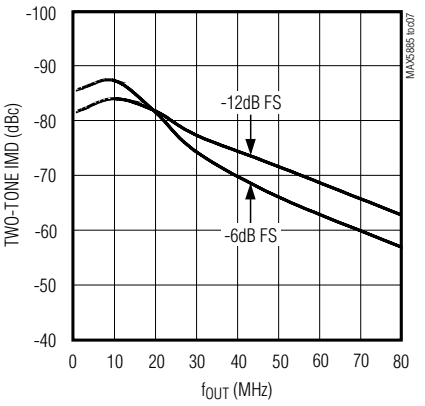

**TWO-TONE IMD vs. OUTPUT FREQUENCY (1MHz CARRIER SPACING, $f_{CLK}$ = 100MHz)**



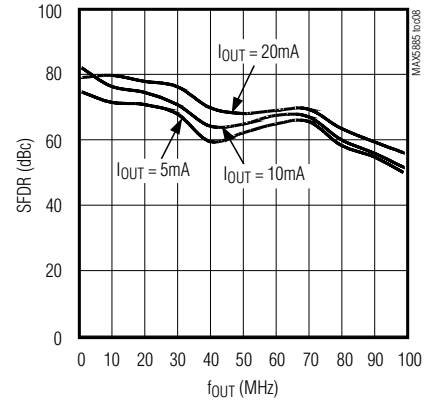

**TWO-TONE INTERMODULATION DISTORTION ($f_{CLK}$ = 100MHz)**



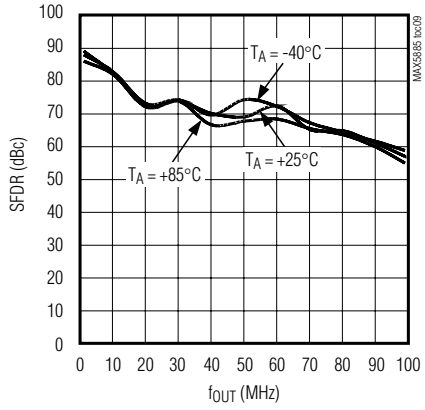

**TWO-TONE IMD vs. OUTPUT FREQUENCY (1MHz CARRIER SPACING, $f_{CLK}$ = 200MHz)**




**SFDR vs. OUTPUT FREQUENCY ($f_{CLK}$ = 200MHz, $A_{OUT}$ = -6dB FS)**




**SFDR vs. $f_{OUT}$ AND TEMPERATURE ($f_{CLK}$ = 200MHz, $A_{OUT}$ = -6dB FS, $I_{FS}$ = 20mA)**

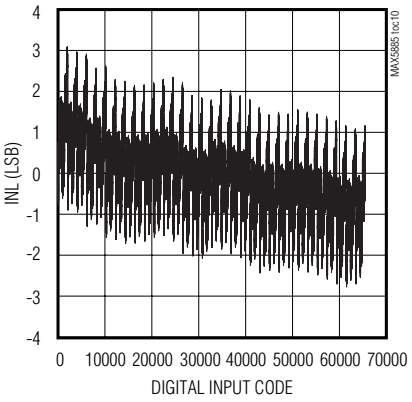


# 3.3V, 16-Bit, 200Msps High Dynamic Performance DAC with CMOS Inputs

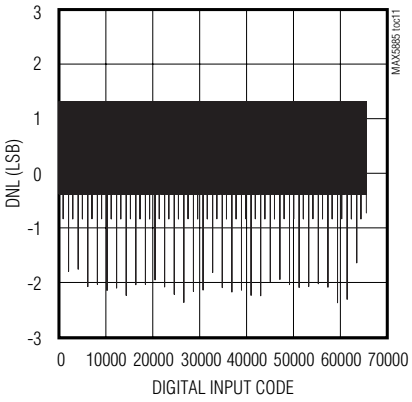
## Typical Operating Characteristics (continued)

($AV_{DD}$ = $DV_{DD}$ = VCLK = 3.3V, external reference, $V_{REFIO}$ = 1.25V, $R_L$ = 50Ω, $I_{OUT}$ = 20mA, $T_A$ = +25°C, unless otherwise noted.)

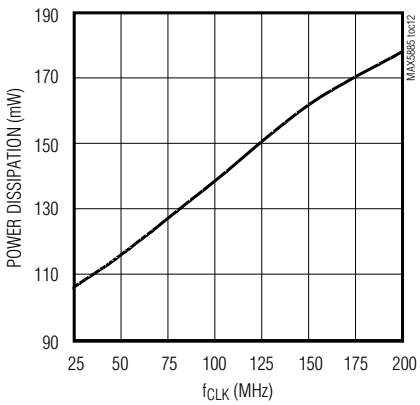
**INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE**



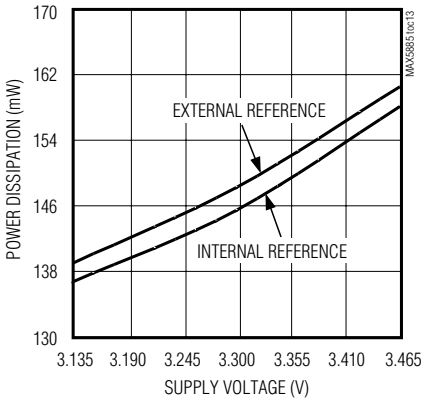

**DIFFERENTIAL NONLINEARTIY vs. DIGITAL INPUT CODE**




**POWER DISSIPATION vs. CLOCK FREQUENCY ($f_{OUT}$ = 10MHz, $A_{OUT}$ = 0dB FS, $I_{OUT}$ = 20mA)**




**POWER DISSIPATION vs. SUPPLY VOLTAGE ($f_{CLK}$ = 100MHz, $f_{OUT}$ = 10MHz, $I_{FS}$ = 20mA)**



## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | B1 | Data Bit 1 |
| 2 | B0 | Data Bit 0 (LSB) |
| 3 | XOR | XOR Input Pin.<br>XOR = 1 inverts the digital input data.<br>XOR = 0 leaves the digital input data unchanged.<br>XOR has an internal pulldown resistor and may be left unconnected if not used. |
| 4, 9 | VCLK | Clock Supply Voltage. Accepts a supply voltage range of 3.135V to 3.465V. Bypass each pin with a 0.1µF capacitor to the nearest CLKGND. |
| 5, 8 | CLKGND | Clock Ground |
| 6 | CLKP | Converter Clock Input. Positive input terminal for the converter clock. |
| 7 | CLKN | Complementary Converter Clock Input. Negative input terminal for the converter clock. |
| 10 | PD | Power-Down Input. PD pulled high enables the DAC's power-down mode. PD pulled low allows for normal operation of the DAC. |
| 11, 21, 23 | $AV_{DD}$ | Analog Supply Voltage. Accepts a supply voltage range of 3.135V to 3.465V. Bypass each pin with a 0.1µF capacitor to the nearest AGND. |
| 12, 17, 20, 22, 24, EP | AGND | Analog Ground. Exposed paddle (EP) must be connected to AGND. |
| 13 | REFIO | Reference I/O. Output of the internal 1.2V precision bandgap reference. Bypass with a 0.1µF capacitor to AGND. Can be driven with an external reference source. |
| 14 | FSADJ | Full-Scale Adjust Input. This input sets the full-scale output current of the DAC. For 20mA full-scale output current, connect a 2kΩ resistor between FSADJ and DACREF. |
| 15 | DACREF | Return Path for the Current Set Resistor. For 20mA full-scale output current, connect a 2kΩ resistor between FSADJ and DACREF. |
| 16, 25, 26, 27, 28, 29 | N.C. | No connection. **Do not connect to these pins. Do not tie these pins together.** |
| 18 | IOUTN | Complementary DAC Output. Negative terminal for differential current output. The full-scale output current range can be set from 2mA to 20mA. |
| 19 | IOUTP | DAC Output. Positive terminal for differential current output. The full-scale output current range can be set from 2mA to 20mA. |
| 30 | SEL0 | Mode Select Input SEL0. This pin has an internal pulldown resistor; it can be left open to disable the segment-shuffling function (see the *Segment Shuffling* section). |
| 31, 43 | $DV_{DD}$ | Digital Supply Voltage. Accepts a supply voltage range of 3.135V to 3.465V. Bypass each pin with a 0.1µF capacitor to the nearest DGND. |
| 32, 42 | DGND | Digital Ground |
| 33 | B15 | Data Bit 15 (MSB) |
| 34 | B14 | Data Bit 14 |
| 35 | B13 | Data Bit 13 |
| 36 | B12 | Data Bit 12 |
| 37 | B11 | Data Bit 11 |

# 3.3V, 16-Bit, 200Msps High Dynamic Performance DAC with CMOS Inputs

## Pin Description (continued)

| PIN | NAME | FUNCTION |
|---|---|---|
| 38 | B10 | Data Bit 10 |
| 39 | B9 | Data Bit 9 |
| 40 | B8 | Data Bit 8 |
| 41 | B7 | Data Bit 7 |
| 44 | B6 | Data Bit 6 |
| 45 | B5 | Data Bit 5 |
| 46 | B4 | Data Bit 4 |
| 47 | B3 | Data Bit 3 |
| 48 | B2 | Data Bit 2 |

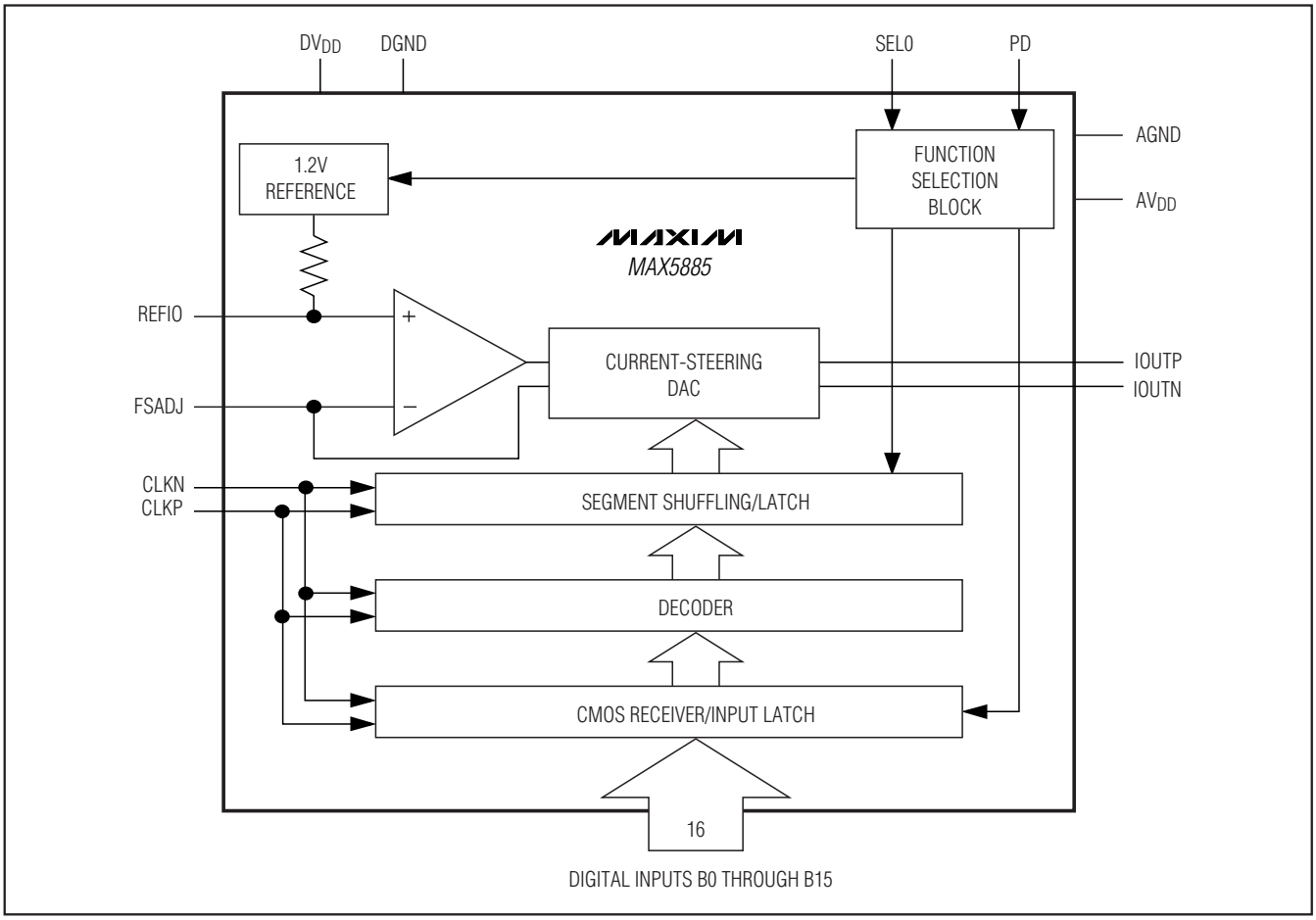



*Figure 1. Simplified MAX5885 Block Diagram*

## Detailed Description

### Architecture

The MAX5885 is a high-performance, 16-bit, current-steering DAC (Figure 1) capable of operating with clock speeds up to 200MHz. The converter consists of separate input and DAC registers, followed by a current-steering circuit. This circuit is capable of generating differential full-scale currents in the range of 2mA to 20mA. An internal current-switching network in combination with external 50Ω termination resistors convert the differential output currents into a differential output voltage with a peak-to-peak output voltage range of 0.1V to 1V. An integrated 1.2V bandgap reference, control amplifier, and user-selectable external resistor determine the data converter's full-scale output range.

### Reference Architecture and Operation

The MAX5885 supports operation with the on-chip 1.2V bandgap reference or an external reference voltage source. REFIO serves as the input for an external, low-impedance reference source, and as the output if the DAC is operating with the internal reference. For stable operation with the internal reference, REFIO should be decoupled to AGND with a 0.1µF capacitor. Due to its limited output drive capability, REFIO must be buffered with an external amplifier, if heavier loading is required.

The MAX5885's reference circuit (Figure 2) employs a control amplifier, designed to regulate the full-scale current $I_{OUT}$ for the differential current outputs of the DAC. Configured as a voltage-to-current amplifier, the output current can be calculated as follows:

$$I_{OUT} = 32 \times I_{REFIO} - 1\ LSB$$

$$I_{OUT} = 32 \times I_{REFIO} - (I_{OUT} / 2^{16})$$

where $I_{REFIO}$ is the reference output current ($I_{REFIO} = V_{REFIO}/R_{SET}$) and $I_{OUT}$ is the full-scale output current of the DAC. Located between FSADJ and DACREF, $R_{SET}$ is the reference resistor, which determines the amplifier's output current for the DAC. See Table 1 for a matrix of different $I_{OUT}$ and $R_{SET}$ selections.

### Analog Outputs (IOUTP, IOUTN)

The MAX5885 outputs two complementary currents (IOUTP, IOUTN) that can be operated in a single-ended or differential configuration. A load resistor can convert these two output currents into complementary single-ended output voltages. The differential voltage existing between IOUTP and IOUTN can also be converted to a single-ended voltage using a transformer or a differential amplifier configuration. If no transformer is used, the output should have a 50Ω termination to the analog ground and a 50Ω resistor between the outputs.

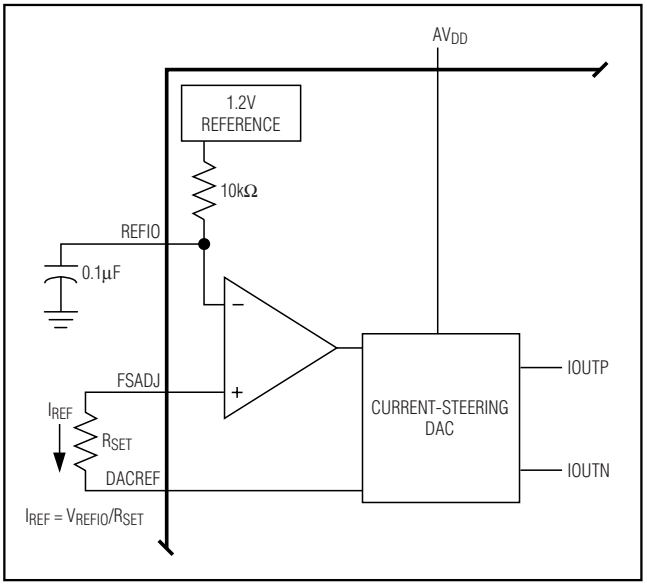



*Figure 2. Reference Architecture, Internal Reference Configuration*

**Table 1. $I_{OUT}$ and $R_{SET}$ Selection Matrix Based on a Typical 1.200V Reference Voltage**

| FULL-SCALE CURRENT $I_{OUT}$ (mA) | REFERENCE CURRENT $I_{REF}$ (µA) | $R_{SET}$ (kΩ) | | OUTPUT VOLTAGE $V_{IOUTP/N}$* ($mV_{P-P}$) |
|---|---|---|---|---|
| | | CALCULATED | 1% EIA STD | |
| 2 | 62.5 | 19.2 | 19.1 | 100 |
| 5 | 156.26 | 7.68 | 7.5 | 250 |
| 10 | 312.5 | 3.84 | 3.83 | 500 |
| 15 | 468.75 | 2.56 | 2.55 | 750 |
| 20 | 625 | 1.92 | 1.91 | 1000 |

**Terminated into a 50Ω load.*

# 3.3V, 16-Bit, 200Msps High Dynamic Performance DAC with CMOS Inputs

Although not recommended because of additional noise pickup from the ground plane, for single-ended operation IOUTP should be selected as the output, with IOUTN connected to AGND. Note that a single-ended output configuration has a higher 2nd-order harmonic distortion at high output frequencies than a differential output configuration.

Figure 3 displays a simplified diagram of the MAX5885's internal output structure.

### Clock Inputs (CLKP, CLKN)

The MAX5885 features a flexible differential clock input (CLKP, CLKN) operating from separate supplies (VCLK, CLKGND) to achieve the best possible jitter performance. The two clock inputs can be driven from a single-ended or a differential clock source. For single-ended operation, CLKP should be driven by a logic source, while CLKN should be bypassed to AGND with a 0.1µF capacitor.

The CLKP and CLKN pins are internally biased to $V_{CLK}/2$. This allows the user to AC-couple clock sources directly to the device without external resistors to define the DC level. The input resistance of CLKP and CLKN is >5kΩ.

See Figure 4 for a convenient and quick way to apply a differential signal created from a single-ended source (e.g., HP 8662A signal generator) and a wideband transformer. These inputs can also be driven from a CMOS-compatible clock source; however, it is recommended to use sinewave or AC-coupled ECL drive for best performance.

### Data Timing Relationship

Figure 5 shows the timing relationship between differential, digital CMOS data, clock, and output signals. The MAX5885 features a 1.25ns hold, a 0.4ns setup, and a 1.8ns propagation delay time. There is a 3.5 clock-cycle latency between CLKP/CLKN transitioning high/low and IOUTP/IOUTN.

### CMOS-Compatible Digital Inputs (B0–B15)

The MAX5885 features single-ended, CMOS-compatible receivers on the bus input interface. These CMOS inputs (B0–B15) allow for a voltage swing of 3.3V.

#### Segment Shuffling (SEL0)

Segment shuffling can improve the SFDR of the MAX5885 at higher output frequencies and amplitudes. Note that an improvement in SFDR can only be achieved at the cost of a slight increase in the DAC's noise floor.

Pin SEL0 controls the segment-shuffling function. If SEL0 is pulled low, the segment-shuffling function of the DAC is disabled. SEL0 can also be left open, because an internal pulldown resistor helps to deactivate the segment-shuffling feature. To activate the MAX5885 segment-shuffling function, SEL0 must be pulled high.

#### XOR Function (XOR)

The MAX5885 is equipped with a single-ended, CMOS-compatible XOR input, which may be left open (XOR provides an internal pulldown resistor) or pulled down to DGND, if not used. Input data is XORed with the bit applied to the XOR pin. Pulling XOR high inverts the input data. Pulling XOR low leaves the input data noninverted. By applying a pseudorandom bit stream to XOR and applying data while XOR is high, the bit transitions in the digital input data can be decorrelated from the DAC output, allowing the user to troubleshoot possible spurious or harmonic distortion degradation due to digital feedthrough on the PC board.

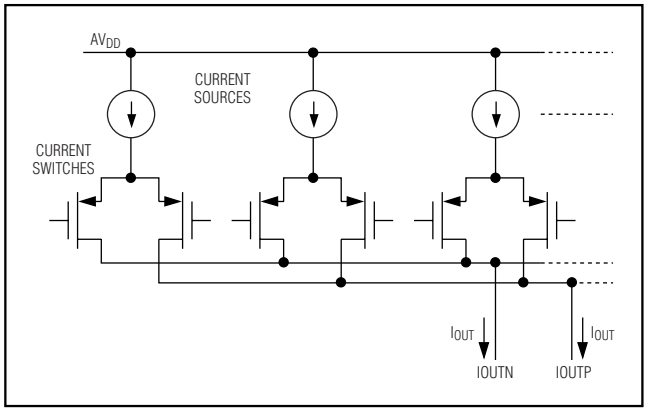



*Figure 3. Simplified Analog Output Structure*

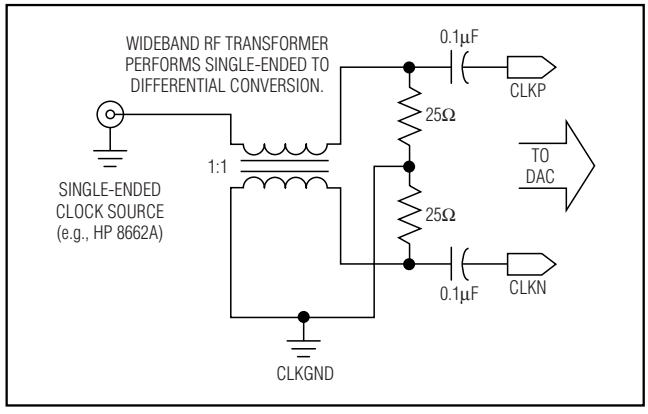



*Figure 4. Differential Clock Signal Generation*

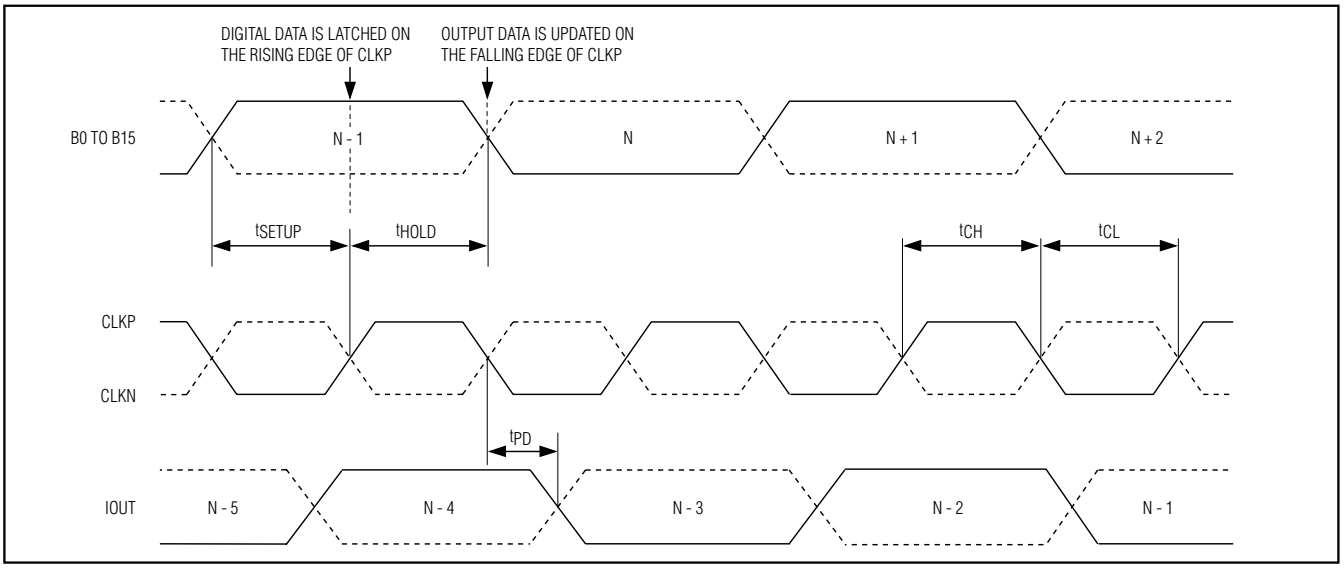



*Figure 5. Detailed Timing Relationship*

### Power-Down Operation (PD)

The MAX5885 also features an active-high power-down mode, which allows the user to cut the DAC's current consumption. A single pin (PD) is used to control the power-down mode (PD = 1) or reactivate the DAC (PD = 0) after power-down. Enabling the power-down mode of this 16-bit CMOS DAC allows the overall power consumption to be reduced to less than 1mW. The MAX5885 requires 10ms to wake up from power-down and enter a fully operational state.

## Applications Information

### Differential Coupling Using a Wideband RF Transformer

The differential voltage existing between IOUTP and IOUTN can also be converted to a single-ended voltage using a transformer (Figure 6) or a differential amplifier configuration. Using a differential transformer-coupled output, in which the output power is limited to 0dBm, can optimize the dynamic performance. However, make sure to pay close attention to the transformer core saturation characteristics when selecting a transformer for the MAX5885. Transformer core saturation can introduce strong 2nd-harmonic distortion, especially at low output frequencies and high signal amplitudes. It is also recommended to center tap the transformer to ground. If no transformer is used, each DAC output should be terminated to ground with a 50Ω resistor. Additionally, a 100Ω resistor should be placed between the outputs (Figure 7).

If a single-ended unipolar output is desirable, IOUTP should be selected as the output, with IOUTN grounded. However, driving the MAX5885 single ended is not recommended since additional noise is added (from the ground plane) in such configurations.

The distortion performance of the DAC depends on the load impedance. The MAX5885 is optimized for a 50Ω double termination. It can be used with a transformer output as shown in Figure 7 or just one 50Ω resistor from each output to ground and one 50Ω resistor between the outputs. This produces a full-scale output power of up to 0dBm depending on the output current setting. Higher termination impedance can be used at the cost of degraded distortion performance and increased output noise voltage.

### Adjacent Channel Leakage Power Ratio (ACLR) Testing for CDMA- and W-CDMA-Based Base Station Transceiver Systems (BTS)

The transmitter sections of BTS applications serving CDMA and W-CDMA architectures must generate carriers with minimal coupling of carrier energy into the adjacent channels. Similar to the GSM/EDGE model (see the *Multitone Testing for GSM/EDGE Applications* section), a transmit mask (Tx mask) exists for this application. The spread-spectrum modulation function applied to the carrier frequency generates a spectral response, which is uniform over a given bandwidth (up to 4MHz) for a W-CDMA-modulated carrier.

# 3.3V, 16-Bit, 200Msps High Dynamic Performance DAC with CMOS Inputs

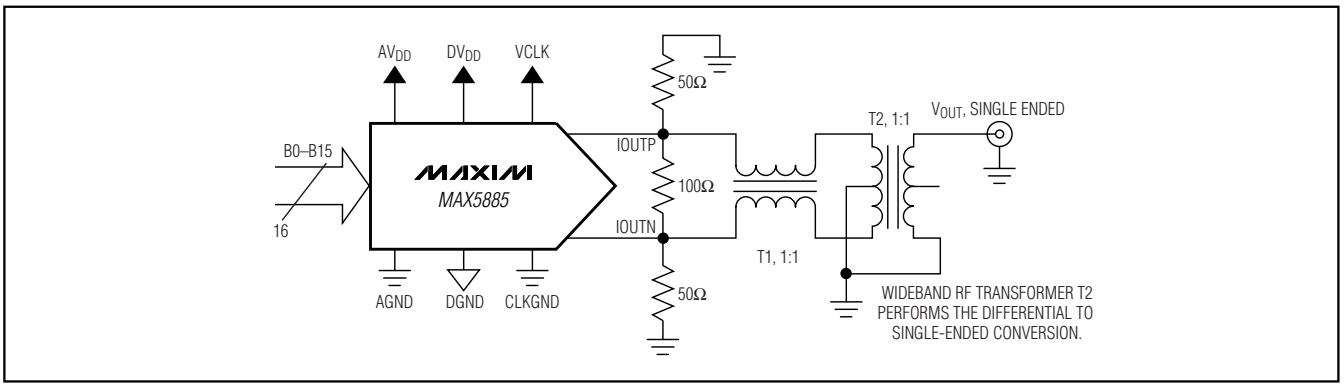



*Figure 6. Differential to Single-Ended Conversion Using a Wideband RF Transformer*

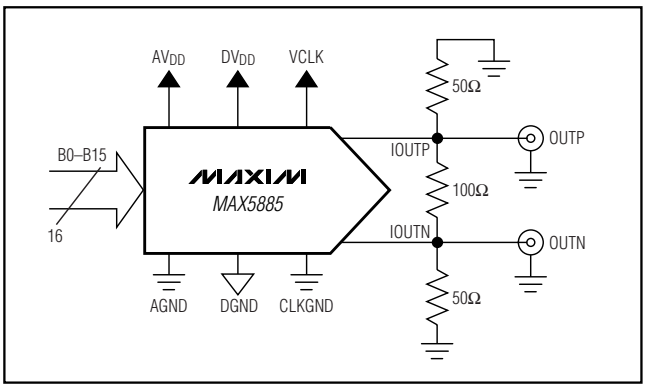



*Figure 7. MAX5885 Differential Output Configuration*

A dominant specification is ACLR, a parameter which reflects the ratio of the power in the desired carrier band to the power in an adjacent carrier band. The specification covers the first two adjacent bands, and is measured on both sides of the desired carrier.

According to the transmit mask for CDMA and W-CDMA architectures, the power ratio of the integrated carrier channel energy to the integrated adjacent channel energy must be >45dB for the first adjacent carrier slot (ACLR 1) and >50dB for the second adjacent carrier slot (ACLR 2). This specification applies to the output of the entire transmitter signal chain. The requirement for only the DAC block of the transmitter must be tighter, with a typical margin of >15dB, requiring the DAC's ACLR 1 to be better than 60dB.

Adjacent channel leakage is caused by a single spread-spectrum carrier, which generates intermodulation (IM) products between the frequency components located within the carrier band. The energy at one end of the carrier band generates IM products with the energy from the opposite end of the carrier band. For single-carrier W-CDMA modulation, these IMD products are spread 3.84MHz over the adjacent sideband. Four contiguous W-CDMA carriers spread their IM products over a bandwidth of 20MHz on either side of the 20MHz total carrier bandwidth. In this four-carrier scenario, only the energy in the first adjacent 3.84MHz sideband is considered for ACLR 1. To measure ACLR, drive the converter with a W-CDMA pattern. Make sure that the signal is backed off by the peak-to-average ratio, such that the DAC is not clipping the signal. ACLR can then be measured with the ACLR measurement function built into your spectrum analyzer.

Figure 8 shows the ACLR performance for a single W-CDMA carrier ($f_{CLK}$ = 184.32MHz, $f_{OUT}$ = 30.72MHz) applied to the MAX5885 (including measurement system limitations*).

Figure 9 illustrates the ACLR test results for the MAX5885 with a four-carrier W-CDMA signal at an output frequency of 30.72MHz and a sampling frequency of 184.32MHz. Considerable care must be taken to ensure accurate measurement of this parameter.

**Note that due to their own IM effects and noise limitations, spectrum analyzers introduce ACLR errors, which can falsify the measurement. For a single-carrier ACLR measurement greater than 70dB, these measurement limitations are significant, becoming even more restricting for multicarrier measurement. Before attempting an ACLR measurement, it is recommended consulting application notes provided by major spectrum analyzer manufacturers that provide useful tips on how to use their instruments for such tests.*

### Multitone Testing for GSM/EDGE Applications

The transmitter sections of multicarrier base station transceiver systems for GSM/EDGE usually present communication DAC manufacturers with the difficult task of providing devices with higher resolution, while simultaneously reducing noise and spurious emissions over a desired bandwidth.

To specify noise and spurious emissions from base stations, a GSM/EDGE Tx mask is used to identify the DAC requirements for these parameters. This mask shows that the allowable levels for noise and spurious emissions are dependent on the offset frequency from the transmitted carrier frequency. The GSM/EDGE mask and its specifications are based on a single active carrier with any other carriers in the transmitter being disabled. Specifications displayed in Figure 10 support per-carrier output power levels of 20W or greater. Lower output power levels yield less-stringent emission requirements.

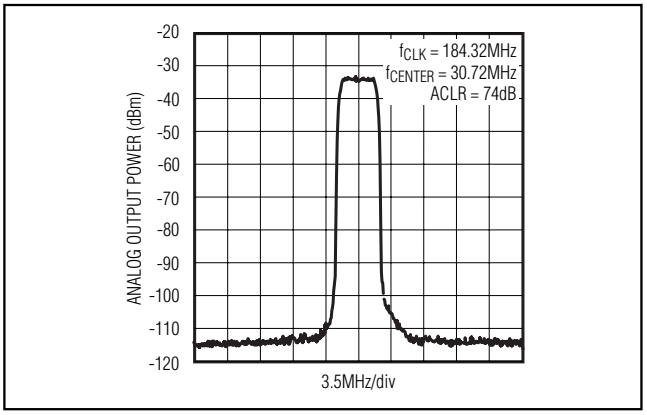



*Figure 8. ACLR for W-CDMA Modulation, Single Carrier*

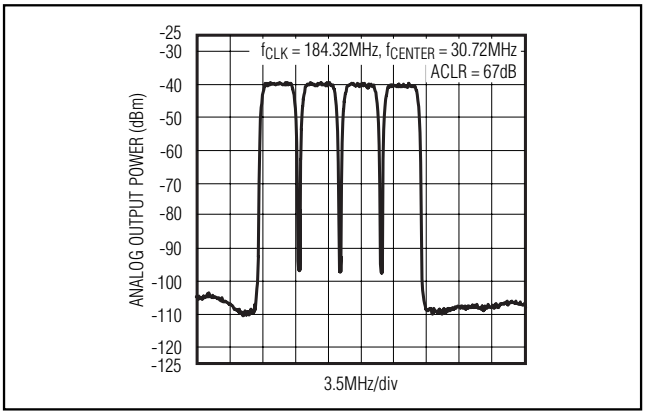



*Figure 9. ACLR for W-CDMA Modulation, Four Carriers*

For GSM/EDGE applications, the DAC demands spurious emission levels of less than -80dBc for offset frequencies ≥6MHz. Spurious products from the DAC can combine with both random noise and spurious products from other circuit elements. The spurious products from the DAC should therefore be backed off by 6dB or more to allow for these other sources and still avoid signal clipping.

The number of carriers and their signal levels with respect to the full scale of the DAC are important as well. Unlike a full-scale sinewave, the inherent nature of a multitone signal contains higher peak-to-RMS ratios, raising the prospect for potential clipping, if the signal level is not backed off appropriately. If a transmitter operates with four/eight in-band carriers, each individual carrier must be operated at less than -12dB FS/-18dB FS to avoid waveform clipping.

The noise density requirements (Table 2) for a GSM/EDGE-based system can again be derived from the system's Tx mask. With a worst-case noise level of -80dBc at frequency offsets of ≥6MHz and a measurement bandwidth of 100kHz, the minimum noise density per hertz is calculated as follows:

$$SNR_{MIN} = -80dBc - 10 \times \log_{10}(100 \times 10^3 Hz)$$

$$SNR_{MIN} = -130dBc/Hz$$

Since random DAC noise adds to both the spurious tones and to random noise from other circuit elements, it is recommended reducing the specification limits by about 10dB to allow for these additional noise contributions while maintaining compliance with the Tx mask values.

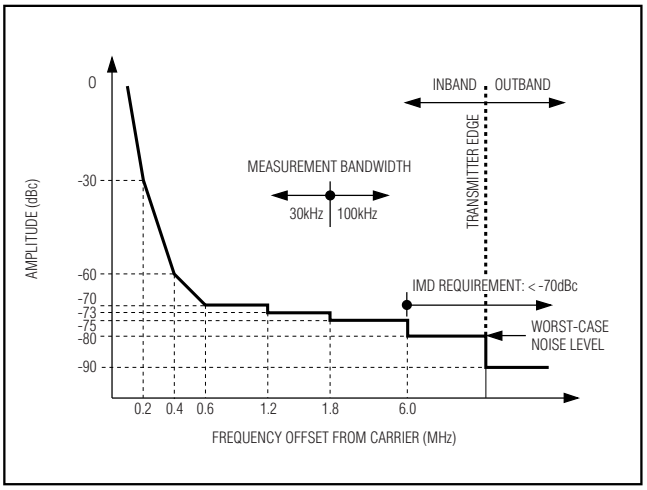



*Figure 10. GSM/EDGE Tx Mask Requirements*

# 3.3V, 16-Bit, 200Msps High Dynamic Performance DAC with CMOS Inputs

## Table 2. GSM/EDGE Noise Requirements for Multicarrier Systems

| NUMBER OF CARRIERS | CARRIER POWER LEVEL (dB FS) | DAC NOISE DENSITY REQUIREMENT (dB FS/Hz) |
|---|---|---|
| 2 | -6 | -146 |
| 4 | -12 | -152 |

Another key factor in selecting the appropriate DAC for the Tx path of a multicarrier GSM/EDGE system is the converter's ability to offer superior IMD and MTPR performance. Multiple carriers in a designated band generate unwanted intermodulation distortion between the individual carrier frequencies. A multitone test vector usually consists of several equally spaced carriers, usually four, with identical amplitudes. Each of these carriers is representative of a channel within the defined bandwidth of interest. To verify MTPR, one or more tones are removed such that the intermodulation distortion performance of the DAC can be evaluated. Nonlinearities associated with the DAC create spurious tones, some of which may fall back into the area of the removed tone, limiting a channel's carrier-to-noise ratio. Other spurious components falling outside the band of interest can also be important, depending on the system's spectral mask and filtering requirements. Going back to the GSM/EDGE Tx mask, the IMD specification for adjacent carriers varies somewhat among the different GSM standards. For the PCS1800 and GSM850 standards, the DAC must meet an average IMD of -70dBc.

Table 3 summarizes the dynamic performance requirements for the entire Tx signal chain in a four-carrier GSM/EDGE-based system and compares the previously established converter requirements with a new-generation high dynamic performance DAC.

The four-tone MTPR plot in Figure 11 demonstrates the MAX5885's excellent dynamic performance. The center frequency ($f_{CENTER}$ = 31.99MHz) has been removed to allow detection and analysis of intermodulation or spurious components falling back into this empty spot from adjacent channels. The four carriers are observed over a 12MHz bandwidth and are equally spaced at 1MHz. Each individual output amplitude is backed off to -12dB FS. Under these conditions, the DAC yields an MTPR performance of -82dBc.

### Grounding, Bypassing, and Power-Supply Considerations

Grounding and power-supply decoupling can strongly influence the performance of the MAX5885. Unwanted digital crosstalk may couple through the input, reference, power supply, and ground connections, affecting dynamic performance. Proper grounding and power-supply decoupling guidelines for high-speed, high-frequency applications should be closely followed. This reduces EMI and internal crosstalk that can significantly affect the dynamic performance of the MAX5885.

Use of a multilayer printed circuit (PC) board with separate ground and power-supply planes is recommended. High-speed signals should run on lines directly above the ground plane. Since the MAX5885 has separate analog and digital ground buses (AGND, CLKGND, and DGND, respectively), the PC board should also have separate analog and digital ground sections with only one point connecting the two planes. Digital signals should be run above the digital ground plane and analog/clock signals above the analog/clock ground plane. Digital signals should be kept as far away from sensitive analog inputs, reference input sense lines, common-mode input, and clock inputs as practical. A symmetric design of clock input and analog output lines is recommended to minimize 2nd-order

## Table 3. Summary of Important AC Performance Parameters for Multicarrier GSM/EDGE Systems

| SPECIFICATION | SYSTEM TRANSMITTER OUTPUT LEVELS | DAC REQUIREMENTS WITH MARGINS | MAX5885 SPECIFICATIONS |
|---|---|---|---|
| SFDR | 80dBc | 86dBc | 85dBc* |
| Noise Spectral Density | -130dBc/Hz | -152dB FS/Hz | -155dB FS/Hz |
| IMD | -70dBc | -75dBc | -79dBc |
| Carrier Amplitude | N/S | -12dB FS | -12dB FS |

**Measured within a 15MHz window.*

harmonic distortion components and optimize the DAC's dynamic performance. Digital signal paths should be kept short and run lengths matched to avoid propagation delay and data skew mismatches.

The MAX5885 supports three separate power-supply inputs for analog ($AV_{DD}$), digital ($DV_{DD}$), and clock (VCLK) circuitry. Each $AV_{DD}$, $DV_{DD}$, and VCLK input should at least be decoupled with a separate 0.1µF capacitor as close to the pin as possible and their opposite ends with the shortest possible connection to the corresponding ground plane (Figure 12). All three power-supply voltages should also be decoupled at the point they enter the PC board with tantalum or electrolytic capacitors. Ferrite beads with additional decoupling capacitors forming a pi network could also improve performance.

The analog and digital power-supply inputs $AV_{DD}$, VCLK, and $DV_{DD}$ of the MAX5885 allow a supply voltage range of 3.3V ±5%.

The MAX5885 is packaged in a 48-pin QFN-EP (package code: G4877-1), providing greater design flexibility, increased thermal efficiency**, and optimized AC performance of the DAC. The EP enables the user to implement grounding techniques, which are necessary to ensure highest performance operation. **The EP must be soldered down to AGND.**

In this package, the data converter die is attached to an EP lead frame with the back of this frame exposed at the package bottom surface, facing the PC board side of the package. This allows a solid attachment of the package to the PC board with standard infrared (IR) flow soldering techniques. A specially created land pattern on the PC board, matching the size of the EP (5mm × 5mm), ensures the proper attachment and grounding of the DAC. Designing vias*** into the land area and implementing large ground planes in the PC board design allow for highest performance operation of the DAC. An array of at least 3 × 3 vias (≤0.3mm diameter per via hole and 1.2mm pitch between via holes) is recommended for this 48-pin QFN-EP package.

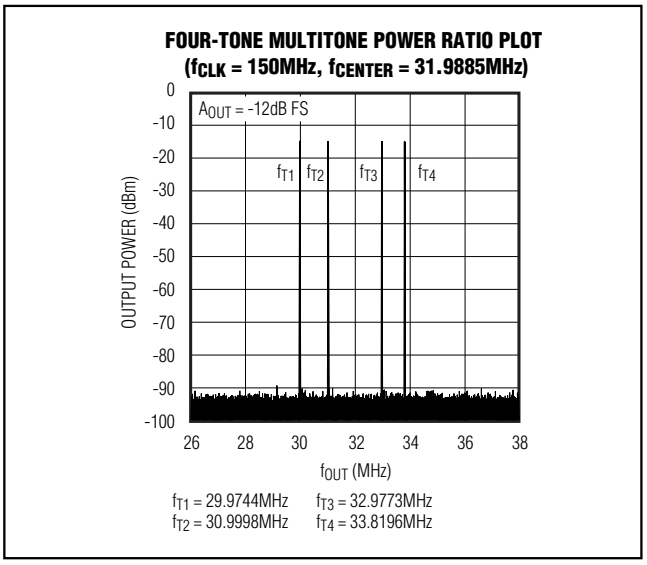



*Figure 11. 4-Tone MTPR Test Results*

## Static Performance Parameter Definitions

### Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from either a best straight line fit (closest approximation to the actual transfer curve) or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. For a DAC, the deviations are measured at every individual step.

### Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step height and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function.

### Offset Error

The offset error is the difference between the ideal and the actual offset point. For a DAC, the offset point is the step value when the digital input is at midscale. This error affects all codes by the same amount.

***Thermal efficiency is not the key factor, since the MAX5885 features low-power operation. The exposed pad is the key element to ensure a solid ground connection between the DAC and the PC board's analog ground layer.*

****Vias connect the land pattern to internal or external copper planes. It is important to connect as many vias as possible to the analog ground plane to minimize inductance.*

# 3.3V, 16-Bit, 200Msps High Dynamic Performance DAC with CMOS Inputs

### Gain Error

A gain error is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

### Settling Time

The settling time is the amount of time required from the start of a transition until the DAC output settles its new output value to within the converter's specified accuracy.

### Glitch Energy

A glitch is generated when a DAC switches between two codes. The largest glitch is usually generated around the midscale transition, when the input pattern transitions from 011...111 to 100...000. The glitch energy is found by integrating the voltage of the glitch at the midscale transition over time. The glitch-energy is usually specified in pV-s.

## Dynamic Performance Parameter Definitions

### Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog output (RMS value) to the RMS quantization error (residual error). The ideal, theoretical maximum SNR can be derived from the DAC's resolution (N bits):

$$SNR_{dB} = 6.02_{dB} \times N + 1.76_{dB}$$

However, noise sources such as thermal noise, reference noise, clock jitter, etc., affect the ideal reading; therefore, SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first four harmonics, and the DC offset.

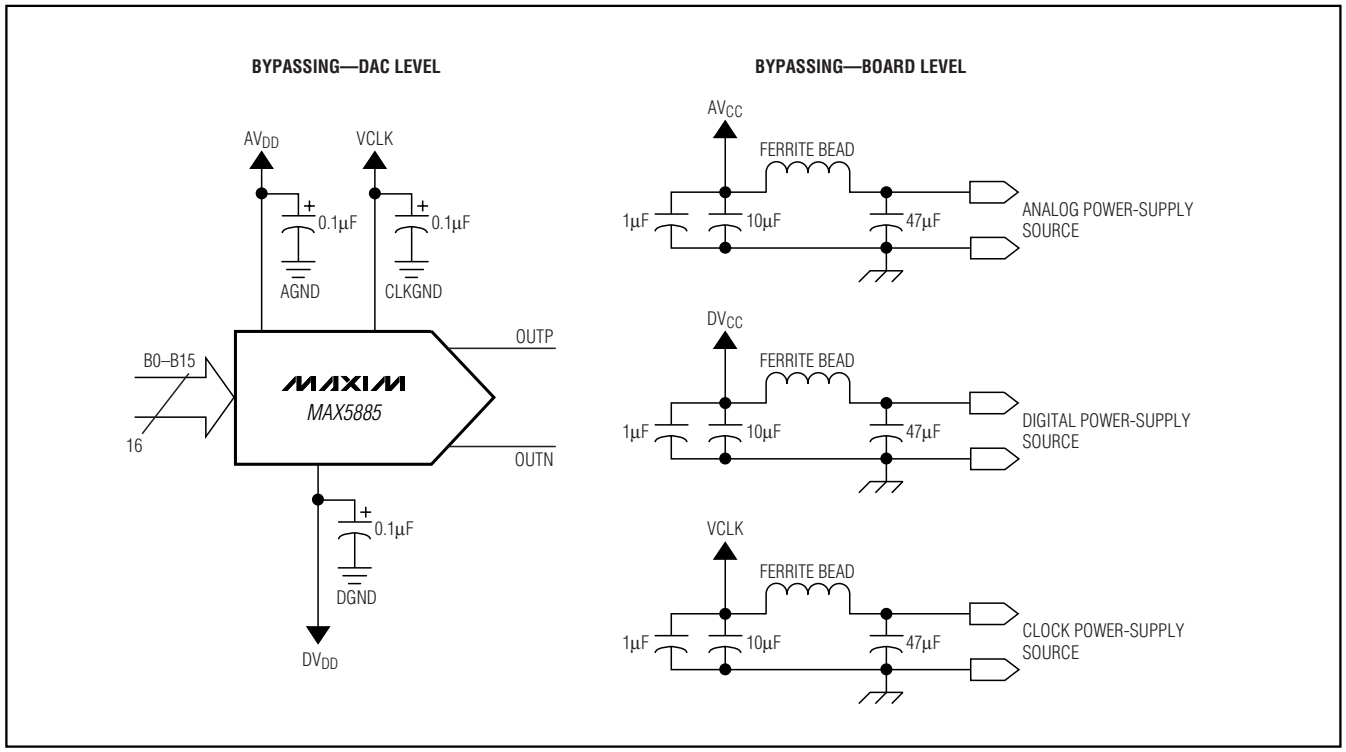



*Figure 12. Recommended Power-Supply Decoupling and Bypassing Circuitry*

### Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of RMS amplitude of the carrier frequency (maximum signal components) to the RMS value of their next-largest distortion component. SFDR is usually measured in dBc and with respect to the carrier frequency amplitude or in dB FS with respect to the DAC's full-scale range. Depending on its test condition, SFDR is observed within a predefined window or to Nyquist.

### Two-/Four-Tone Intermodulation Distortion (IMD)

The two-tone IMD is the ratio expressed in dBc (or dB FS) of either input tone to the worst 3rd-order (or higher) IMD products. Note that 2nd-order IMD products usually fall at frequencies that can be easily removed by digital filtering; therefore, they are not as critical as 3rd-order IMDs. The two-tone IMD performance of the MAX5885 was tested with the two individual input tone levels set to at least -6dB FS and the four-tone performance was tested according to the GSM model at an output frequency of 32MHz and amplitude of -12dB FS.

### Adjacent Channel Leakage Power Ratio (ACLR)

Commonly used in combination with W-CDMA, ACLR reflects the leakage power ratio in dB between the measured power within a channel relative to its adjacent channel. ACLR provides a quantifiable method of determining out-of-band spectral energy and its influence on an adjacent channel when a bandwidth-limited RF signal passes through a nonlinear device.

## Chip Information

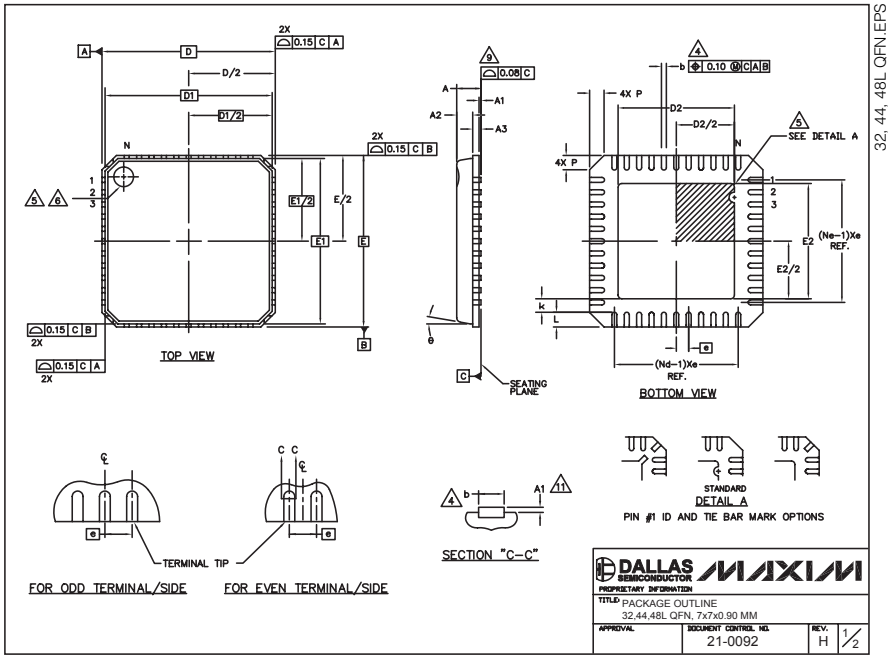
TRANSISTOR COUNT: 10,721

PROCESS: CMOS

# 3.3V, 16-Bit, 200Msps High Dynamic Performance DAC with CMOS Inputs

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)




| COMMON DIMENSIONS | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| PKG | 32L 7x7 | | | 44L 7x7 | | | 48L 7x7 | | |
| SYMBOL | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.80 | 0.90 | 1.00 | 0.80 | 0.90 | 1.00 | 0.80 | 0.90 | 1.00 |
| A1 | 0.00 | 0.01 | 0.05 | 0.00 | 0.01 | 0.05 | 0.00 | 0.01 | 0.05 |
| A2 | 0.00 | 0.65 | 1.00 | 0.00 | 0.65 | 1.00 | 0.00 | 0.65 | 1.00 |
| A3 | 0.20 REF | | | 0.20 REF | | | 0.20 REF | | |
| b | 0.23 | 0.28 | 0.35 | 0.18 | 0.23 | 0.30 | 0.18 | 0.23 | 0.30 |
| D | 6.90 | 7.00 | 7.10 | 6.90 | 7.00 | 7.10 | 6.90 | 7.00 | 7.10 |
| D1 | 6.75 BSC | | | 6.75 BSC | | | 6.75 BSC | | |
| E | 6.90 | 7.00 | 7.10 | 6.90 | 7.00 | 7.10 | 6.90 | 7.00 | 7.10 |
| E1 | 6.75 BSC | | | 6.75 BSC | | | 6.75 BSC | | |
| e | 0.65 BSC | | | 0.50 BSC | | | 0.50 BSC | | |
| k | 0.25 | – | – | 0.25 | – | – | 0.25 | – | – |
| L | 0.35 | 0.55 | 0.75 | 0.35 | 0.55 | 0.75 | 0.30 | 0.40 | 0.50 |
| N | 32 | | | 44 | | | 48 | | |
| Nd | 8 | | | 11 | | | 12 | | |
| Ne | 8 | | | 11 | | | 12 | | |
| P | 0.00 | 0.42 | 0.60 | 0.00 | 0.42 | 0.60 | 0.00 | 0.42 | 0.60 |
| U | 0° | | 12° | 0° | | 12° | 0° | | 12° |

| EXPOSED PAD VARIATIONS | | | | | | |
|---|---|---|---|---|---|---|
| PKG. CODES | D2 | | | E2 | | |
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| G3277-2 | 4.55 | 4.70 | 4.85 | 4.55 | 4.70 | 4.85 |
| G4477-1 | 3.65 | 3.80 | 3.95 | 3.65 | 3.80 | 3.95 |
| G4477-2 | 4.55 | 4.70 | 4.85 | 4.55 | 4.70 | 4.85 |
| G4477-3 | 3.15 | 3.30 | 3.45 | 3.15 | 3.30 | 3.45 |
| G4877-1 | 4.95 | 5.10 | 5.25 | 4.95 | 5.10 | 5.25 |
| G4877-2 | 5.45 | 5.60 | 5.75 | 5.45 | 5.60 | 5.75 |

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM).
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.08mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220 EXCEPT DIMENSION "b" MINIMUM.
11. APPLY ONLY FOR TERMINAL.
12. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION(STEPPED SIDES).

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 32,44,48L QFN, 7x7x0.90 MM
APPROVAL
DOCUMENT CONTROL NO. 21-0092
REV. H
2/2

*MAX5885 Package Code: G4877-1*

*Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.*



© 2003 Maxim Integrated Products Printed USA MAXIM is a registered trademark of Maxim Integrated Products.