

CSD95492QVM 同步降压 NexFET™智能power stage

1 特性

- 20A 持续工作电流
- 12A 电流下系统效率超过 94%
- 工作频率高（高达 1.25MHz）
- 二极管仿真功能
- 温度补偿双向电流检测
- 模拟温度输出
- 故障监控
- 3.3V 和 5V 脉宽调制 (PWM) 信号兼容
- 三态 PWM 输入
- 集成自举开关
- 用于击穿保护的经优化死区时间
- 高密度 4mm × 5mm VSON 封装
- 超低电感封装
- 系统已优化的 PCB 封装
- 符合 RoHS 环保标准 – 无铅引脚镀层
- 无卤素

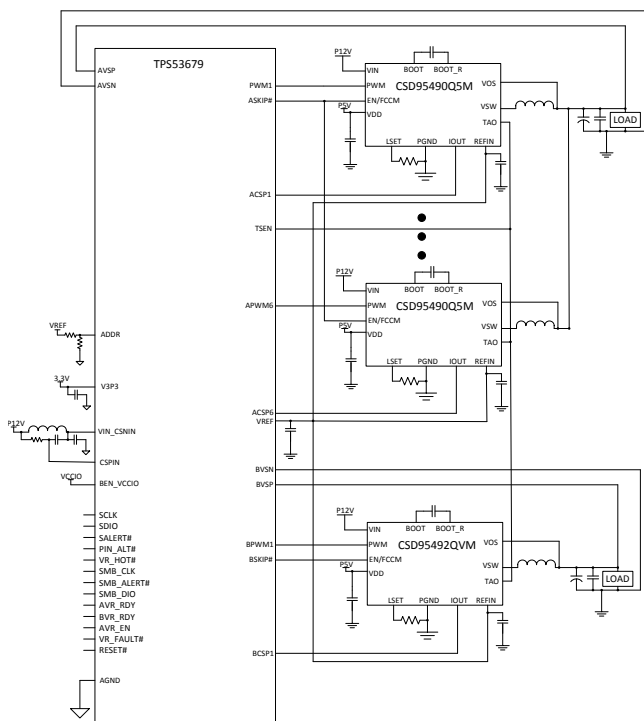
2 应用

- 多相位同步降压转换器
 - 高频 应用
 - 高电流、低占空比 应用
- 负载点 (POL) 直流/直流转换器
- 内存和图形卡
- 台式机和服务器 VR12.x/VR13.x VRM 同步降压转换器

3 说明

CSD95492QVM NexFET™power stage是经过高度优化的设计，用于高功率、高功率密度场合的同步降压转换器。这款产品集成了驱动器 IC 和功率 MOSFET 来完善功率级开关功能。该组合可在 4mm × 5mm 外形尺寸封装中提供高电流、高效率以及高速切换功能。它还集成了准确电流检测和温度感测功能，以简化系统设计并提高准确度。此外，PCB 封装已经过优化，可帮助减少设计时间并简化总体系统设计。

应用图表



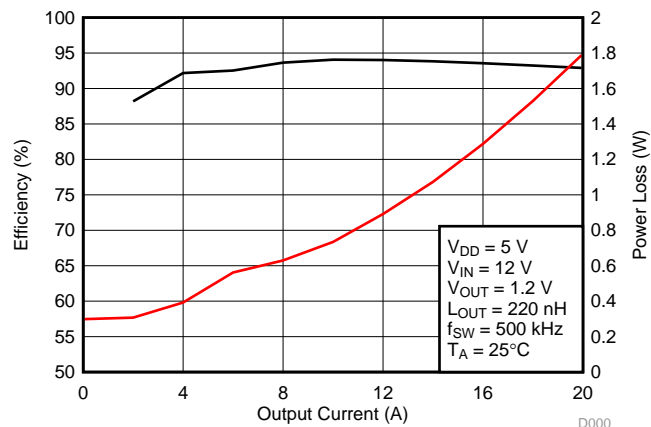
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器件信息(1)

器件	包装介质	数量	封装	发货
CSD95492QVM	13 英寸卷带	2500	4.00mm × 5.00mm VSON 封装	卷带 封装
CSD95492QVMT	7 英寸卷带	250		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型功率级效率与功率损耗



D000



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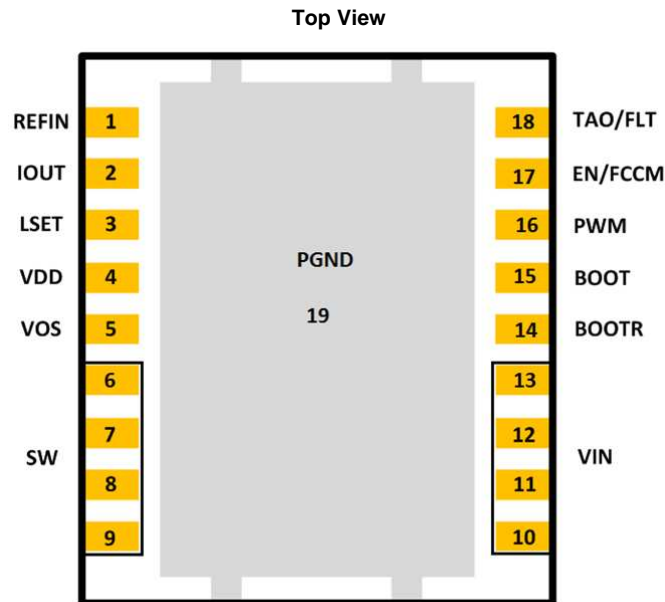
4 Revision History

Changes from Original (June 2017) to Revision A

Page

<ul style="list-style-type: none"> • 更新了机械制图部分 7 	7
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5 Pin Configuration and Functions



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
REFIN	1	External reference voltage input for current sensing amplifier.
IOUT	2	Output of current sensing amplifier. $V(IOUT) - V(REFIN)$ is proportional to the phase current.
LSET	3	A resistor from this pin to PGND pin sets the inductor value for the internal current sensing circuitry.
VDD	4	Supply voltage for gate drivers and internal circuitry.
VOS	5	Output voltage sensing pin for the internal current sensing circuitry.
SW	6-9	Phase node connecting the HS MOSFET source and LS MOSFET drain – pin connection to the output inductor.
VIN	10-13	Input voltage pin. Connect input capacitors close to this pin.
BOOTR	14	Return path for HS gate driver. It is connected to VSW internally.
BOOT	15	Bootstrap capacitor connection. Connect a minimum 0.1- μ F, 16-V, X5R ceramic cap from BOOT to BOOTR pins. The bootstrap capacitor provides the charge to turn on the control FET. The bootstrap diode is integrated.
PWM	16	Tri-state input from external controller. Logic low sets control FET gate low and sync FET gate high. Logic high sets control FET gate high and sync FET gate low. Both MOSFET gates are set low if PWM stays in Hi-Z for greater than the tri-state shutdown holdoff time (t_{3HT}).
EN/FCCM	17	This dual function pin either enables the diode emulation function or can be used as a simple enable for the device. When this pin is driven into the tri-state window and held there for more than the tri-state holdoff time, Diode Emulation Mode is enabled for sync FET. When the pin is high, device operates in Forced Continuous Conduction Mode. When the pin is low, both FETs are held off. An internal resistor pulls this pin low if left floating.
TAO/FAULT	18	Temperature Amplifier Output. Reports a voltage proportional to the IC temperature. An ORing diode is integrated in the IC. When used in multiphase application, a single wire can be used to connect the TAO pins of all the ICs. Only the highest temperature will be reported. TAO will be pulled up to 3.3 V if thermal shutdown, LSOC, or HSS detection circuit is tripped.
PGND	19	Power ground.

6 Specifications

6.1 Absolute Maximum Ratings

 $T_A = 25^\circ\text{C}$ (unless otherwise stated)⁽¹⁾

	MIN	MAX	UNIT
V_{IN} to P_{GND}	-0.3	20	V
V_{IN} to V_{SW}	-0.3	20	V
V_{IN} to V_{SW} (10 ns)		23	V
V_{SW} to P_{GND}	-0.3	20	V
V_{SW} to P_{GND} (10 ns)	-7	23	V
V_{DD} to P_{GND}	-0.3	7	V
EN/FCCM, TAO/FLT, LSET to P_{GND} ⁽²⁾	-0.3	$V_{DD} + 0.3$	V
IOUT, VOS, PWM to P_{GND}	-0.3	7	V
REFIN	-0.3	3.6	V
BOOT to BOOTR ⁽²⁾	-0.3	$V_{DD} + 0.3$	V
BOOT to P_{GND}	-0.3	30	V
T_J Operating junction temperature	-55	150	$^\circ\text{C}$
T_{stg} Storage temperature	-55	150	$^\circ\text{C}$

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Should not exceed 7 V.

6.2 ESD Ratings

	VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM)	± 2000
	Charged-device model (CDM)	± 500
		V

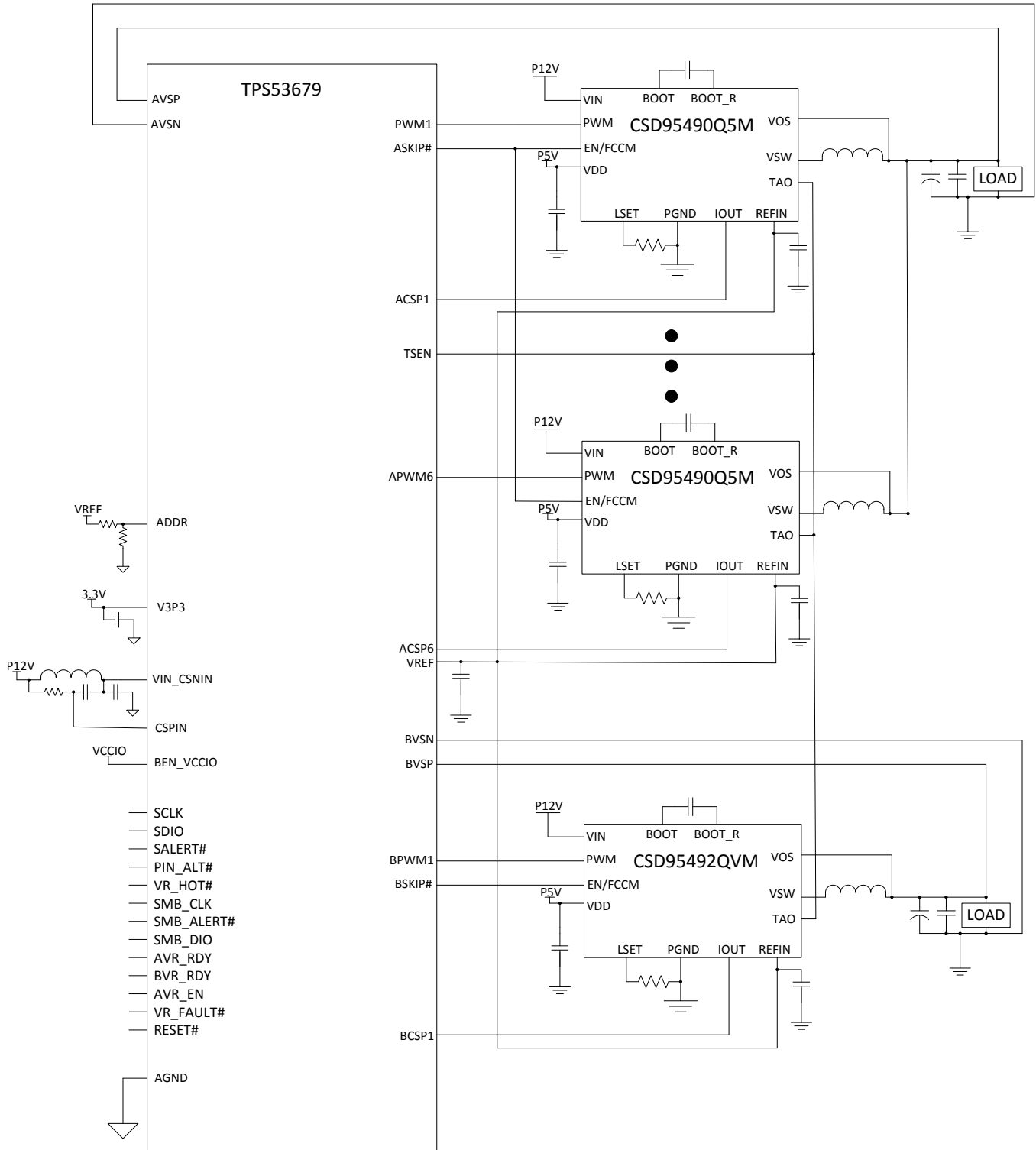
6.3 Recommended Operating Conditions

 $T_A = 25^\circ\text{C}$ (unless otherwise stated)

	MIN	MAX	UNIT
V_{DD} Driver supply voltage	4.5	5.5	V
V_{IN} Input supply voltage ⁽¹⁾	4.5	16	V
V_{OUT} Output voltage		5.5	V
PWM PWM to P_{GND}		V_{DD}	V
I_{OUT} Continuous output current	$V_{IN} = 12\text{ V}$, $V_{DD} = 5\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $f_{SW} = 500\text{ kHz}$ ⁽²⁾	20	A
I_{OUT-PK} Peak output current ⁽³⁾		30	A
f_{SW} Switching frequency	$C_{BST} = 0.1\ \mu\text{F}$ (min), $V_{OUT} = 2.5\text{ V}$ (max)	1250	kHz
On-time duty cycle	$f_{SW} = 1\text{ MHz}$	85%	
Minimum PWM on-time		20	ns
Operating junction temperature	-40	125	$^\circ\text{C}$

- (1) Operating at high V_{IN} can create excessive AC voltage overshoots on the switch node (V_{SW}) during MOSFET switching transients. For reliable operation, the switch node (V_{SW}) to ground voltage must remain at or below the *Absolute Maximum Ratings*.
- (2) Measurement made with six 10- μF (TDK C3216X7R1C106KT or equivalent) ceramic capacitors across V_{IN} to P_{GND} pins.
- (3) System conditions as defined in Note 2. Peak output current is applied for $t_p = 50\ \mu\text{s}$.

7 Application Schematic



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Figure 1. Application Schematic

Note: The schematic in [Figure 1](#) is a conceptual drawing only. Actual designs may require additional components not shown.

8 器件和文档支持

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. 有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 Community Resources

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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设计支持 *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

8.3 商标

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8.4 静电放电警告



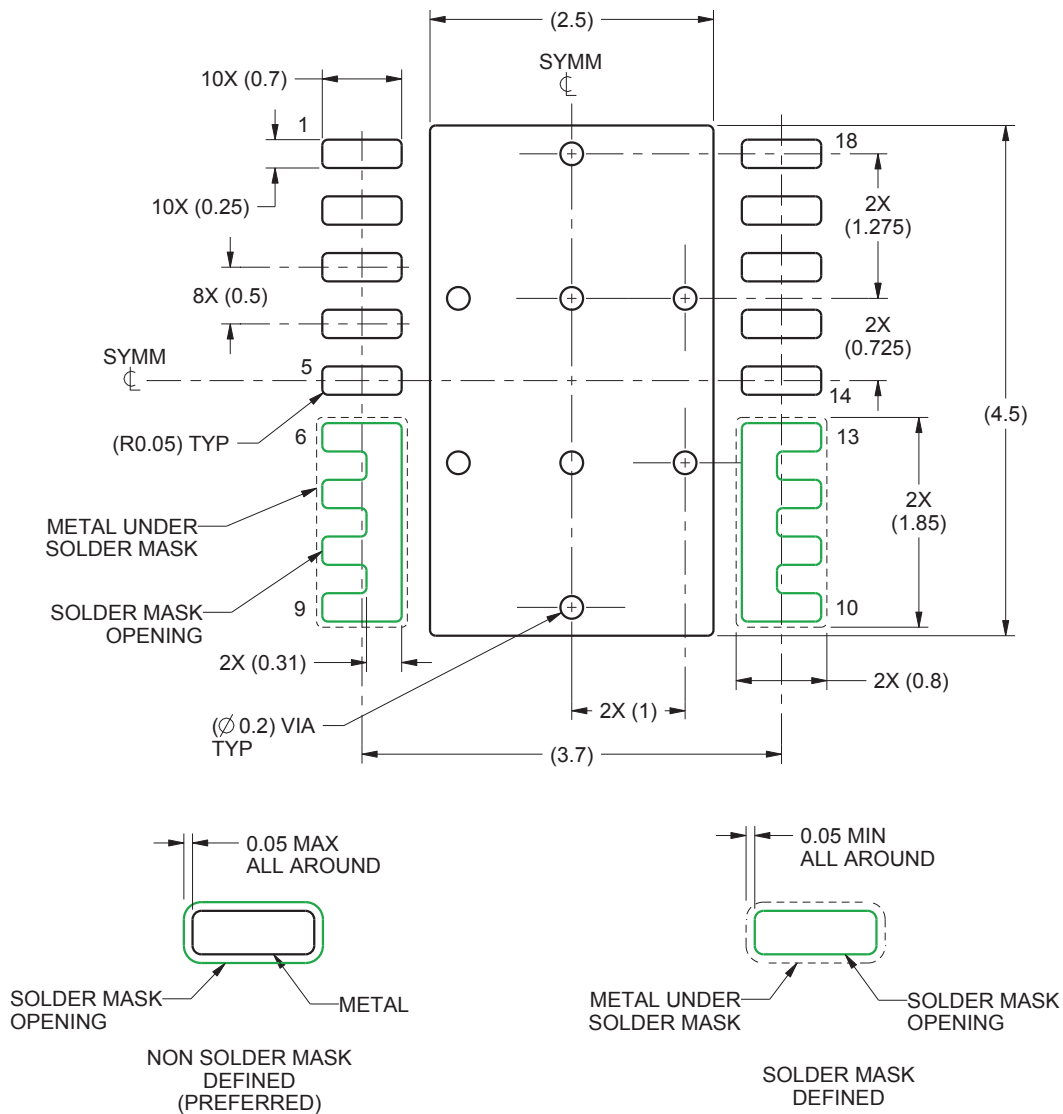
这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

8.5 Glossary

SLYZ022 — *TI Glossary*.

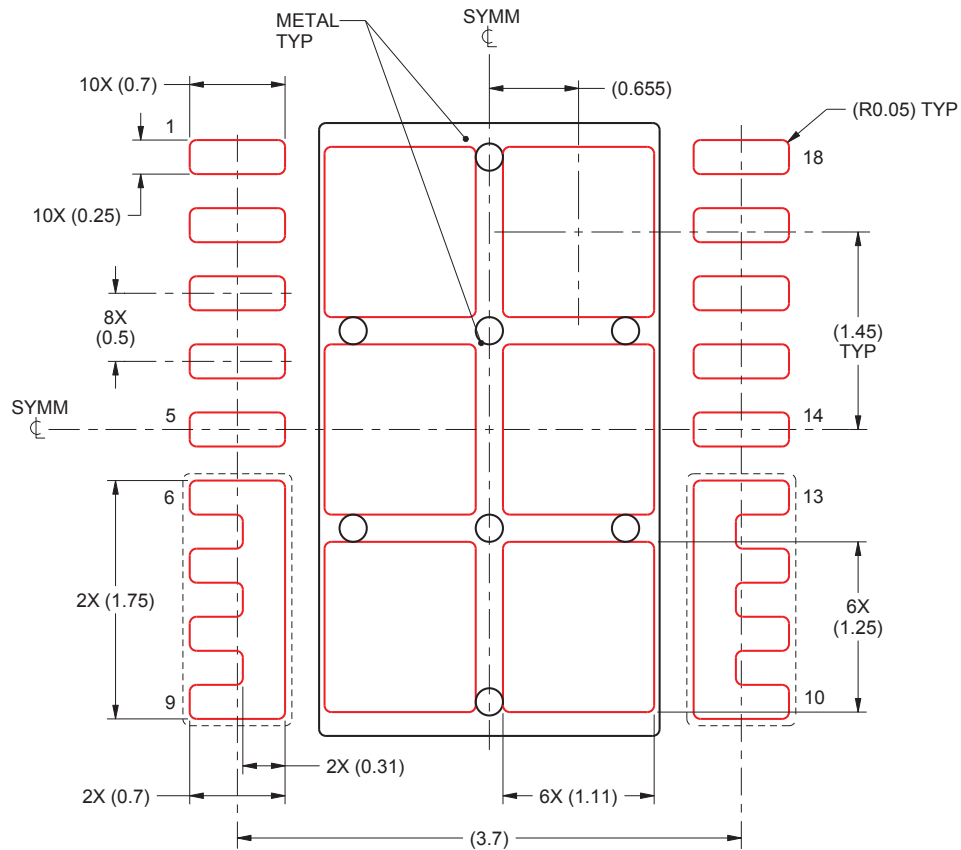
This glossary lists and explains terms, acronyms, and definitions.

9.2 推荐 PCB 焊盘图案



1. 所有线性尺寸的单位均为毫米。括号中的任何尺寸仅供参考。尺寸和公差值符合 ASME Y14.5M 标准。
2. 本图如有变更，恕不另行通知。
3. 此封装设计用于焊接到电路板的散热焊盘上。有关更多信息，请参阅《QFN/Son PCB 连接》(SLUA271)。

9.3 推荐模版开孔



1. 所有线性尺寸的单位均为毫米。括号中的任何尺寸仅供参考。尺寸和公差值符合 ASME Y14.5M 标准。
2. 本图如有变更，恕不另行通知。
3. 具有漏斗形壁和圆角的激光切割孔可提供更佳的锡膏脱离。IPC-7525 可能提供替代设计建议。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD95492QVM	NRND	Production	VSON-CLIP (DMH) 18	2500 LARGE T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 150	95492QM
CSD95492QVM.Z	NRND	Production	VSON-CLIP (DMH) 18	2500 LARGE T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 150	95492QM
CSD95492QVMT	NRND	Production	VSON-CLIP (DMH) 18	250 SMALL T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 150	95492QM
CSD95492QVMT.Z	NRND	Production	VSON-CLIP (DMH) 18	250 SMALL T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 150	95492QM

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD95492QVM	VSON-CLIP	DMH	18	2500	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
CSD95492QVMT	VSON-CLIP	DMH	18	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD95492QVM	VSON-CLIP	DMH	18	2500	367.0	367.0	38.0
CSD95492QVMT	VSON-CLIP	DMH	18	250	213.0	191.0	35.0

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