

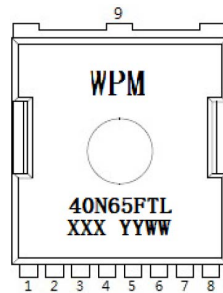
Features

- 650V Super-junction MOSFET
- Ultra fast body diode: trr=202ns(typ.)
- Low drain-source On-resistance: $R_{DS(on)}=0.099\Omega$ (Max.)
- 100% avalanche tested
- RoHS compliant device

Ordering Information

Part Number	Marking	Package
WTM40N65FTL	40N65FTL	TOLL-8L

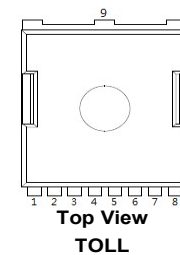
Marking Information



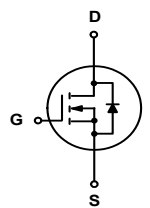
Pin Description

Pin	Description
1	Gate(G)
2,3,4,5,6,7,8	Source(S)
9	Drain(D)

Simplified Outline



Symbol



Absolute maximum ratings ($T_c=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	650	V
Gate-source voltage	V_{GSS}	± 30	V
Drain current (DC) (Note 1)	I_D	$T_c=25^\circ\text{C}$	40
		$T_c=100^\circ\text{C}$	25
Drain current (Pulsed) (Note 1)	I_{DM}	160	A
Single pulsed avalanche energy (Note 2)	E_{AS}	470	mJ
Repetitive avalanche current (Note 1)	I_{AR}	9	A
Repetitive avalanche energy (Note 1)	E_{AR}	2.3	mJ
Power dissipation	P_D	230	W
Diode dv/dt ruggedness (Note 3)	dv/dt	50	V/ns
MOSFET dv/dt ruggedness (Note 4)	dv/dt	50	V/ns
Junction temperature	T_J	150	$^\circ\text{C}$
Storage temperature range	T_{stg}	-55~150	$^\circ\text{C}$

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 0.543	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 50	

Electrical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0$	650	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}$, $V_{DS}=V_{GS}$	3	4	5	V
Drain-source cut-off current	I_{DSS}	$V_{DS}=650\text{V}$, $V_{GS}=0\text{V}$	-	-	10	μA
Gate leakage current	I_{GSS}	$V_{DS}=0\text{V}$, $V_{GS}=\pm 30\text{V}$	-	-	1000	nA
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=15.4\text{A}$	-	0.081	0.099	Ω
Internal gate resistance	R_g	$F=1\text{MHz}$, open drain	-	10	-	Ω
Input capacitance	C_{iss}	$V_{DS}=100\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	-	3596	-	pF
Output capacitance	C_{oss}		-	122	-	
Reverse transfer capacitance	C_{rss}		-	3.7	-	
Turn-on delay time (Note 5)	$t_{d(on)}$	$V_{DS}=400\text{V}$, $I_D=15.4\text{A}$, $R_G=10\Omega$	-	120	-	ns
Rise time (Note 5)	t_r		-	80	-	
Turn-off delay time (Note 5)	$t_{d(off)}$		-	165	-	
Fall time (Note 5)	t_f		-	8.5	-	
Total gate charge (Note 6)	Q_g	$V_{DS}=400\text{V}$, $V_{GS}=10\text{V}$, $I_D=30.8\text{A}$	-	74	-	nC
Gate-source charge (Note 6)	Q_{gs}		-	26.5	-	
Gate-drain charge (Note 6)	Q_{gd}		-	27.5	-	
Gate plateau voltage (Note 6)	$V_{plateau}$		-	7.2	-	V

Source-Drain Diode Ratings and Characteristics ($T_c=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	40	A
Source current (Pulsed)	I_{SM}		-	-	160	A
Forward voltage	V_{SD}	$V_{GS}=0\text{V}$, $I_S=30.8\text{A}$	-	-	1.5	V
Reverse recovery time (Note 5, 6)	t_{rr}	$I_S=15.4\text{A}$, $V_{GS}=0\text{V}$, $di_S/dt=100\text{A}/\mu\text{s}$	-	200	-	ns
Reverse recovery charge (Note 5, 6)	Q_{rr}		-	0.51	-	μC

Note:

1. Calculated continuous current based on maximum allowable junction temperature
2. $L=10\text{mH}$, $I_{AS}=9\text{A}$, $V_{DD}=90\text{V}$, Starting $T_J=25^\circ\text{C}$
3. $I_S \leq 9\text{A}$, $V_{DS} \leq 400\text{V}$, $di_S/dt \leq 100\text{A}/\mu\text{s}$, $T_J=25^\circ\text{C}$
4. $V_{DS} \leq 400\text{V}$, $T_J=25^\circ\text{C}$
5. Guaranteed by design, not subject to production testing
6. Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$

Typical Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

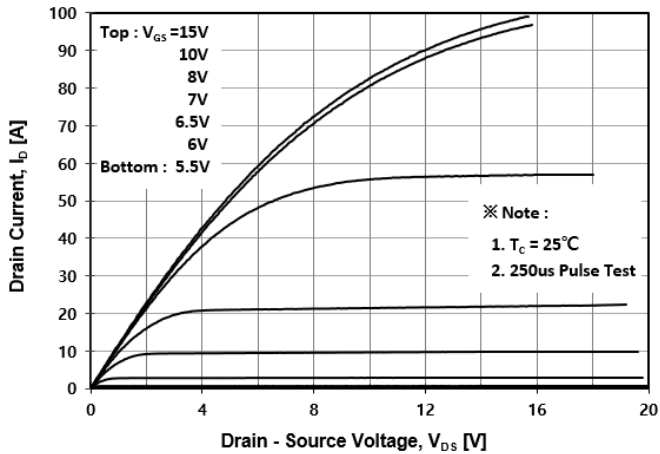


Fig. 2 Typical Transfer Characteristics

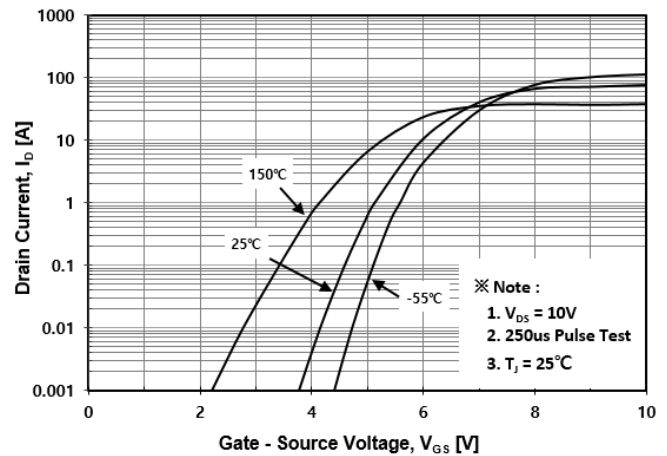


Fig.3 On-Resistance Variation with Drain Current and Gate Voltage

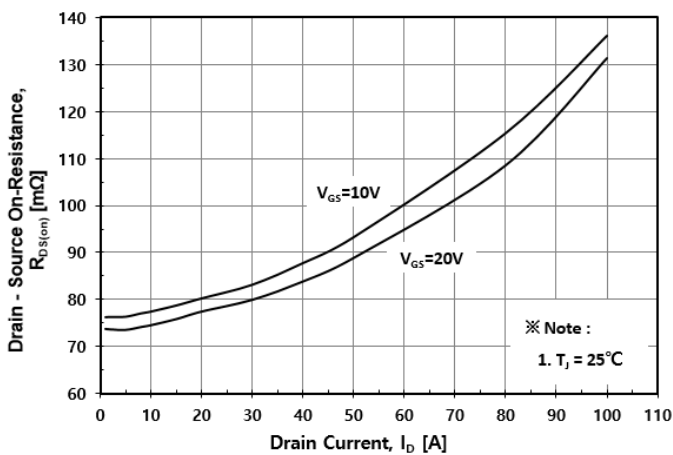


Fig. 4 Body Diode Forward Voltage Variation with Source Current

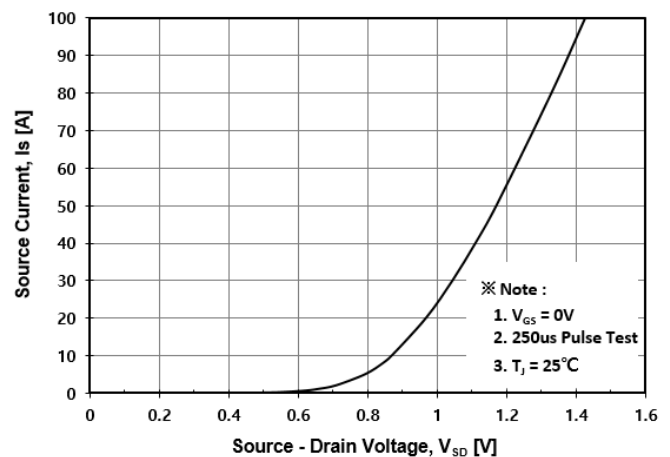


Fig. 5 Typical Capacitance Characteristics

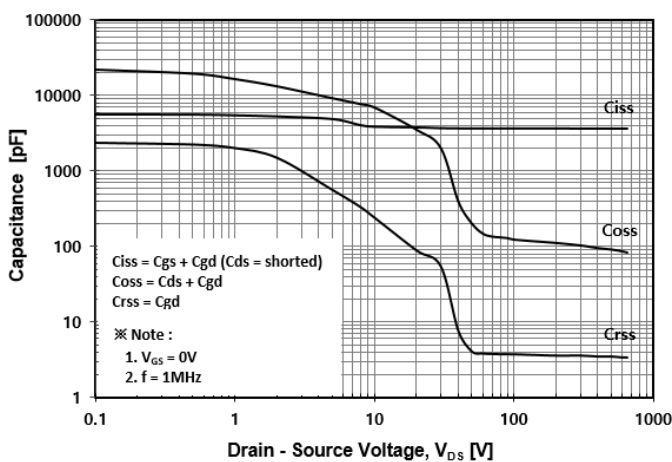


Fig. 6 Typical Total Gate Charge Characteristics

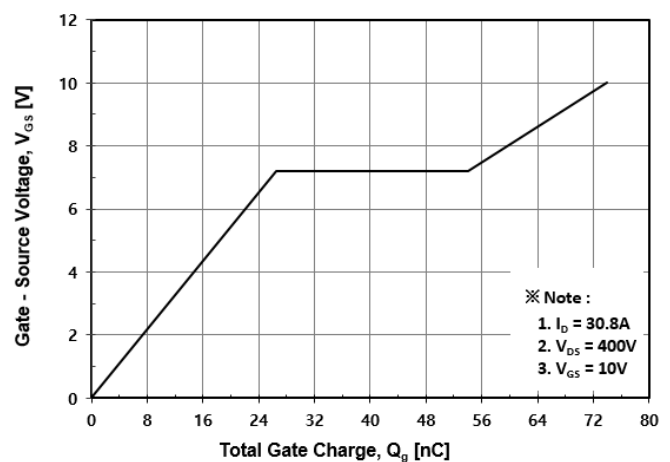


Fig. 7 Breakdown Voltage Variation vs. Temperature

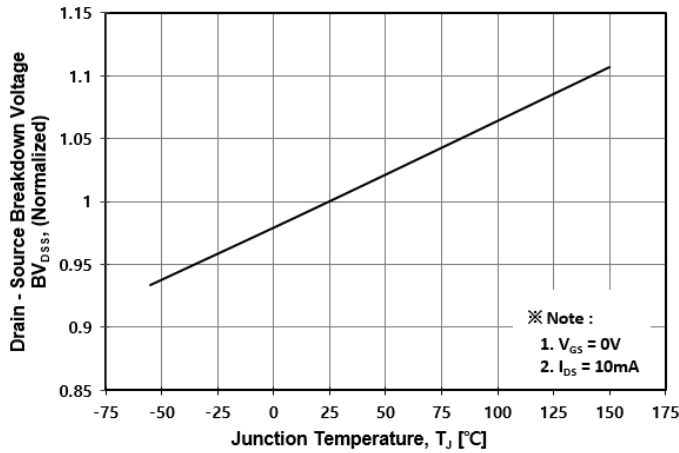


Fig. 8 On-Resistance Variation vs. Temperature

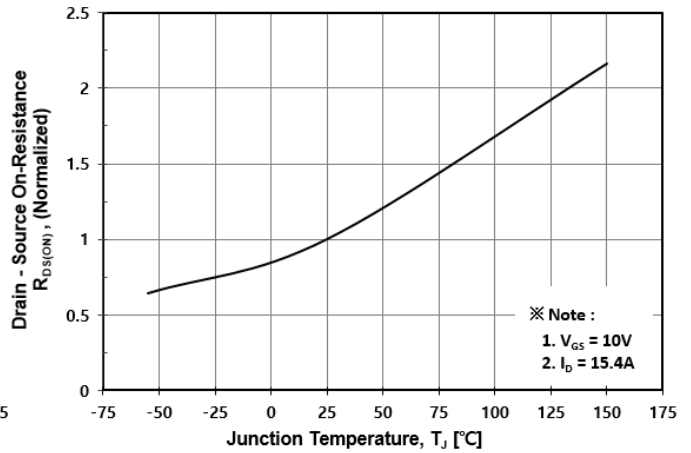


Fig. 9 Maximum Drain Current vs. Case Temperature

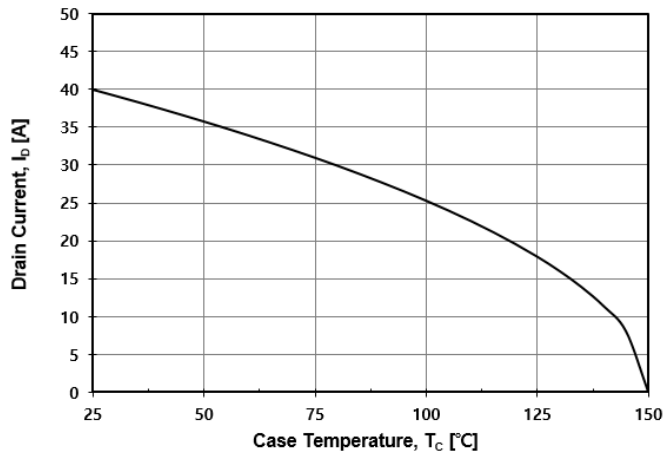


Fig. 10 Maximum Safe Operating Area

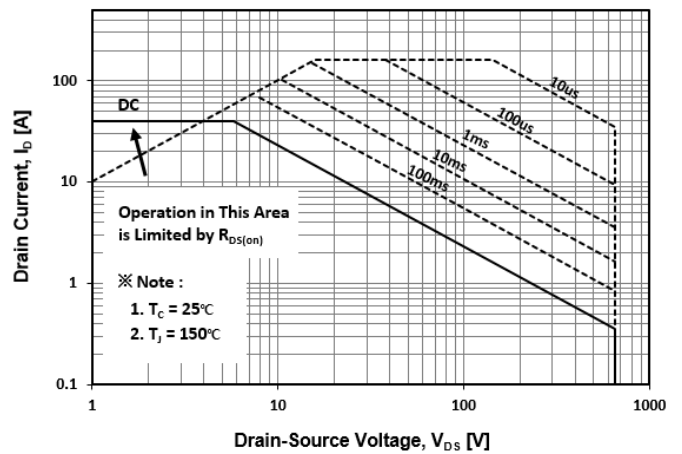


Fig. 11 Transient Thermal Impedance

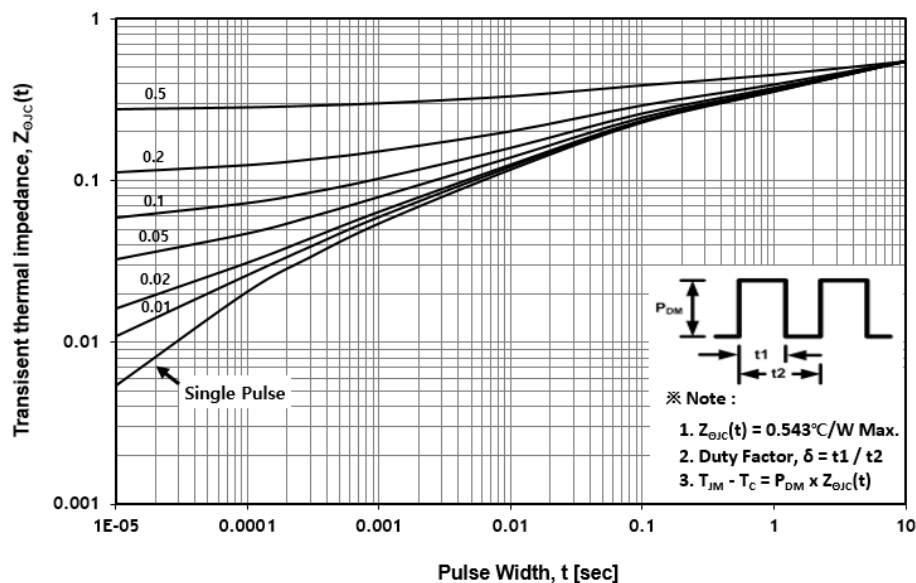


Fig. 12 Gate Charge Test Circuit & Waveform

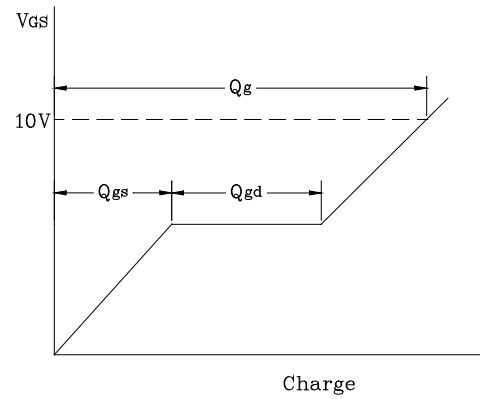
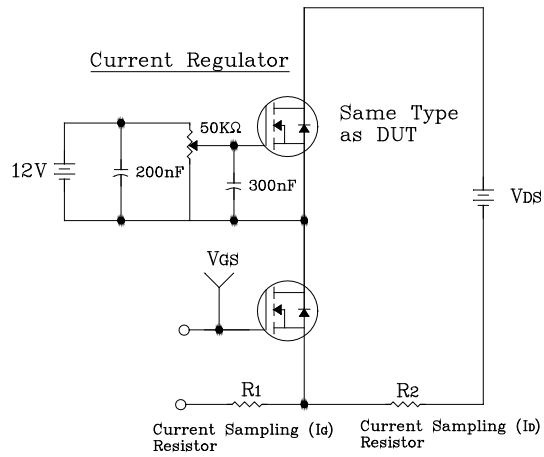


Fig. 13 Resistive Switching Test Circuit & Waveform

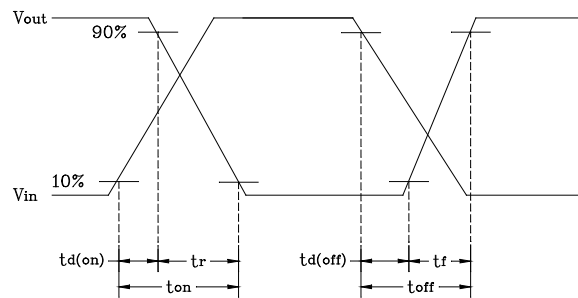
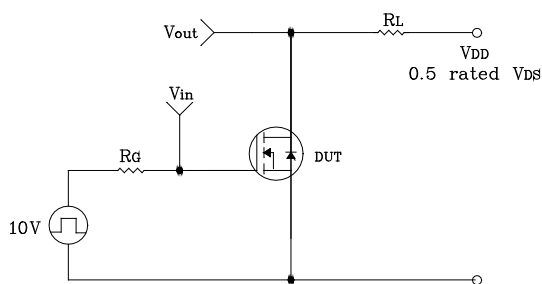
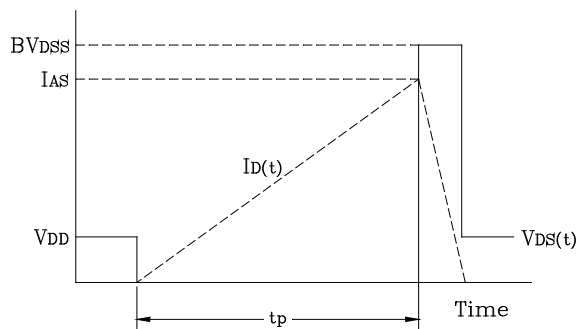
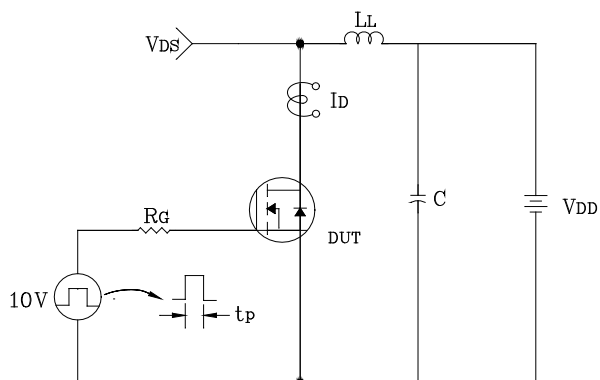
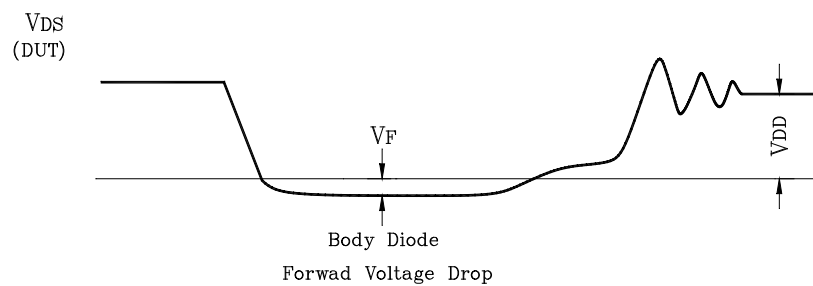
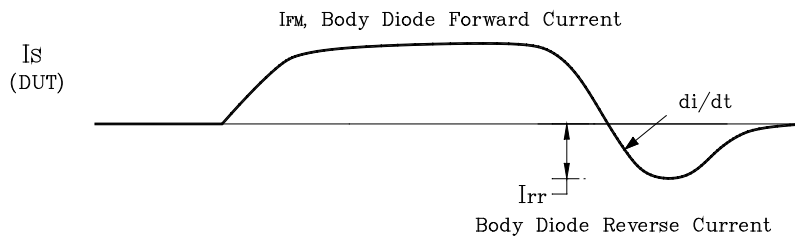
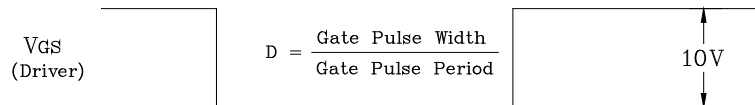
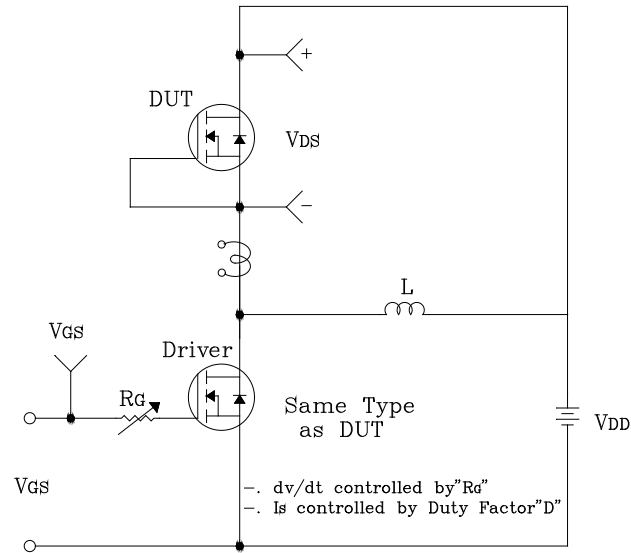
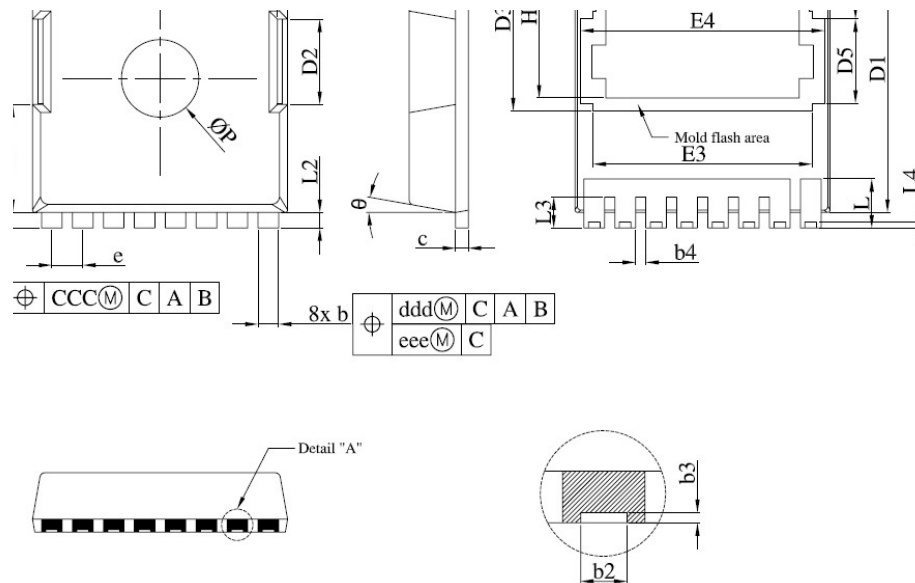


Fig. 14 E_{AS} Test Circuit & Waveform





8. Package Dimensions TOLL-8L Package



Symbol	Dimensions In Millimeters	
	MIN.	MAX.
b	0.70	0.90
b3	0.05	/
b6	3.00	3.20
D1	10.98	11.18
D4	3.59	
E	9.80	10.00

Symbol	Dimensions In Millimeters	
	MIN.	MAX.
E3	8.50	
H1	6.55	6.75
L1	0.50	0.90
L4	0.13	0.33
θ	10°REF	
ccc	0.20	
ddd	0.25	

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