

PBSS5220PAPS-Q

20V, 2 A PNP/PNP low VCEsat double transistor

25 September 2023 **Product data sheet**

1. General description

PNP/PNP low V_{CEsat} double transistor in a leadless medium power DFN2020D-6 (SOT1118D) Surface-Mounted Device (SMD) plastic package with visible and solderable side pads.

NPN/NPN complement: PBSS4220PANS

2. Features and benefits

- Very low collector-emitter saturation voltage V_{CEsat}
- High collector current capability I_C and I_{CM}
- High collector current gain h_{FE} at high I_C
- Reduced Printed-Circuit Board (PCB) requirements
- Exposed heat sink for excellent thermal and electrical conductivity
- High energy efficiency due to less heat generation
- Suitable for Automatic Optical Inspection (AOI) of solder joints
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- Load switch
- Battery-driven devices
- Power management
- Charging circuits
- LED lighting
- Power switches (e.g. motors, fans)

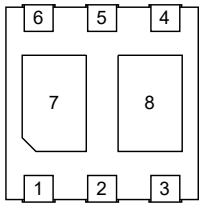
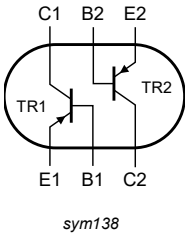
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
V_{CEO}	collector-emitter voltage	open base		-	-	-20	V
I_C	collector current			-	-	-2	A
I_{CM}	peak collector current	single pulse; $t_p \leq$ 1 ms		-	-	-3	A

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E1	emitter TR1	 Transparent top view **DFN2020D-6 (SOT1118D)**	 *sym138*
2	B1	base TR1		
3	C2	collector TR2		
4	E2	emitter TR2		
5	B2	base TR2		
6	C1	collector TR1		
7	C1	collector TR1		
8	C2	collector TR2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBSS5220PAPS-Q	DFN2020D-6	plastic, leadless thermally enhanced ultra thin and small outline package with side-wettable flanks (SWF); 6 terminals; 0.65 mm pitch; 2 mm x 2 mm x 0.65 mm body	SOT1118D

7. Marking

Table 4. Marking codes

Type number	Marking code
PBSS5220PAPS-Q	3P

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8. Limiting values

Table 5. Limiting values

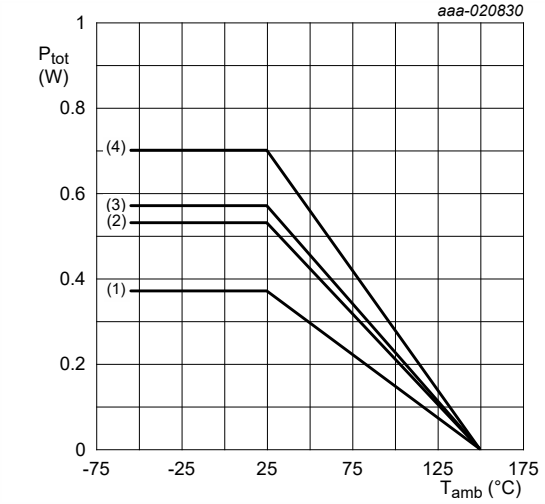
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V_{CBO}	collector-base voltage	open emitter		-	-20	V
V_{CEO}	collector-emitter voltage	open base		-	-20	V
V_{EBO}	emitter-base voltage	open collector		-	-7	V
I_C	collector current			-	-2	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms		-	-3	A
I_B	base current			-	-0.3	A
I_{BM}	peak base current	single pulse; $t_p \leq 1$ ms		-	-1	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	370	mW
			[2]	-	570	mW
			[3]	-	530	mW
			[4]	-	700	mW
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	510	mW
			[2]	-	780	mW
			[3]	-	730	mW
			[4]	-	960	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single sided copper, tin-plated; mounting pad for collector 1 cm^2.
[3] Device mounted on an FR4 Printed-Circuit Board (PCB), 4-layer copper, tin-plated and standard footprint.
[4] Device mounted on an FR4 Printed-Circuit Board (PCB), 4-layer copper, tin-plated; mounting pad for collector 1 cm^2.

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(1) FR4 PCB, single-sided copper, standard footprint
(2) FR4 PCB, 4-layer copper, standard footprint
(3) FR4 PCB, single-sided copper, 1 cm^2
(4) FR4 PCB, 4-layer copper, 1 cm^2

Fig. 1. Power derating curves

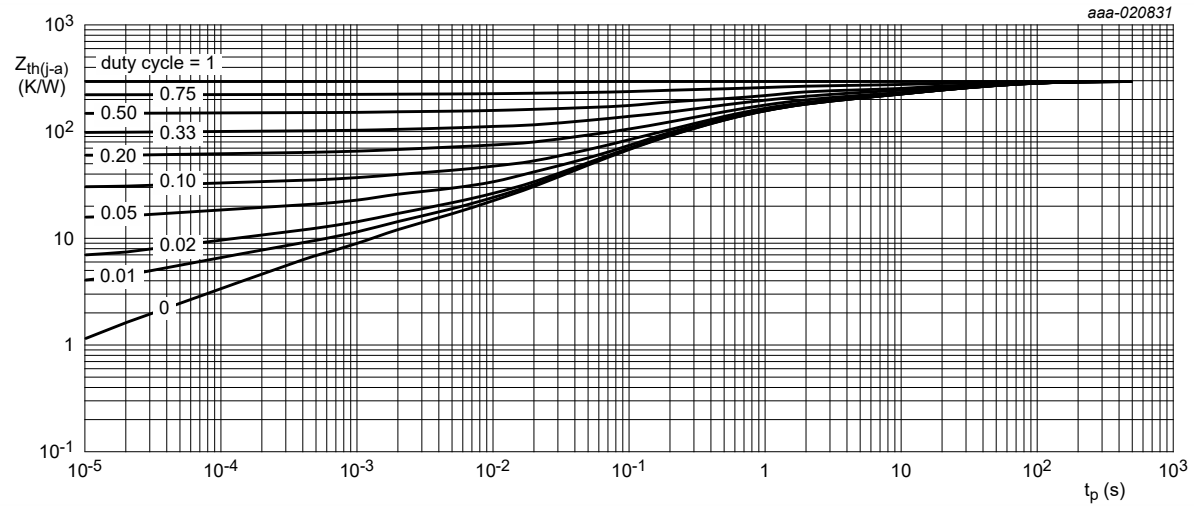
9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	338	K/W
			[2]	-	-	219	K/W
			[3]	-	-	236	K/W
			[4]	-	-	179	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	246	K/W
			[2]	-	-	161	K/W
			[3]	-	-	172	K/W
			[4]	-	-	131	K/W

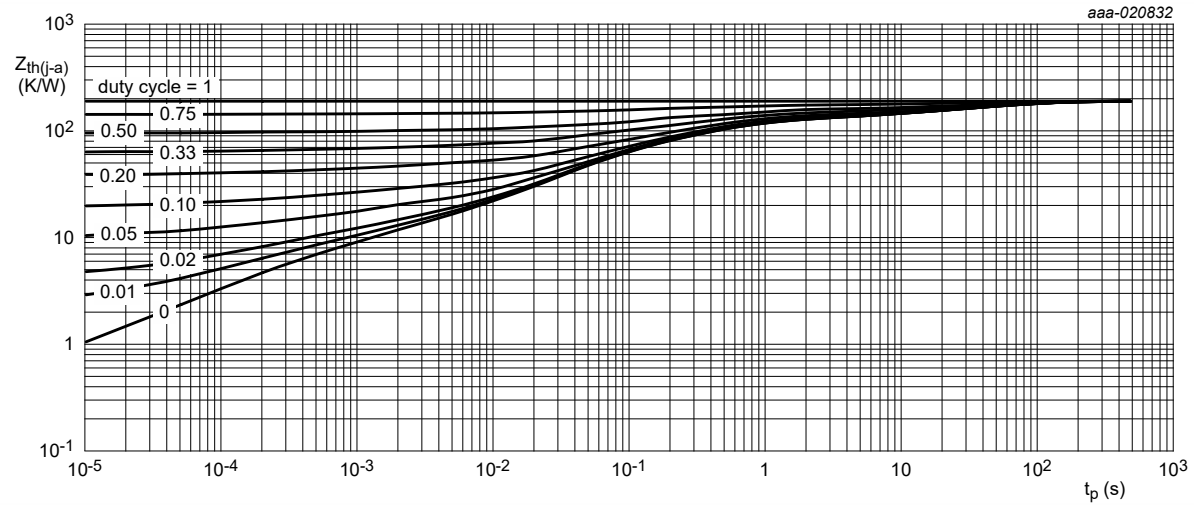
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for collector 1 cm^2.
[3] Device mounted on an FR4 Printed-Circuit Board (PCB), 4-layer copper, tin-plated and standard footprint.
[4] Device mounted on an FR4 Printed-Circuit Board (PCB), 4-layer copper, tin-plated, mounting pad for collector 1 cm^2.

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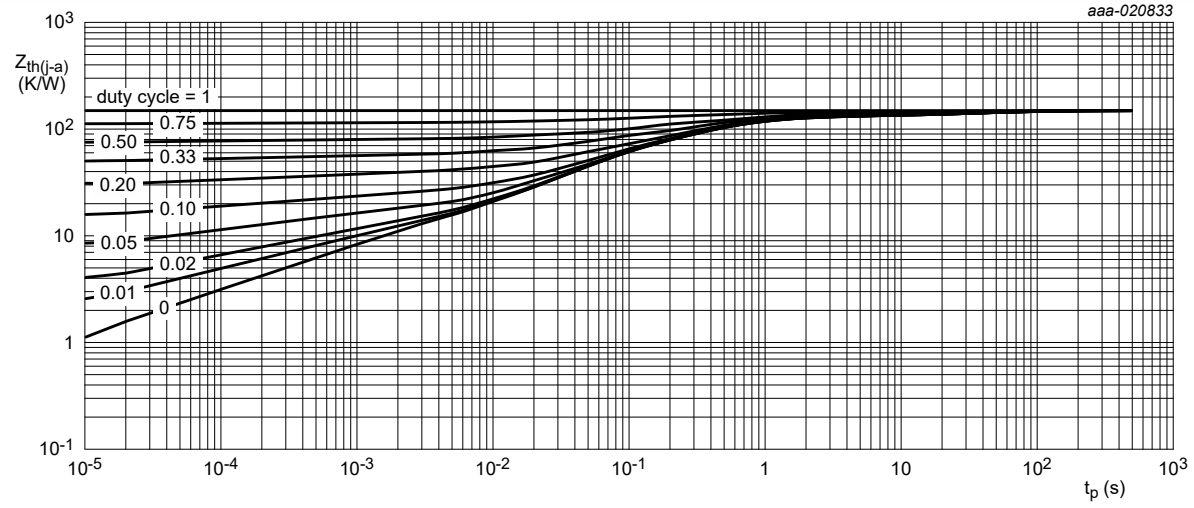
FR4 PCB, standard footprint

Fig. 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for collector 1 cm^2

Fig. 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

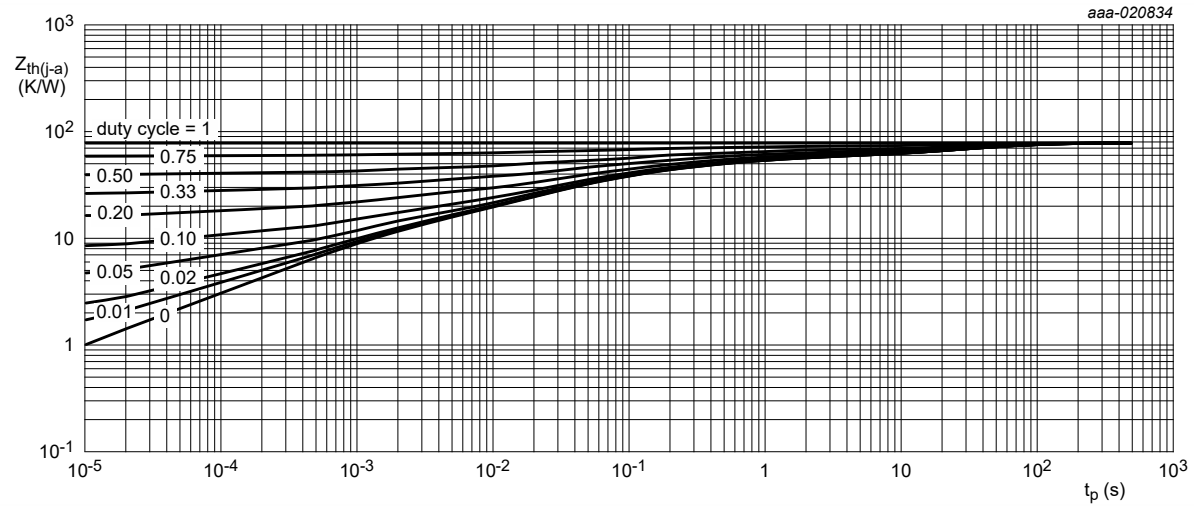


FR4 PCB, 4-layer copper, standard footprint

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

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FR4 PCB, 4-layer copper, mounting pad for collector 1 cm^2

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

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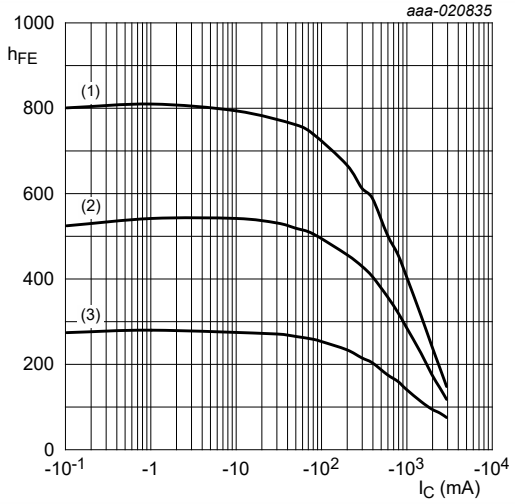
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
I_{CBO}	collector-base cut-off current	V_{CB} = -16 V; I_E = 0 A; T_{amb} = 25 °C		-	-	-100	nA
		V_{CB} = -16 V; I_E = 0 A; T_j = 150 °C		-	-	-50	µA
I_{EBO}	emitter-base cut-off current	V_{EB} = -5 V; I_C = 0 A; T_{amb} = 25 °C		-	-	-100	nA
I_{CES}	collector-emitter cut-off current	V_{CE} = -16 V; V_{BE} = 0 V; T_{amb} = 25 °C		-	-	-100	nA
h_{FE}	DC current gain	V_{CE} = -2 V; I_C = -100 mA; pulsed; $t_p \leq$ 300 µs; $\delta \leq$ 0.02; T_{amb} = 25 °C		250	400	-	
		V_{CE} = -2 V; I_C = -500 mA; pulsed; $t_p \leq$ 300 µs; $\delta \leq$ 0.02; T_{amb} = 25 °C		210	300	-	
		V_{CE} = -2 V; I_C = -1 A; pulsed; $t_p \leq$ 300 µs; $\delta \leq$ 0.02; T_{amb} = 25 °C		160	250	-	
		V_{CE} = -2 V; I_C = -2 A; pulsed; $t_p \leq$ 300 µs; $\delta \leq$ 0.02		100	150	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = -0.5 A; I_B = -50 mA; pulsed; $t_p \leq$ 300 µs; $\delta \leq$ 0.02; T_{amb} = 25 °C		-	-70	-110	mV
		I_C = -1 A; I_B = -50 mA; pulsed; $t_p \leq$ 300 µs; $\delta \leq$ 0.02; T_{amb} = 25 °C		-	-150	-220	mV
		I_C = -0.7 A; I_B = -7 mA; pulsed; $t_p \leq$ 300 µs; $\delta \leq$ 0.02; T_{amb} = 25 °C		-	-145	-200	mV
		I_C = -2 A; I_B = -200 mA; pulsed; $t_p \leq$ 300 µs; $\delta \leq$ 0.02		-	-260	-390	mV
R_{CEsat}	collector-emitter saturation resistance	I_C = -1 A; I_B = -50 mA; pulsed; $t_p \leq$ 300 µs; $\delta \leq$ 0.02; T_{amb} = 25 °C		-	-	220	mΩ
V_{BEsat}	base-emitter saturation voltage	I_C = -0.5 A; I_B = -50 mA; pulsed; $t_p \leq$ 300 µs; $\delta \leq$ 0.02; T_{amb} = 25 °C		-	-0.9	-1	V
		I_C = -1 A; I_B = -50 mA; pulsed; $t_p \leq$ 300 µs; $\delta \leq$ 0.02; T_{amb} = 25 °C		-	-0.94	-1.1	V
		I_C = -2 A; I_B = -200 mA; pulsed; $t_p \leq$ 300 µs; $\delta \leq$ 0.02; T_{amb} = 25 °C		-	-1.13	-1.25	V
V_{BE}	base-emitter voltage	V_{CE} = -2 V; I_C = -0.5 A; T_{amb} = 25 °C		-	-0.75	-0.9	V
t_d	delay time	I_C = -1 A; I_{Bon} = -50 mA; I_{Boff} = 50 mA; T_{amb} = 25 °C		-	10	-	ns
t_r	rise time			-	50	-	ns
t_{on}	turn-on time			-	60	-	ns
t_s	storage time			-	200	-	ns
t_f	fall time			-	45	-	ns
t_{off}	turn-off time			-	245	-	ns
f_T	transition frequency	V_{CE} = -10 V; I_C = -50 mA; f = 100 MHz; T_{amb} = 25 °C		-	95	-	MHz
C_c	collector capacitance	V_{CB} = -10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	25	-	pF

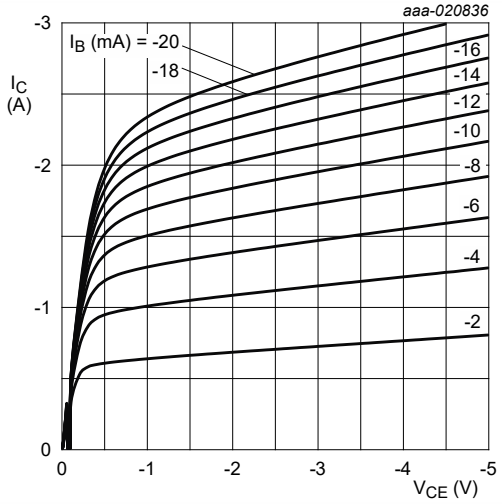
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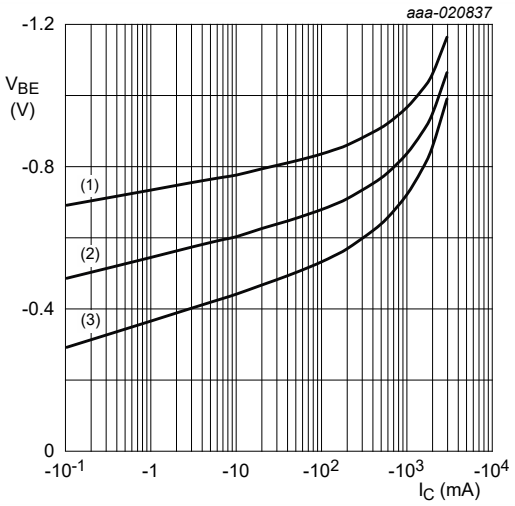
V_{CE} = −2 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = −55 °C

Fig. 6. DC current gain as a function of collector current; typical values



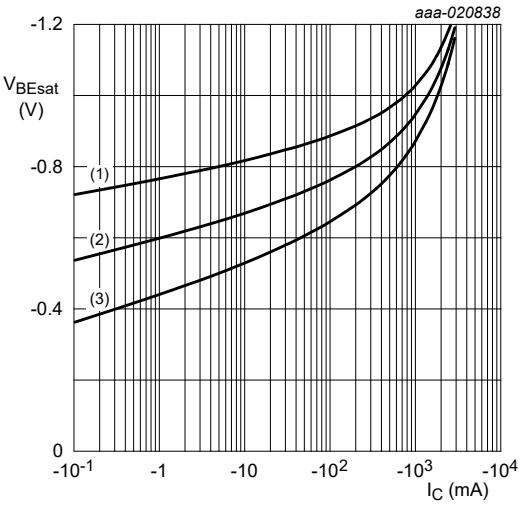
T_{amb} = 25 °C

Fig. 7. Collector current as a function of collector-emitter voltage; typical values



V_{CE} = −2 V
(1) T_{amb} = −55 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 8. Base-emitter voltage as a function of collector current; typical values

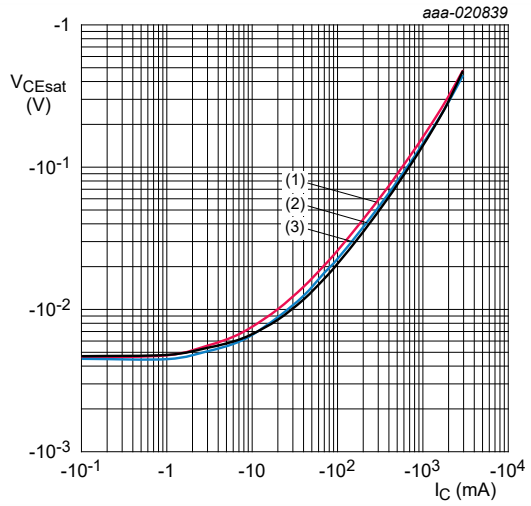


I_C/I_B = 20
(1) T_{amb} = −55 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 9. Base-emitter saturation voltage as a function of collector current; typical values

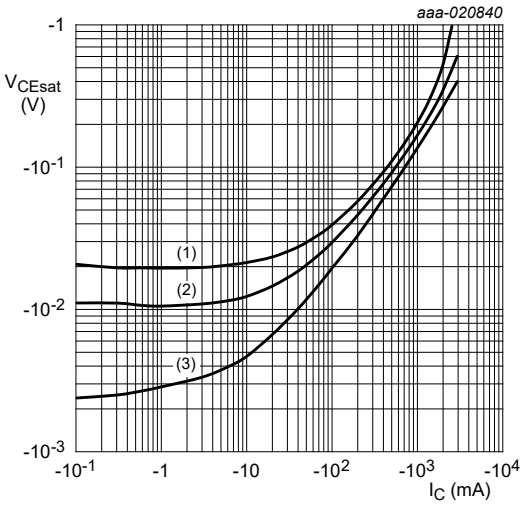
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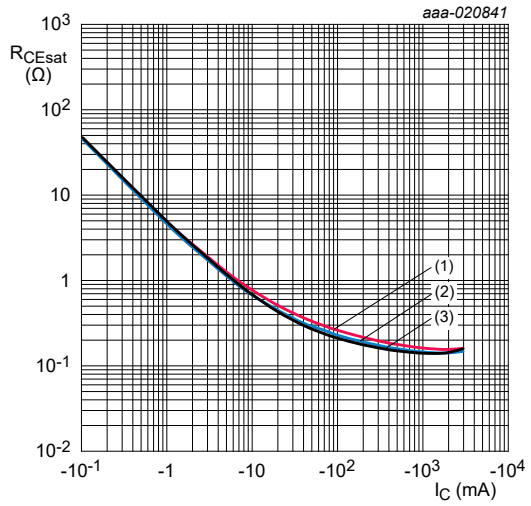
I_C/I_B = 20
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = −55 °C

Fig. 10. Collector-emitter saturation voltage as a function of collector current; typical values



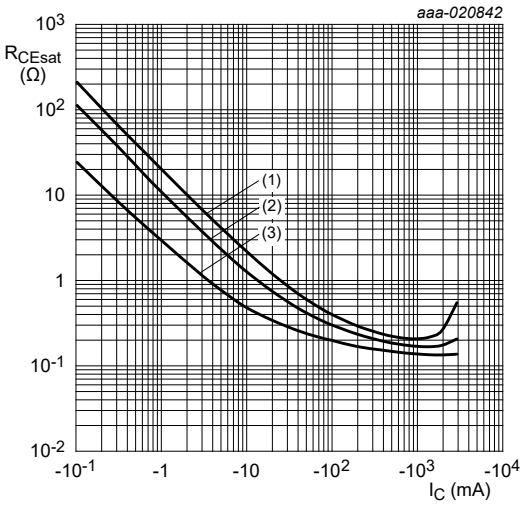
T_{amb} = 25 °C
(1) I_C/I_B = 100
(2) I_C/I_B = 50
(3) I_C/I_B = 10

Fig. 11. Collector-emitter saturation voltage as a function of collector current; typical values



I_C/I_B = 20
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = −55 °C

Fig. 12. Collector-emitter saturation resistance as a function of collector current; typical values



T_{amb} = 25 °C
(1) I_C/I_B = 100
(2) I_C/I_B = 50
(3) I_C/I_B = 10

Fig. 13. Collector-emitter saturation resistance as a function of collector current; typical values

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11. Test information

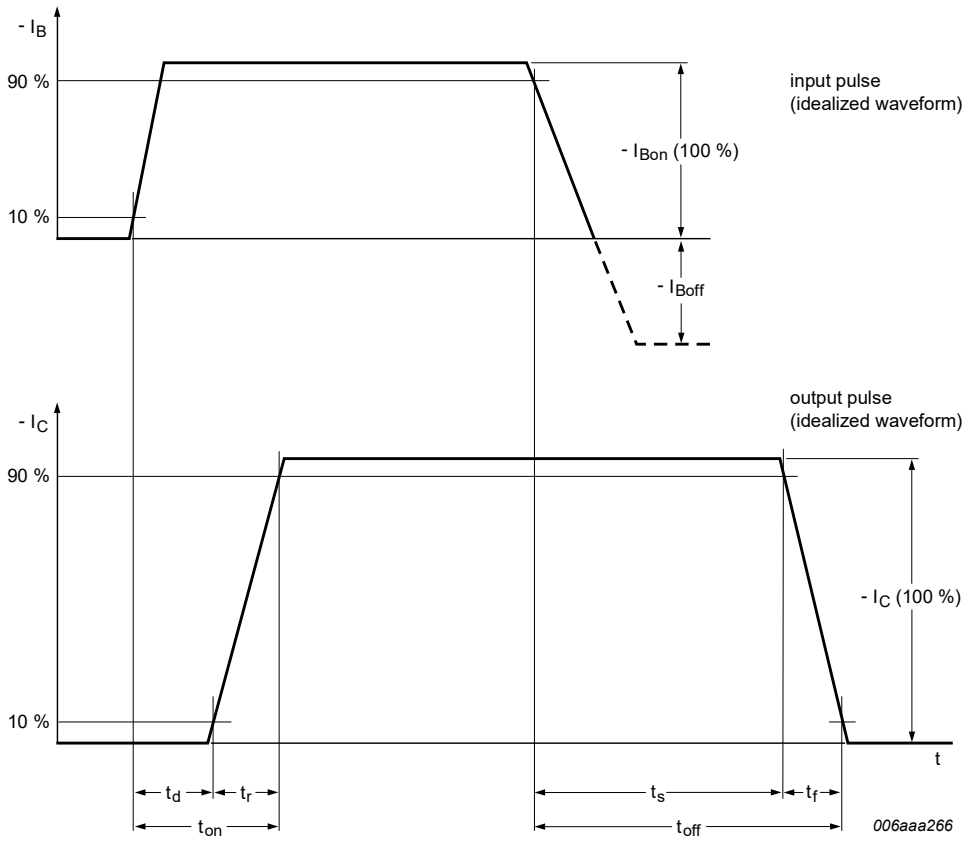


Fig. 14. Transistor switching time definition

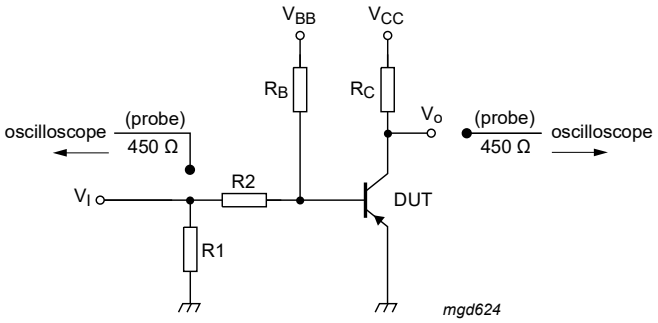


Fig. 15. Test circuit for switching times

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

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12. Package outline

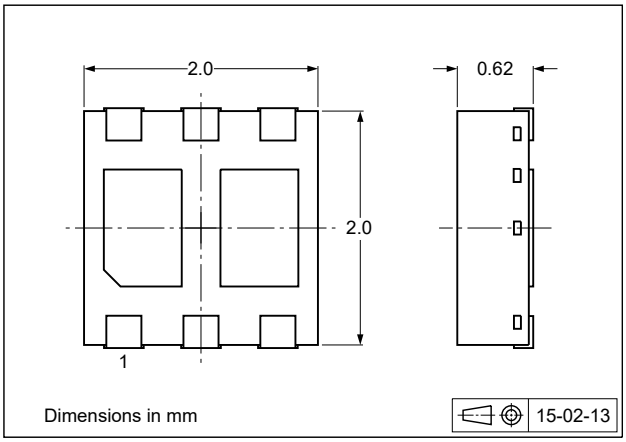


Fig. 16. Package outline DFN2020D-6 (SOT1118D)

13. Soldering

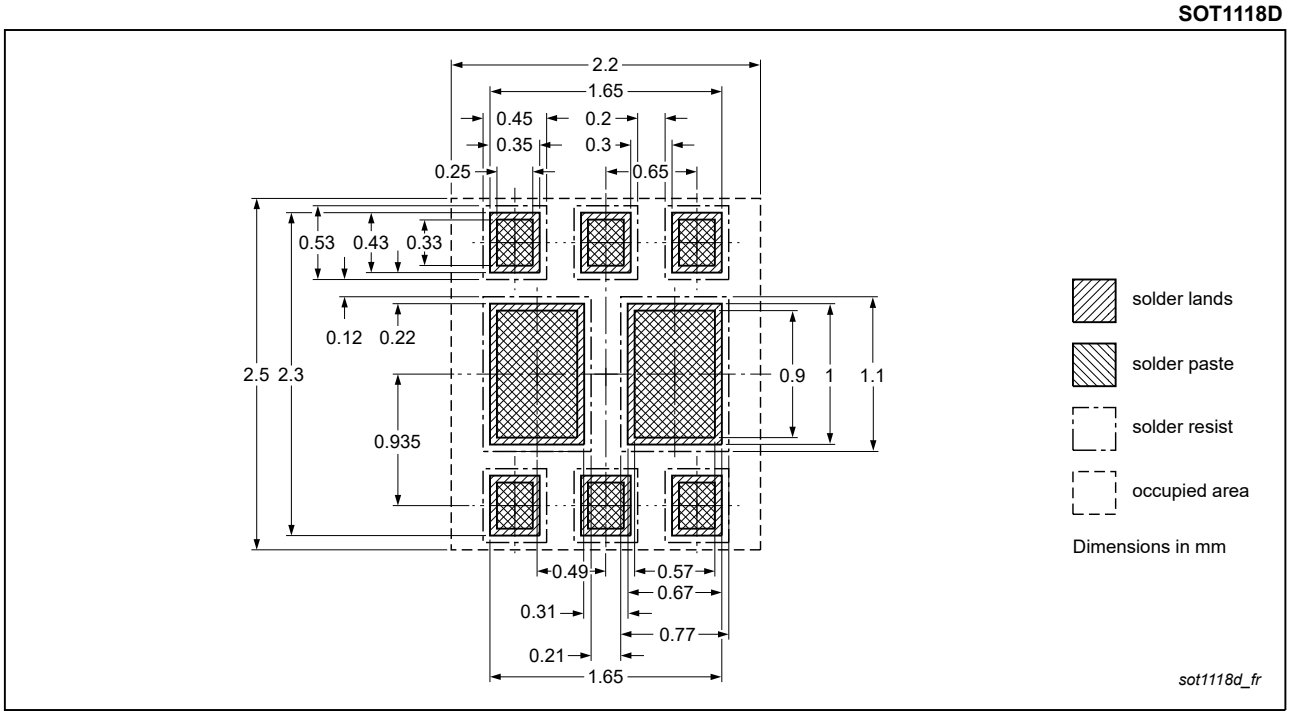


Fig. 17. Reflow soldering footprint for DFN2020D-6 (SOT1118D)

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14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PBSS5220PAPS-Q v.1	20230925	Product data sheet	-	-

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15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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For more information, please visit: http://www.nexperia.com
For sales office addresses, please send an email to: salesaddresses@nexperia.com
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