650V GaN Power Stage

1 FEATURES

- Monolithically-Integrated gate driver
- 7V-20V Wide Supply Voltage Range
- -5V - 20V Wide Logic Input Voltage Capability
- TTL Input-Logic Threshold
- 650V GaN HEMT with Low 150 mΩ On Resistance
- Zero reverse recovery charge
- Up to 1 MHz operation
- Low Quiescent Current: 120uA
- Output Low When Input Floating
- Available in PDFN 5x6 mm Package

2 APPLICATIONS

- AC-DC, DC-DC
- Buck, boost, half bridge, full bridge
- Active Clamp Flyback, LLC resonant
- Mobile fast-chargers, adapters
- Notebook adaptors
- LED lighting, solar micro-inverters
- TV / monitor, wireless power
- Server, telecom & networking SMPS

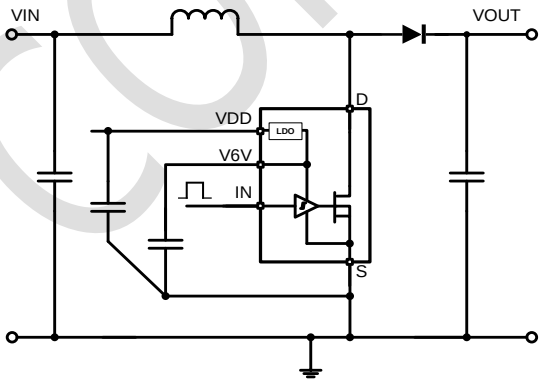
3 ORDERING INFORMATION

TYPE	MARKING	PACKAGE
GBP65200GPMAR	65200	PDFN 5x6

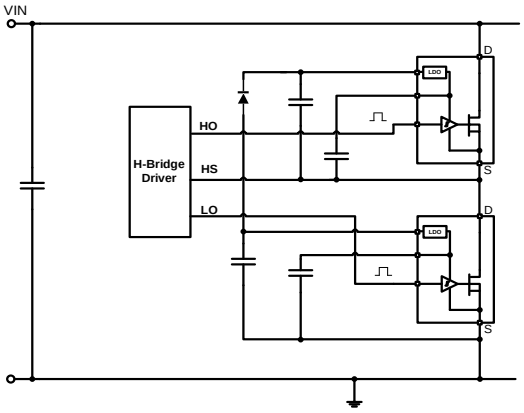
4 DISCRIPTION

The GBP65200G is a 650V GaN Power Stage, optimized for high frequency, soft-switching topologies. The monolithic integration of GaN, driver and logic create an easy-to-use high-performance powertrain building block, enabling designers to create the fastest, smallest, most efficient integrated powertrain. Down to -5V input capability enhances the input noise immunity. Very low quiescent current reduces the stand by power loss in the power converter. The device adopts non-overlap driver design to avoid the shoot-through of output stage.

5 TYPICAL APPLICATIONS

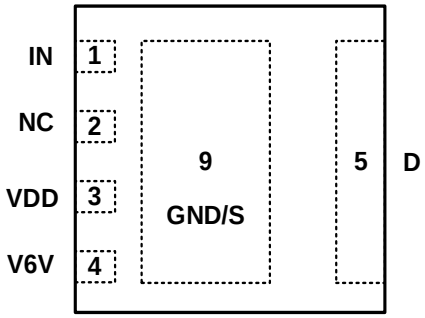


BOOST



Half Bridge

6 PIN CONFIGURATION AND FUNCTIONS



Top View: GBP65200G PDFN 5x6

PIN OUT		I/O	PIN FUNCTION
NAME	NO.		
IN	1	I	Logic input, TTL compatible. Floating logic low. Apply PWM signal on this pin.
NC	2	N/A	No Connection inside. Must be connected to terminal S.
VDD	3	I	Power supply of gate driver circuit, must be decoupled by ceramic cap. A 0.1uF, and 1uF or 10uF are recommended.
V6V	4	I	An integrated LDO output, must be decoupled by ceramic cap. A 0.1uF, and 1uF or 10uF are recommended.
GND/S	9	I	GaN IC supply ground & Source of power HEMT. Must be soldered directly to ground planes for improved thermal performance and electrical contact.
D	5~8	O	Drain of power HEMT.

7 SPECIFICATIONS

7.1 ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
Drain to Source Voltage	V_{DS}	0	650	V
Power Supply Voltage	V_{DD}	7	22	V
V6V Voltage	V_{V6V}	0	6.5	V

PWM Input Voltage	V_{IN}	-5	22	V
Operating junction temperature T_J (2)	T_J	-40	125	°C
Storage temperature T_{STG}	T_{STOR}	-65	150	°C

(1) Stresses beyond those listed under Absolut Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

7.2 ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)	-2	+2	kV
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins (1)	-1	+1	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

7.3 RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{DS}	Drain to Source Voltage	0	650	V
V_{DD}	Power Supply Voltage	8	20	V
V_{V6V}	V6V LDO Output Voltage	0	6.5	V
T_J	Operating junction temperature T_J	-40	125	°C

7.4 THERMAL INFORMATION

PARAMETER	THERMAL METRIC	PDFN 5x6	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance	50	°C/W
$R_{\theta JC}$	Junction to case thermal resistance	2.2	°C/W

7.5 ELECTRICAL CHARACTERISTICS

V_{DD}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
VDD Power Supply						
V_{DD}	Operating supply voltage		8		20	V
V_{DD_UVLO}	Input UVLO	V_{DD} rising		5	5.2	V
	Hysteresis			500		mV
I_Q	Quiescent current	V_{PWM}=GND, V_{DD}=12V		120	200	uA
V_{V6V}	LDO output voltage	V_{DD}=12V, I_{V6V}=0mA	5.8	6.2	6.5	V
		V_{DD}=12V, I_{V6V}=10mA	5.8	6.2	6.5	V
PWM INPUTS						
V_{IN_H}	Input logic high threshold			3.1	3.5	V
V_{IN_L}	Input logic low threshold		0.8	1.1		V
V_{IN+_Hys}	Hysteresis			2.0		V
Timing						
T_R	Output rising time	V_{DS}=0V to 400V, I_{DS}=4A, see Figure 2		8		ns
T_F	Output falling time	V_{DS}=400V to 0V, I_{DS}=4A, see Figure 2		4		ns
T_{ON}	Turn on propagation delay	See Figure 2		15		ns
T_{OFF}	Turn off propagation delay	See Figure 2		15		ns
T_{MIN_ON}	Minimum input pulse width			20	30	ns
F_{SW}	Switching Frequency				1	MHz
GaN HEMT						
I_{DS}	Continuous Drain-Source current	V_{PWM}=6V, V_{DS}=1V		6.8		A
I_{DSS}	Drain-Source leakage current	V_{DS}=650V, V_{PWM}=0V		0.3	1	uA
$R_{DS(ON)}$	On state Drain-Source resistance	V_{PWM}=6V, I_{DS}=4A		150	180	mΩ
V_{SD}	Source-Drain reverse voltage	V_{PWM}=0V, I_{SD}=4A		3		V
C_{OSS}	Output capacitance	V_{DS}=400V, V_{PWM}=0V		30		pF
Q_{OSS}	Output charge	V_{DS}=400V, V_{PWM}=0V		25		nC

7.6 Switching Characteristics

(GaN HEMT, Tc=25C unless otherwise specified)

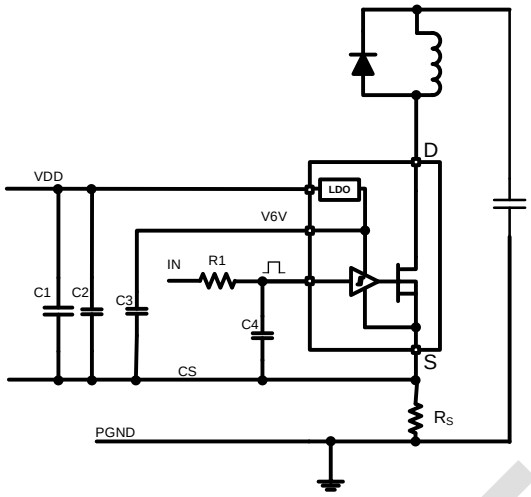


Figure 1. Inductive double pulse test bench

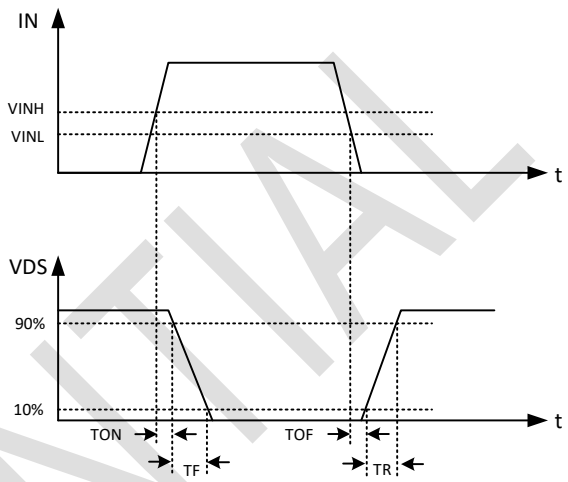


Figure 2. Switching timing definition

8 DISCRIPTION

(GaN HEMT, Tc=25°C unless otherwise specified)

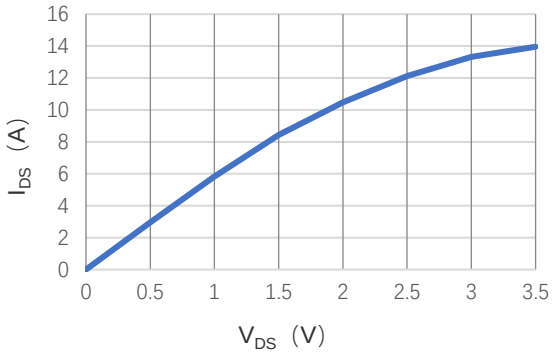


Figure 3. I_{DS} Vs Drain to Source V_{DS}

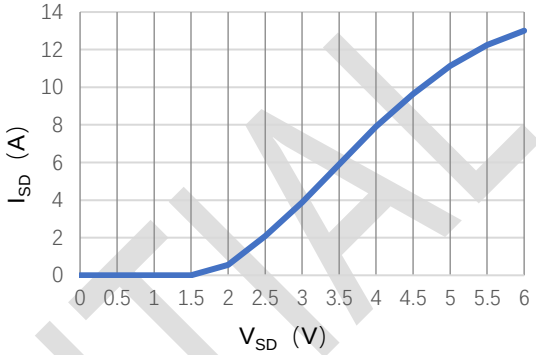


Figure 4. I_{SD} Vs Source to Drain V_{SD}

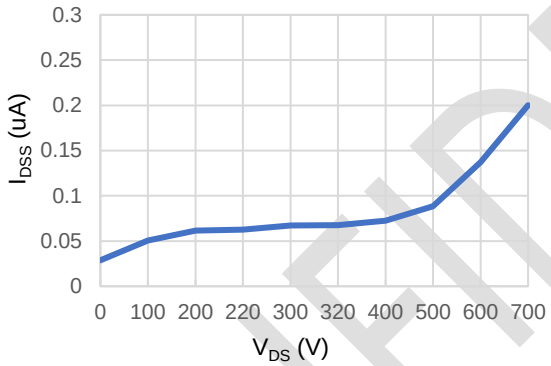


Figure 5. I_{DSS} Vs Drain to Source V_{DS}

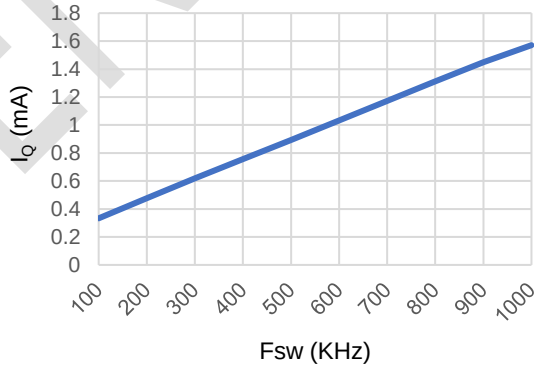


Figure 6. I_Q Vs. Switching Frequency

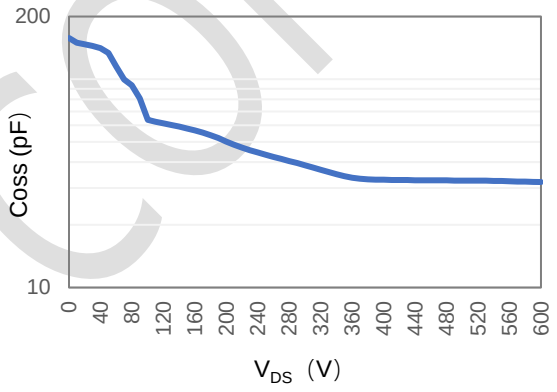


Figure 7. C_{OSS} Vs. Drain to Source Voltage V_{DS}

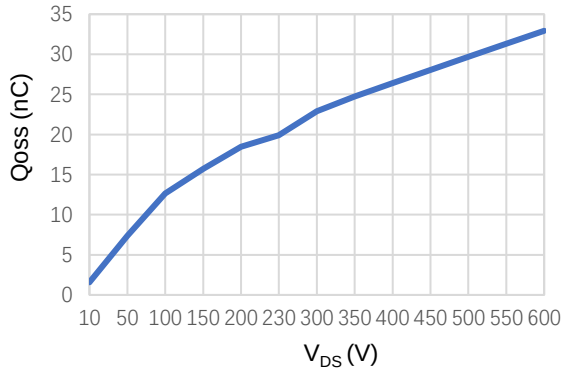


Figure 8, Qoss Vs. Drain to Source Voltage V_{DS}

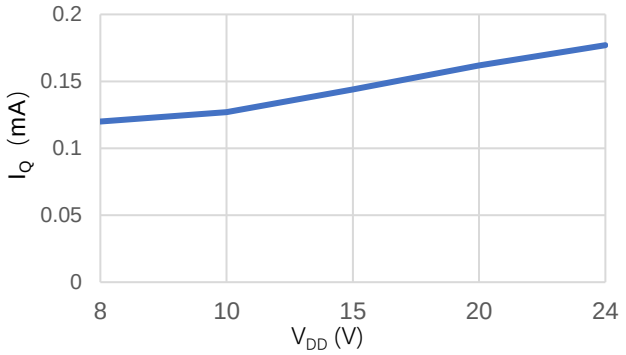


Figure 9. I_Q Vs. VDD

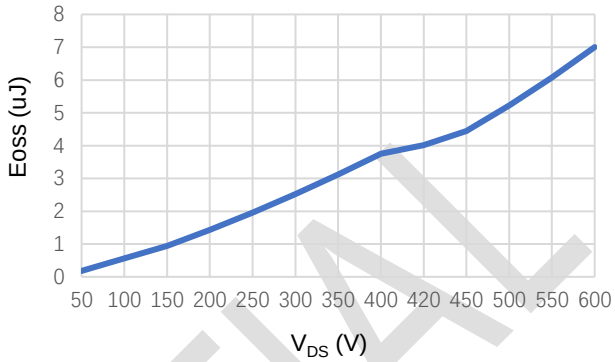


Figure 10. Eoss Vs Drain to Source Voltage V_{DS}

9 DISCRIPTION

9.1 GENERAL DESCRIPTION

The GBP65200G is a 650V GaN Power Stage, integrated high-speed driver and a 150 mΩ GaN HEMT, which is optimized for high frequency, soft-switching topologies. Up to 1MHz switching frequency allows designers to develop higher power density power supply.

The GBP65200G supports wide PWM input hysteresis which is compatible for TTL low voltage logic. TTL logic input simplifies the PWM input circuit design without any extra buffer or level shift circuit. Meanwhile, the wide hysteresis increases the noise immunity. The GBP65200G has very low quiescent current that reduces the standby power loss in the power converter.

A 6.2V LDO is integrated in the gate driver, the LDO supplies the power to the gate of HEMT GaN directly, which simplifies the off chip components and minimize the PCB board in the layout.

The GBP65200G internal driver provides minimum propagation delay 15ns from input to output. The ability to handle -5V DC input increases the driver input stage noise immunity, and the rail-to-rail driver improves the GBP65200G output stage robustness during the switching load fast transition.

9.2 VDD POWER SUPPLY

The GBP65200G supply voltage is ranging between 7V to 20V. For best circuit performance, two VDD bypass capacitors in parallel are recommended to prevent noise problems on supply VDD. A 0.1-μF surface mount ceramic capacitor must be located as close as possible to the VDD to GND pins. In addition, a big-value capacitor (exp. 1μF or 10uF) with relatively low ESR must be connected in parallel, in order to avoid unexpected VDD supply glitch. The parallel combination of capacitors presents a low impedance characteristic for the expected current levels and switching frequencies in the application.

9.3 PWM INPUT

The PWM input is compatible to TTL logic, which make the device easy-to-use by PWM control signals.

The wide input hysteresis, with typically 3.1V high threshold and 1.1V low threshold, offers enhanced noise immunity compared to traditional TTL logic implementation. GBP65200G also features tight control of the input threshold voltage that ensures stable operation across temperature. The low input capacitance on the input pins increases switching speed and reduces the propagation delay.

9.4 UNDER VOLTAGE LOCK OUT (UVLO)

The GBP65200G implements the Under Voltage Lock Out (UVLO) with rising threshold of typically 5 V along with 500mV typical hysteresis. The UVLO holds the output low regardless of the input status when

VDD is rising but the level is below the UVLO threshold. The hysteresis prevents output bouncing for avoiding the noise impact on the power supply. During power up, the driver output remains low until the VDD voltage reaches the UVLO threshold. The magnitude of the OUT signal rises with VDD till steady state VDD reached.

Figure 11 shows that the output remains low till the UVLO threshold reached, and then the VDS is in-phase with the PWM input.

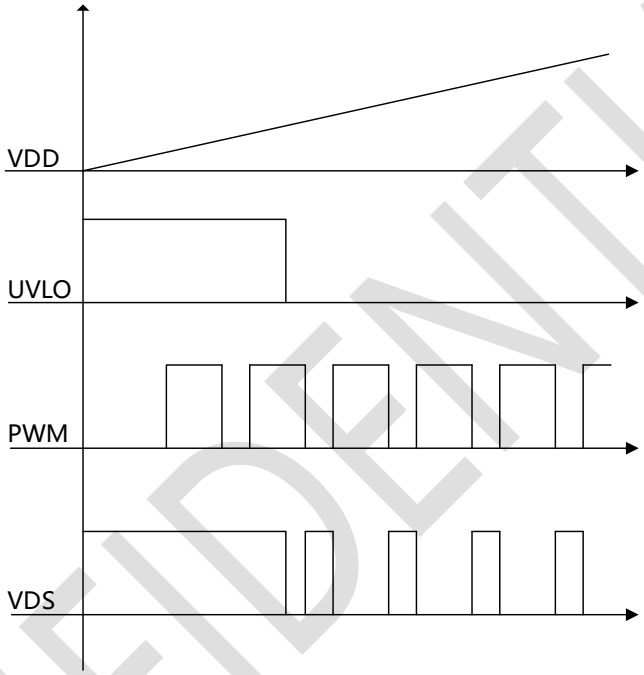


Figure 11 GBP65200G VDS Vs VDD

9.5 START UP

The GBP65200G holds the driver low when VDD is below Under Voltage Lock Out threshold (VDD_UVLO). For example, in active clamp flyback (ACF) applications, the half-bridge must be ready very quickly due to the soft-start mode of the ACF controller. As Figure 12 shows, when the first few PWM pulses are generated by the ACF controller, the high-side supply pins of the GBP65200G will require a few low-side pulses to charge up (through the external bootstrap diode) before the high-side starts to switch.

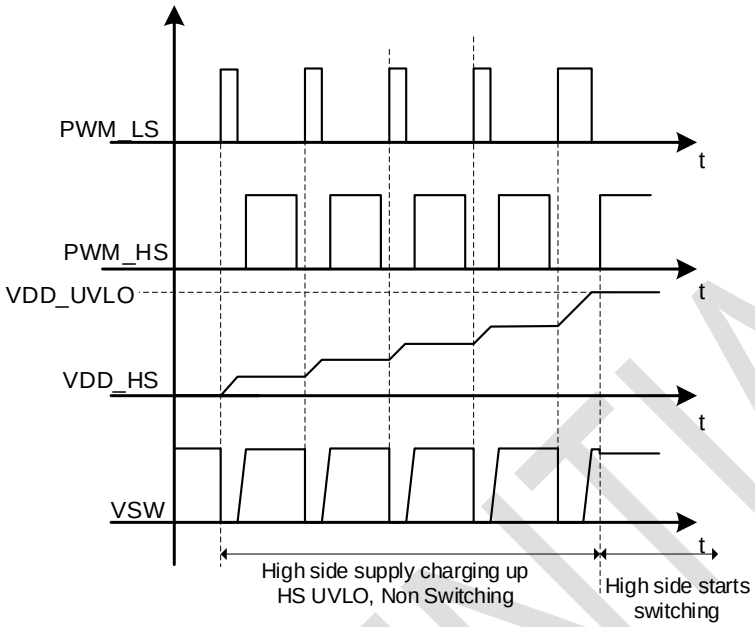


Figure 12 ACF half-bridge start-up timing

To achieve the minimum R_{dson} of GaN HEMT, the gate of GaN HEMT needs be as high as 6V. As a result, the recommend minimum VDD of GBP65200 is 8V.

10 APPLICATION INFORMATION

10.1 TYPICAL APPLICATION

Figure 13 is typical application schematic with current sensing resistor. Table1 shows the recommended component values for this application. Those components should be put as close as possible to the power stage. Please see layout guideline for more information.

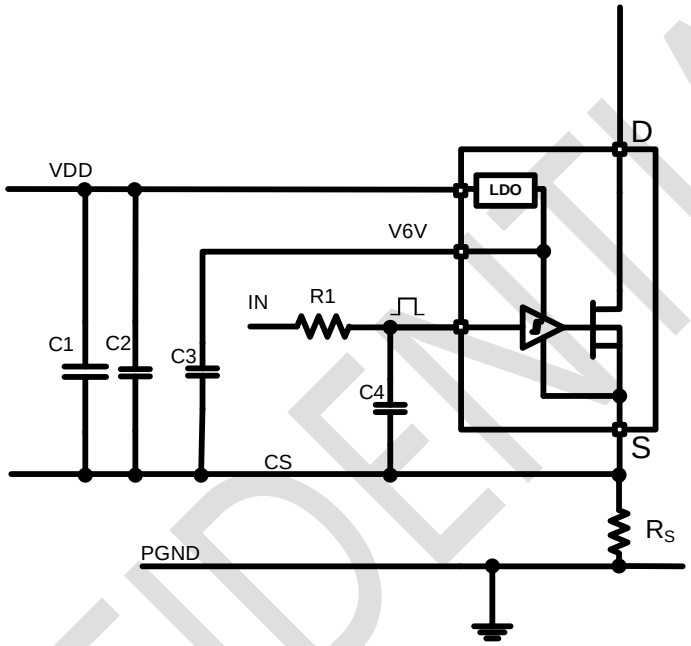


Figure 13 Typical Application Schematic

Table 1 Recommended Component value

Symbol	Description	Value	Unit
C1	VDD input capacitor	10	uF
C2	VDD decouple capacitor	0.1	uF
R1	PWM filter resistor	10	Ω
C4	PWM filter capacitor	100	pF
C3	LDO output capacitor	4.7	uF

11 LAYOUT GUIDELINE

The GBP65200G provides features very short rising and falling time at the power topology. The high di/dt causes unexpected ringing when high di/dt loop is not optimized. The regulator could suffer from malfunction and EMI noise if the device has serious ringing. Below are the layout recommendations with using GBP65200G and the layout example with sensing resistor.

The following rules should be followed carefully during the design of the PCB layout:

1) Place all IC filter and programming components directly next to the IC. These components include C_{VDD}, R_{PWM}, C_{PWM}, C_{V6V}.

2) Keep ground trace of IC filter and programming components separate from power GND trace. Do not run power GND currents through ground trace of filter components.

3) For best thermal management, place thermal vias in the source pad area to conduct the heat out through the bottom of the package and through the PCB board to other layers.

4) Use large PCB thermal planes (connected with thermal vias to the source pad) and additional PCB layers to reduce IC temperatures as much as possible. (for example, 4-layers)

5) For half-bridge layouts, do not extend copper planes from one IC across the components or pads of the other IC.

6) For high density designs use a 4-layer PCB and 2 oz. copper to route signal connections. This allows layout to maintain large thermal copper planes and reduce power device temperature.

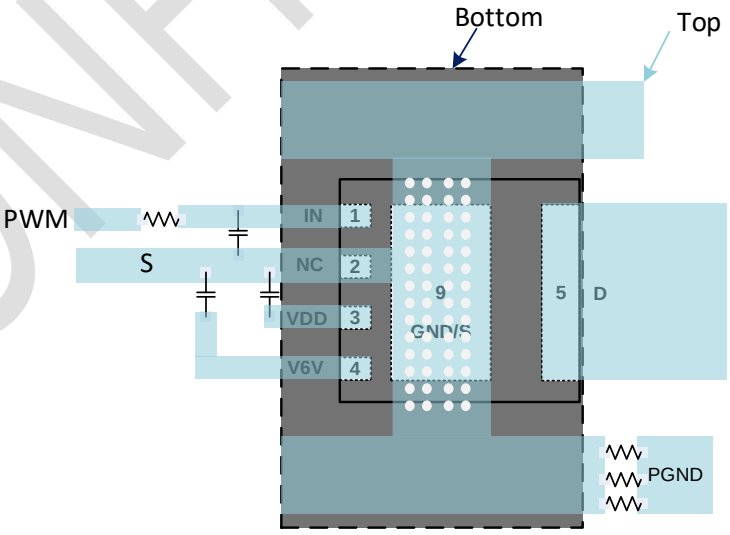


Figure 14 GBP65200G PCB Layout Example with sensing resistor

11.1 THERMAL CONSIDERATIONS

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation (1).

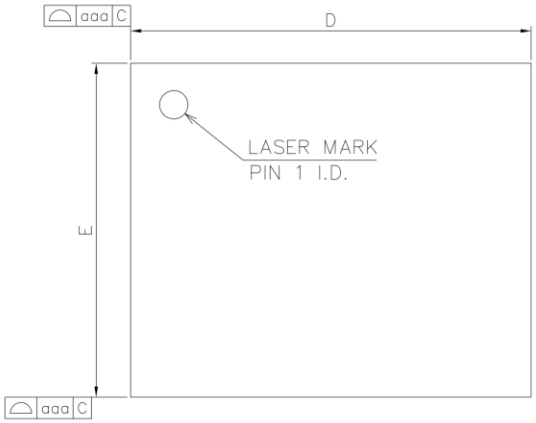
$$P_{D(MAX)} = \frac{125 - T_A}{R_{\theta JA}} \quad (1)$$

where

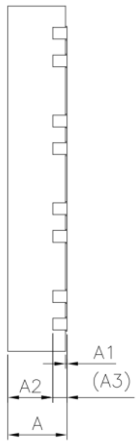
- T_A is the maximum ambient temperature for the application.
- $R_{\theta JA}$ is the junction-to-ambient thermal resistance given in the Thermal Information table.

The real junction-to-ambient thermal resistance $R_{\theta JA}$ of the package greatly depends on the PCB type, layout, and environmental factor. Soldering the ground pin to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

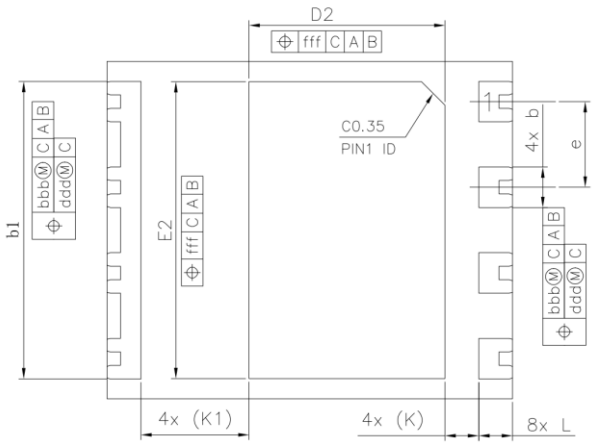
PACKAGE INFORMATION



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Item		Symbol	MIN.	NOM.	MAX.
total height		A	0.80	0.85	0.90
stand off		A1	0.00	0.02	0.05
mold thickness		A2	–	0.65	–
leadframe thickness		A3		0.20 REF.	
lead width		b	0.55	0.60	0.65
		b1	0.36	0.41	0.46
package size	X	D	5.90	6.00	6.10
	Y	E	4.90	5.00	5.10
E-PAD size	X	D2	2.80	2.90	3.00
	Y	E2	4.30	4.40	4.50
lead length		L	0.40	0.50	0.60
lead pitch		e		1.27 bsc	
lead tip to exposed pad edge		K		0.50 ref	
		K1		1.60 ref	
Package edge tolerance		aaa		0.10	
Lead offset		bbb		0.05	
Mold flatness		ccc		0.10	
Coplanarity		eee		0.08	
Exposed pad offset		fff		0.10	

Note:

All dimensions do not include mold flash or protrusions.

All dimensions are with unite of ‘mm’.

