TMUX405x 24V, 8:1, 1-Channel, 4:1, 2-Channel and 2:1, 3-Channel Multiplexers with 1.8V Logic

1 Features

- Single supply range: 5V to 24V
- Dual supply range: up to ±12V
- Low capacitance: 3pF
- –55°C to +125°C operating temperature
- Bidirectional signal path
- Rail-to-rail operation
- 1.8V logic compatible
- Break-before-make switching
- ESD protection HBM: 2000V
- TMUX405x – pin compatible with:
  - Industry standard 4051, 4052, and 4053 muxes

2 Applications

- Analog multiplexing and demultiplexing
- Factory automation and control
- Appliances
- Battery test equipment
- Power delivery
- Medical
- Building automation
- Grid infrastructure

3 Description

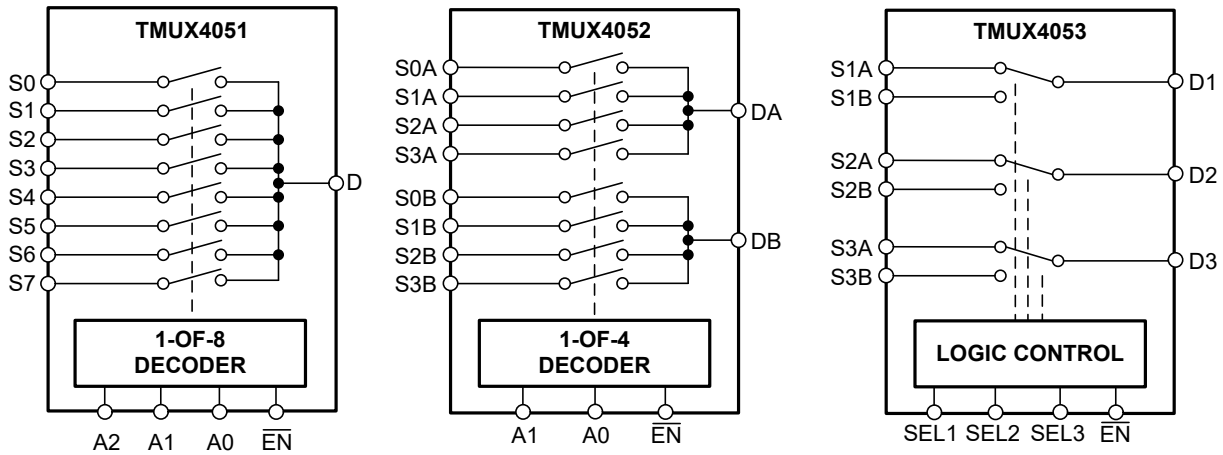
The TMUX405x devices are general purpose complementary metal-oxide semiconductor (CMOS) multiplexers (MUX). The TMUX4051 is an 8:1, 1-channel multiplexer, the TMUX4052 is a 4:1, 2-channel multiplexer, and the TMUX4053 is 2:1, 3 channel switch. The devices work with a single supply (5V to 24V), dual supplies (up to ±12V), or asymmetric supplies (such as V_{DD} = 12V, V_{SS} = –5V). The wide supply voltage range allows the TMUX405x devices to be used in a broad array of applications from battery testers to appliances.

The TMUX405x devices support bidirectional analog signals on the source (Sx) and drain (Dx) pins ranging from V_{SS} to V_{DD}. All logic inputs have 1.8V logic compatible thresholds, which is compatible for both TTL and CMOS logic when operating with a valid supply voltage.

Table 3-1. Package Information

PART NUMBER (1)	CHANNEL COUNT	PACKAGE (2)
TMUX4051	1-Channel	PW (TSSOP, 16)
TMUX4052	2-Channel	DYY (SOT-23-THIN, 16)
TMUX4053	3-Channel	BQB (WQFN, 16)

(1) See the Device Comparison Table
(2) For more information, see Section 12.



TMUX4051, TMUX4052, and TMUX4053 Block Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Device Comparison Table

PRODUCT	DESCRIPTION
TMUX4051	8:1, 1-channel multiplexer
TMUX4052	4:1, 2-channel multiplexer
TMUX4053	2:1, 3-channel switch

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5 Pin Configuration and Functions

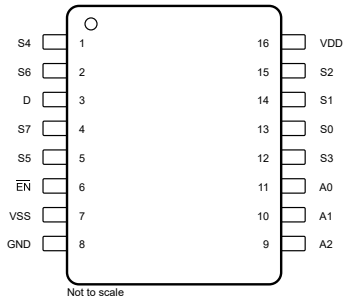


Figure 5-1. TMUX4051 PW Package, 16-Pin TSSOP (Top View)

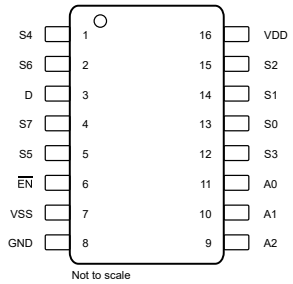


Figure 5-2. TMUX4051 DYY Package, 16-Pin SOT-23-THIN (Top View)

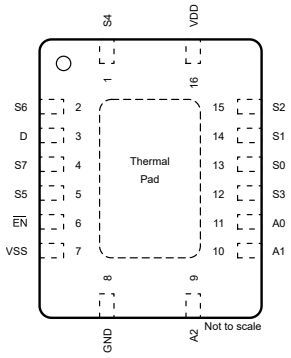


Figure 5-3. TMUX4051 BQB Package, 16-Pin WQFN (Top View)

Table 5-1. Pin Functions TMUX4051

PIN		TYPE[1]	DESCRIPTION[2]
NAME	NO.		
S4	1	I/O	Source pin 4. Signal path can be an input or output.
S6	2	I/O	Source pin 6. Signal path can be an input or output.
D	3	I/O	Drain pin (common). Signal path can be an input or output.
S7	4	I/O	Source pin 7. Signal path can be an input or output.
S5	5	I/O	Source pin 5. Signal path can be an input or output.
$\overline{EN}$	6	I	Active low logic enable. When this pin is high, all switches are turned off. Table 8-1 lists how the A[2:0] address inputs determine which switch is turned on when this pin is low.
V_{SS}	7	P	Negative power supply. This pin is the most negative power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between V_{SS} and GND.
GND	8	P	Ground (0V) reference
A2	9	I	Address line 2. Table 8-1 provides information about how A2 controls the switch configuration.
A1	10	I	Address line 1. Table 8-1 provides information about how A1 controls the switch configuration.
A0	11	I	Address line 0. Table 8-1 provides information about how A0 controls the switch configuration.
S3	12	I/O	Source pin 3. Signal path can be an input or output.
S0	13	I/O	Source pin 0. Signal path can be an input or output.
S1	14	I/O	Source pin 1. Signal path can be an input or output.
S2	15	I/O	Source pin 2. Signal path can be an input or output.
V_{DD}	16	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between V_{DD} and GND.
Thermal pad		—	The thermal pad is not connected internally. It is recommended that the pad be left floating or tied to GND.

(1) I = input, O = output, I/O = input and output, P = power.
(2) For what to do with unused pins, refer to Section 8.3.4.

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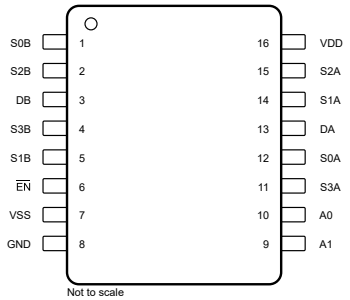


Figure 5-4. TMUX4052 PW Package, 16-Pin TSSOP (Top View)

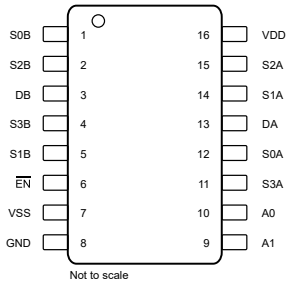


Figure 5-5. TMUX4052 DYY Package, 16-Pin SOT-23-THIN (Top View)

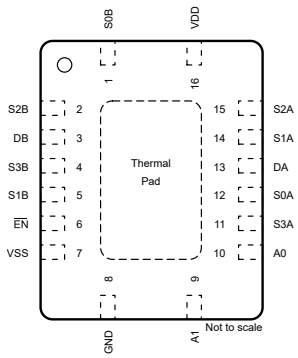


Figure 5-6. TMUX4052 BQB Package, 16-Pin WQFN (Top View)

Table 5-2. Pin Functions TMUX4052

PIN		TYPE[1]	DESCRIPTION[2]
NAME	NO.		
S0B	1	I/O	Source pin 0 of mux B. Can be an input or output.
S2B	2	I/O	Source pin 2 of mux B. Can be an input or output.
DB	3	I/O	Drain pin (common) of mux B. Can be an input or output.
S3B	4	I/O	Source pin 3 of mux B. Can be an input or output.
S1B	5	I/O	Source pin 1 of mux B. Can be an input or output.
$\overline{EN}$	6	I	Active low logic enable. When this pin is high, all switches are turned off. When this pin is low, the A[1:0] address inputs determine which switch is turned on.
V_{SS}	7	P	Negative power supply. This pin is the most negative power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between V_{SS} and GND.
GND	8	P	Ground (0V) reference
A1	9	I	Address line 1. Table 8-2 provides information about how A1 controls the switch configuration.
A0	10	I	Address line 0. Table 8-2 provides information about how A0 controls the switch configuration.
S3A	11	I/O	Source pin 3 of mux A. Can be an input or output.
S0A	12	I/O	Source pin 0 of mux A. Can be an input or output.
DA	13	I/O	Drain pin (common) of mux A. Can be an input or output.
S1A	14	I/O	Source pin 1 of mux A. Can be an input or output.
S2A	15	I/O	Source pin 2 of mux A. Can be an input or output.
V_{DD}	16	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between V_{DD} and GND.
Thermal pad		—	The thermal pad is not connected internally. It is recommended that the pad be left floating or tied to GND.

(1) I = input, O = output, I/O = input and output, P = power.
(2) For what to do with unused pins, refer to Section 8.3.4 .

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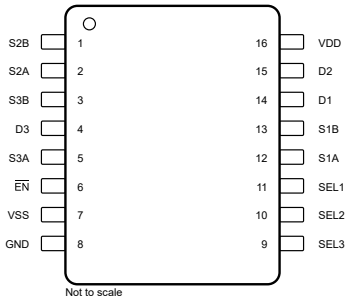


Figure 5-7. TMUX4053 PW Package, 16-Pin TSSOP (Top View)

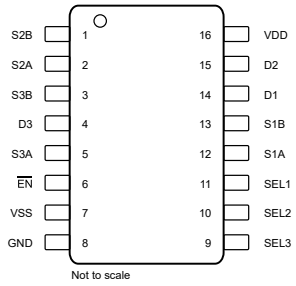


Figure 5-8. TMUX4053 DYY Package, 16-Pin SOT-23-THIN (Top View)

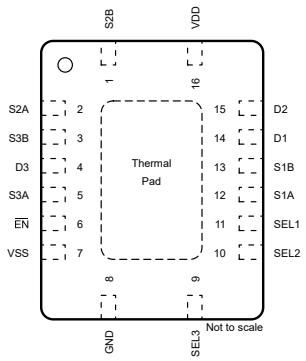


Figure 5-9. TMUX4053 BQB Package, 16-Pin WQFN (Top View)

Table 5-3. Pin Functions TMUX4053

PIN		TYPE[1]	DESCRIPTION[2]
NAME	NO.		
S2B	1	I/O	Source pin B of switch 2. Can be an input or output.
S2A	2	I/O	Source pin A of switch 2. Can be an input or output.
S3B	3	I/O	Source pin B of switch 3. Can be an input or output.
D3	4	I/O	Drain pin (common) of switch 3. Can be an input or output.
S3A	5	I/O	Source pin A of switch 3. Can be an input or output.
$\overline{EN}$	6	I	Active low logic enable. When this pin is high, all switches are turned off. When this pin is low, the SEL[x] logic control inputs determine which switch is turned on.
V_{SS}	7	P	Negative power supply. This pin is the most negative power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between V_{SS} and GND.
GND	8	P	Ground (0V) reference
SEL3	9	I	Logic control select pin 3. Table 8-2 provides controls switch 3 configuration.
SEL2	10	I	Logic control select pin 2. Table 8-2 provides controls switch 2 configuration.
SEL1	11	I	Logic control select pin 1. Table 8-2 provides controls switch 1 configuration.
S1A	12	I/O	Source pin A of switch 1. Can be an input or output.
S1B	13	I/O	Source pin B of switch 1. Can be an input or output.
D1	14	I/O	Drain pin (common) of switch 1. Can be an input or output.
D2	15	I/O	Drain pin (common) of switch 2. Can be an input or output.
V_{DD}	16	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between V_{DD} and GND.
Thermal pad		—	The thermal pad is not connected internally. It is recommended that the pad be left floating or tied to GND.

(1) I = input, O = output, I/O = input and output, P = power.
(2) For what to do with unused pins, refer to Section 8.3.4.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (3)

		MIN	MAX	UNIT
$V_{DD} - V_{SS}$	Supply voltage		28	V
V_{DD}		–0.5	28	V
V_{SS}		–28	0.5	V
V_{SEL} or V_{EN}	Logic control input pin voltage ($\overline{EN}$, Ax, SELx)	–0.5	28	V
I_{SEL} or I_{EN}	Logic control input pin current ($\overline{EN}$, Ax, SELx)	–0.5	28	mA
V_S or V_D	Source or drain voltage (Sx, D)	V_{SS}–0.5	V_{DD}+0.5	V
I_{IK}	Diode clamp current(2)	–30	30	mA
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)	–10	10	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(3) To avoid drawing excess current from V_{DD}, or into V_{SS}, the voltage drop across the bidirectional switch path (ΔV_{switch}) must not exceed 1.2V (600mV for high temperature).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Thermal Information: TMUX405x

THERMAL METRIC[1]		TMUX4051 / TMUX4052 / TMUX4053			UNIT
		PW (TSSOP)	DYY (SOT)	BQB (WQFN)	
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.5	138.9	70.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.2	70.3	67.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.0	69.1	40.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	6.4	5.1	3.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	62.1	69.0	40.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	18.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD} – V_{SS}$ [1]	Power supply voltage differential	5		24	V
V_{DD}	Positive power supply voltage	5		24	V
V_{SS}	Negative power supply voltage	–15		0	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	V_{SS}		V_{DD}	V
V_{Ax} or V_{EN}	Address or enable pin voltage	0		V_{DD}	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)	–10		10	mA
T_A	Ambient temperature	–55		125	°C

(1) V_{DD} and V_{SS} can be any value as long as $5V \le (V_{DD} – V_{SS}) \le 24V$, and the minimum V_{DD} and V_{SS} are met.

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6.5 Electrical Characteristics

Over operating free-air temperature range,
Typical at T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{DD}	V_{SS}	T_A	MIN	TYP	MAX	UNIT
POWER SUPPLY								
Supply current I_{DD}	Address inputs = 0V, 5V, or V_{DD} $\overline{EN}$ = 0V	5V	0V	–55°C			60	µA
				25°C		17	60	
				85°C			80	
				125°C			80	
	Address inputs = 0V, 5V, or V_{DD} $\overline{EN}$ = 0V	10V	0V	–55°C			60	
				25°C		18	60	
				85°C			80	
				125°C			80	
	Address inputs = 0V, 5V, or V_{DD} $\overline{EN}$ = 0V	24V	0V	–55°C			60	
				25°C		21	60	
				85°C			80	
				125°C			80	
	Address inputs = 0V, 5V, or V_{DD} $\overline{EN}$ = 0V	5V	–5V	–55°C			60	
				25°C		18	60	
				85°C			80	
				125°C			80	
	Address inputs = 0V, 5V, or V_{DD} $\overline{EN}$ = 0V	12V	–12V	–55°C			60	
				25°C		20	60	
				85°C			80	
				125°C			80	
Negative supply current I_{SS}	Address inputs = 0V, 5V, or V_{DD} $\overline{EN}$ = 0V	5V	–5V	–55°C			20	µA
				25°C		6	20	
				85°C			25	
				125°C			25	
	Address inputs = 0V, 5V, or V_{DD} $\overline{EN}$ = 0V	12V	–12V	–55°C			22	
				25°C		7	22	
				85°C			26	
				125°C			26	
I_{DD} disable	$\overline{EN}$ = 5V or V_{DD}	All		25°C		8		µA
				–55°C to 125°C			20	

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6.5 Electrical Characteristics (continued)

Over operating free-air temperature range,
Typical at T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{DD}	V_{SS}	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH								
R_{ON} Source to Drain ON-Resistance	V_S = V_{SS} to V_{DD}, I_D = –1mA	5V	0V	–55°C			800	Ω
				25°C		75	1050	
				85°C			1200	
				125°C			1300	
	V_S = V_{SS} to V_{DD}, I_D = –1mA	10V	0V	–55°C			310	
				25°C		60	400	
				85°C			520	
				125°C			550	
	V_S = V_{SS} to V_{DD}, I_D = –1mA	24V	0V	–55°C			200	
				25°C		60	240	
				85°C			300	
				125°C			300	
	V_S = V_{SS} to V_{DD}, I_D = –1mA	5V	–5V	–55°C			310	
				25°C		60	400	
				85°C			520	
				125°C			550	
	V_S = V_{SS} to V_{DD}, I_D = –1mA	12V	–12V	–55°C			200	
				25°C		60	240	
				85°C			300	
				125°C			300	
ΔR_{ON}	V_S = V_{SS} to V_{DD}, I_D = –1mA	All		25°C		2		Ω
$R_{ON\ FLAT}$	V_S = V_{SS} to V_{DD}, I_D = –1mA	All		25°C		60		Ω
				–55°C to 85°C			150	
				–55°C to 125°C			150	
$I_{S(OFF)}$ $I_{D(OFF)}$	Switch State is off V_S = V_{SS} / V_{DD} V_D = V_{DD} / V_{SS}	24V	0V	25°C		±0.3	±100	nA
				–55°C to 85°C			±200	
				–55°C to 125°C			±1000	
I_{ON}	Switch State is on V_S = V_D = V_{SS} or V_{DD}	24V	0V	25°C		±0.3	±100	nA
				–55°C to 85°C			±200	
				–55°C to 125°C			±1000	
LOGIC INPUTS (ADDRESS / ENABLE pins)								
V_{IH}	Input High Voltage	All		–55°C to 125°C	1.35		V_{DD}	V
V_{IL}	Input Low Voltage	All		–55°C to 125°C	0		0.8	V
I_{IH} I_{IL} Logic Input Current	V_{LOGIC} = 0V, 5V, or V_{DD}	All		25°C		±0.6		µA
				–55°C to 125°C	–1		1	
C_{IN}		All		25°C		2		pF

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6.6 AC Performance Characteristics

Typical at T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS				T_A = –55°C to 125°C			UNIT
	CONDITION	V_{DD}	V_{SS}	GPN	MIN	TYP	MAX	
CAPACITANCE								
$C_{S(OFF)}$	V_S = (V_{DD} + V_{SS}) / 2V f = 1MHz	5V	–5V	All		3		pF
		24V	0V			3		
$C_{D(OFF)}$	V_S = (V_{DD} + V_{SS}) / 2V f = 1MHz	5V	–5V	TMUX4051		11		pF
		24V	0V			9		
		5V	–5V	TMUX4052		6		
		24V	0V			5		
		5V	–5V	TMUX4053		4		
		24V	0V			3		
$C_{S(ON)}$ $C_{D(ON)}$	V_S = (V_{DD} + V_{SS}) / 2V f = 1MHz	5V	–5V	TMUX4051		13		pF
		24V	0V			11		
		5V	–5V	TMUX4052		8		
		24V	0V			7		
		5V	–5V	TMUX4053		10		
		24V	0V			5		
DYNAMIC CHARACTERISTICS								
Bandwidth (BW) (Sine Wave Input)	V_{BIAS} = (V_{DD} + V_{SS}) / 2 (1) V_S = 200mVpp R_L = 50Ω, C_L = 5pF	+5V	–5V	TMUX4051		280		MHz
		24V	0V			430		
		+5V	–5V	TMUX4052		600		
		24V	0V			700		
		+5V	–5V	TMUX4053		750		
		24V	0V			850		
Off Isolation Channel OFF (Sine Wave Input)	V_{BIAS} = (V_{DD} + V_{SS}) / 2 (1) V_S = 200mVpp R_L = 50Ω, C_L = 5pF f = 1MHz	+5V	–5V	All		–95		dB
		24V	0V			–95		
Crosstalk (Sine Wave Input)	V_{BIAS} = (V_{DD} + V_{SS}) / 2 (1) V_S = 200mVpp R_L = 50Ω, C_L = 5pF f = 1MHz	+5V	–5V	All		–90		dB
		24V	0V			–90		
Charge Injection	V_S = (V_{DD} + V_{SS}) / 2 R_S = 0Ω, C_L = 100pF	+5V	–5V	TMUX4051		6		pC
		24V	0V			2		

(1) Peak-to-Peak voltage symmetrical about (V_{DD} + V_{SS}) / 2.

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6.7 Timing Characteristics

Over operating free-air temperature range,
Typical at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
		CONDITION	V_{DD}	V_{SS}	T_A				
Prop Delay	Signal Input to Signal Output	V_S = V_{SS} to V_{DD}	5V	0V	25°C		4	20	ns
			10V	0V	25°C		4	20	
			24V	0V	25°C		3	20	
			5V	–5V	25°C		4	20	
			12V	–12V	25°C		3	20	
t_{TRAN}	Address-to-Signal OUT Transition time between inputs	t_r , t_f = 20ns, C_L = 50pF, R_L = 10kΩ	5V	0V	25°C		105		ns
					–55°C to +125°C			190	
			10V	0V	25°C		100		
					–55°C to +125°C			190	
			24V	0V	25°C		110		
					–55°C to +125°C			230	
			5V	–5V	25°C		100		
					–55°C to +125°C			190	
			12V	–12V	25°C		100		
					–55°C to +125°C			190	
$t_{ON (EN)}$	Enable-to-Signal OUT Channel turning ON	t_r , t_f = 20ns, C_L = 50pF, R_L = 10kΩ	5V	0V	25°C		100		ns
					–55°C to +125°C			190	
			10V	0V	25°C		95		
					–55°C to +125°C			190	
			24V	0V	25°C		110		
					–55°C to +125°C			230	
			5V	–5V	25°C		100		
					–55°C to +125°C			190	
			12V	–12V	25°C		100		
					–55°C to +125°C			190	
$t_{OFF (EN)}$	Enable-to-Signal OUT Channel turning OFF	t_r , t_f = 20ns, C_L = 50pF, R_L = 10kΩ	5V	0V	25°C		90		ns
					–55°C to +125°C			140	
			10V	0V	25°C		90		
					–55°C to +125°C			140	
			24V	0V	25°C		85		
					–55°C to +125°C			140	
			5V	–5V	25°C		100		
					–55°C to +125°C			160	
			12V	–12V	25°C		90		
					–55°C to +125°C			140	

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6.7 Timing Characteristics (continued)

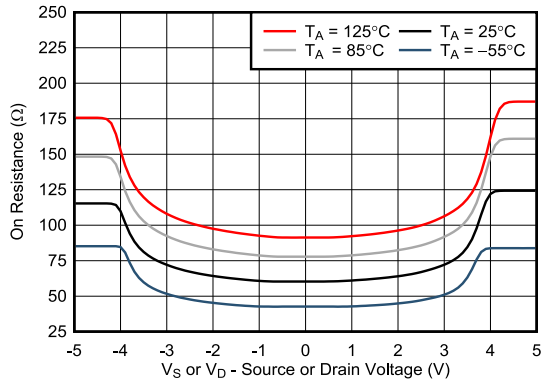
Over operating free-air temperature range,
Typical at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
		CONDITION	V_{DD}	V_{SS}	T_A				
t_{BBM}		C_L = 15pF, R_L = 10kΩ	5V	0V	25°C		60		ns
					–55°C to +125°C	1			
			10V	0V	25°C		45		
					–55°C to +125°C	1			
			5V	–5V	25°C		45		
					–55°C to +125°C	1			
			12V	–12V	25°C		55		
					–55°C to +125°C	1			
			24V	0V	25°C		75		
					–55°C to +125°C	1			

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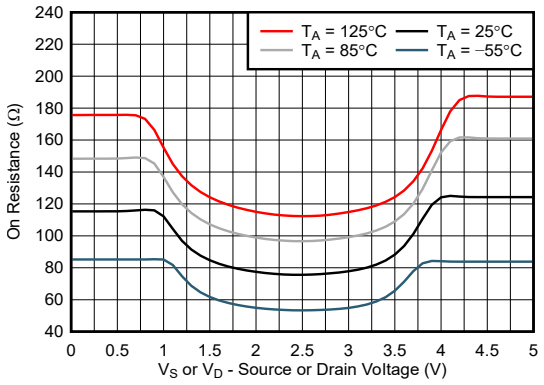
6.8 Typical Characteristics

at T_A = 25°C, V_{DD} = 5V (unless otherwise noted)



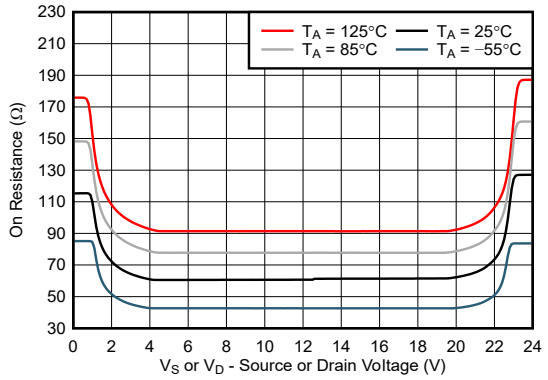
V_{DD} = 5V, V_{SS} = -5V

Figure 6-1. On-Resistance vs Temperature



V_{DD} = 5V

Figure 6-2. On-Resistance vs Temperature



V_{DD} = 24V

Figure 6-3. On-Resistance vs Temperature

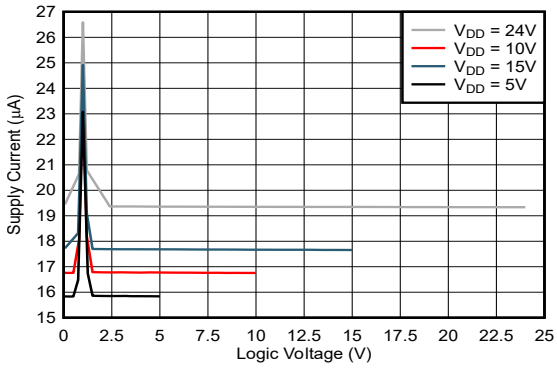
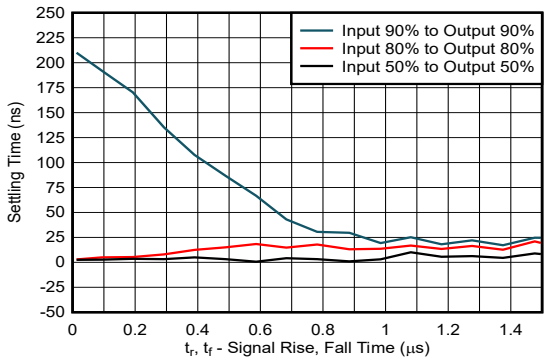


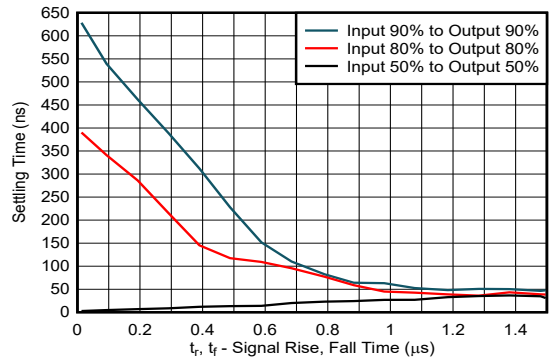
Figure 6-4. Supply Current vs Logic Voltage



V_{DD} = 5V, V_{signal} = 5V

R_L = 200kΩ, C_L = 15pF

Figure 6-5. System Settling Time



V_{DD} = 5V, V_{signal} = 5V

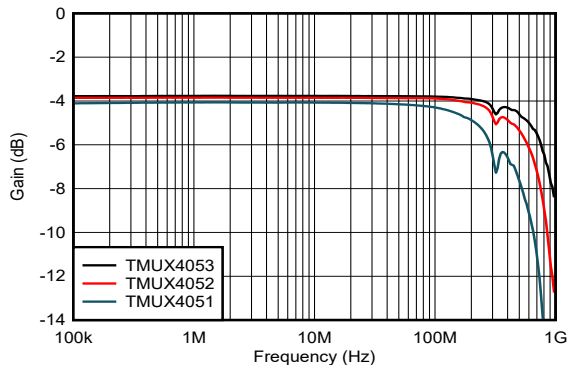
R_L = 10kΩ, C_L = 15pF

Figure 6-6. System Settling Time

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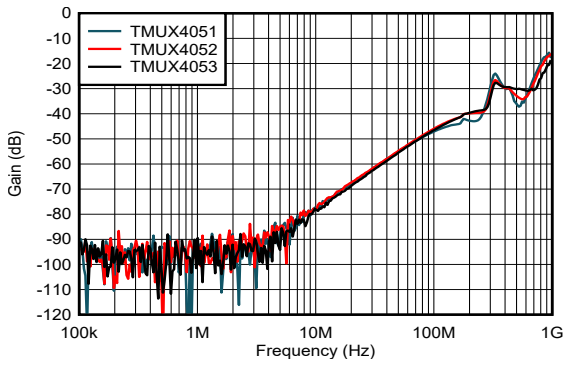
6.8 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5V (unless otherwise noted)



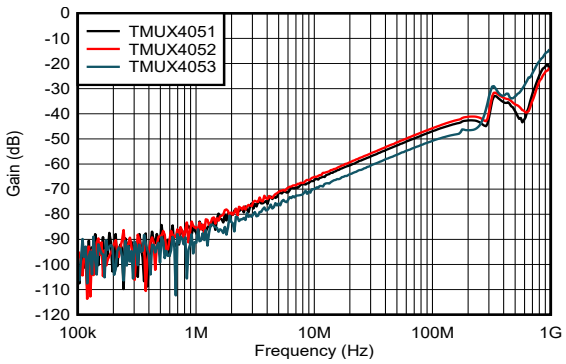
V_{DD} = 12V, V_{SS} = -12V

Figure 6-7. On Response vs Frequency



V_{DD} = 12V, V_{SS} = -12V

Figure 6-8. Off-Isolation vs Frequency



V_{DD} = 12V, V_{SS} = -12V

Figure 6-9. Xtalk vs Frequency

7 Parameter Measurement Information

7.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in the following figure. Figure 7-1 shows how the R_{ON} is computed with R_{ON} = V / I_{SD}, and the voltage (V) and current (I_{SD}) are measured using this setup.

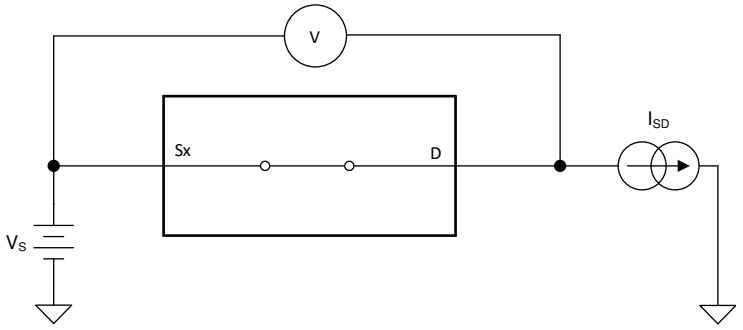


Figure 7-1. On-Resistance Measurement Setup

7.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current.
2. Drain off-leakage current.

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

Figure 7-2 shows the setup used to measure both off-leakage currents.

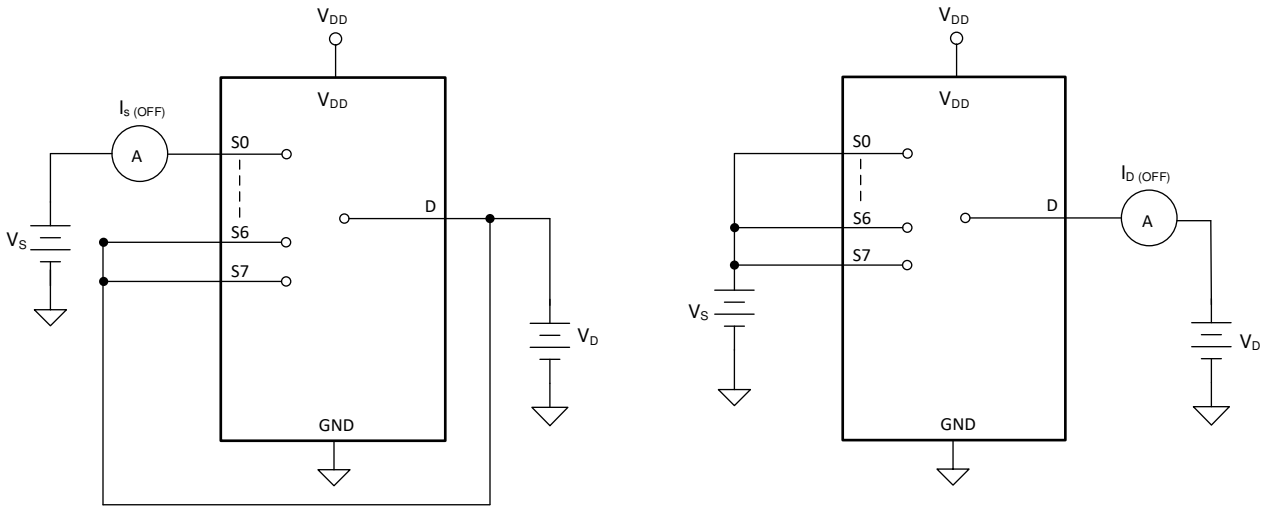


Figure 7-2. Off-Leakage Measurement Setup

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7.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 7-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

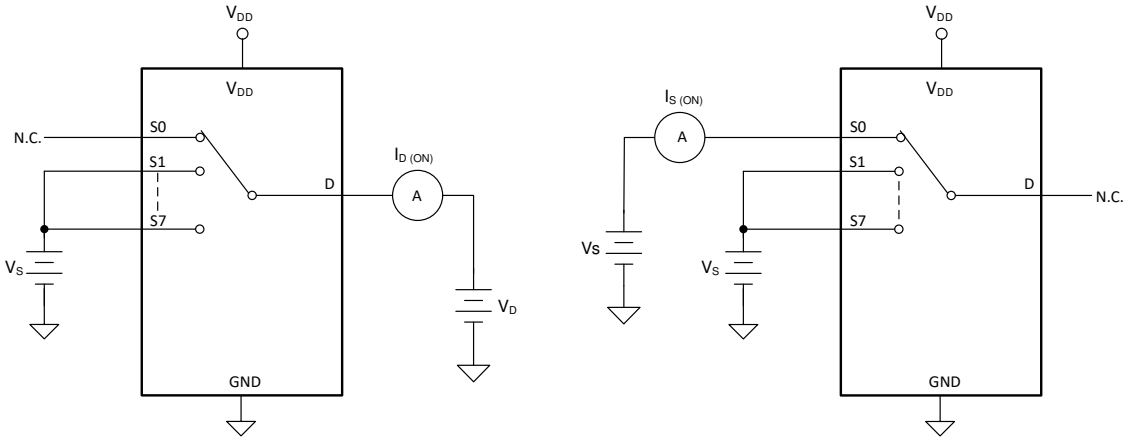


Figure 7-3. On-Leakage Measurement Setup

7.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the address signal has risen or fallen past the 50% threshold. Figure 7-4 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

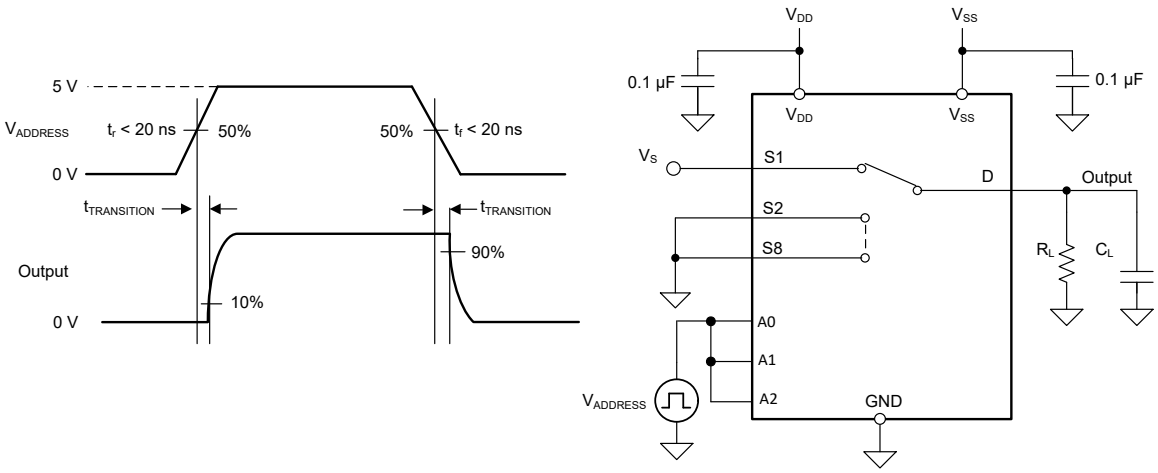


Figure 7-4. Transition-Time Measurement Setup

7.5 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 7-5 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

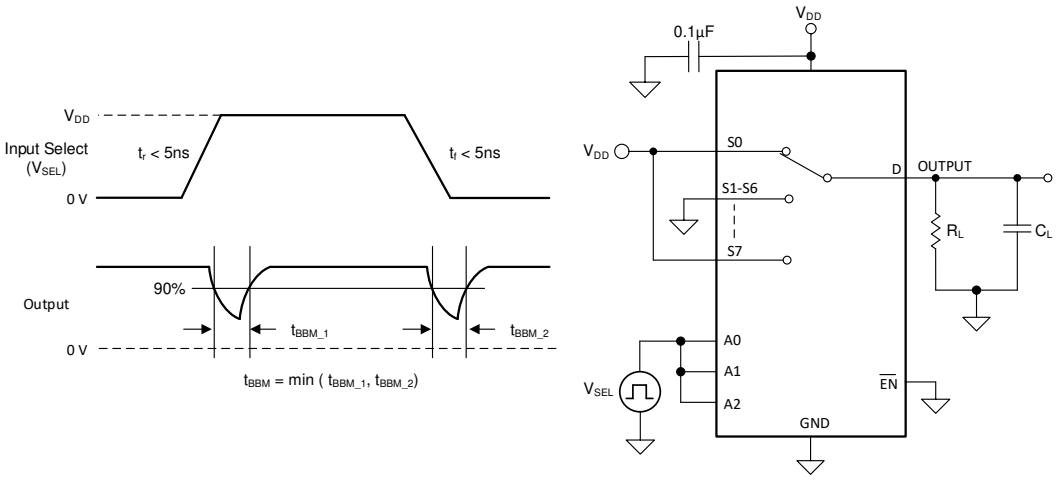


Figure 7-5. Break-Before-Make Delay Measurement Setup

7.6 $t_{ON(EN)}$ and $t_{OFF(EN)}$

Turn-on time is defined as the time taken by the output of the device to rise to 10% after the enable has risen past the 50% threshold. The 10% measurement is utilized to provide the timing of the device, system level timing can then account for the time constant added from the load resistance and load capacitance. Figure 7-6 shows the setup used to measure transition time, denoted by the symbol $t_{ON(EN)}$.

Turn-off time is defined as the time taken by the output of the device to fall to 90% after the enable has fallen past the 50% threshold. The 90% measurement is utilized to provide the timing of the device, system level timing can then account for the time constant added from the load resistance and load capacitance. Figure 7-6 shows the setup used to measure transition time, denoted by the symbol $t_{OFF(EN)}$.

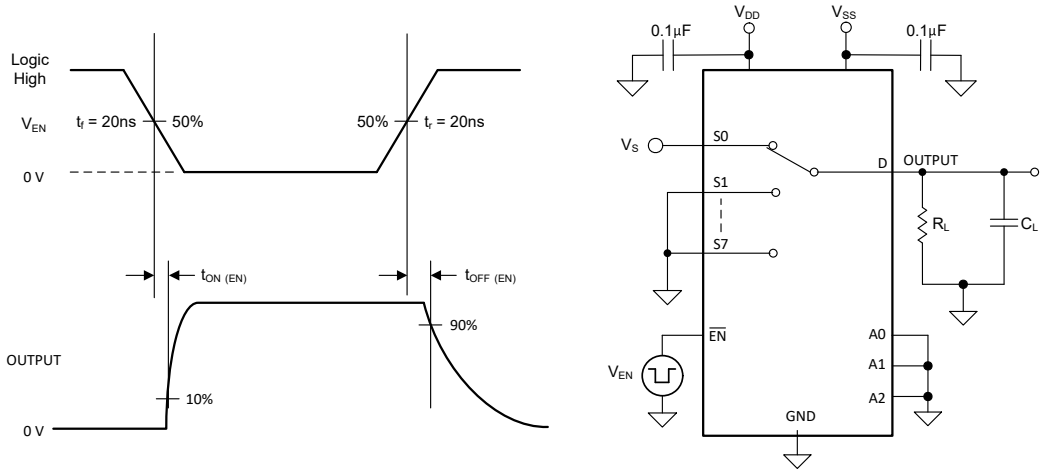


Figure 7-6. Turn-On and Turn-Off Time Measurement Setup

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7.7 Propagation Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold. Figure 7-7 shows the setup used to measure propagation delay, denoted by the symbol t_{PD}.

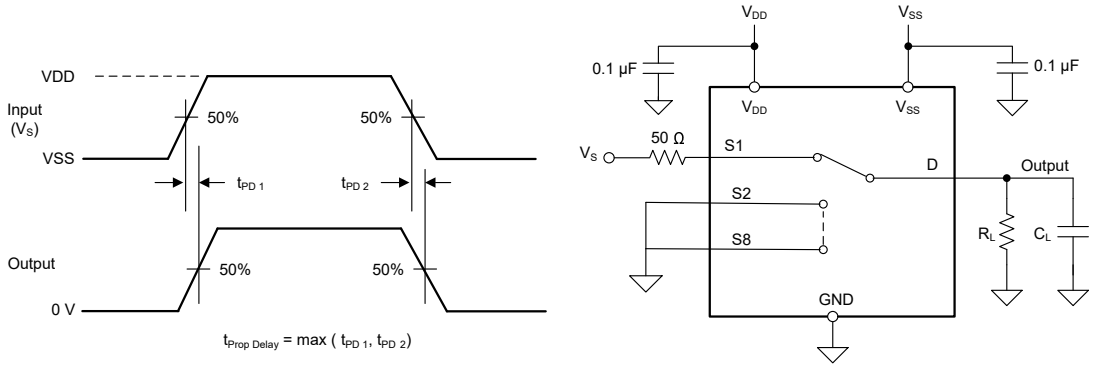


Figure 7-7. Propagation Delay Measurement Setup

7.8 Charge Injection

Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. Figure 7-8 shows the setup used to measure charge injection from source (Sx) to drain (D).

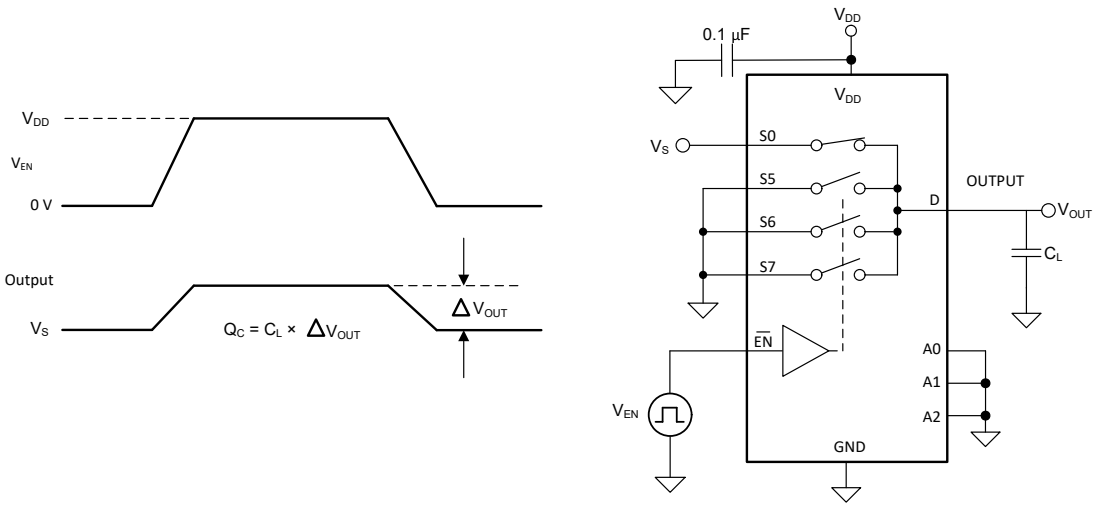


Figure 7-8. Charge-Injection Measurement Setup

7.9 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. Figure 7-9 shows the setup used to measure, and the equation to compute off isolation.

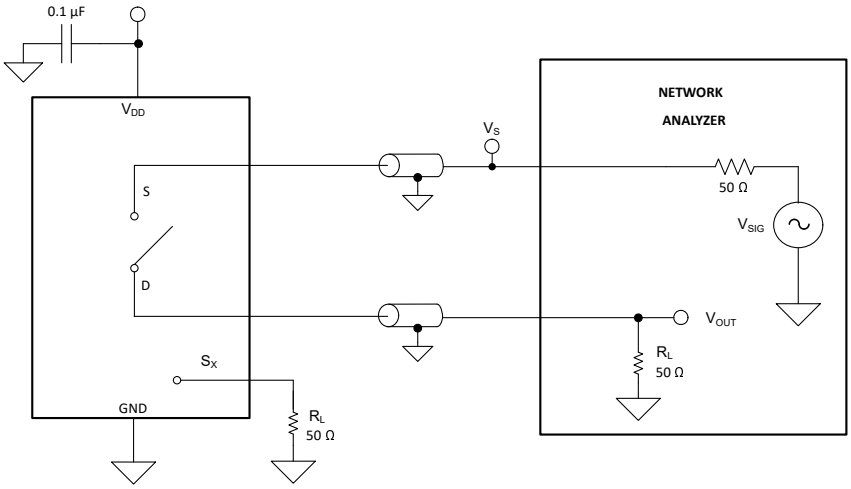


Figure 7-9. Off Isolation Measurement Setup

$$Off\ Isolation\ =\ 20\ \times\ Log\left(\frac{V_{OUT}}{V_S}\right) \quad (1)$$

7.10 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. Figure 7-10 shows the setup used to measure, and the equation used to compute crosstalk.

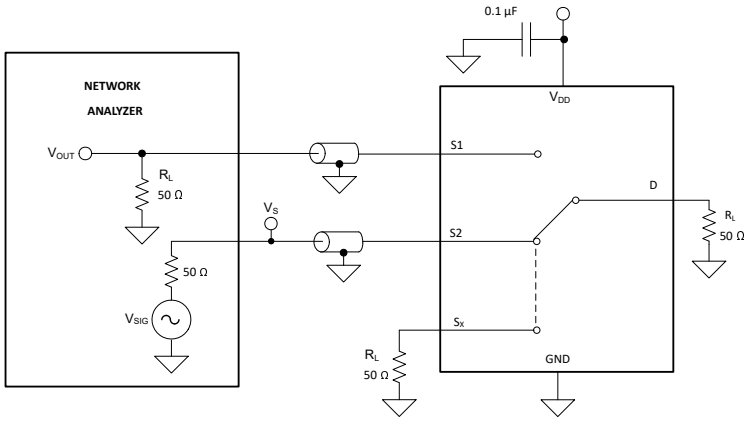


Figure 7-10. Channel-to-Channel Crosstalk Measurement Setup

$$Channel-to-Channel\ Crosstalk\ =\ 20\ \times\ Log\left(\frac{V_{OUT}}{V_S}\right) \quad (2)$$

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7.11 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. Figure 7-11 shows the setup used to measure bandwidth.

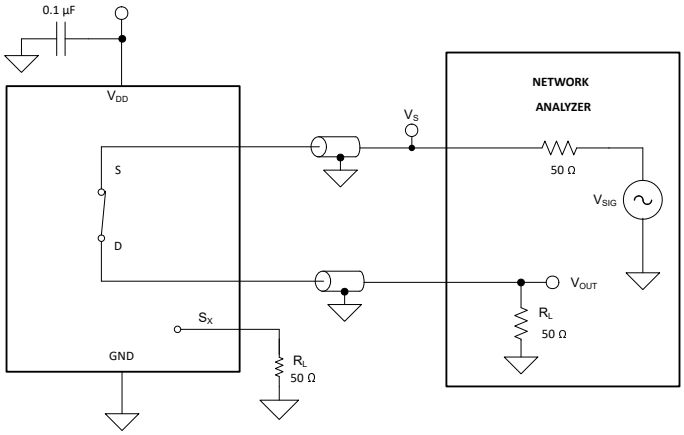


Figure 7-11. Bandwidth Measurement Setup

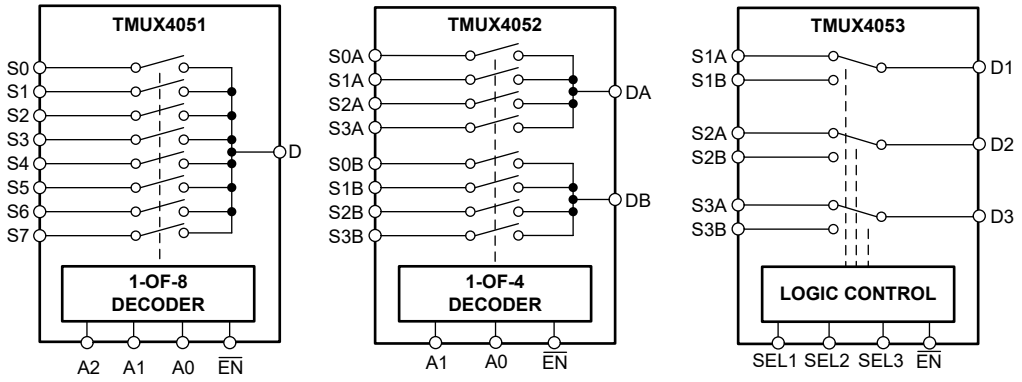
$$Attenuation = 20 \times Log\left(\frac{V_2}{V_1}\right) \quad (3)$$

8 Detailed Description

8.1 Overview

The TMUX4051 is an 8:1, single-ended (1-channel) mux, the TMUX4052 is a 4:1, differential (2-channel) multiplexer, and the TMUX4053 is 2:1, 3 channel switch. Each channel is turned on or turned off based on the state of the address lines and enable pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Bidirectional Operation

The TMUX4051, TMUX4052, and TMUX4053 devices conduct equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each signal path has very similar characteristics in both directions so they can be used as both multiplexers and demultiplexer to support analog signals.

8.3.2 Rail-to-Rail Operation

The valid signal path input and output voltage for the TMUX4051, TMUX4052, and TMUX4053 ranges from V_{SS} to V_{DD}.

8.3.3 1.8V Logic Compatible Inputs

The TMUX4051, TMUX4052, and TMUX4053 support 1.8V logic compatible control for all logic control inputs. 1.8V logic level inputs allows the multiplexers to interface with processors that have lower logic I/O rails and eliminates the need for an external voltage translator, which saves both space and BOM cost. For more information on 1.8V logic implementation, refer to Simplifying Design with 1.8V logic Muxes and Switches.

8.3.4 Device Functional Modes

When the $\overline{EN}$ pin of the TMUX405x devices is pulled low, one of the switches is closed based on the state of the address or select pins. When the $\overline{EN}$ pin is pulled high, all the switches are in an open state regardless of the state of the address or select pins.

Unused logic control pins must be tied to GND or V_{DD} to be certain that the device does not consume additional current as highlighted in Implications of Slow or Floating CMOS Inputs. Unused signal path inputs (Sx and Dx) should be connected to GND.

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8.3.5 Truth Tables

Table 8-1, Table 8-2, and Table 8-3 provides the truth tables for the TMUX4051 respectively.

Table 8-1. TMUX4051 Truth Table

$\overline{EN}$	A2	A1	A0	Selected Signal Path Connected To Drain (D) Pin
0	0	0	0	S0
0	0	0	1	S1
0	0	1	0	S2
0	0	1	1	S3
0	1	0	0	S4
0	1	0	1	S5
0	1	1	0	S6
0	1	1	1	S7
1	X(1)	X(1)	X(1)	All inputs are unselected (HI-Z)

(1) X denotes *do not care*.

Table 8-2. TMUX4052 Truth Table

$\overline{EN}$	A1	A0	Selected Signal Path Connected To Drain (DA and DB) Pins
0	0	0	S0A to DA S0B to DB
0	0	1	S1A to DA S1B to DB
0	1	0	S2A to DA S2B to DB
0	1	1	S3A to DA S3B to DB
1	X(1)	X(1)	All inputs are unselected (HI-Z)

(1) X denotes *do not care*.

Table 8-3. TMUX4053 Truth Table

$\overline{EN}$	SEL1	SEL2	SEL3	Selected Signal Path Connected To Drain Pins
0	0	X	X	S1A to D1
0	1	X	X	S1B to D1
0	X	0	X	S2A to D2
0	X	1	X	S2B to D2
0	X	X	0	S3A to D3
0	X	X	1	S3B to D3
1	X(1)	X(1)	X(1)	All inputs are unselected (HI-Z)

(1) X denotes *do not care*.

The Enable pin, $\overline{EN}$, of the TMUX405x devices have a weak internal pull-up resistor to put the devices into a disabled state upon power up. The SELx / Address pins (Ax) have weak internal pull-down resistors to put the switch into a defined logic state.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TMUX405x devices offer good system performance across a wide operating supply (5V to 24V). These devices include 1.8V logic compatible control input pins that enable operation in systems with 1.8V I/O rails. These features make the TMUX405x a family of general purpose multiplexers and switches that can reduce system complexity, board size, and overall system cost.

9.2 Typical Application

One useful application to take advantage of the TMUX405x features is multiplexing various signals into an ADC that is integrated into an MCU. Utilizing an integrated ADC in an MCU allows a system to minimize cost with a potential tradeoff of system performance when compared to an external ADC. The multiplexer allows for multiple inputs or sensors to be monitored with a single ADC pin of the device, which is critical in systems with limited I/O. The TMUX4052 is suitable for a similar design example using differential signals, or as two 4:1 multiplexers.

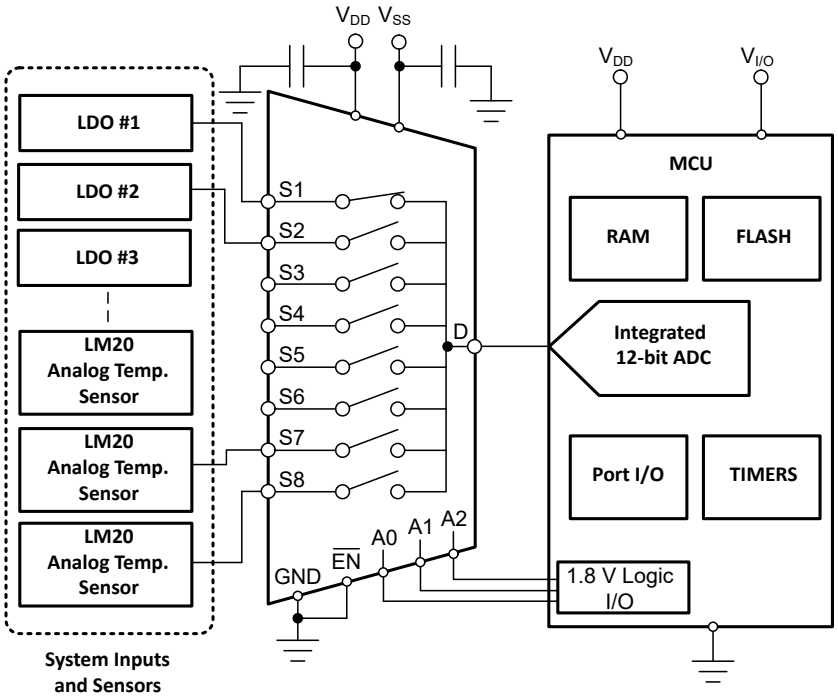


Figure 9-1. Multiplexing Signals to an Integrated ADC with TMUX4051

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9.3 Design Requirements

Table 9-1 lists the parameters that must be used for this design example.

Table 9-1. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	12V
I/O signal range	0V to V_{DD} (rail-to-rail)
Control logic thresholds	1.8V compatible

9.4 Detailed Design Procedure

The TMUX4051, TMUX4052, and TMUX4053 can operate without any external components except for the supply decoupling capacitors. The MCU can control the enable and address pins through GPIOs to toggle between various inputs of the multiplexer. The enable pin should be connected to ground if the functionality is not required in the system. All inputs being muxed to the ADC of the MCU must fall within the *Recommended Operating Conditions*, including signal range and continuous current. For this design with a supply of 12V, the signal range can be 0V to 12V.

9.5 Application Curves

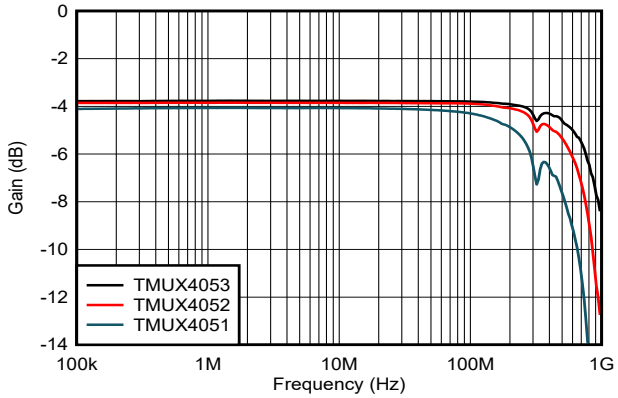


Figure 9-2. Bandwidth

9.6 Power Supply Recommendations

The TMUX4051, TMUX4052, and TMUX4053 devices operate across a wide supply range of 5V to 24V.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply pins to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1µF to 10µF from V_{DD} to ground and V_{SS} to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems or systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

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9.7 Layout

9.7.1 Layout Guidelines

Route high-speed signals using minimal vias and corners, which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Figure 9-3 shows an example of a PCB layout with the TMUX4051, TMUX4052, and TMUX4053. Some key considerations are as follows:

- Decouple the V_{DD} and V_{SS} pins with a 0.1µF capacitor, placed as close to the pin as possible. Ensure that the capacitor voltage rating is sufficient.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

9.7.2 Layout Example

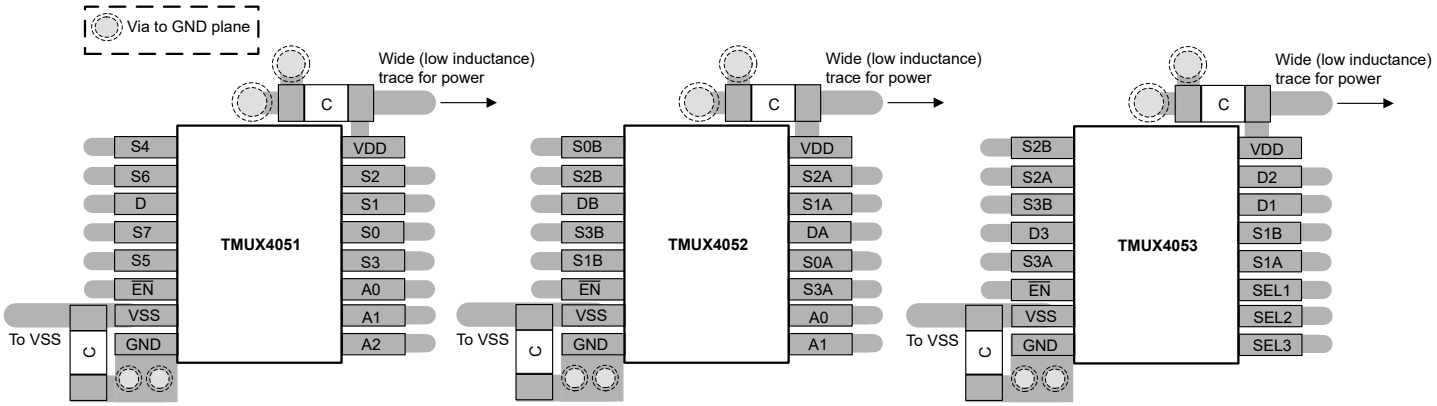


Figure 9-3. TMUX4051, TMUX4052, and TMUX4053 Layout Example

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10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Simplifying Design with 1.8V logic Muxes and Switches* application brief
- Texas Instruments, *QFN/SON PCB Attachment* application report
- Texas Instruments, *Quad Flatpack No-Lead Logic Packages* application report

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

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10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (July 2024) to Revision E (September 2024)	Page
• Added TMUX4052 and TMUX4053 pin drawings	4

Changes from Revision C (July 2024) to Revision D (July 2024)	Page
• Added back Figure 6-7, Figure 6-8, Figure 6-9	14
• Added back Figure 9-2	25

Changes from Revision B (March 2023) to Revision C (July 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated Is(off) or Id(off) values	9
• Updated Ion values	9
• Added the Typical Characteristics	14

Changes from Revision A (September 2022) to Revision B (March 2023)	Page
• Changed the status DYY and BQB packages from: *preview* to: *active*	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX4051BQBR	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T4051
TMUX4051DYYR	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T4051
TMUX4051PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T4051
TMUX4052BQBR	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T4052
TMUX4052DYYR	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T4052
TMUX4052PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T4052
TMUX4053BQBR	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T4053
TMUX4053DYYR	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T4053
TMUX4053PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T4053

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TMUX4051, TMUX4052 :

- Automotive : TMUX4051-Q1, TMUX4052-Q1

NOTE: Qualified Version Definitions:

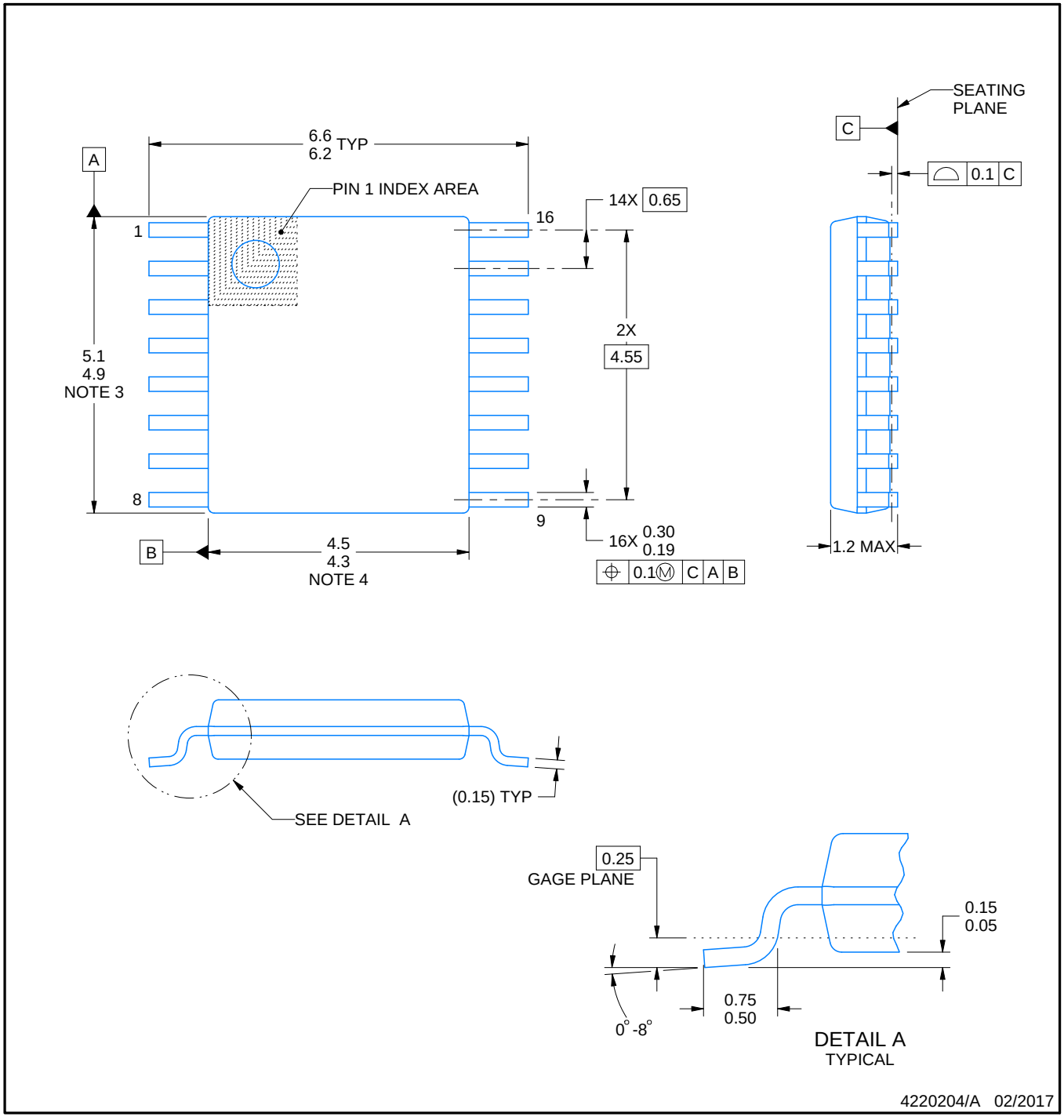
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE OUTLINE

PW0016A

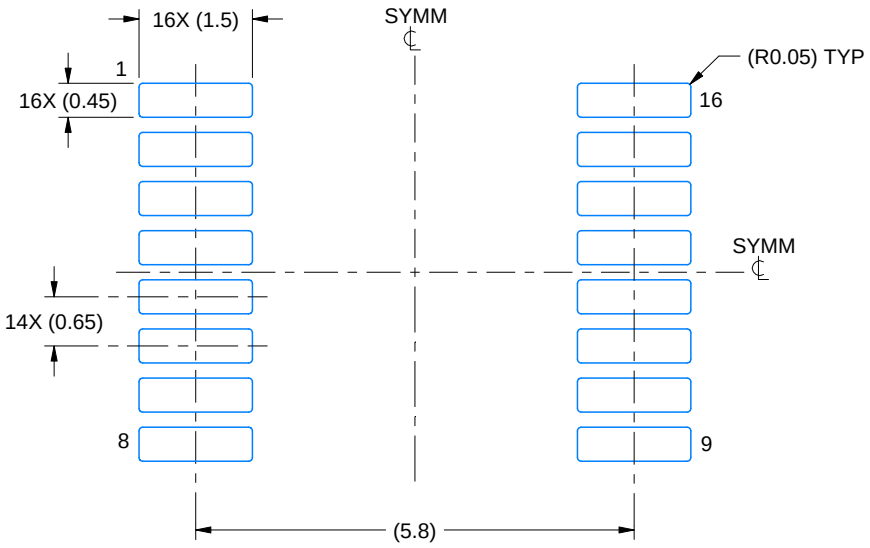
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

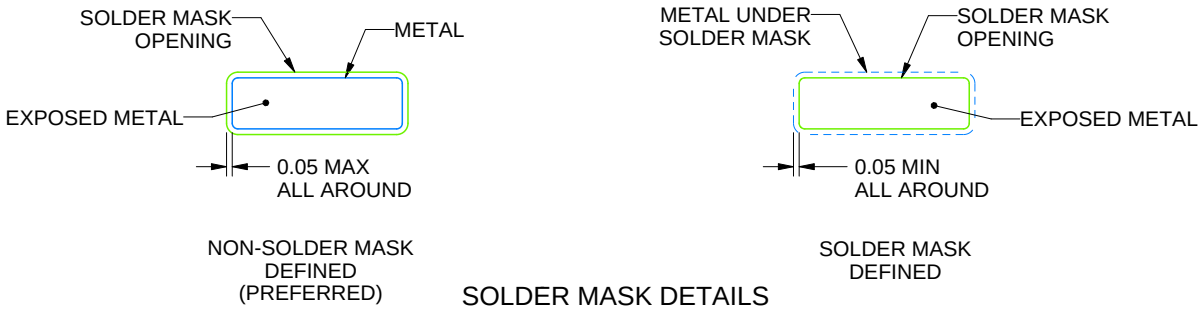


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

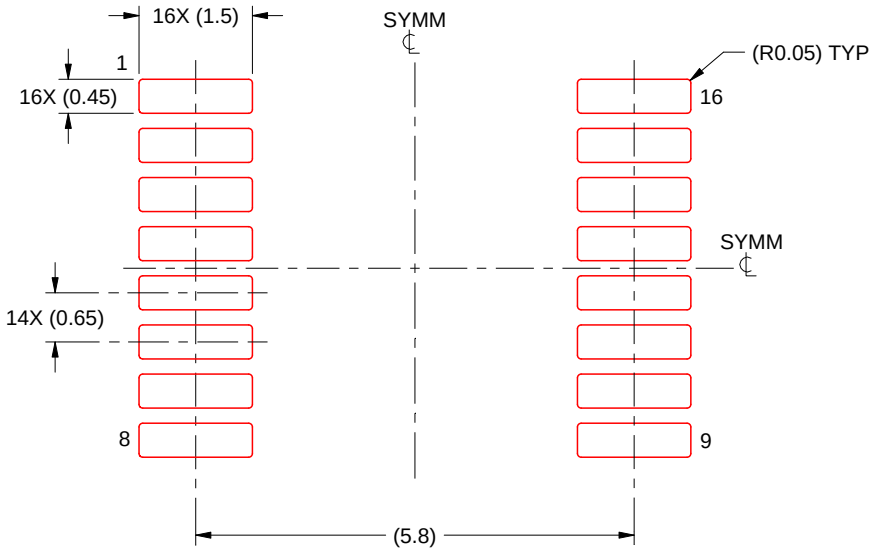


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

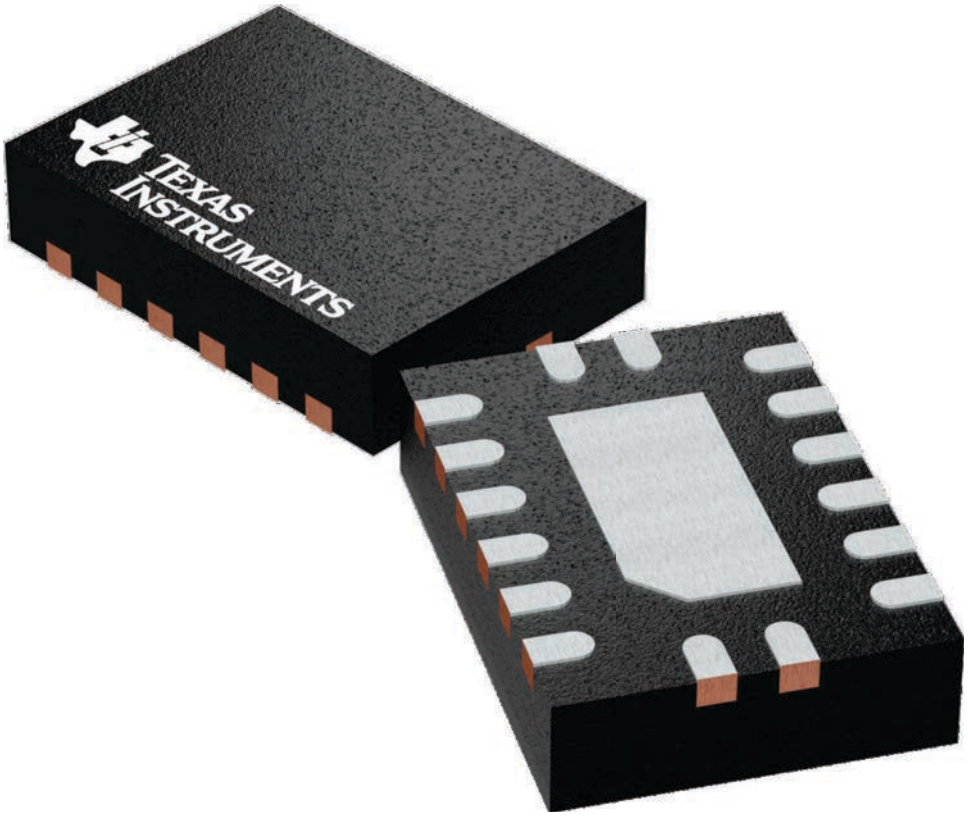
BQB 16

WQFN - 0.8 mm max height

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



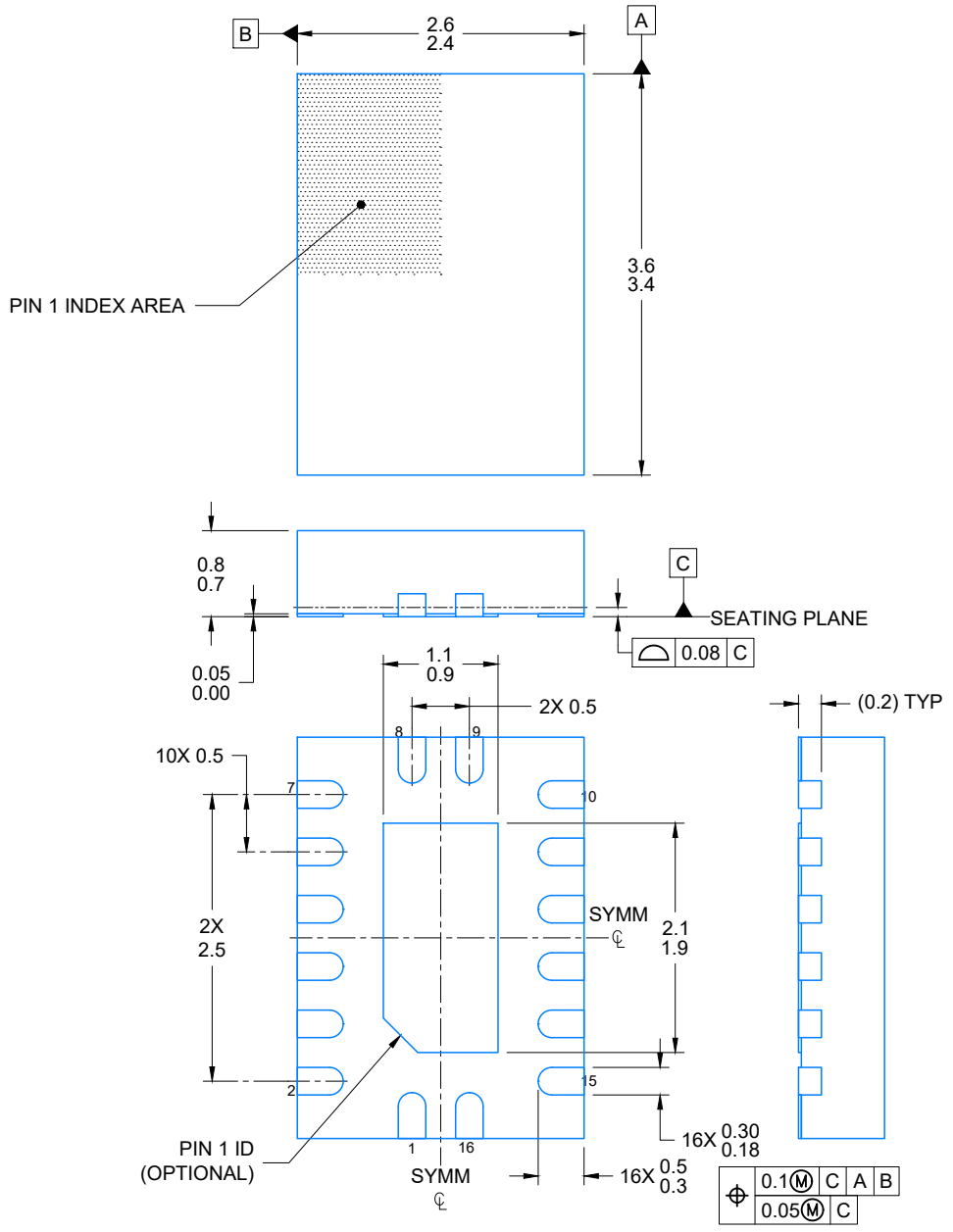
4226161/A

PACKAGE OUTLINE

BQB0016A

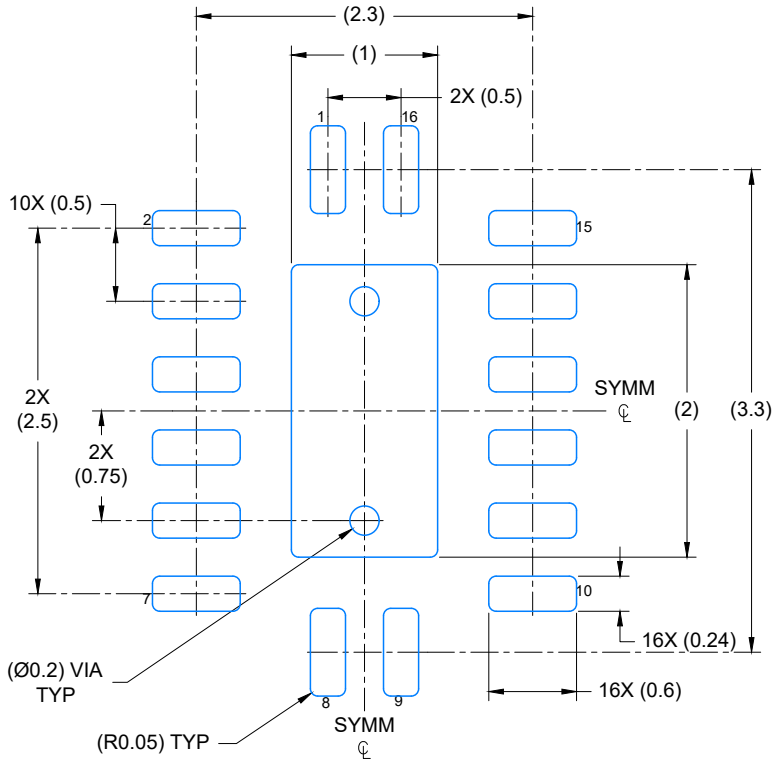
WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

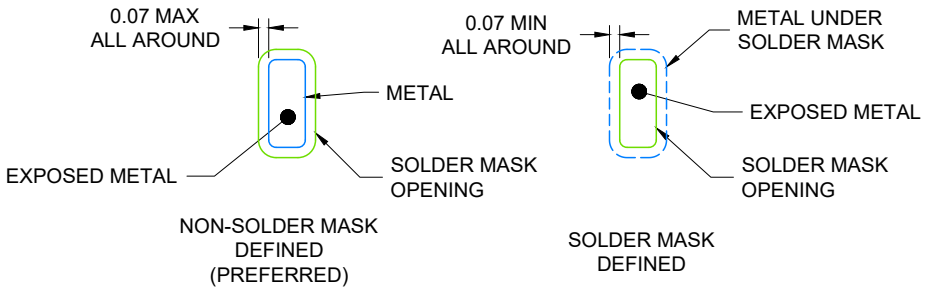


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



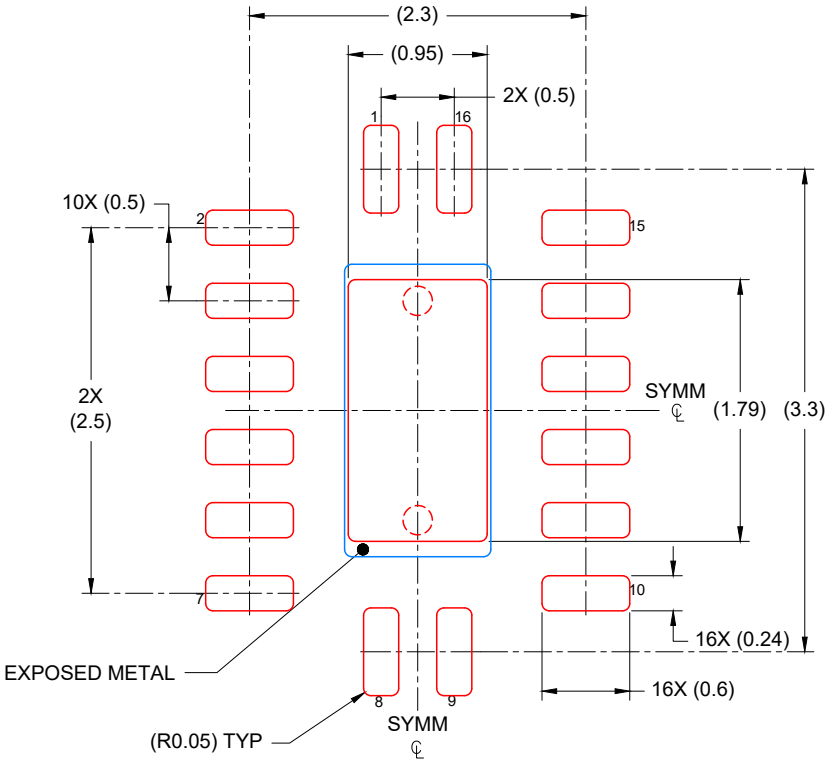
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224640/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4224640/A 11/2018

NOTES: (continued)

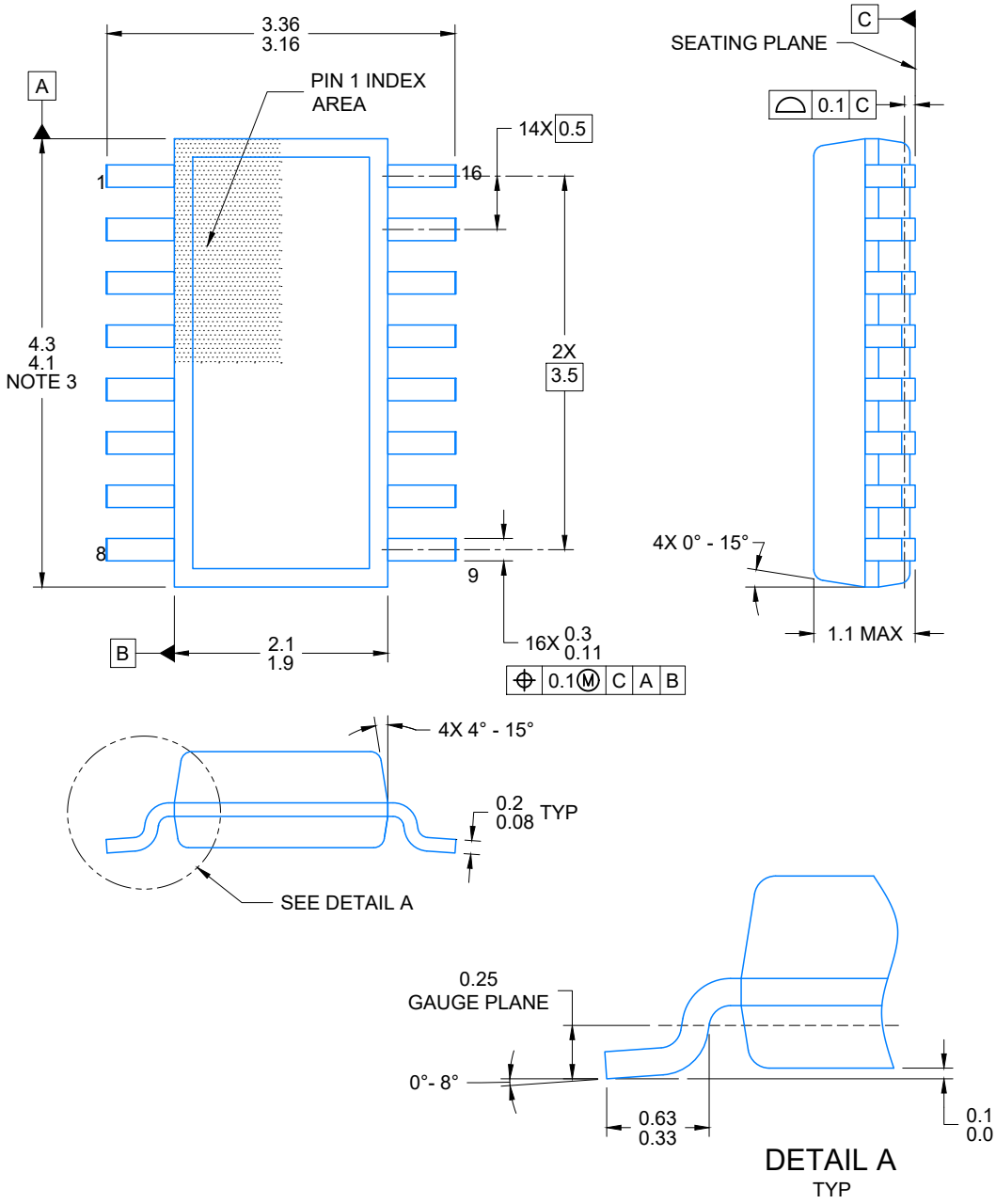
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DYY0016A

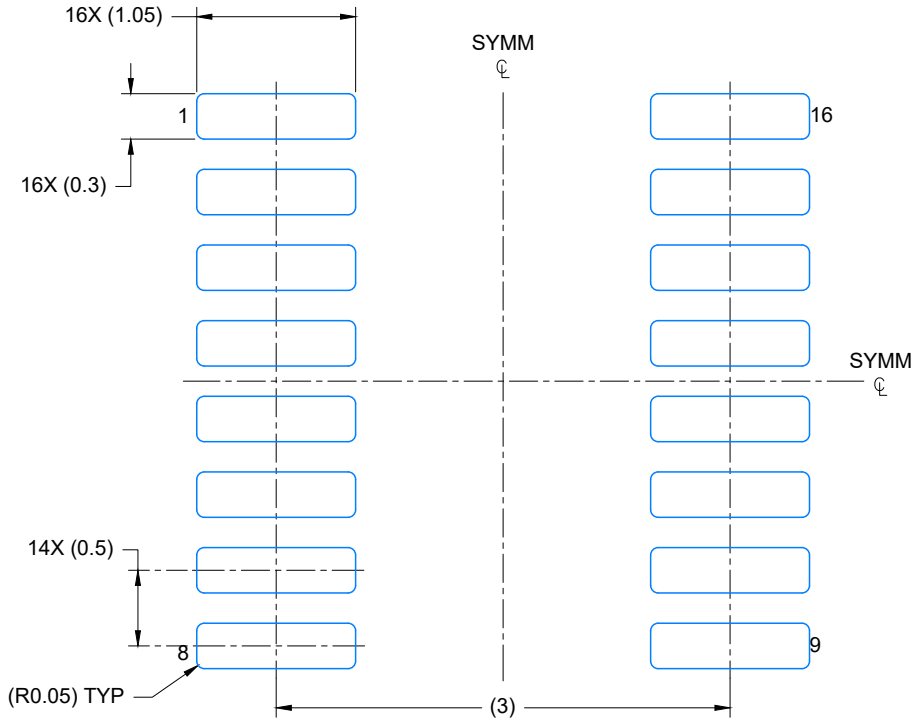
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

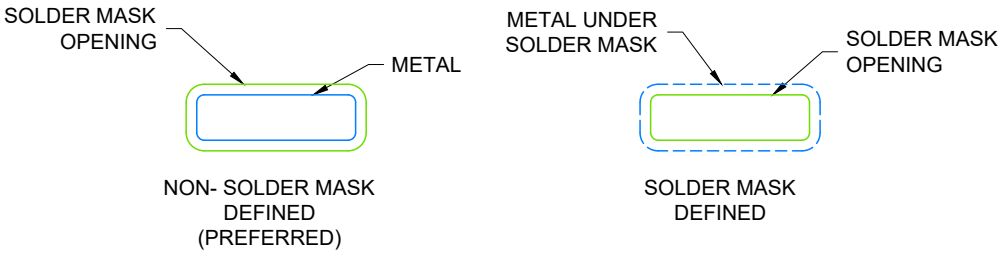


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224642/D 07/2024

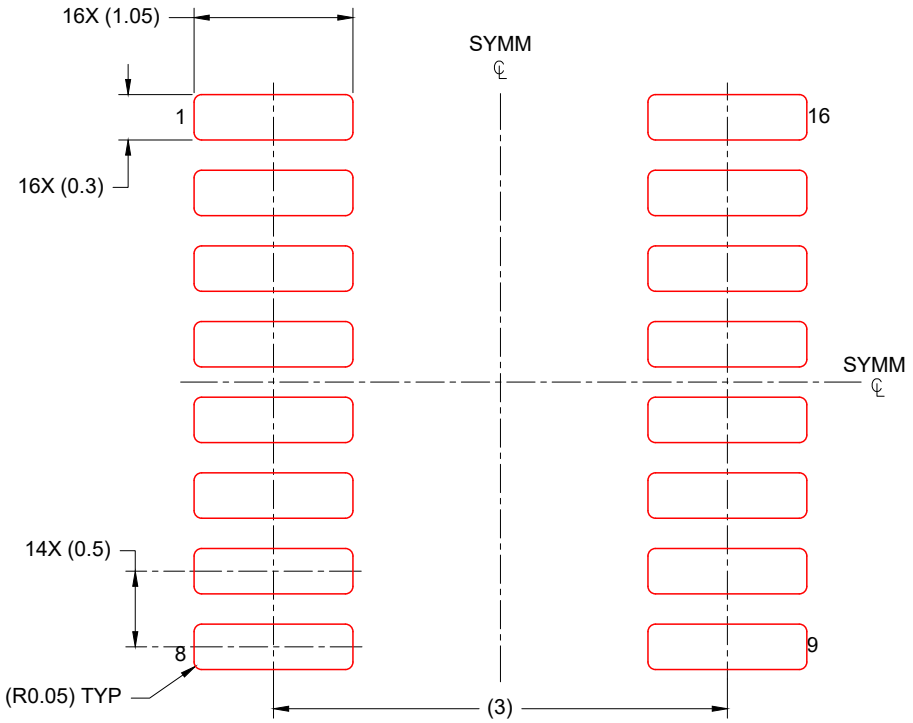
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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