

800-KSPS, ULTRA LOW POWER, 8-BIT, MINIATURE SAR ANALOG-TO-DIGITAL CONVERTER

FEATURES

- Fast Throughput Rate:
800 KSPS for XC7888
- Single 4V to 5.25V Supply Operation for
XC7888
- Zero Latency
- $\pm 0.5\text{LSB INL}, \pm 0.5\text{LSB DNL}$
- 16MHz Serial Interface
- Variable Power Management
- Low Power (XC7888 typical):
2.80mW (4V, 800KSPS)
4.90mW (5V, 800KSPS)
- Second-Source for ADS7888
- 6-Pin SOT-23 Package

APPLICATIONS

- Base Band Converters in
Radio Communication
- Optical Networking
- Optical Sensors
- Medical Instrumentations
- Battery-Powered Systems
- High-speed Closed-Loop
Systems
- High-Speed Data Acquisition
Systems

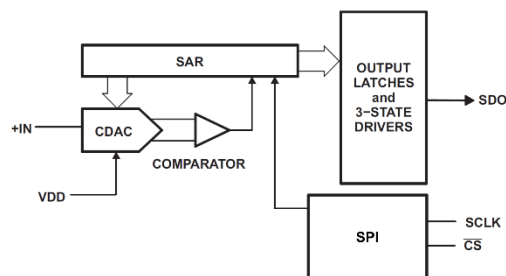
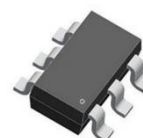


Figure 1. Functional Block Diagram

DESCRIPTION

The XC7888 is an 8-bit, high speed, low power, and small-sized Successive-Approximation-Register (SAR) ADC. This device can operate from a single 4 V to 5.25 V supply with an 800 KSPS throughput.

The XC7888 is available in a 6-pin SOT-23 package and has an operating temperature range of -40°C to 85°C.

The XC7888 is a drop-in replacement for the ADS7888 and consumes only half dynamic power of their counterpart.

SPECIFICATIONS

At -40°C to 85°C, $f_{\text{SAMPLE}} = 800$ KSPS and $f_{\text{SCLK}} = 16$ MHz if $4\text{ V} \leq V_{\text{DD}} \leq 5.25\text{ V}$. (unless otherwise noted)

PARAMETER	TEST CONDITIONS	XC7886			XC7887			XC7888			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SYSTEM PERFORMANCE											
Resolution		12			10			8			Bits
No missing codes		12			10			8			Bits
Integral linearity		-1.5		1.5	-1		1	-0.5		0.5	LSB
Differential linearity		-1.25		1.25	-0.75		0.75	-0.5		0.5	LSB
fsAMPLE Throughput rate	fSCLK = 16 MHz, 4 V ≤ VDD ≤ 5.25 V	800			800			800			KSPS
SNR	fIN = 100 kHz	72.5			61.5			49.5			dB
THD	fIN = 100 kHz	-84.5			-74.5			-68.5			dB

XC7888

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
I _{DD} Supply current, normal operation	Digital inputs = 0 V or V _{DD}	f _{SAMPLE} = 800 KSPS, f _{SCLK} = 16 MHz, V _{DD} = 4 V	0.70		0.82	mA
		f _{SAMPLE} =800 KSPS, f _{SCLK} = 16 MHz, V _{DD} = 5 V	0.98		1.10	
		f _{SAMPLE} = 500 KSPS, f _{SCLK} = 10 MHz, V _{DD} = 4 V	0.40		0.48	
		f _{SAMPLE} = 500 KSPS, f _{SCLK} = 10 MHz, V _{DD} = 5 V	0.70		0.80	
POWER DISSIPATION, XC7888						
Normal operation		f _{SAMPLE} = 800 KSPS, f _{SCLK} = 16 MHz, V _{DD} = 4 V	2.80		3.30	mW
		f _{SAMPLE} = 800 KSPS, f _{SCLK} = 16 MHz, V _{DD} = 5 V	4.90		5.50	mW

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

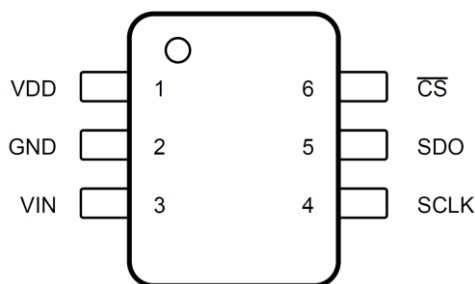


Figure 2. Pin Configuration

TERMINAL		DESCRIPTION
NAME	NO.	
VDD	1	Power supply input also acts like a reference voltage to ADC.
GND	2	Ground for power supply, all analog and digital signals are referred with respect to this pin.
VIN	3	Analog signal input. This signal can range from 0 V to VDD.
SCLK	4	Digital clock input. This clock directly controls the conversion and readout processes.
SDO	5	Digital data output. The output samples are clocked out of this pin on falling edges of the SCLK pin.
CS	6	Chip Select. On the falling edge of CS, a conversion process begins.

TYPICAL CONNECTION

Figure 3 shows a typical connection diagram for the XC7888. The 5 V supply should come from a stable power supply such as an LDO. The supply to XC7888 should be decoupled to the ground. A 1-μF and a 10-nF decoupling capacitor are required between the VDD and GND pins of the converter. This capacitor should be placed as close as possible to the pins of the device. Always set the VDD supply to be greater than or equal to the maximum input signal to avoid saturation of codes.

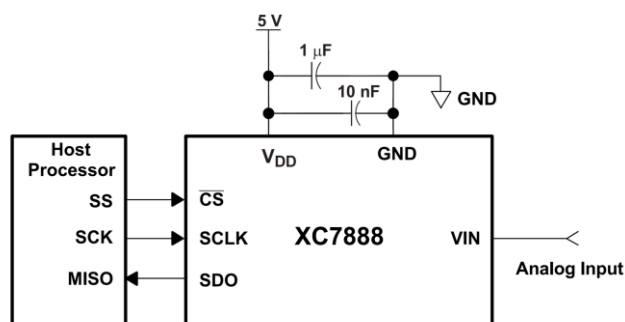


Figure 3. Typical Circuit Configuration

TIMING DIAGRAM

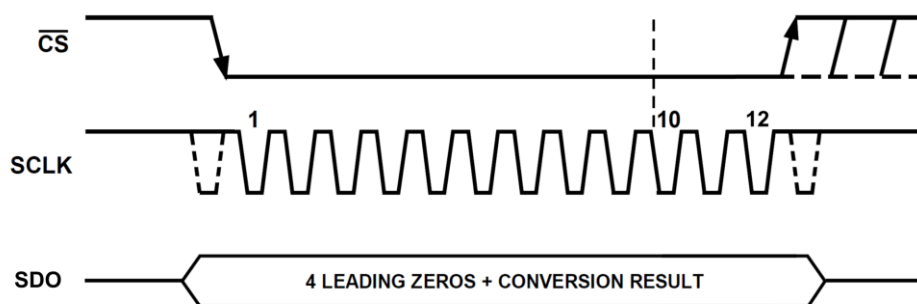


Figure 4. Timing Diagram

The conversion is initiated on the falling edge of \overline{CS} . The device outputs data while the conversion is in progress, and it requires 12 serial clock cycles to complete the conversion and access the full results. The XC7888 data word contains 4 leading zeros, followed by 8-bit data in MSB first format.

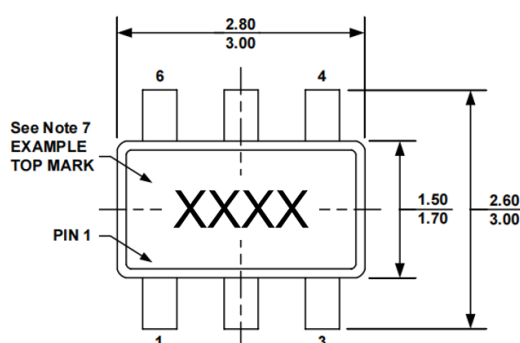
Once a data transfer is complete, SDO will return to the tri-state mode, and another conversion can be initiated after the quiet time has elapsed by again bringing \overline{CS} low.

POWER-DOWN MODE

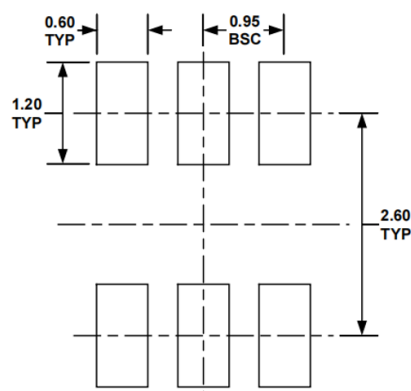
The XC7888 has an auto power-down feature. Besides powering down all circuitry, the converter consumes only a small amount of current in this mode. The device automatically wakes up when \overline{CS} falls. However, not all of the functional blocks are fully powered until sometime before the third falling edge of SCLK. The device powers down once it reaches the end of conversion which is the 12th falling edge of SCLK for the XC7888. The device enters power down mode if \overline{CS} goes high before the 10th SCLK falling edge. Ongoing conversion stops and SDO goes to three-state under this power down condition.

These converters achieve lower power dissipation for a fixed throughput rate by using higher SCLK frequencies. Higher SCLK frequencies reduce the acquisition time and conversion time. This means the converters spend more time in auto power-down mode per conversion cycle. For a particular SCLK frequency, the acquisition time and conversion time are fixed. Therefore, a lower throughput increases the proportion of the time the converters are in power down, thereby reducing power consumption.

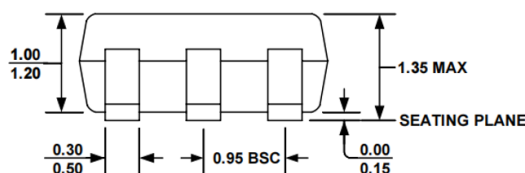
OUTLINE DIMENSIONS



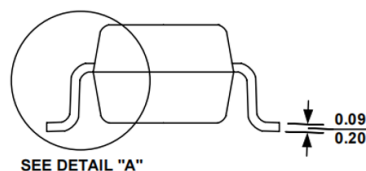
TOP VIEW



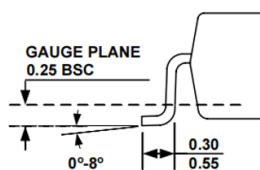
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) DRAWING CONFORMS TO JEDEC MO-178, VARIATION AB.
- 6) DRAWING IS NOT TO SCALE.
- 7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

NOTES

1. Unpacked ICs, tube-mounted ICs, etc. must be stored in a drying cabinet, and the humidity in the drying cabinet < 20% R.H.
2. After access, the components are stored in an electrostatic packaging protective bag.
3. Anti-static damage: the device is an electrostatic sensitive device, and sufficient anti-static measures should be taken during transmission, assembly and testing.
4. The user should conduct a visual inspection before use, and the bottom, side and surrounding of the circuit can be welded only if it is bright. If oxidation occurs, the circuit can be processed by means of oxidation, and the circuit must be soldered within 12 hours after processing.