BROADCOM®

Data Sheet

APDS-9306-A65

Miniature Surface-Mount Digital Ambient Light Sensor

Description

The Broadcom® APDS-9306-A65 is a low-voltage digital ambient light sensor that converts light intensity to digital signal output with I^2C interface. It consists of photodiode, ADC, oscillator and power-on reset to ensure consistent start-up. ADCs convert the photodiode currents to a digital output and the device is capable of rejecting 50-Hz and 60-Hz flicker caused by artificial light sources.

The APDS-9306-A65 approximates the response of the human eye to provide direct read out where the output count is proportional to ambient light level. Low-light functionality enables operation behind darkened glass. The APDS-9306-A65 supports programmable hardware interrupt with hysteresis to respond to events.

The APDS-9306-A65 has been re-engineered from the previous generation to provide higher ALS gain and improved dynamic range.

Applications

- Cell phone touch-screen disable
- Detection of ambient light to control display backlighting under OLED/LED/LCD
- Mobile devices: cell phone, PDAs
- Wearable devices: smart watch
- Computing devices: notebook, tablet PC
- Consumer devices: OLED/LED monitor and TV, digital still camera

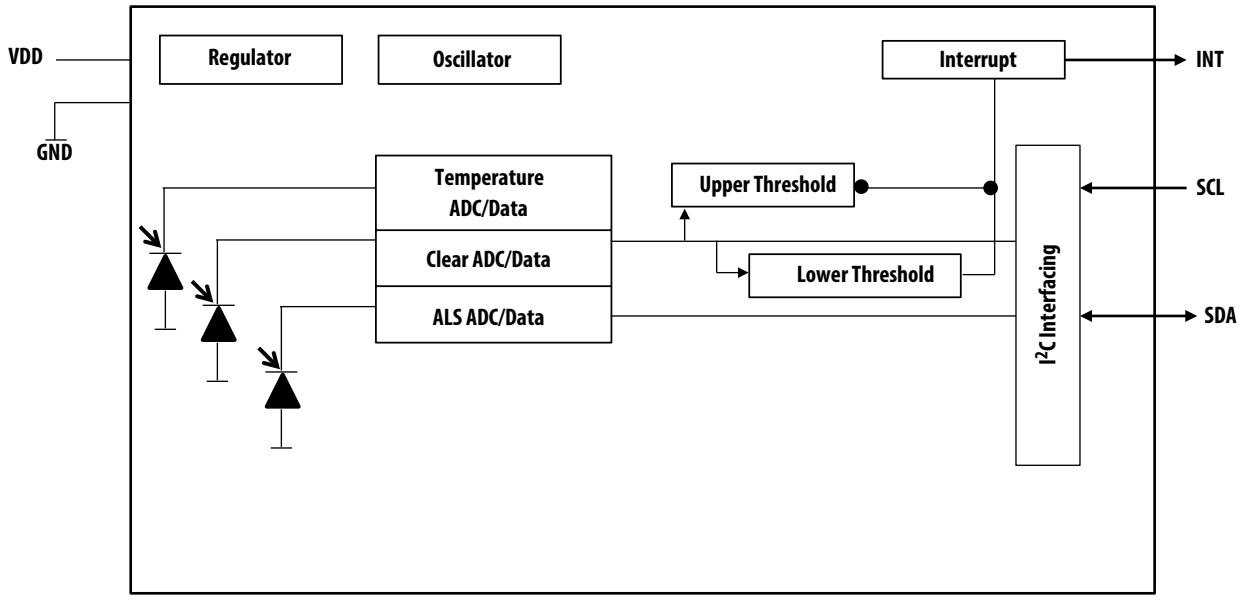
Features

- Ambient light sensing (ALS)
  - Light output proportional to light intensity
  - Uses optical coating technology to emulate human eye spectral response
  - Works well under different light source conditions
  - Low-light sensitivity; operates behind darkened glass
  - Wide dynamic range 54,000,000:1
  - Low lux performance
  - Fluorescent light flicker immunity
  - 50-Hz/60-Hz light flicker immunity
  - Programmable interrupt function with upper, lower thresholds and persists function
  - Programmable ALS integration time
  - Programmable ALS gain setting
  - Up to 20-bit resolution
- Supply voltage 1.7V to 3.6V
- Power management
  - Low active current
  - Low standby current
- I^2C interface compatible
  - Up to 400 kHz (I_2C fast-mode)
- Package dimension
  - L 2.00 mm × W 2.00 mm × H 0.65mm

Ordering Information

Part Number	Packaging	Quantity
APDS-9306-A65	Tape and Reel	2,500

Functional Block Diagram



I/O Pins Configuration

Pin	Name	Type	Description
1	SCL	I	I^2C serial clock input terminal. Clock signal for I^2C serial data
2	SDA	I/O	Serial data I/O for I^2C
3	VDD	Supply	Power supply voltage
4	INT	O	Interrupt. Open drain
5	NC		No Connect
6	GND	Ground	Power supply ground. All voltages are referenced to GND

Absolute Maximum Ratings

Over operating free-air temperature range (see note).

Parameter	Symbol	Min.	Max.	Units	Conditions
Power Supply Voltage[a]	V_{DD}	—	3.8	V	
Digital Voltage Range		–0.5	3.8	V	
Storage Temperature Range	Tstg	–45	85	°C	

a. All voltages are with respect to GND.

NOTE: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Ambient Temperature	T_A	–40	—	85	°C
Supply Voltage	V_{DD}	1.7	—	3.6	V
Supply Voltage Accuracy, V_{DD} total error including transients		–3	—	3	%

Operating Characteristics

V_{DD} = 2.8V, T_A = 25°C (unless otherwise noted).

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
SCL, SDA Input High Voltage	V_{IH}	1.5	—	V_{DD}	V	
SCL, SDA Input Low Voltage	V_{IL}	0	—	0.4	V	
INT, SDA Output Low Voltage	V_{OL}	0	—	0.4	V	
Leakage Current, SDA, SCL, INT Pins	I_{LEAK}	–5	—	5	µA	

ALS Characteristics

V_{DD} = 2.8V, T_A = 25°C (unless otherwise noted)

arameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Supply Current	I_{DD}	—	50	70	µA	Active mode
		—	1	2	µA	Standby mode
Peak Wavelength	λ_P	—	560	—	nm	
Min. Integration Time	$T_{intmin1}$	—	3.125	—	ms	
	$T_{intmin2}$	—	50	—	ms	With 50-Hz/60-Hz rejection
Max Integration Time	T_{intmax}	—	400	—	ms	With 50-Hz/60-Hz rejection
Output Resolution	RES_{ALS}	13	18	20	bit	Programmable
Full Scale ADC Count Value		—	—	65535	counts	
Dark ALS ADC Count Value		0	—	3	counts	G = 64, 50-ms integration time, Ee = 0
ALS ADC Count Value		1600	2000	2400	counts	λ = 530 nm, G = 3x, 100 ms integration time, Ee = 43 µW/cm^2

Figure 1: Spectral Response

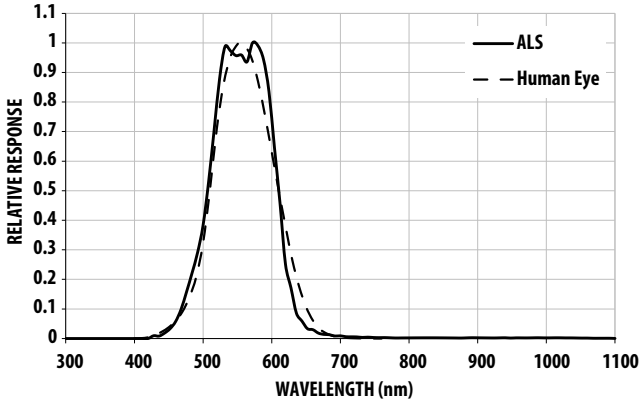
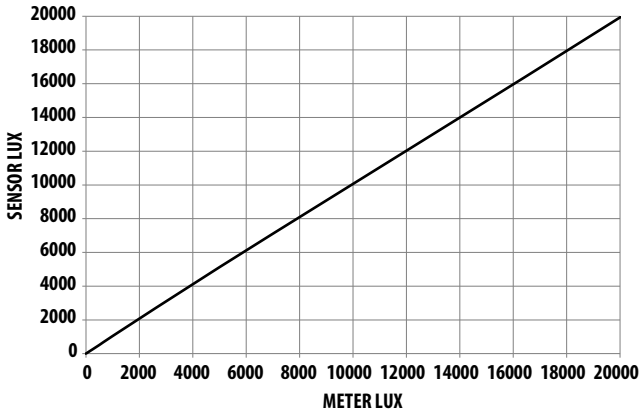


Figure 2: ALS Sensor LUX vs. Meter LUX Using White Light



(Pls use the diagram from AV02-4755EN, page 5)

Figure 3: ALS Sensor LUX vs. Meter LUX Using White Light

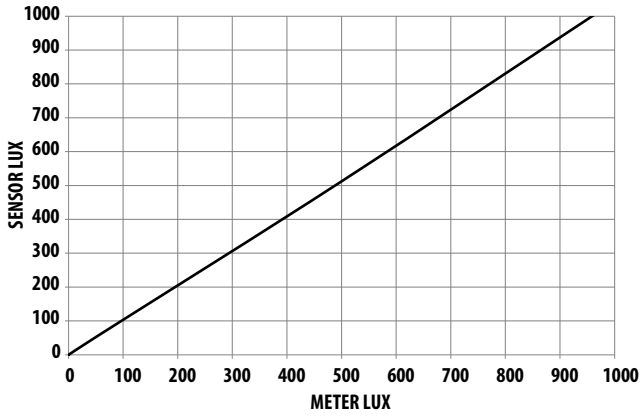


Figure 4: ALS Sensor LUX vs. Meter LUX Using White Light

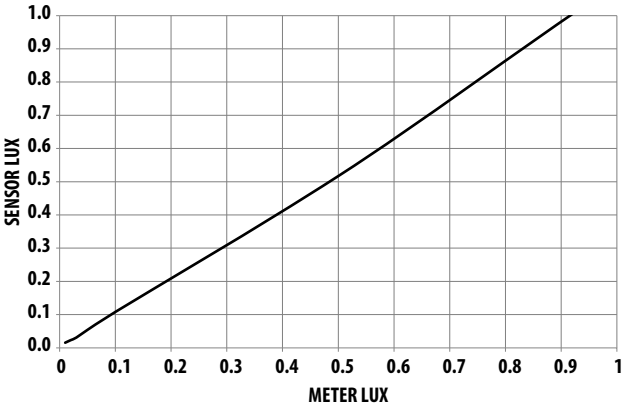


Figure 5: ALS Sensor LUX vs. Meter LUX Using White Light

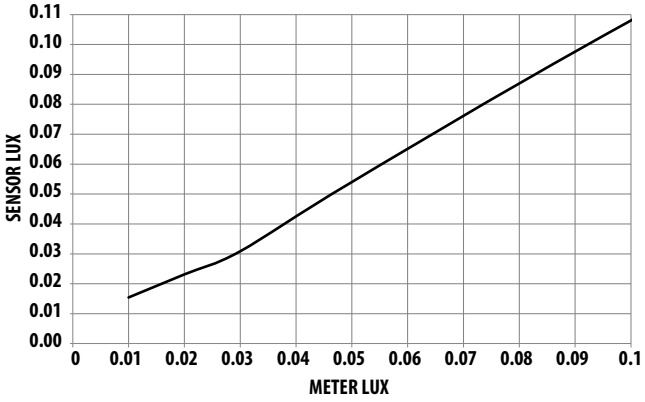


Figure 6: ALS Sensor LUX vs. Meter LUX Using Incandescent Light

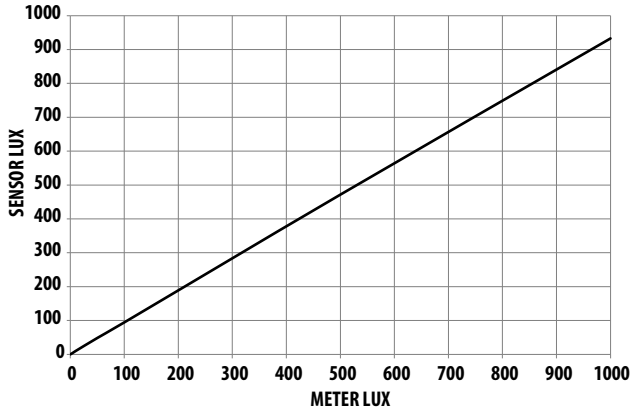


Figure 7: ALS Sensor LUX vs. Meter LUX Using Incandescent Light

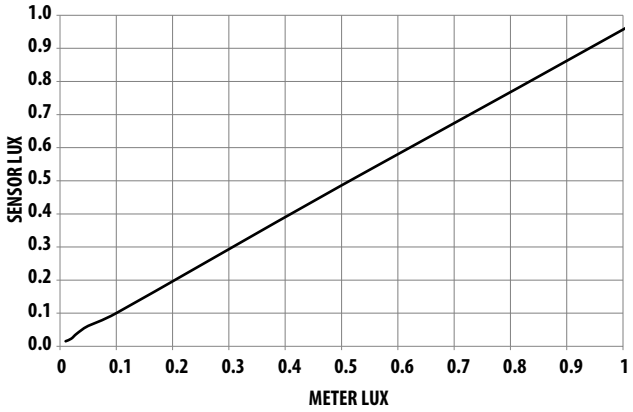


Figure 8: ALS Sensor LUX vs. Meter LUX Using Halogen Light

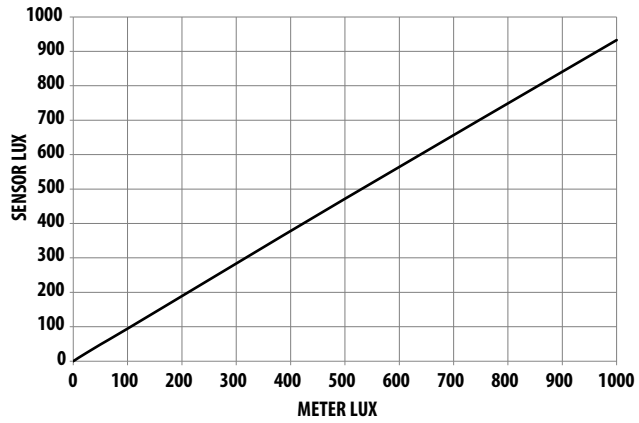


Figure 9: Normalized I_{DD} vs. V_{DD}

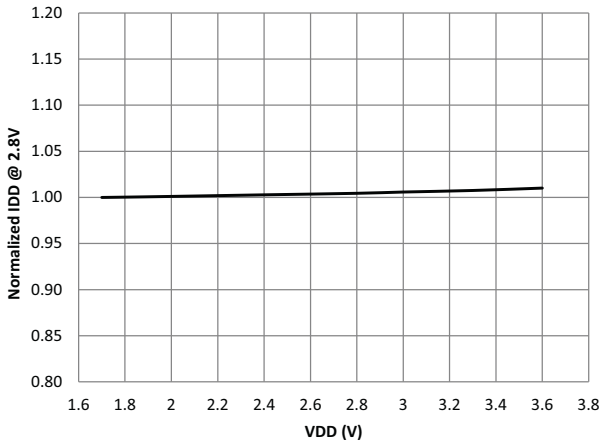


Figure 10: Normalized IDD vs. Temperature

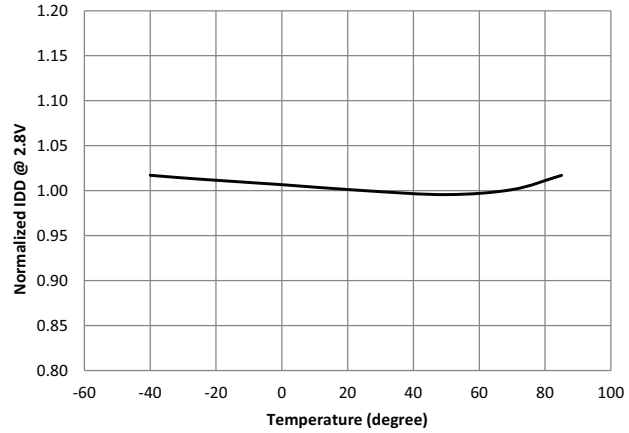
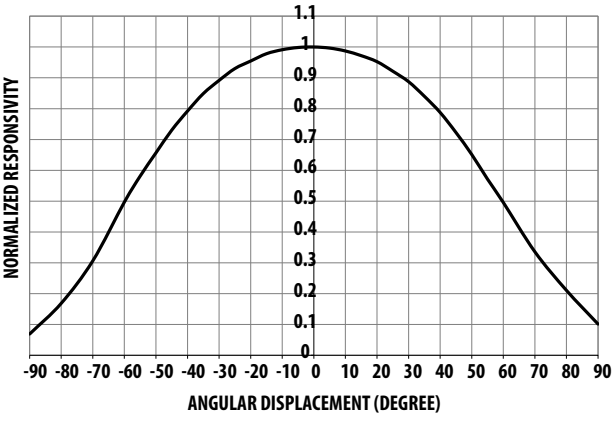


Figure 11: Normalized ALS PD Angular Response



Principles of Operation

System State Machine

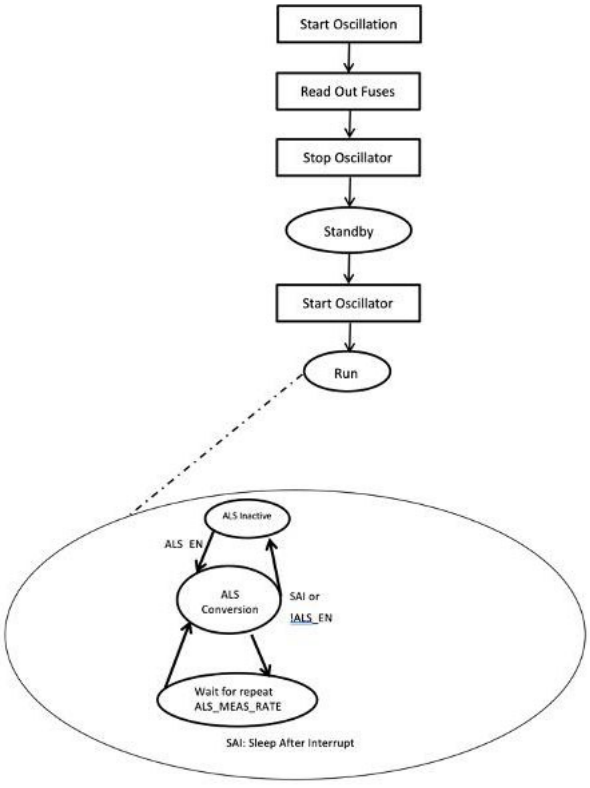
The main state machine is set to start state during power-on or software reset. As soon as the reset is released, the internal oscillator starts. The programmed I^2C address and the trim values are read from the internal nonvolatile memory (NVM) trimming data block. The APDS-9306-A65 enters into standby mode as soon as the idle state is reached.

If any of the sensor operation modes becomes activated through an I^2C command (ALS_EN bit is set to 1 and the sensor mode is selected with the respective bit in the MAIN_CTRL register), the internal support blocks are immediately powered on. When the voltages and currents are settled (typical after 500 µs), the state machine checks for trigger events from a measurement scheduler to start conversions according to the selected measurement repeat rates.

When the user resets the ALS_EN bit to 0, a running conversion is completed and the relevant ADCs move to standby mode thereafter. The support blocks only move to standby mode if all sensors are inactive. If any of the sensors is programmed to sleep after interrupt with the according bit in the MAIN_CTRL register, the relevant ADCs move to standby mode after the interrupt condition occurred. Also the sensor's Enable bit ALS_EN will be reset after following read out of the main status register.

The deactivation of ALS in the MAIN_CTRL register does not clear the related status bit in the MAIN_STATUS register. They are always reset upon activation of the respective sensor.

Figure 12: State Diagram



Interrupt

Interrupts will be triggered if upper or lower threshold values are crossed. It is possible to deactivate a sensor after an interrupt event occurred. Therefore, a bit for the respective sensor must be set in the MAIN_CTRL register (SAI_ALS). An interrupt can also be triggered if the output count variation of consecutive conversions has exceeded a defined limit.

The ALS interrupt signals are active low at the INT pad. A cleared ALS interrupt status flag will also clear the interrupt signal on the INT pad.

The interrupt is configured by the bit in the INT_CFG register. It can function as either threshold triggered (ALS_VAR_MODE = 0) or variance trigged (ALS_VAR_MODE = 1).

The ALS threshold interrupt is enabled with ALS_INT_EN = 1 and ALS_VAR_MODE = 0. The interrupt is set when the respective *_DATA register of the selected interrupt source channel is above the upper or below the lower threshold configured in the ALS_THRES_UP and ALS_THRES_LOW registers for a specified number of consecutive measurements.

The variance interrupt is enabled with ALS_INT_EN = 1 and ALS_VAR_MODE = 1. It is set when the absolute value difference between the preceding and the current output data of the selected interrupt source channel is above the decoded variance threshold for a specified number of consecutive measurements (1+ALS_PERSIST).

I²C Protocol

Interface and control of the APDS-9306-A65 is accomplished through an I²C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The device supports a single slave address of 0x52 using 7-bit addressing protocol.

The I²C standard provides for three types of bus transaction: read, write, and a combine protocol. During a write operation, the first byte written is a command byte followed by data. In a combine protocol, the first byte written is the command byte followed by reading a series of bytes. If a read command is issued, the register address from the previous command will be used for data access.

Likewise, if the MSB of the command is not set, the device will write a series of bytes at the address stored in the last valid command with a register address. For a complete description of I²C protocols, review the I2C specification at: http://www.NXP.com.

Figure 13: Start and Stop Conditions

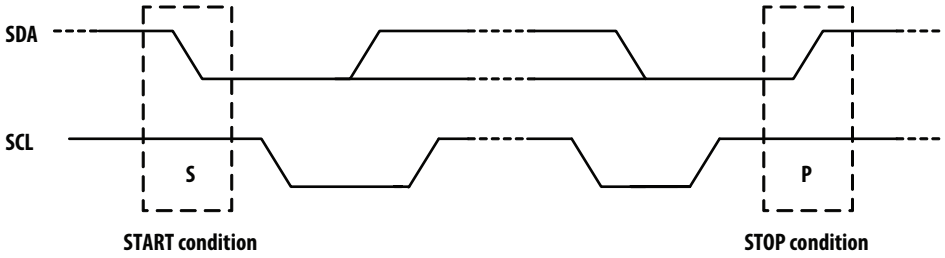


Figure 14: Data Transfer on an I^2C Bus

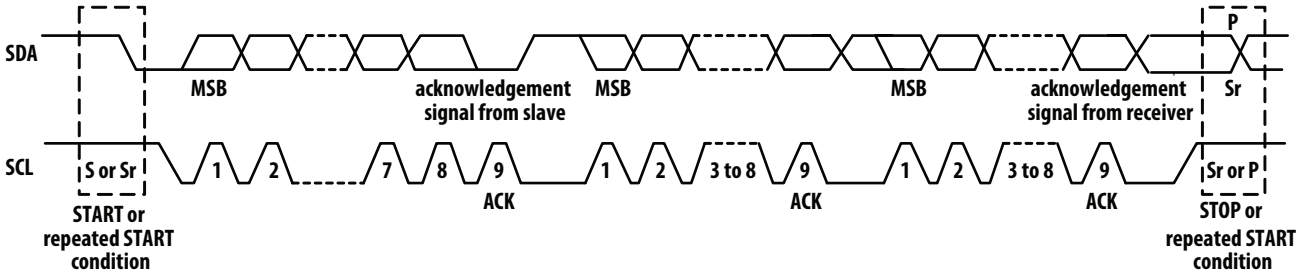
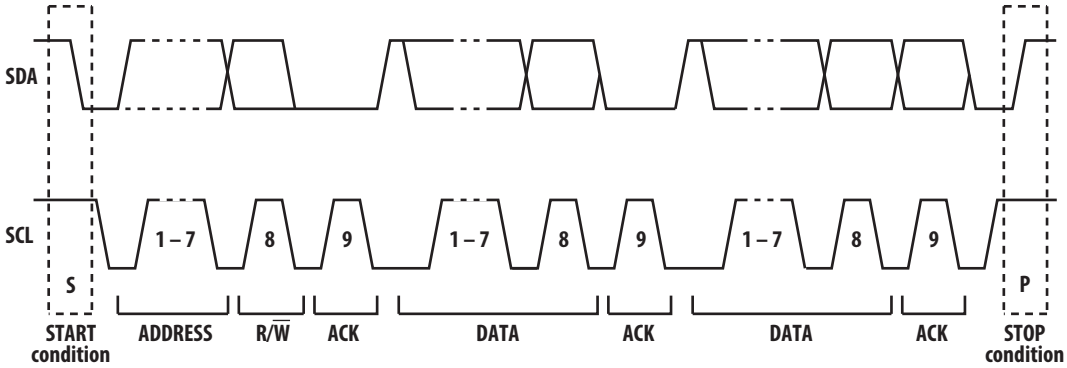


Figure 15: A Complete Data Transfer



A	Acknowledge (0)
N	Not Acknowledged (1)
P	Stop Condition
R	Read (1)
S	Start Condition
Sr	Repeated Start Condition
W	Write (0)
…	Continuation of Protocol
	Master-to-Slave
	Slave-to-Master

I²C Write Protocol

For the continuous Write operation, the pointer register gets auto incremented. Every byte is acknowledged by the slave.

S	Slave Address	W	A	Register Address	A	DATA	A	P

I²C Read Protocol

For the continuous Read operation, the pointer register gets autoincremented. The continuous Read stops when the Master does not acknowledge a byte.

S	Slave Address	R	A	DATA	A	P

I_2C Read Protocol – Combined Format

S	Slave Address	W	A	Register Address	A	Sr	Slave Address	R	A

DATA	A	P

Register Set

The APDS-9306-A65 is controlled and monitored by data registers and a command registers accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions.

Address	Type	Name	Description	Reset Value
00HEX	RW	MAIN_CTRL	Operation selection, software reset	00HEX
04HEX	RW	ALS_MEAS_RATE	ALS measurement rate and resolution setting	22HEX
05HEX	RW	ALS_GAIN	ALS analog gain range setting	01HEX
06HEX	R	DEV_ID	Device ID	B3HEX
07HEX	R	MAIN_STATUS	Power-on status, interrupt and data status	20HEX
0AHEX	R	ALS_CLEAR_DATA_0	ALS clear ADC measurement data - LSB	00HEX
0BHEX	R	ALS_CLEAR_DATA_1	ALS clear ADC measurement data	00HEX
0CHEX	R	ALS_CLEAR_DATA_2	ALS clear ADC measurement data - MSB	00HEX
0DHEX	R	ALS_DATA_0	ALS ADC measurement data - LSB	00HEX
0EHEX	R	ALS_DATA_1	ALS ADC measurement data	00HEX
0FHEX	R	ALS_DATA_2	ALS ADC measurement data - MSB	00HEX
19HEX	RW	INT_CFG	Interrupt configuration	10HEX
1AHEX	RW	INT_PST	Interrupt persist setting	00HEX
24HEX	RW	ALS_THRES_UP_0	ALS interrupt upper threshold, LSB	FFHEX
25HEX	RW	ALS_THRES_UP_1	ALS interrupt upper threshold	FFHEX
26HEX	RW	ALS_THRES_UP_2	ALS interrupt upper threshold, MSB	0FHEX
27HEX	RW	ALS_THRES_LOW_0	ALS interrupt lower threshold, LSB	00HEX
28HEX	RW	ALS_THRES_LOW_1	ALS interrupt lower threshold	00HEX
29HEX	RW	ALS_THRES_LOW_2	ALS interrupt lower threshold, MSB	00HEX
2AHEX	RW	ALS_THRES_VAR	ALS interrupt variance threshold	00HEX

MAIN_CTRL

Register	B7	B6	B5	B4	B3	B2	B1	B0	Register Address	Reset State	R/W
Operation selection, software reset	0	0	SAI_ALS	SW_RESET	0	0	ALS_EN	0	00HEX	00HEX	R/W

Field	Bit	Description
SAI_ALS	5	Sleep after interrupt for Light Sensor (SAI_ALS). When this bit is set, the ALS returns to standby (ALS_EN is cleared when the measurement is finished and MAIN_STATUS is read) when an interrupt occurs. This bit reacts on ALS interrupt status bit in the MAIN_STATUS register.
SW_RESET	4	■ 1: Reset will be triggered. If bit is set to 1, a software reset will be triggered. When SW_RESET bit is set, the device has to send an ACK and the RESET shall be executed when the stop bit is sent.
ALS_EN	1	■ 0: Ambient Light Sensor inactive (default). ■ 1: Ambient Light Sensor active.

ALS_MEAS_RATE

Register	B7	B6	B5	B4	B3	B2	B1	B0	Register Address	Reset State	R/W
ALS measurement rate and resolution setting	0	ALS Resolution/Bit Width			0	ALS Measurement Rate			04HEX	22HEX	R/W

Field	Bit	Description
ALS Resolution/ Bit Width	6:4	■ 000: 20 bit – 400 ms ■ 001: 19 bit – 200 ms ■ 010: 18 bit – 100 ms **(default)** ■ 011: 17 bit – 50 ms ■ 100: 16 bit – 25 ms ■ 101: 13 bit – 3.125 ms ■ 110: Reserved ■ 111: Reserved
ALS Measurement Rate	2:0	■ 000: 25 ms ■ 001: 50 ms ■ 010: 100 ms **(default)** ■ 011: 200 ms ■ 100: 500 ms ■ 101: 1000 ms ■ 110: 2000 ms ■ 111: 2000 ms

When the measurement repeat rate is programmed to be faster than possible for the programmed ADC measurement time, the repeat rate will be lower than programmed (maximum speed).

Writing to this register resets ALS state machine and starts new measurements.

ALS_GAIN

Register	B7	B6	B5	B4	B3	B2	B1	B0	Register Address	Reset State	R/W
ALS analog gain range	0	0	0	0	0	ALS Gain Range			05HEX	01HEX	RW

Field	Bit	Description
ALS Gain Range	2:0	■ 000: Gain 1 ■ 001: Gain 3 **(default)** ■ 010: Gain 6 ■ 011: Gain 18 ■ 100: Gain 54

Writing to this register resets ALS state machine and starts new measurements.

DEV_ID

Register	B7	B6	B5	B4	B3	B2	B1	B0	Register Address	Reset State	R/W
Device ID	DEVICE ID								06HEX	B3HEX	R

Field	Bit	Description
Device ID	7:0	Device number.

MAIN_STATUS

Register	B7	B6	B5	B4	B3	B2	B1	B0	Register Address	Reset State	R/W
Power on status, interrupt and data status	0	0	Power On Status	ALS Interrupt Status	ALS Data Status	0	0	0	07HEX	20HEX	R

Field	Bit	Description
Power On Status	5	■ 1: Part went through a power-up event, either because the part was turned on or because there was power supply voltage disturbance **(default at first register read)**. All interrupt threshold settings in the registers have been reset to power-on default states and should be examined if necessary. The flag is cleared after the register is read.
ALS Interrupt Status	4	■ 0: Interrupt condition has not occurred **(default)**. ■ 1: Interrupt condition has occurred (cleared after read).
ALS Data Status	3	■ 0: Old data, already read **(default)**. ■ 1: New data, not yet read (cleared after read).

ALS_CLEAR_DATA

Register	B7	B6	B5	B4	B3	B2	B1	B0	Register Address	Reset State	R/W
ALS Clear ADC measurement data, LSB	ALS_CLEAR_DATA_0								0AHEX	00HEX	R
ALS Clear ADC measurement data	ALS_CLEAR_DATA_1								0BHEX	00HEX	R
ALS Clear ADC measurement data, MSB	0	0	0	0	ALS_CLEAR_DATA_2				0CHEX	00HEX	R

CLEAR channel digital output data (unsigned integer, 13 bit to 20 bit, LSB-aligned).

The channel out is already compensated internally: ALS_CLEAR_DATA = ALS_CLEAR_{int} – COMP.

When an I^2C read operation is active and points to an address in the range 07HEX to 18HEX, all registers in this range are locked until the I^2C read operation is completed or this address range is left.

This guarantees that the data in the registers comes from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the actual *_DATA registers are updated as soon as there is no ongoing I²C read operation to the address range 07HEX to 18HEX.

Reg 0AHEX	7:0	Clear PD data least significant data byte
Reg 0BHEX	7:0	Clear PD data intervening data byte
Reg 0CHEX	3:0	Clear PD data most significant data byte

ALS_DATA

Register	B7	B6	B5	B4	B3	B2	B1	B0	Register Address	Reset State	R/W
ALS ADC measurement data, LSB	ALS_DATA_0								0DHEX	00HEX	R
ALS ADC measurement data	ALS_DATA_1								0EHEX	00HEX	R
ALS ADC measurement data, MSB	0	0	0	0	ALS_DATA_2				0FHEX	00HEX	R

ALS channel digital output data (unsigned integer, 13 bit to 20 bit, LSB-aligned).

The channel out is already compensated internally: ALS_DATA = ALS_{int} – COMP.

When an I^2C read operation is active and points to an address in the range 07HEX to 18HEX, all registers in this range are locked until the I^2C read operation is completed or this address range is left.

This guarantees that the data in the registers comes from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the actual *_DATA registers are updated as soon as there is no ongoing I^2C read operation to the address range 07HEX to 18HEX.

Reg 0DHEX	7:0	ALS data least significant data byte
Reg 0EHEX	7:0	ALS data intervening data byte
Reg 0FHEX	3:0	ALS data most significant data byte

INT_CFG

Register	B7	B6	B5	B4	B3	B2	B1	B0	Register Address	Reset State	R/W
Interrupt configuration	0	0	ALS_INT_SEL	ALS_VAR_MODE	ALS_INT_EN	0	0	19HEX	10HEX	RW	

Field	Bit	Description
ALS_INT_SEL	5:4	■ 00: Clear channel. ■ 01: ALS channel **(default)**.
ALS_VAR_MODE	3	■ 0: ALS threshold interrupt mode (default). ■ 1: ALS variation interrupt mode.
ALS_INT_EN	2	■ 0: ALS interrupt disabled (default). ■ 1: ALS interrupt enabled.

INT_PST

Register	B7	B6	B5	B4	B3	B2	B1	B0	Register Address	Reset State	R/W
INT_PST	ALS_PERSIST				0				1AHEX	00HEX	RW

FIELD	BIT	DESCRIPTION
ALS_PERSIST	7:4	■ 0000: Every ALS value out of threshold range (default) asserts an interrupt. ■ 0001: 2 consecutive ALS values out of threshold range assert an interrupt. ■ … ■ 1111: 16 consecutive ALS values out of threshold range assert an interrupt.

ALS_THRES_UP

Register	B7	B6	B5	B4	B3	B2	B1	B0	Register Address	Reset State	R/W
ALS interrupt upper threshold, LSB	ALS_THRES_UP_0								24HEX	FFHEX	RW
ALS interrupt upper threshold	ALS_THRES_UP_1								25HEX	FFHEX	RW
ALS interrupt upper threshold, MSB	0	0	0	0	ALS_THRES_UP_2				26HEX	0FHEX	RW

ALS_THRES_UP sets the upper threshold value for the ALS interrupt. The interrupt controller compares the value in ALS_THRES_UP against measured data in the ALS_DATA registers of the selected ALS interrupt channel. It generates an interrupt event if ALS_DATA exceeds the threshold level.

The data format for ALS_THRES_UP must match that of the ALS_DATA registers.

Writing to these registers resets the ALS state machine and starts new measurements.

Reg 24HEX	7:0	ALS upper interrupt threshold value, LSB
Reg 25HEX	7:0	ALS upper interrupt threshold value, intervening byte
Reg 26HEX	3:0	ALS upper interrupt threshold value, MSB

ALS_THRES_LOW

Register	B7	B6	B5	B4	B3	B2	B1	B0	Register Address	Reset State	R/W
ALS interrupt lower threshold, LSB	ALS_THRES_LOW_0								27HEX	00HEX	RW
ALS interrupt lower threshold	ALS_THRES_LOW_1								28HEX	00HEX	RW
ALS interrupt lower threshold, MSB	0	0	0	0	ALS_THRES_UP_2				29HEX	00HEX	RW

ALS_THRES_LOW sets the lower threshold value for the ALS interrupt. The interrupt controller compares the value in ALS_THRES_LOW against measured data in the ALS_DATA registers of the selected ALS interrupt channel. It generates an interrupt event if ALS_DATA exceeds the threshold level.

The data format for ALS_THRES_LOW must match that of the ALS_DATA registers.

Writing to these registers resets the ALS state machine and starts new measurements.

Reg 27HEX	7:0	ALS lower interrupt threshold value, LSB
Reg 28HEX	7:0	ALS lower interrupt threshold value, intervening byte
Reg 29HEX	3:0	ALS lower interrupt threshold value, MSB

ALS_THRES_VAR

Register	B7	B6	B5	B4	B3	B2	B1	B0	Register Address	Reset Sate	R/W
ALS interrupt variance threshold	0	0	0	0	ALS_ THRES_UP_2				2AHEX	00HEX	RW

Writing to these registers resets the ALS state machine and starts new measurements.

FIELD	BIT	DESCRIPTION
ALS_THRES_VAR	2:0	■ 000: New ALS_DATA varies by 8 counts compared to previous result. ■ 001: new ALS_DATA varies by 16 counts compared to previous result. ■ 010: new ALS_DATA varies by 32 counts compared to previous result. ■ 011: new ALS_DATA varies by 64 counts compared to previous result. ■ 100: new ALS_DATA varies by 128 counts compared to previous result. ■ 101: new ALS_DATA varies by 256 counts compared to previous result. ■ 110: new ALS_DATA varies by 512 counts compared to previous result. ■ 111: new ALS_DATA varies by 1024 counts compared to previous result.

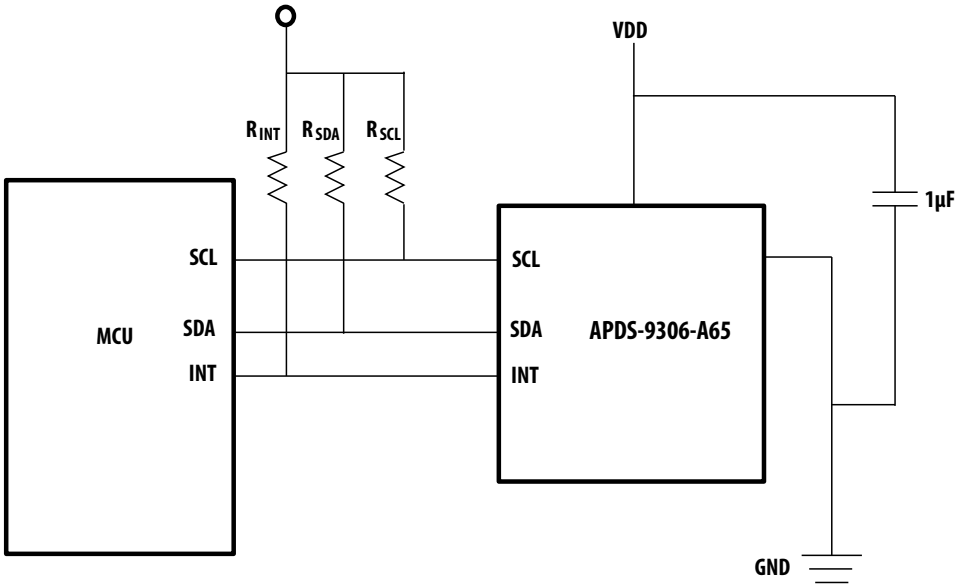
Application Information: Hardware

The application hardware circuit for implementing an ALS is simple with the APDS-9306-A65 and is shown in the following figure. The bypass capacitor is placed as close to the V_{DD} pin and is connected directly to the power source and to the ground, as shown in the figure. It allows the AC component of the V_{DD} to pass through to ground. Use bypass capacitor with low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents caused by internal logic switching.

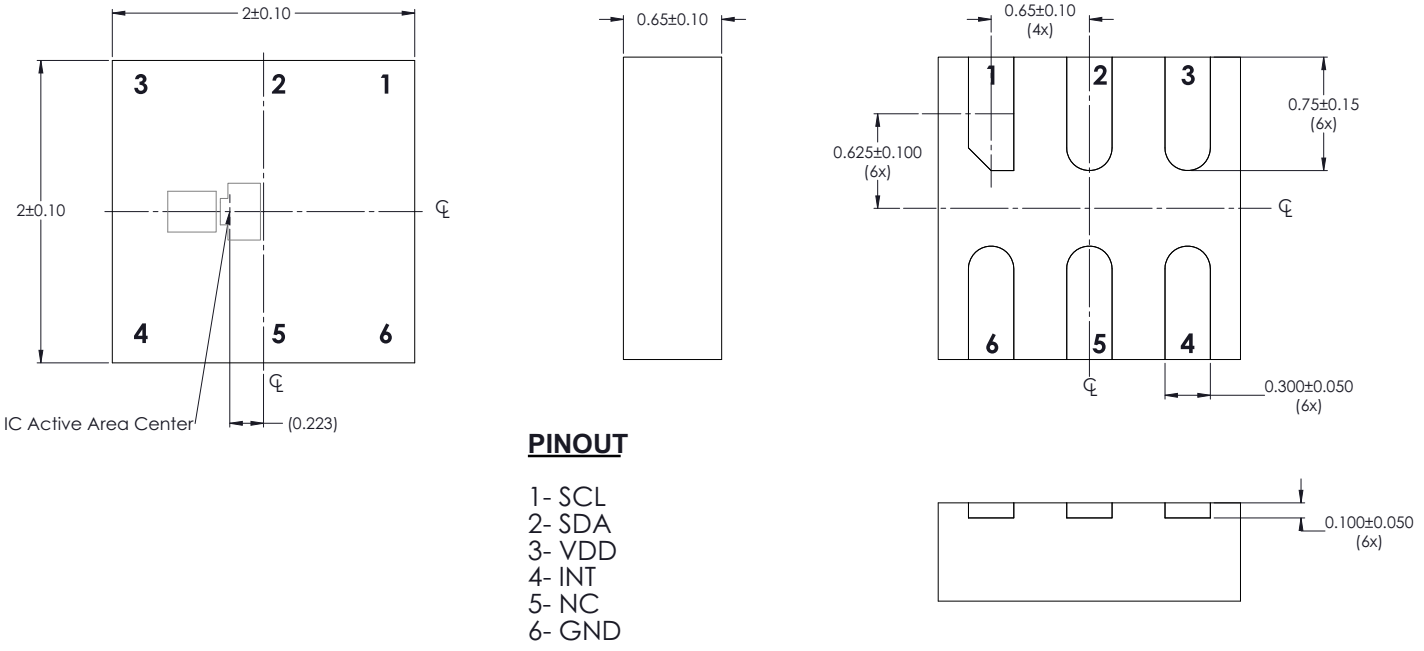
Pull-up resistors, RSDA and RSCL, maintain the SDA and SCL lines at a high level when the bus is free and ensure the signals are pulled up from a low to a high level within the required rise time. A pull-up resistor, RINT, is also required for the interrupt (INT), which functions as a wired-AND signal in a similar fashion to the SCL and SDA lines. A typical impedance value of 10 kΩ can be used.

For a complete description of I^2C maximum and minimum R1 and R2 values, review the I^2C Specification at http:// www.semiconductors.philips.com.

Figure 16: APDS-9306-A65 Supply Application Circuit



Package Outline Dimensions

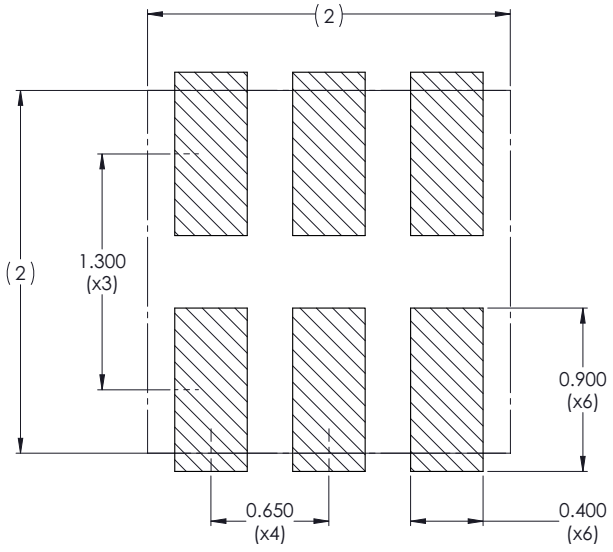


PINOUT

1- SCL
2- SDA
3- VDD
4- INT
5- NC
6- GND

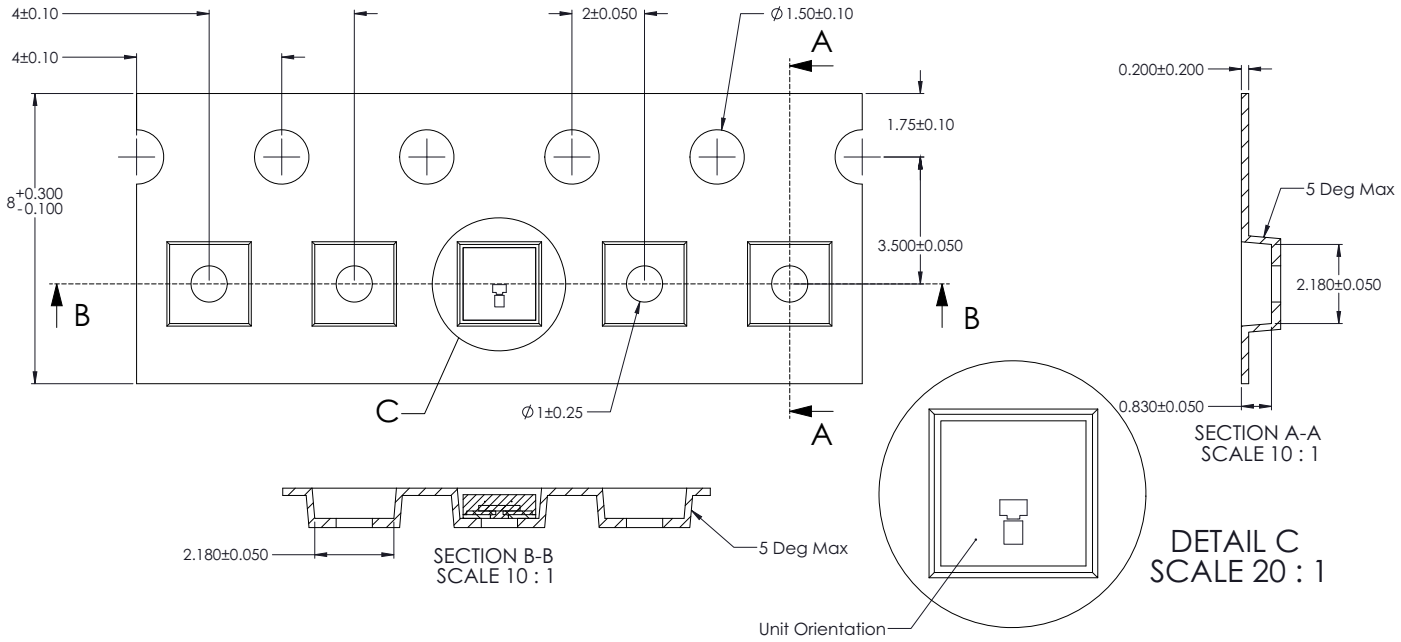
NOTE: All dimensions are in mm.

PCB Pad Layout



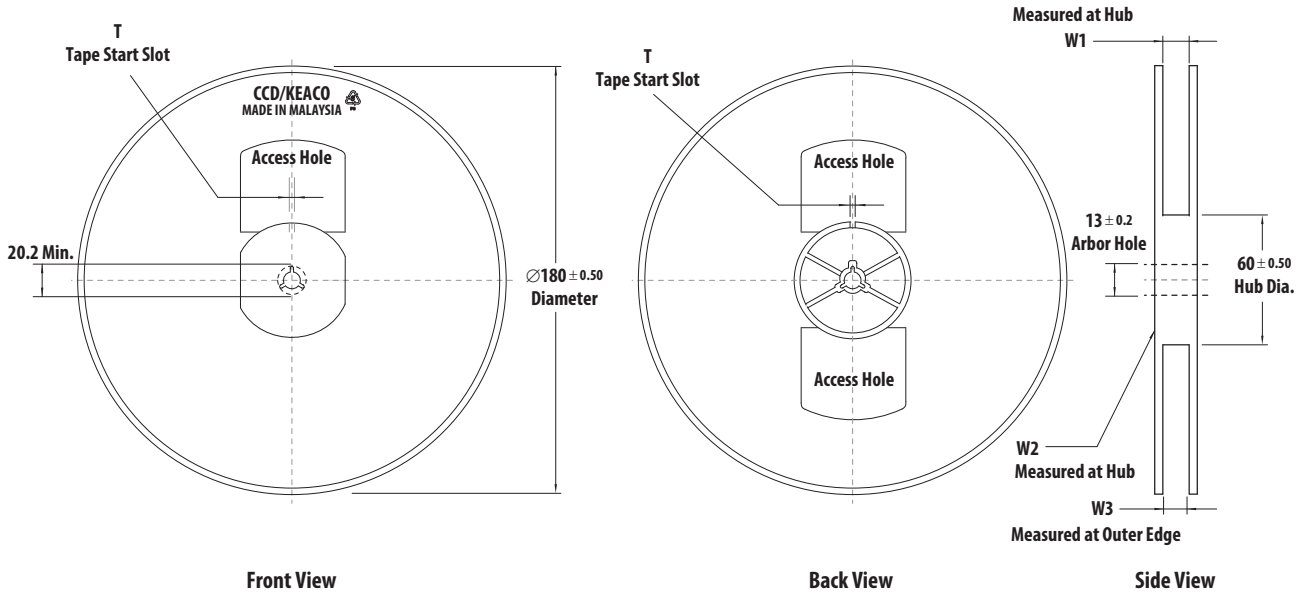
NOTE: All dimensions are in mm.

Tape Dimensions



NOTE: All linear dimensions are in mm.

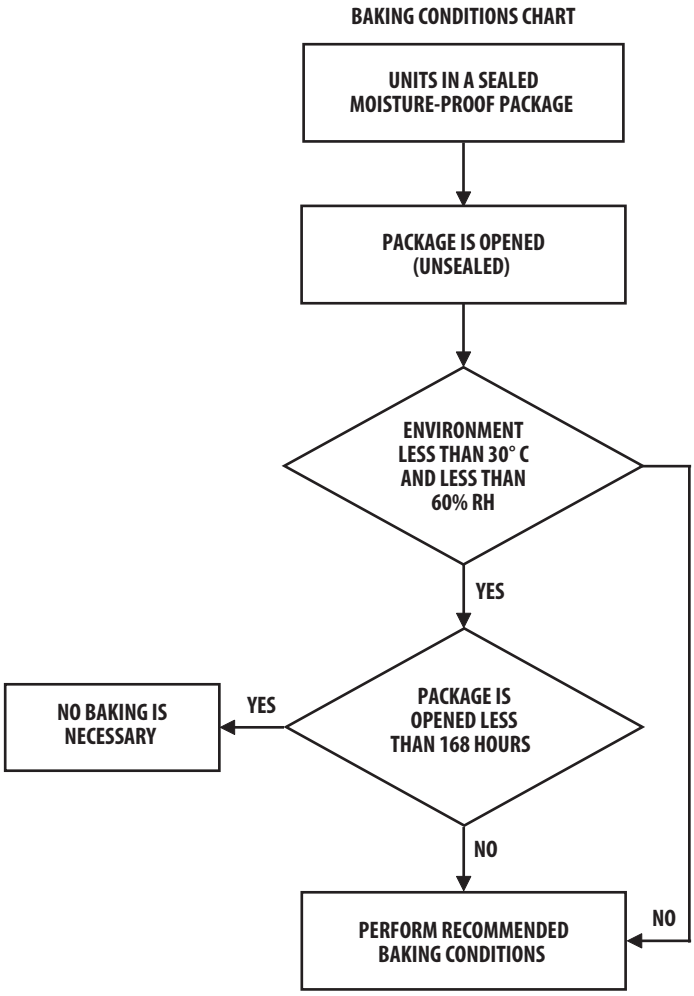
Reel Dimensions



NOTE: All linear dimensions are in mm.

Moisture Proof Packaging

All APDS-9306-A65 options are shipped in moisture proof package. When opened, moisture absorption begins. This part is compliant to JEDEC MSL 3.



Baking Conditions

Package	Temperature	Time
In Reel	60°C	48 hours
In Bulk	100°C	4 hours

If the parts are not stored in dry conditions, they must be baked before reflow to prevent damage to the parts.

Baking should only be done once.

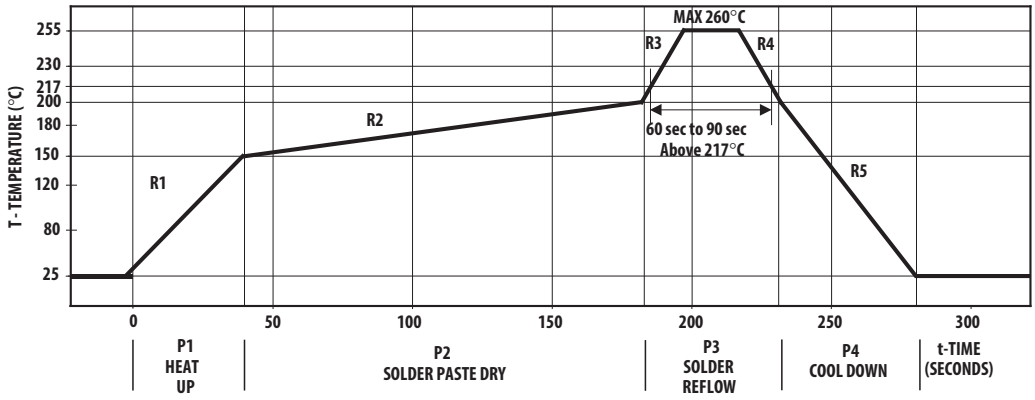
Recommended Storage Conditions

Storage Temperature	10°C to 30°C
Relative Humidity	Below 60% RH

Time from Unsealing to Soldering

After removal from the bag, the parts should be soldered within 168 hours if stored at the recommended storage conditions. If times longer than 168 hours are needed, the parts must be stored in a dry box.

Recommended Reflow Profile



Process Zone	Symbol	ΔT	Maximum ΔT/Δtime or Duration
Heat Up	P1, R1	25° to 150°C	3°C/s
Solder Paste Dry	P2, R2	150°C to 200°C	100s to 180s
Solder Reflow	P3, R3	200°C to 260°C	3°C/s
	P3, R4	260°C to 200°C	–6°C
Cool Down	P4, R5	200°C to 25°C	–6°C
Time maintained above liquidus point, 217°C		> 217°C	60s to 90s
Peak Temperature		260°C	—
Time within 5°C of actual Peak Temperature		—	20s to 40s
Time 25°C to Peak Temperature		25°C to 260°C	8 minutes

The reflow profile is a straight-line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different ΔT/Δtime temperature change rates or duration. The ΔT/Δtime rates or duration are detailed in the above table. The temperatures are measured at the component to printed circuit board connections.

In **process zone P1**, the PC board and component pins are heated to a temperature of 150°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 3°C per second to allow for even heating of both the PC board and component pins.

Process zone P2 should be of sufficient time duration (100 to 180 seconds) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder.

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 260°C (500°F) for optimum results. The dwell time above the liquidus point of solder should be between 60 and 90 seconds. This is to assure proper coalescing of the solder paste into liquid solder and the formation of good solder connections. Beyond the recommended dwell time the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed 6°C per second maximum. This limitation is necessary to allow the PC board and component pins to change dimensions evenly, putting minimal stresses on the component.

It is recommended to perform refl ow soldering no more than twice.