19-3692; Rev 1; 5/11

Ultra-Low-Voltage Level Translators

General Description

The MAX13000E–MAX13005E 6-channel level translators provide the level shifting necessary to allow data transfer in multivoltage systems. Externally applied voltages, V_{CC} and V_L, set the logic levels on either side of the device. Logic signals present on the V_L side of the device appear as higher voltage logic signals on the V_{CC} side of the device, and vice-versa.

The MAX13000E–MAX13005E feature a low V_{CC} and V_L quiescent supply current less than 4µA. The MAX13000E–MAX13005E also have ±15kV ESD protection on the I/O V_{CC} side for greater protection in applications that route signals externally. The ESD protection is specified using the Human Body Model (HBM). The MAX13000E/MAX13001E/MAX13002E operate at a guaranteed 230kbps data rate. The MAX13003E/MAX13004E/MAX13005E operate at a guaranteed 20Mbps data rate when V_{CC} > +1.65V.

The MAX13000E/MAX13003E are bidirectional level translators, allowing data translation in either direction ($V_L \leftrightarrow V_{CC}$) on any single data line without a DIRECTION input. The MAX13001E/MAX13002E/MAX13004E/MAX13005E unidirectional level translators level shift data in one direction ($V_L \rightarrow V_{CC}$ or $V_{CC} \rightarrow V_L$) on any single data line. The MAX13001E/MAX13002E/MAX13004E/MAX13005E unidirectional translators' inputs have the capability to interface with both CMOS and open-drain (OD) outputs. For more information see the *Ordering Information, Selector Guide,* and the *Input-Driver Requirements* sections.

The MAX13000E–MAX13005E operate with +0.9V to +3.6V V_L voltages and +1.5V to +3.6V V_{CC} voltages. The MAX13000E–MAX13005E are available in 16-bump UCSP™ and 16-pin TSSOP packages, and are specified over the extended -40°C to +85°C operating temperature range.

Applications

CMOS Logic-Level Translation
Open-Drain I/O Translation
OD-to-CMOS Signal Conversion
Low-Voltage ASIC Level Translation
Cell Phones
SPI™ and MICROWIRE® Level Translation
Smart-Card Readers
Portable POS Systems
Portable Communication Devices
Low-Cost Serial Interfaces
Telecommunications Equipment

Features

- **Guaranteed Data-Rate Options**
  - **230kbps (MAX13000E/MAX13001E/MAX13002E)**
  - **20Mbps (MAX13003E/MAX13004E/MAX13005E)**
- **Bidirectional Level Translation Without a DIRECTION Input**
- **Operational Down to +0.9V on V_L and +1.5V on V_{CC}**
- **±15kV ESD Protection on I/O V_{CC} Lines per HBM**
- **Low <4µA Quiescent Current**
- **Enable/Shutdown Control**
- **2mm x 2mm, 16-Bump UCSP and Lead Packaging Options**
- **CMOS or Open-Drain Outputs Interface Capability**

UCSP is a trademark of Maxim Integrated Products, Inc.
SPI is a trademark of Motorola, Inc.
MICROWIRE is a registered trademark of National Semiconductor Corp.

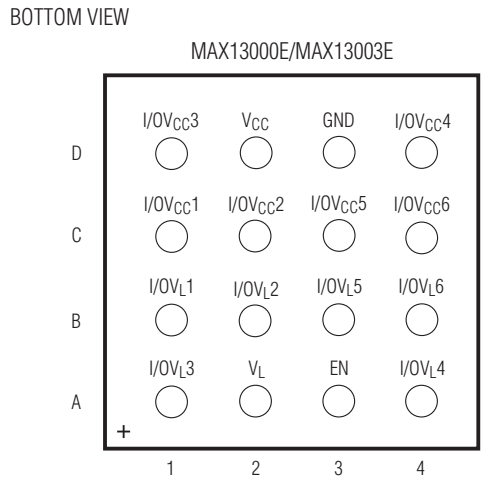
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX13000EEUE+	-40°C to +85°C	16 TSSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Ordering Information continued at end of data sheet.

Pin Configurations



4 X 4 UCSP

Pin Configurations continued at end of data sheet.

Typical Operating Circuits and Selector Guide appear at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

Voltages referenced to GND.
V_{CC} .....-0.3V to +4V
V_L .....-0.3V to +4V
$I/O_{VCC_}$ .....-0.3V to (V_{CC} + 0.3V)
$I/O_{VL_}$ .....-0.3V to (V_L + 0.3V)
EN .....-0.3V to (V_L + 0.3V)
Short-Circuit Duration $I/O_{VL_}$, $I/O_{VCC_}$ to GND .....Continuous

Continuous Power Dissipation (T_A = +70°C)
16-Pin TSSOP (derate 9.4mW/°C at +70°C) 755mW
16-Bump UCSP (derate 8.2mW/°C at +70°C) 659mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +1.5V to +3.6V, V_L = +0.9V to V_{CC}, $C_{I/OVL} \le 15pF$, $C_{I/OVCC} \le 50pF$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_L Supply Range	V_L	$V_L \le V_{CC}$ (Note 2)		0.9		V_{CC}	V
V_{CC} Supply Range	V_{CC}	(Note 2)		1.5		3.6	V
Supply Current from V_{CC} (Note 3)	I_{QVCC}	T_A = +25°C				4	µA
		T_A = +85°C				40	
Supply Current from V_L (Note 3)	I_{QVL}	T_A = +25°C	(Note 3)		1	5	µA
			$V_L < V_{CC}$ - 0.2V			2	
		T_A = +85°C	(Note 3)		4	40	
			$V_L < V_{CC}$ - 0.2V			20	
V_{CC} Shutdown Supply Current (Note 3)	$I_{SHDN-VCC}$	EN = GND, T_A = +25°C				2	µA
		EN = GND, T_A = +85°C				20	
V_L Shutdown Supply Current (Note 3)		T_A = +25°C	$V_L < V_{CC}$ - 0.2V, EN = GND			2	µA
			EN = GND		1	4	
		T_A = +85°C	$V_L < V_{CC}$ - 0.2V, EN = GND			20	
			EN = GND			40	
I/O Tri-State Output Leakage Current		I/O $V_{L_}$, I/O $V_{CC_}$, EN = GND	T_A = +25°C			0.35	µA
			T_A = +85°C			1	
I/O Tri-Stated Output Leakage Current		$V_L < V_{CC}$ - 0.2V, I/O $V_{L_}$, I/O $V_{CC_}$, EN = GND	T_A = +25°C			0.2	µA
			T_A = +85°C			0.5	
EN Input Leakage Current		T_A = +25°C				0.35	µA
		T_A = +85°C				1	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +1.5V to +3.6V, V_L = +0.9V to V_{CC}, $C_{I/OVL} \le 15pF$, $C_{I/OVCC} \le 50pF$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC-LEVEL THRESHOLDS						
I/$OV_{L_}$ Input-Voltage-High Threshold	V_{IHL}				2/3 × V_L	V
I/$OV_{L_}$ Input-Voltage-Low Threshold	V_{ILL}		1/3 × V_L			V
I/$OV_{CC_}$ Input-Voltage-High Threshold	V_{IHC}				2/3 × V_{CC}	V
I/$OV_{CC_}$ Input-Voltage-Low Threshold	V_{ILC}		1/3 × V_{CC}			V
EN Input-Voltage-High Threshold	V_{IHEN}				2/3 × V_L	V
EN Input-Voltage-Low Threshold	V_{ILEN}		1/3 × V_L			V
I/$OV_{L_}$ Output-Voltage High	V_{OHL}	I/$OV_{L_}$ source current = 20µA	V_L - 0.25			V
I/$OV_{L_}$ Output-Voltage Low	V_{OLL}	MAX13002E/MAX13005E, $OV_{L_}$ sink current = 1µA			0.3	V
		MAX13000E/MAX13001E/MAX13003E/ MAX13004E, I/$OV_{L_}$ sink current = 20µA			0.25	
I/$OV_{CC_}$ Output-Voltage High	V_{OHC}	I/$OV_{CC_}$ source current = 20µA	V_{CC} - 0.25			V
I/$OV_{CC_}$ Output-Voltage Low	V_{OLC}	MAX13001E/MAX13004E, $OV_{CC_}$ sink current = 1µA			0.3	V
		MAX13000E/MAX13002E/MAX13003E/ MAX13005E, I/$OV_{CC_}$ sink current = 20µA			0.25	
OUTPUT CURRENTS						
Output Sink Current During Transient (V_{CC} Side)		V_{CC} = +1.65V, MAX13003E/MAX13004E/MAX13005E		25		mA
		V_{CC} = +1.65V, MAX13000E/MAX13001E/MAX13002E		1		
Output Sink Current During Transient (V_L Side)		V_L = +1.2V, V_{CC} = +1.65V, MAX13003E/MAX13004E/MAX13005E		30		mA
		V_L = +1.2V, V_{CC} = +1.65V, MAX13000E/MAX13001E/MAX13002E		1		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +1.5V to +3.6V, V_L = +0.9V to V_{CC}, $C_{I/OVL}$ ≤ 15pF, $C_{I/OVCC}$ ≤ 50pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Source Current During Transient (V_{CC} Side)		V_{CC} = +1.65V, MAX13003E/MAX13004E/MAX13005E		22		mA
		V_{CC} = +1.65V, MAX13000E/MAX13001E/MAX13002E		1		
Output Source Current During Transient (V_L Side)		V_L = +1.2V, V_{CC} = +1.65V, MAX13003E/MAX13004E/MAX13005E		25		mA
		V_L = +1.2V, V_{CC} = +1.65V, MAX13000E/MAX13001E/MAX13002E		1		
ESD PROTECTION						
I/OV_{CC}_		Human Body Model		±15		kV
		Air-Gap Discharge (IEC61000-4-2)		±10		
		Contact Discharge (IEC61000-4-2)		±8		

TIMING CHARACTERISTICS

(V_{CC} = +1.5V to +3.6V, V_L = +0.9V to V_{CC}, $C_{I/OVL}$ ≤ 15pF, $C_{I/OVCC}$ ≤ 50pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/OV_{CC}_ Rise Time	t_{RVCC}	$C_{I/OVCC}$ = 50pF, MAX13003E/MAX13004E/MAX13005E, V_{CC} = +1.65V, Figures 1a, 1b			15	ns
		$C_{I/OVCC}$ = 50pF, MAX13003E/MAX13004E/MAX13005E, V_{CC} = +1.5V, Figures 1a, 1b			15	
		$C_{I/OVCC}$ = 50pF, MAX13000E/MAX13001E/MAX13002E, Figures 1a, 1b	400		1400	
I/OV_{CC}_ Fall Time	t_{FVCC}	$C_{I/OVCC}$ = 50pF, MAX13003E/MAX13004E/MAX13005E, V_{CC} = +1.65V, Figures 1a, 1b			15	ns
		$C_{I/OVCC}$ = 50pF, MAX13003E/MAX13004E/MAX13005E, V_{CC} = +1.5V, Figures 1a, 1b			15	
		$C_{I/OVCC}$ = 50pF, MAX13000E/MAX13001E/MAX13002E, Figures 1a, 1b	400		1400	

TIMING CHARACTERISTICS (continued)

(V_{CC} = +1.5V to +3.6V, V_L = +0.9V to V_{CC}, $C_{I/OVL}$ ≤ 15pF, $C_{I/OVCC}$ ≤ 50pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/OV$_L$_ Rise Time	t_{RVL}	$C_{I/OVL}$ = 50pF, MAX13003E/MAX13004E/MAX13005E, V_{CC} = +1.65V, Figures 2a, 2b			15	ns
		$C_{I/OVL}$ = 15pF, MAX13003E/MAX13004E/MAX13005E, V_{CC} = +1.5V, Figures 2a, 2b			15	
		$C_{I/OVL}$ = 50pF, MAX13000E/MAX13001E/MAX13002E, Figures 2a, 2b	300		1200	
I/OV$_L$_ Fall Time	t_{FVL}	$C_{I/OVL}$ = 50pF, MAX13003E/MAX13004E/MAX13005E, V_{CC} = +1.65V, Figures 2a, 2b			15	ns
		$C_{I/OVL}$ = 15pF, MAX13003E/MAX13004E/MAX13005E, V_{CC} = +1.5V, Figures 2a, 2b			15	
		$C_{I/OVL}$ = 50pF, MAX13000E/MAX13001E/MAX13002E, Figures 2a, 2b	300		1200	
Propagation Delay (Driving I/OV$_L$_)	I/O_{VL-VCC}	$C_{I/OVCC}$ = 50pF, MAX13003E/MAX13004E/MAX13005E, Figures 1a, 1b			20	ns
		$C_{I/OVCC}$ = 50pF, MAX13000E/MAX13001E/MAX13002E, Figures 1a, 1b			1000	
Propagation Delay (Driving I/OV$_{CC}$_)	I/O_{VCC-VL}	V_{CC} > +1.65V, $C_{I/OVL}$ = 50pF, MAX13003E/MAX13004E/MAX13005E, Figures 2a, 2b			20	ns
		V_{CC} = 1.5V, $C_{I/OVL}$ = 15pF, MAX13003E/MAX13004E/MAX13005E, Figures 2a, 2b			20	
		$C_{I/OVL}$ = 50pF, MAX13000E/MAX13001E/MAX13002E, Figures 2a, 2b			1000	
Propagation Delay from I/OV$_L$ to I/OV$_{CC}$_ after EN (Note 5)	t_{EN-VCC}	$C_{I/OVCC}$ = 50pF, CMOS output, Figure 3			2	µs
		$C_{I/OVCC}$ = 50pF, OD output, Figure 3			6	

TIMING CHARACTERISTICS (continued)

(V_{CC} = +1.5V to +3.6V, V_L = +0.9V to V_{CC}, $C_{I/OVL}$ ≤ 15pF, $C_{I/OVCC}$ ≤ 50pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 4)

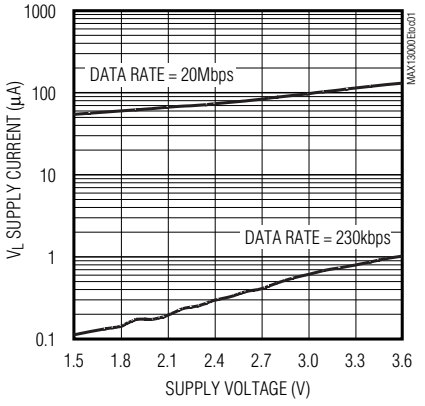
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay from I/OV_{CC} to I/OV_L after EN (Note 5)	t_{EN-VL}	$C_{I/OVL}$ = 50pF, CMOS output, Figure 4			2	µs
		$C_{I/OVL}$ = 50pF, OD output, Figure 4			6	
Channel-to-Channel Skew	t_{SKEW}	Each translator equally loaded, MAX13003E/MAX13004E/MAX13005E			±5	ns
		Each translator equally loaded, MAX13000E/MAX13001E/MAX13002E			±250	
Part-to-Part Skew (Note 6)	t_{PPSKEW}	$C_{I/OVL}$ = 15pF, $C_{I/OVCC}$ = 15pF, V_L = +1.8V, V_{CC} = +2V, ΔT = +5°C, MAX13003E/MAX13004E/MAX13005E			10	ns
Maximum Data Rate		MAX13003E/MAX13004E/MAX13005E V_{CC} > +1.65V, $C_{I/OVL}$ = 50pF, $C_{I/OVCC}$ = 50pF	20			Mbps
		MAX13000E/MAX13001E/MAX13002E $C_{I/OVL}$ = 50pF, $C_{I/OVCC}$ = 50pF	230			kbps

Note 1: All devices are 100% production tested at T_A = +25°C. Limits are guaranteed by design over the entire temperature range.
Note 2: V_L must be less than or equal to V_{CC} during normal operation. However, V_L can be greater than V_{CC} during startup and shutdown conditions.
Note 3: This consumption is referred to as no signal transmission.
Note 4: Guaranteed by design with an input signal full swing, rise/fall time ≤ 3ns, source resistance is 50Ω.
Note 5: Enable input signal full swing and rise/fall time ≤ 50ns.
Note 6: Guaranteed by design, not production tested.

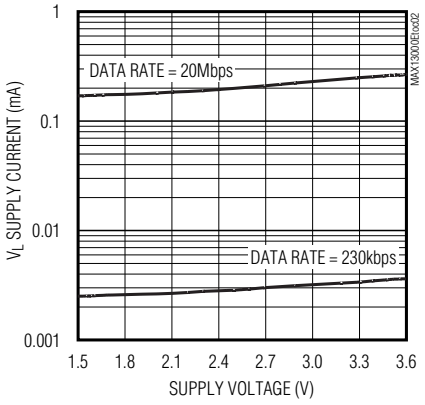
Typical Operating Characteristics

(V_{CC} = +3.3V, V_L = +0.9V, T_A = +25°C, MAX13003E.)

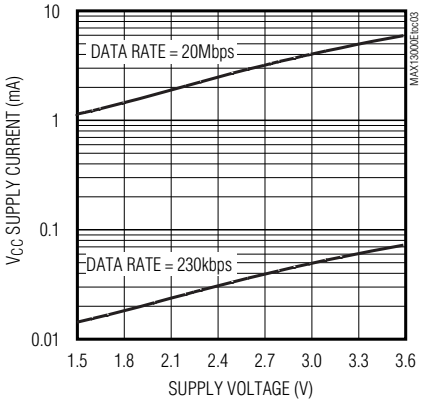
V_L SUPPLY CURRENT vs. SUPPLY VOLTAGE (DRIVING I/O V_L, V_L = 0.9V)



V_L SUPPLY CURRENT vs. SUPPLY VOLTAGE (DRIVING I/O V_{CC}, V_L = 0.9V)



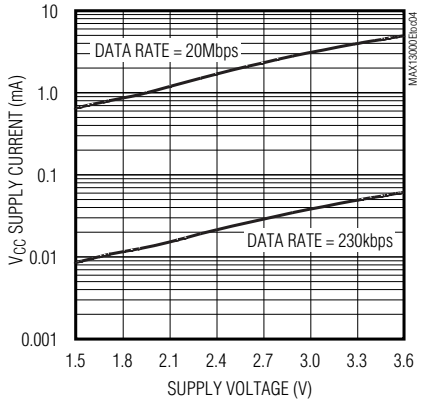
V_{CC} SUPPLY CURRENT vs. SUPPLY VOLTAGE (DRIVING I/O V_L, V_L = 0.9V)



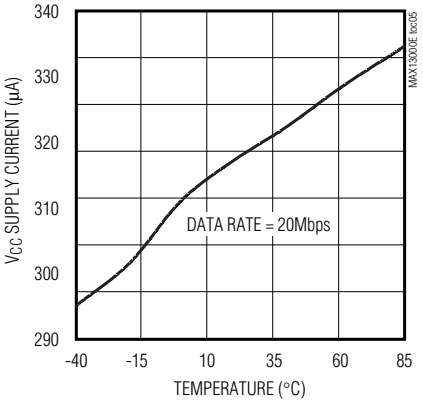
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, V_L = +0.9V, T_A = +25°C, MAX13003E.)

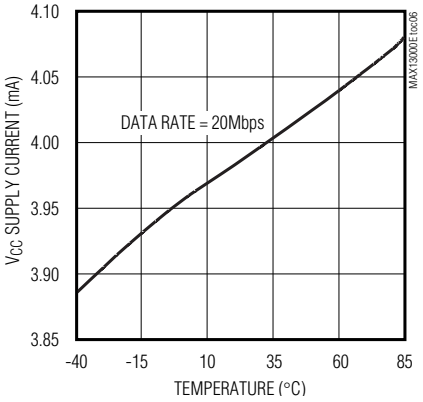
V_{CC} SUPPLY CURRENT vs. SUPPLY VOLTAGE (DRIVING I/OV_{CC}, V_L = +0.9V)



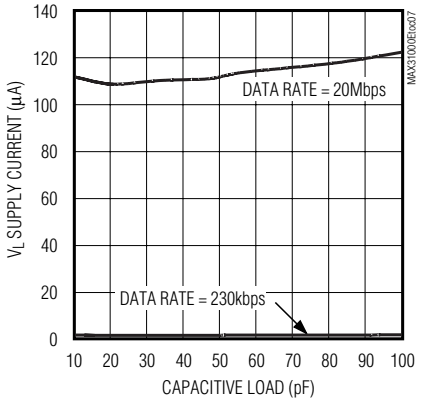
V_L SUPPLY CURRENT vs. TEMPERATURE (DRIVING I/OV_{CC}, V_{CC} = +3.3V, V_L = +0.9V)



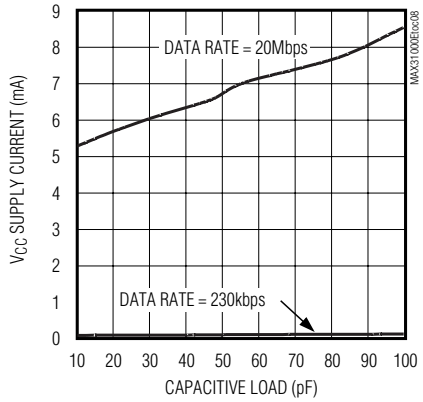
V_{CC} SUPPLY CURRENT vs. TEMPERATURE (DRIVING I/OV_{CC}, V_{CC} = +3.3V, V_L = +0.9V)



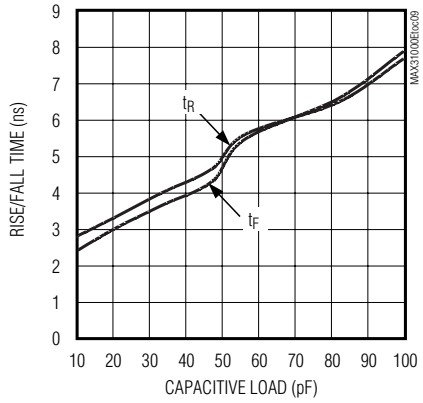
V_L SUPPLY CURRENT vs. CAPACITIVE LOAD ON I/O V_{CC} (DRIVING I/OV_L, V_{CC} = 3.3V, V_L = +0.9V)



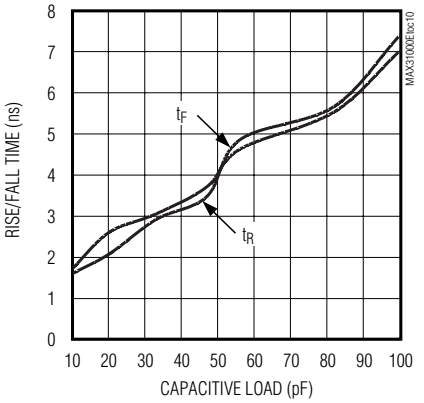
V_{CC} SUPPLY CURRENT vs. CAPACITIVE LOAD ON I/O V_{CC} (DRIVING I/OV_L, V_{CC} = 3.3V, V_L = +0.9V)



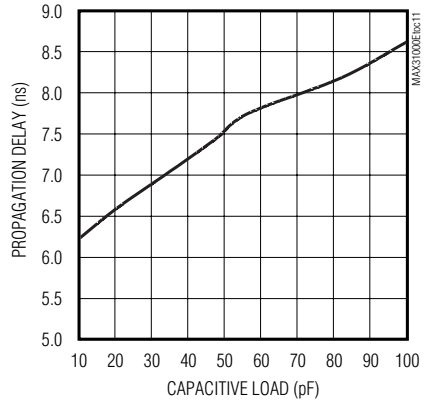
RISE/FALL TIME vs. CAPACITIVE LOAD ON I/O V_{CC} (DRIVING I/OV_L, V_{CC} = 3.3V, V_L = +0.9V)



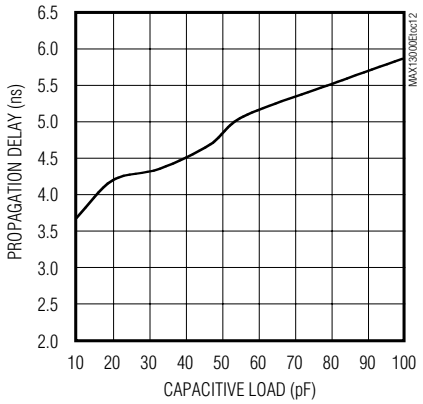
RISE/FALL TIME vs. CAPACITIVE LOAD ON I/O V_L (DRIVING I/OV_{CC}, = 3.3V, V_L = +0.9V)



PROPAGATION DELAY vs. CAPACITIVE LOAD ON I/O V_{CC} (DRIVING I/OV_L, V_{CC}, = 3.3V, V_L = +0.9V)



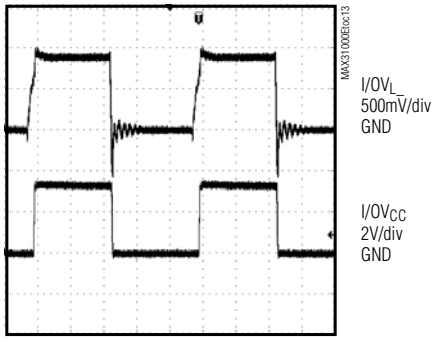
PROPAGATION DELAY vs. CAPACITIVE LOAD ON I/O V_L (DRIVING I/OV_{CC}, V_{CC} = 3.3V, V_L = +0.9V)



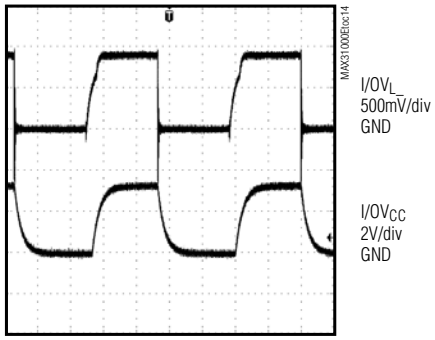
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, V_L = +0.9V, T_A = +25°C, MAX13003E.)

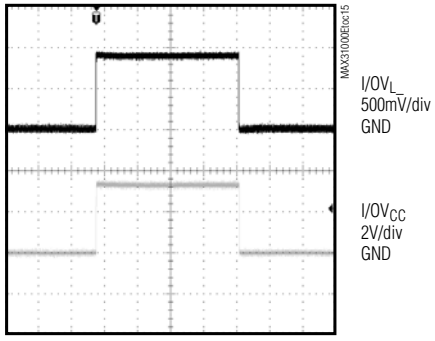
OD RAIL-TO-RAIL DRIVING (MAX13005E)
(DRIVING I/OV_L, V_{CC} = +3.3V, V_L = +0.9V, $C_{I/OVCC}$ = 56pF, DATA RATE = 230Mbps, R_{PULLUP} = 1kΩ)



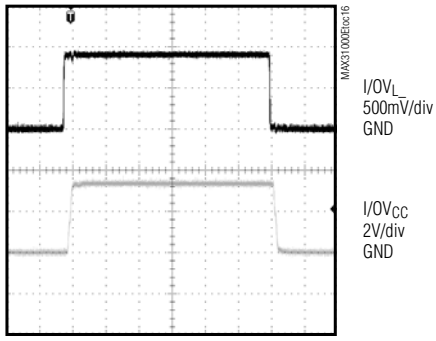
OD RAIL-TO-RAIL DRIVING (MAX13002E)
(DRIVING I/OV_L, V_{CC} = +3.3V, V_L = +0.9V, $C_{I/OVCC}$ = 56pF, DATA RATE = 230kbps, R_{PULLUP} = 15kΩ)



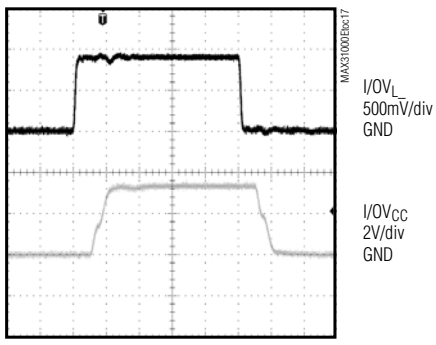
RAIL-TO-RAIL DRIVING
(DRIVING I/OV_L, V_{CC} = +3.3V, V_L = +0.9V, $C_{I/OVCC}$ = 50pF, DATA RATE = 230kbps)



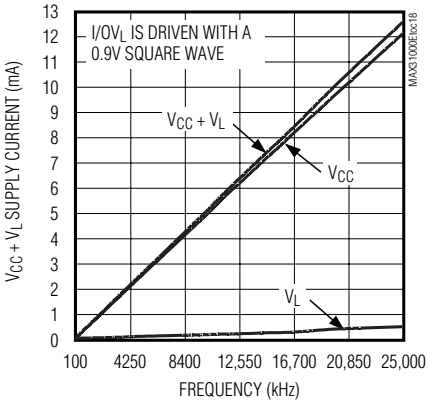
RAIL-TO-RAIL DRIVING
(DRIVING I/OV_L V_{CC} = +3.3V, V_L = +0.9V, $C_{I/OVCC}$ = 50pF, DATA RATE = 4Mbps)



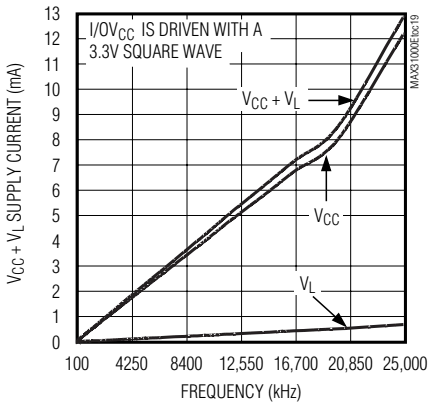
RAIL-TO-RAIL DRIVING
(DRIVING I/OV_L, V_{CC} = +3.3V, V_L = +0.9V, $C_{I/OVCC}$ = 50pF, DATA RATE = 20Mbps)



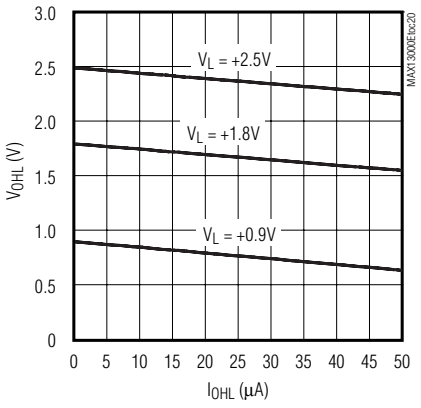
V_{CC} + V_L SUPPLY CURRENT vs. FREQUENCY
(DRIVING I/OV_L, V_{CC} = +3.3V, V_L = +0.9V)



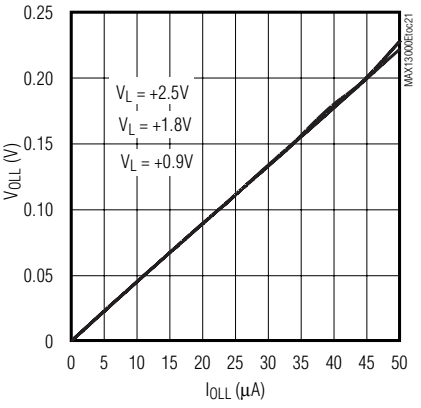
V_{CC} + V_L SUPPLY CURRENT vs. FREQUENCY
(DRIVING I/OV_{CC}, V_{CC} = +3.3V, V_L = +0.9V)



V_{OHL} vs. I_{OHL} FOR V_L SIDE
(V_{CC} = 3.3V)

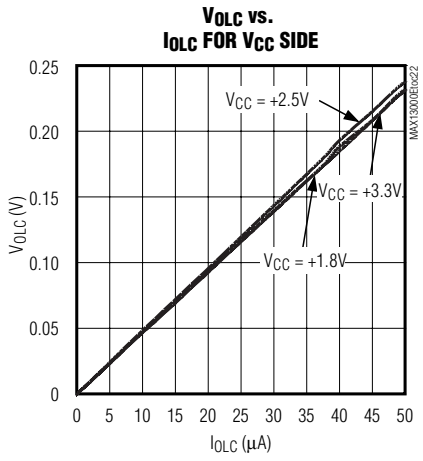


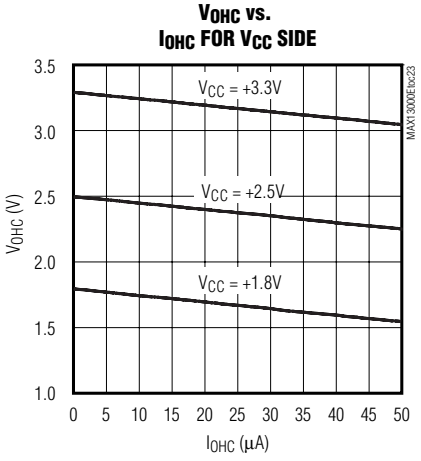
V_{OLL} vs. I_{OLL} FOR V_L SIDE
(V_{CC} = 3.3V)



Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, V_L = +0.9V, T_A = +25°C, MAX13003E.)





Pin Descriptions

MAX13000E/MAX13003E

PIN		NAME	FUNCTION
TSSOP	UCSP		
1	B1	I/OV_L1	CMOS Input/Output 1, Referenced to V_L
2	B2	I/OV_L2	CMOS Input/Output 2, Referenced to V_L
3	A1	I/OV_L3	CMOS Input/Output 3, Referenced to V_L
4	A2	V_L	Logic Input Voltage, +0.9V ≤ V_L ≤ V_{CC}. Bypass V_L to GND with a 0.1µF capacitor.
5	A3	EN	Enable Input. When EN is pulled low, I/O V_{CC}1 to I/O V_{CC}6 and I/O V_L1 to I/O V_L6 are tri-stated. Drive EN high (V_L) for normal operation.
6	A4	I/OV_L4	CMOS Input/Output 4, Referenced to V_L
7	B3	I/OV_L5	CMOS Input/Output 5, Referenced to V_L
8	B4	I/OV_L6	CMOS Input/Output 6, Referenced to V_L
9	C4	I/OV_{CC}6	CMOS Input/Output 6, Referenced to V_{CC}
10	C3	I/OV_{CC}5	CMOS Input/Output 5, Referenced to V_{CC}
11	D4	I/OV_{CC}4	CMOS Input/Output 4, Referenced to V_{CC}
12	D3	GND	Ground
13	D2	V_{CC}	V_{CC} Input Voltage, +1.5V ≤ V_{CC} ≤ 3.6V. Bypass V_{CC} to GND with a 0.1µF capacitor. For full ESD protection, use a 1µF bypass capacitor on V_{CC}.
14	D1	I/OV_{CC}3	CMOS Input/Output 3, Referenced to V_{CC}
15	C2	I/OV_{CC}2	CMOS Input/Output 2, Referenced to V_{CC}
16	C1	I/OV_{CC}1	CMOS Input/Output 1, Referenced to V_{CC}

Pin Descriptions (continued)

MAX13001E/MAX13004E

PIN		NAME	FUNCTION
TSSOP	UCSP		
1	B1	OV_L1	CMOS Output 1, Referenced to V_L
2	B2	OV_L2	CMOS Output 2, Referenced to V_L
3	A1	OV_L3	CMOS Output 3, Referenced to V_L
4	A2	V_L	Logic Input Voltage, $+0.9V \le V_L \le V_{CC}$. Bypass V_L to GND with a 0.1µF capacitor.
5	A3	EN	Enable Input. When EN is pulled low, $OV_{CC}1$ to $OV_{CC}6$ and IV_L1 to IV_L6 are tri-stated. Drive EN high (V_L) for normal operation.
6	A4	OV_L4	CMOS Output 4, Referenced to V_L
7	B3	OV_L5	CMOS Output 5, Referenced to V_L
8	B4	OV_L6	CMOS Output 6, Referenced to V_L
9	C4	$IV_{CC}6$	Open-Drain-Compatible Input 6, Reference to V_{CC}
10	C3	$IV_{CC}5$	Open-Drain-Compatible Input 5, Referenced to V_{CC}
11	D4	$IV_{CC}4$	Open-Drain-Compatible Input 4, Referenced to V_{CC}
12	D3	GND	Ground
13	D2	V_{CC}	V_{CC} Input Voltage, $+1.5V \le V_{CC} \le 3.6V$. Bypass V_{CC} to GND with a 0.1µF capacitor. For full ESD protection, use a 1µF bypass capacitor on V_{CC}.
14	D1	$IV_{CC}3$	Open-Drain-Compatible Input 3, Referenced to V_{CC}
15	C2	$IV_{CC}2$	Open-Drain-Compatible Input 2, Referenced to V_{CC}
16	C1	$IV_{CC}1$	Open-Drain-Compatible Input 1, Referenced to V_{CC}

Pin Descriptions (continued)

MAX13002E/MAX13005E

PIN		NAME	FUNCTION
TSSOP	UCSP		
1	B1	IV_L1	Open-Drain-Compatible Input 1, Referenced to V_L
2	B2	IV_L2	Open-Drain-Compatible Input 2, Referenced to V_L
3	A1	IV_L3	Open-Drain-Compatible Input 3, Referenced to V_L
4	A2	V_L	Logic Input Voltage, $+0.9V \le V_L \le V_{CC}$. Bypass V_L to GND with a 0.1µF capacitor.
5	A3	EN	Enable Input. When EN is pulled low, $OV_{CC}1$ to $OV_{CC}6$ and IV_L1 to IV_L6 are tri-stated. Drive EN high (V_L) for normal operation.
6	A4	IV_L4	Open-Drain-Compatible Input 4, Referenced to V_L
7	B3	IV_L5	Open-Drain-Compatible Input 5, Referenced to V_L
8	B4	IV_L6	Open-Drain-Compatible Input 6, Referenced to V_L
9	C4	$OV_{CC}6$	CMOS Output 6, Referenced to V_{CC}
10	C3	$OV_{CC}5$	CMOS Output 5, Referenced to V_{CC}
11	D4	$OV_{CC}4$	CMOS Output 4, Referenced to V_{CC}
12	D3	GND	Ground
13	D2	V_{CC}	V_{CC} Input Voltage, $+1.5V \le V_{CC} \le 3.6V$. Bypass V_{CC} to GND with a 0.1µF capacitor. For full ESD protection, use a 1µF bypass capacitor on V_{CC}.
14	D1	$OV_{CC}3$	CMOS Output 3, Referenced to V_{CC}
15	C2	$OV_{CC}2$	CMOS Output 2, Referenced to V_{CC}
16	C1	$OV_{CC}1$	CMOS Output 1, Referenced to V_{CC}

Test Circuits/Timing Diagrams

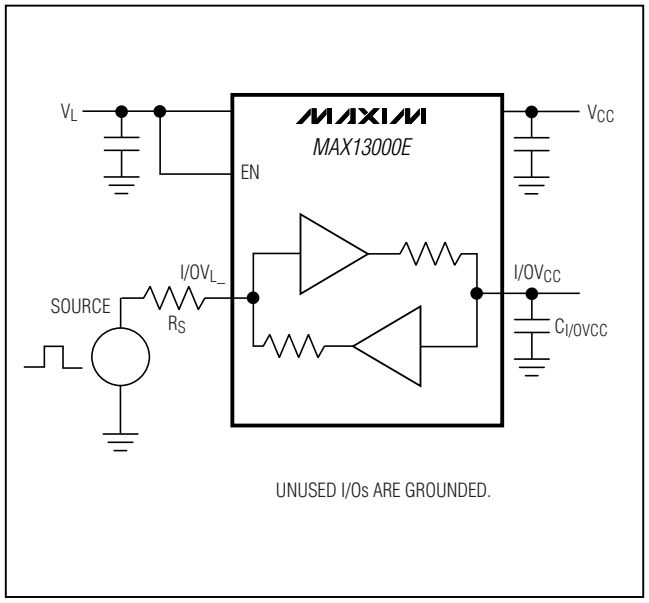


Figure 1a. Driving I/OVL

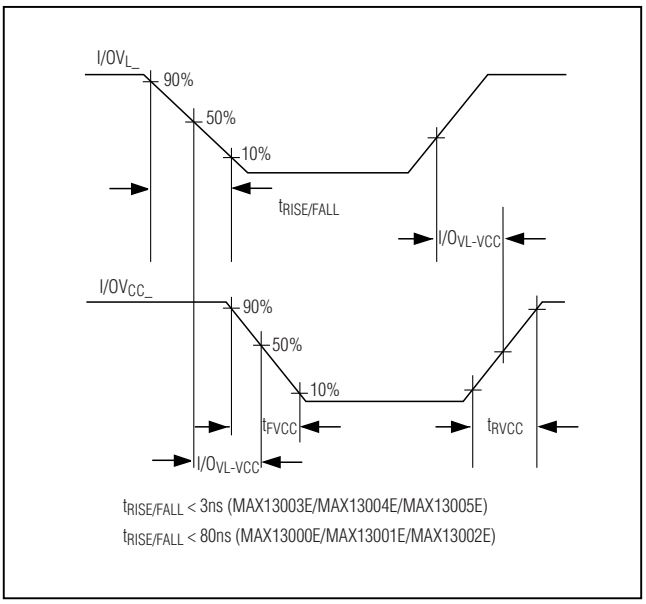


Figure 1b. Timing for Driving I/OV_L

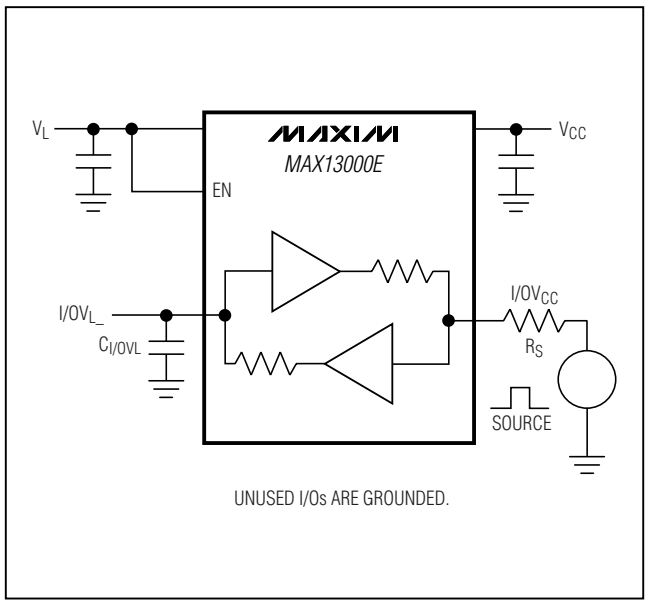


Figure 2a. Driving I/OV_{CC}

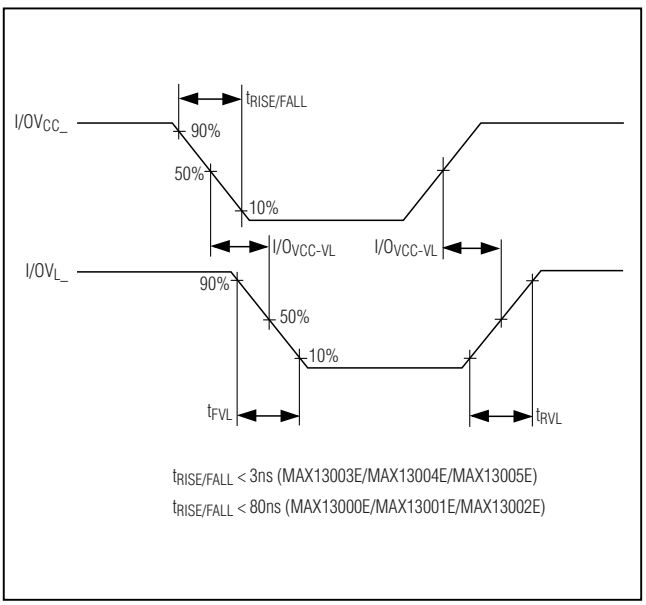


Figure 2b. Timing for Driving I/OV_{CC}

Test Circuits/Timing Diagrams (continued)

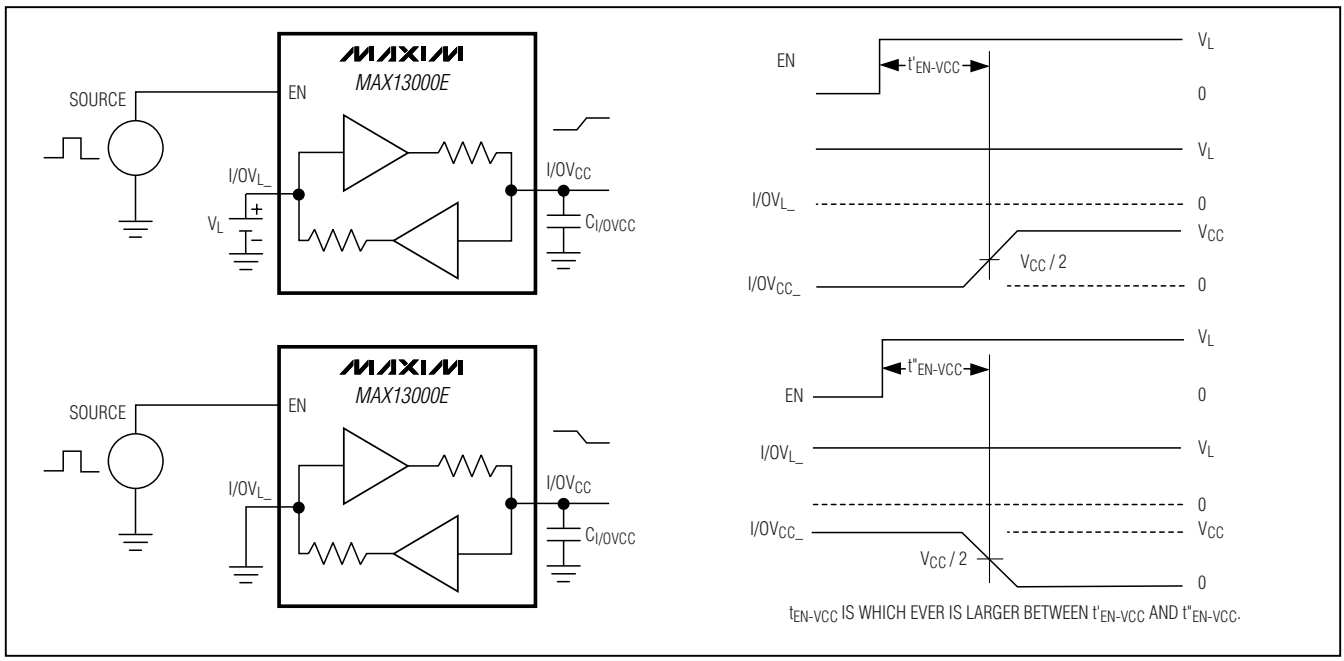


Figure 3. Propagation Delay from I/OV$_L$ to I/OV$_{CC}$ After EN

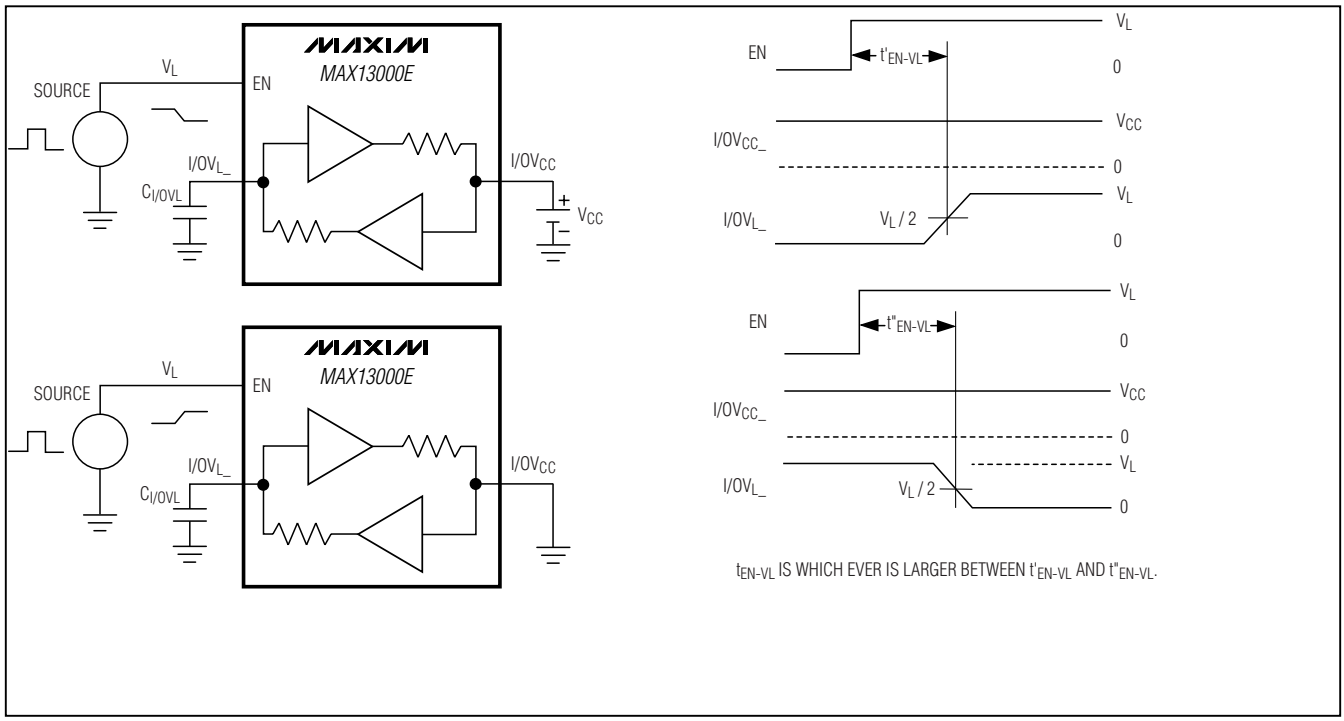


Figure 4. Propagation Delay from I/OV$_{CC}$ to I/OV$_L$ After EN

Detailed Description

The MAX13000E–MAX13005E logic-level translators provide the level shifting necessary to allow data transfer in multivoltage systems. Externally applied voltages, V_{CC} and V_L, set the logic levels on each side of the device. Logic signals present on the V_L side of the device appear as higher voltage logic signals on the V_{CC} side of the device, and vice-versa.

The MAX13000E/MAX13003E are bidirectional level translators allowing data translation in either direction ($V_L \leftrightarrow V_{CC}$) on any single data line without the use of a DIRECTION input. The MAX13001E/MAX13002E/MAX13004E/MAX13005E unidirectional level translators level shift data in one direction ($V_L \rightarrow V_{CC}$ or $V_{CC} \rightarrow V_L$) on any single data line. The MAX13001E/MAX13002E/MAX13004E/MAX13005E unidirectional translators' inputs have the capability to interface with both CMOS and open-drain (OD) outputs. For more information, see the *Ordering Information* section and the *Input Driver Requirements* section.

The MAX13000E–MAX13005E accept V_L from +0.9V to +3.6V. All devices have V_{CC} ranging from +1.5V to +3.6V, making them ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems.

The MAX13000E–MAX13005E feature low V_{CC} quiescent supply current of less than 4µA, and V_L quiescent supply current of less than 2µA when in shutdown. The MAX13000E–MAX13005E have ±15kV ESD protection on the V_{CC} side for greater protection in applications that route signals externally. The ESD protection is specified using the Human Body Model (HBM).The MAX13000E/MAX13001E/MAX13002E operate at a guaranteed 230kbps data rate. The MAX13003E/MAX13004E/MAX13005E operate at a guaranteed 20Mbps data rate when V_{CC} > +1.65V.

Level Translation

For normal operation, ensure that $+1.5V \le V_{CC} \le +3.6V$, and $+0.9V \le V_L \le V_{CC}$. During power-up sequencing, $V_L \ge V_{CC}$ does not damage the device whenever V_L is within the absolute maximum ratings (see the *Absolute Maximum Ratings* section). During power-supply sequencing, when V_{CC} is floating and V_L is powered up, 1mA of current can be sourced to each load on the V_L side, yet the device does not latch up.

The MAX13000E–MAX13005E are designed to have $V_{CC} \ge V_L$ at all times; however, if V_{CC} is turned off, the part will not be damaged and will not latch up. To prevent excessive leakage currents in either the I/O or supply lines, the I/O on the V_L side must be left in the high state.

The maximum data rate for the MAX13000E–MAX13005E depends heavily on the load capacitance (see the *Typical Operating Characteristics*), output impedance of the driver, and the operational voltage range (see the *Timing Characteristics* table).

Open-Drain Operation

The MAX13001E/MAX13002E/MAX13004E/MAX13005E have input stages specifically designed to accommodate external open-drain drivers. When using open-drain drivers, the MAX13001E/MAX13002E/MAX13004E/MAX13005E operate in a unidirectional-only mode, translating from the OD side to the CMOS side. For improved performance, the rise- and fall-time accelerators are present on both the CMOS and the OD side. See the *Input-Driver Requirement* section. Do not use pullup resistors greater than 15kΩ for proper operation, and smaller pullup resistance may be needed for higher speed operation.

Input-Driver Requirements

The MAX13000E–MAX13005E feature four different architectures based on the speed of the part, as well as on whether the translator is a CMOS-to-CMOS translator, or whether it is an OD-to-CMOS translator.

20Mbps CMOS-to-CMOS Bidirectional Translator (MAX13003E)

The MAX13003E architecture is based on a one-shot accelerator output stage (Figure 5). Accelerator output stages are always in tri-state, except when there is a transition on any of the translators on the input side, either I/OV_L or I/OV_{CC}. A short pulse is generated during which the one-shot output stage becomes active and charges/discharges the capacitances at the I/Os. Due to its bidirectional nature, the accelerator stages on both the I/OV_{CC} and the I/OV_L become active during an I/O transition from low to high or high to low. This can lead to some current feeding into the external source that is driving the translator. However, this behavior helps speed up the transition on the driven side.

The type of devices that drive the inputs of the MAX13003E is usually specified with an output drive-current capability (I_{OUT}). When driving the inputs of the MAX13003E, the maximum achievable speed is constrained by the drive current of the external driver. To insure the maximum possible throughput of 20Mbps, the external driver should meet the following requirement:

$$I_{OUT} \ge 1.67 \times 10^8 \times V \times (C_{IN} + C_P)$$

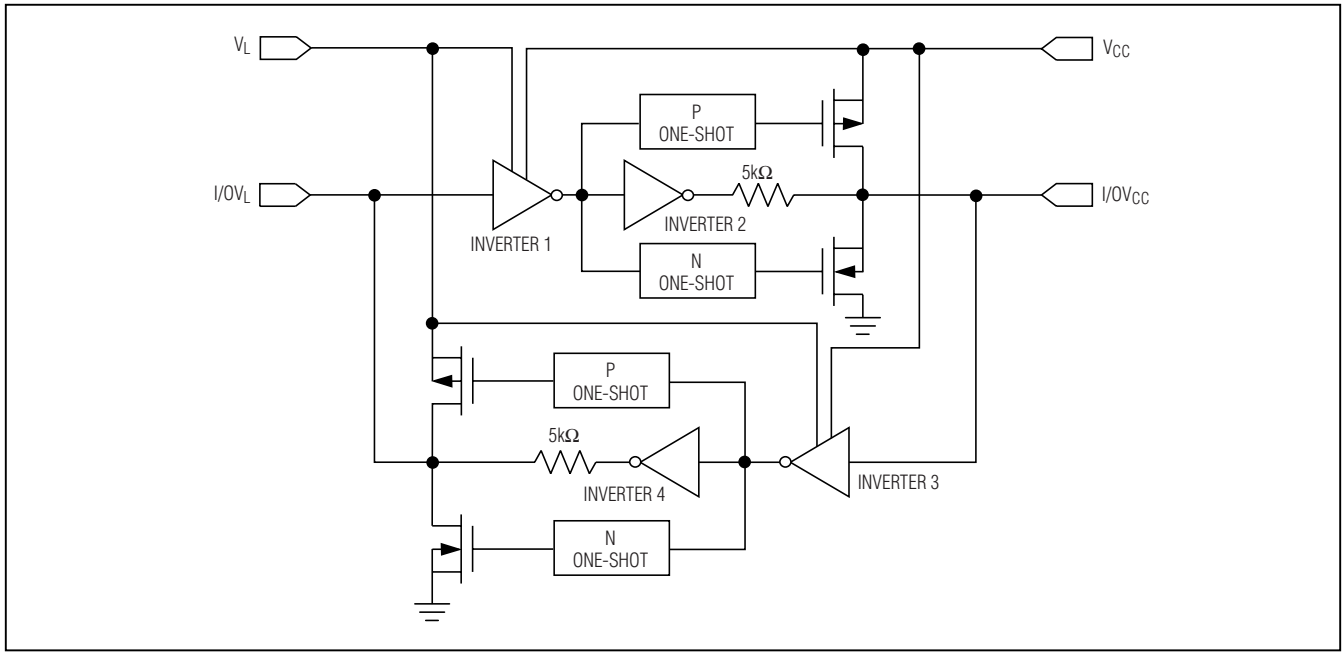


Figure 5. Architecture of 20Mbps, CMOS-to-CMOS Bidirectional Translators

where, C_P is the parasitic capacitance of the traces, V is the supply voltage of the driven side (i.e., V_L or V_{CC}), and C_{IN} is the input capacitance of the driven side (C_{IN} = 10pF for V_L side, C_{IN} = 20pF for V_{CC} side).

20Mbps OD-to-CMOS Unidirectional Translators (MAX13004E/MAX13005E)

The MAX13004E/MAX13005E architecture is virtually the same as that for the bidirectional CMOS-to-CMOS translators, the only difference being that the output inverter (inverter 4) at the driving side accommodates the driving capabilities of an open-drain output (Figure 6).

For proper operation, a pullup resistor needs to be connected from the open-drain output to the power supply of the driving side. Use pullup resistors no larger than 15kΩ.

230kbps CMOS-to-CMOS Bidirectional Translator (MAX13000E)

The architecture of the MAX13000E lacks the one-shot accelerator output stages since the transitions that this device handles are limited by its data rate, 230kbps (Figure 7).

For proper operation, the driver must meet the following conditions: 1kΩ maximum output impedance and 1mA minimum output current.

230kbps OD-to-CMOS Unidirectional Translators (MAX13001E/MAX13002E)

The architecture of the MAX13001E/MAX13002E is similar to that of the 230kbps CMOS-to-CMOS part, with the difference that it accommodates the driving capability of an open-drain output on the driving side, and also that it has only a single one-shot output stage (Figure 8).

For proper operation, a pullup resistor needs to be connected from the open-drain output to the power supply of the driving side. Use pullup resistors no larger than 15kΩ.

Figure 9 shows a graph of the typical input current versus input voltage for all of the above configurations.

Enable Output Mode (EN)

The MAX13000E–MAX13005E feature an enable (EN) input. Drive EN low to set the MAX13000E–MAX13005E I/Os in tri-state mode. Drive EN high (V_L) for normal operation.

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The I/OV_{CC} lines have extra protection against static discharge. Maxim's engineers have developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD

Ultra-Low-Voltage Level Translators

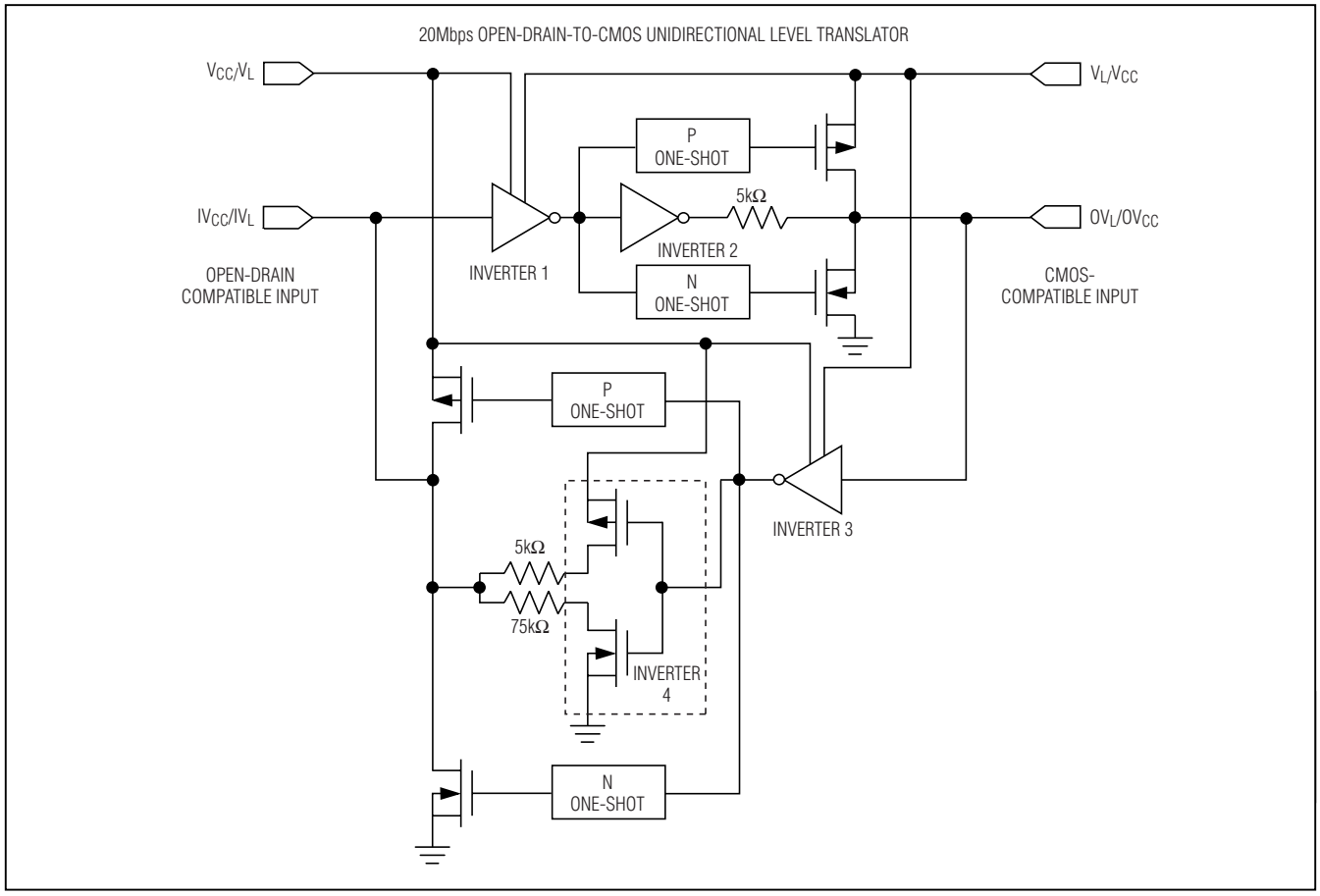


Figure 6. Architecture of 20Mbps, OD-to-CMOS Unidirectional Translators

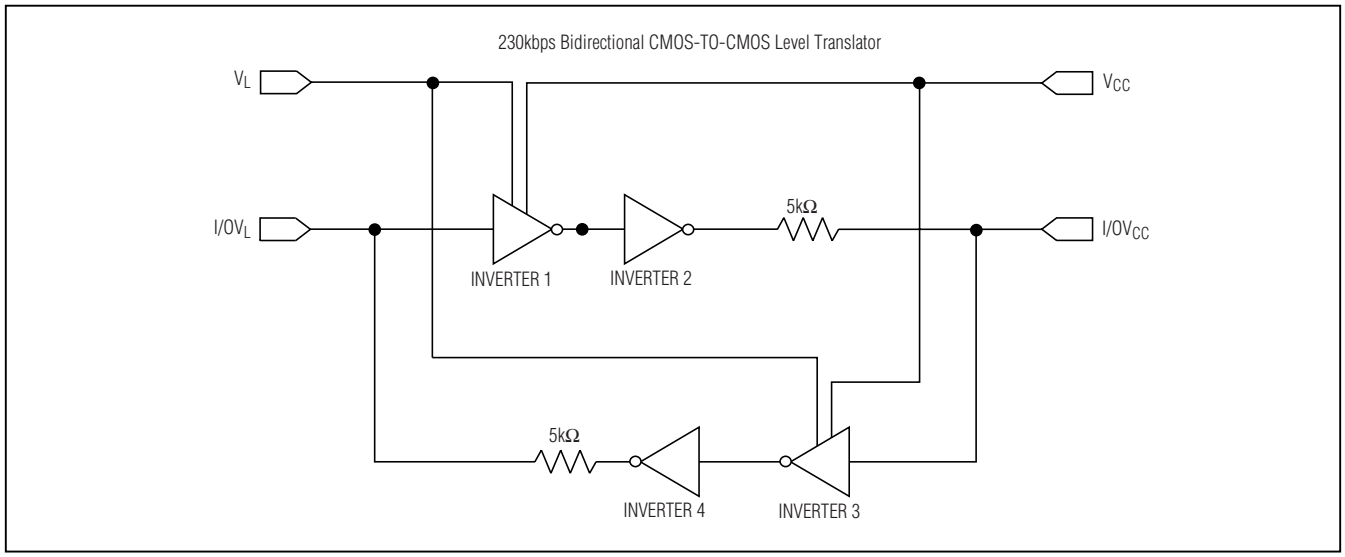


Figure 7. Architecture of 230kbps, CMOS-to-CMOS Bidirectional Translator

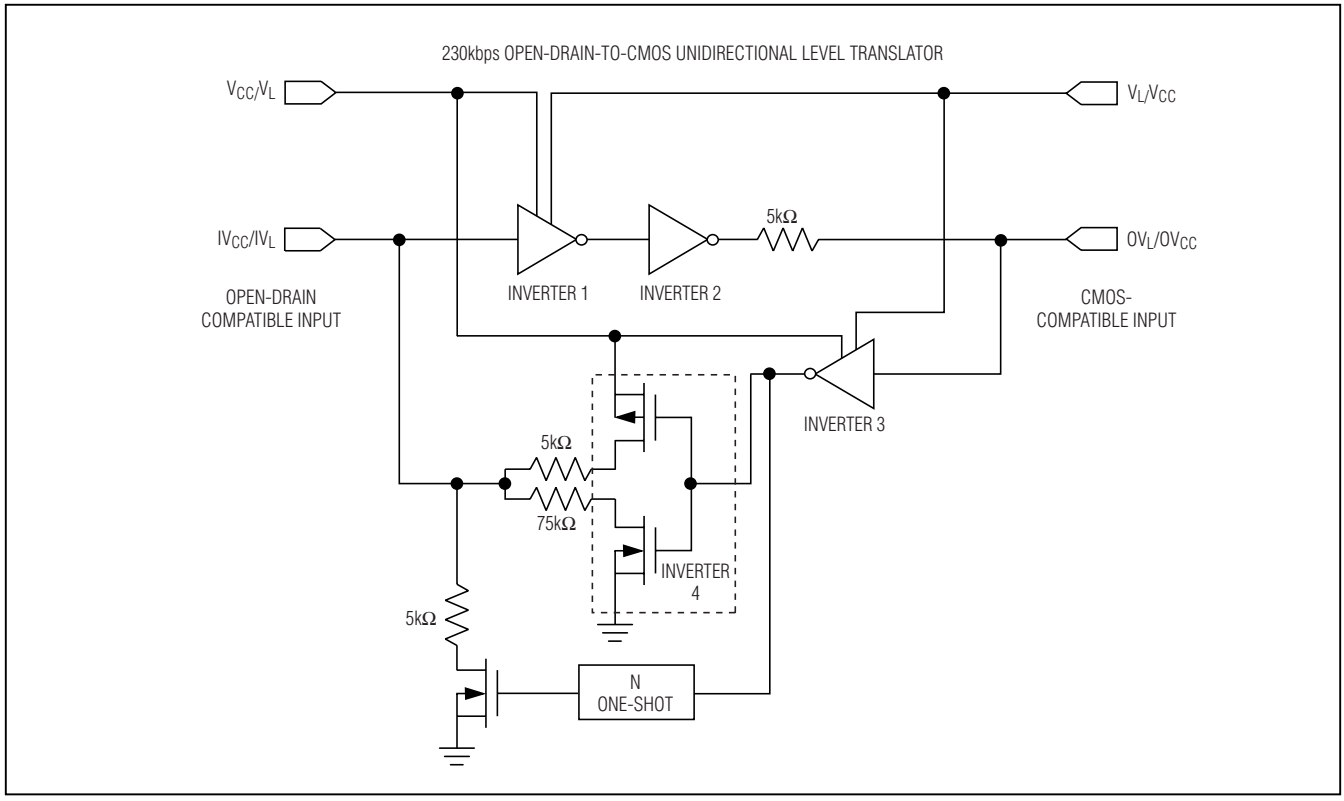


Figure 8. Architecture of 230kbps, OD-to-CMOS Unidirectional Translator

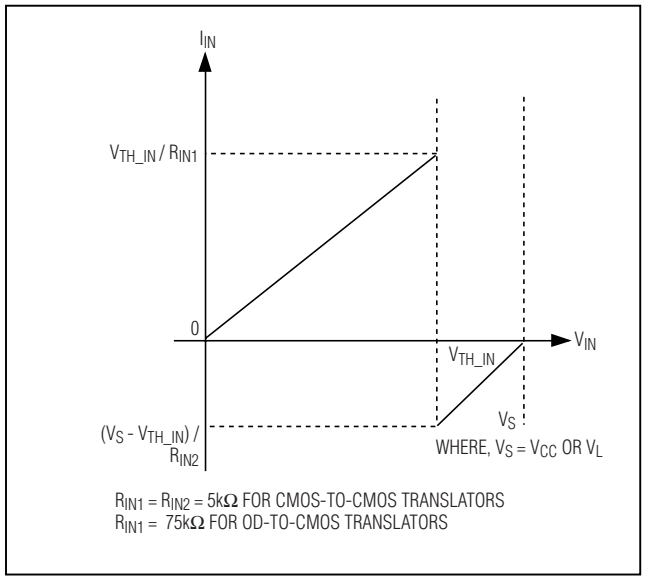


Figure 9. Typical I_{IN} vs. V_{IN}

structures withstand high ESD in all states: normal operation, tri-state output mode, and power-down. After an ESD event, Maxim's E-versions keep working without latchup, whereas competing products can latch and must be powered-down to remove latchup.

ESD protection can be tested in various ways. The I/OV_{CC} lines of the MAX13000E–MAX13005E are characterized for protection to ±15kV using the Human Body Model.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 10 shows the Human Body Model and Figure 11 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

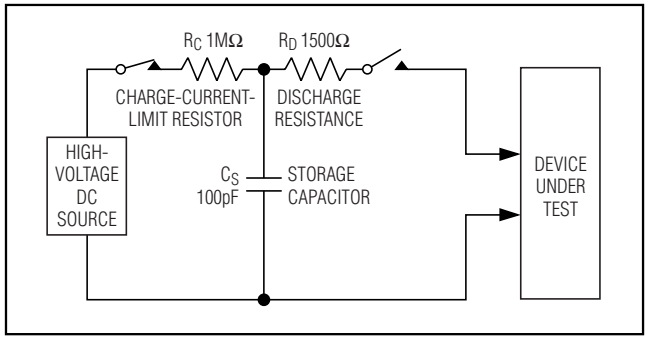


Figure 10. Human Body ESD Test Model

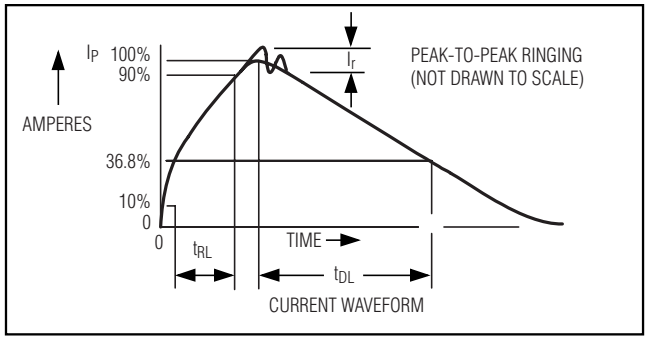


Figure 11. Human Body Current Waveform

IEC 61000-4-2 Standard ESD Protection

The IEC 61000-4-2 standard (Figure 12) specifies ESD tolerance for electronic systems. The IEC61000-4-2 model specifies a 150pF capacitor that is discharged into the device through a 330Ω resistor. The MAX13000E–MAX13005E's I/O on the V_{CC} side are rated for IEC 61000-4-2 standard, (8kV Contact Discharge and ±10kV Air-Gap Discharge).

The IEC 61000-4-2 model discharges higher peak current and more energy than the HBM due to the lower series resistance and larger capacitor.

Applications Information

Power-Supply Decoupling

To reduce ripple and the chance of transmitting incorrect data, bypass V_L and V_{CC} to ground with a 0.1µF capacitor. To ensure full ±15kV ESD protection, bypass V_{CC} to ground with a 1µF capacitor. Place all capacitors as close to the power-supply inputs as possible.

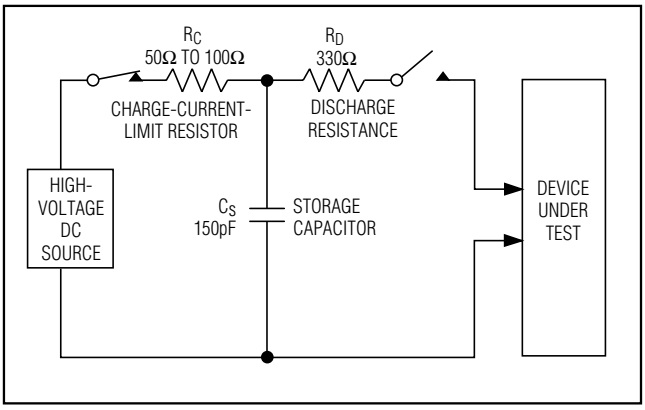


Figure 12. IEC 61000-4-2 Contact Discharge Test Model

UCSP Package Considerations

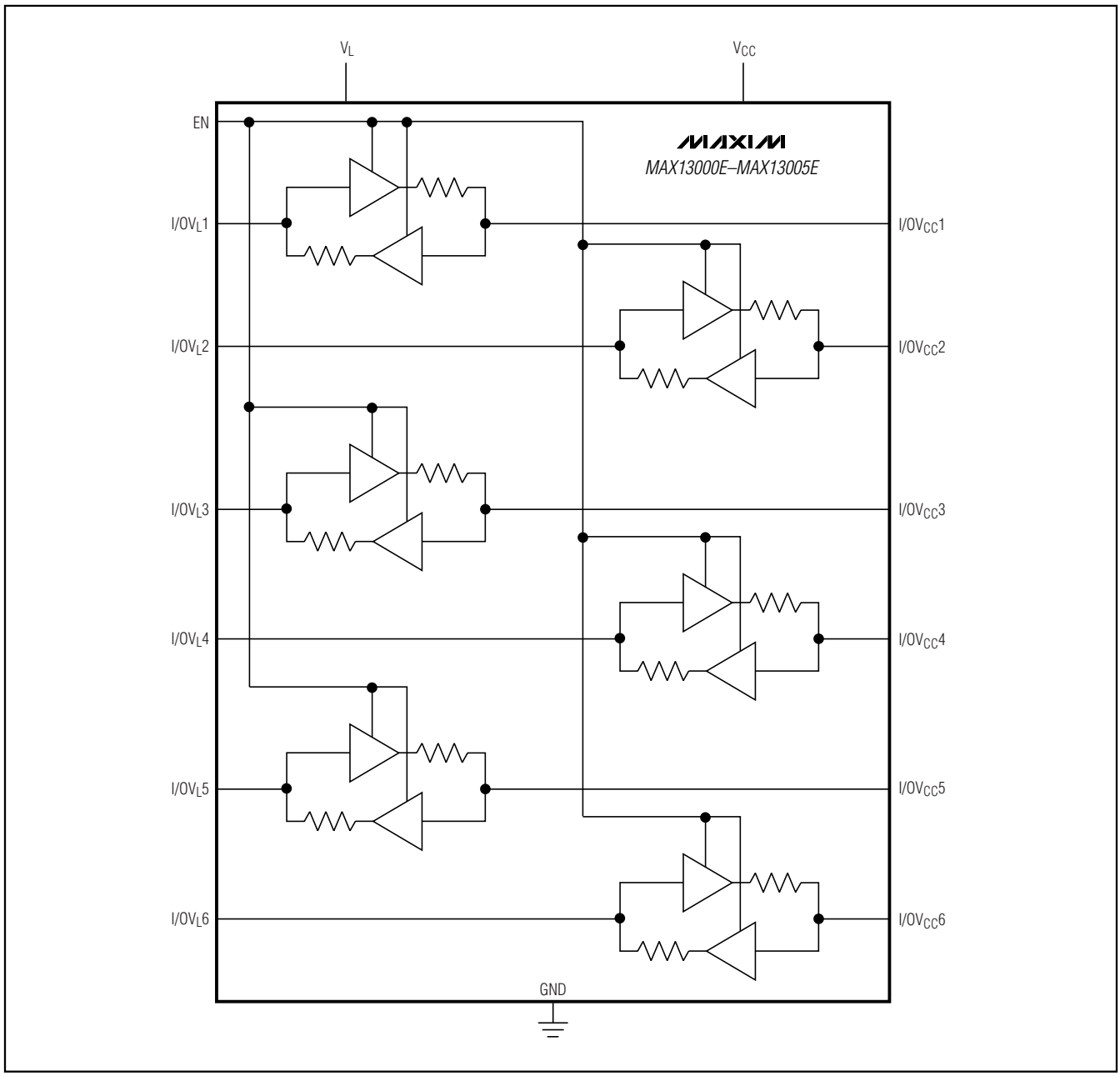
For general UCSP package information and PC layout considerations, please refer to Maxim application note: Wafer-Level Chip-Scale Package.

UCSP Reliability

The chip-scale package (UCSP) represents a unique packaging form factor that may not perform equally to a packaged product through traditional mechanical reliability tests. UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and usage environment. The user should closely review these areas when considering use of a UCSP package. Performance through Operating Life Test and Moisture Resistance remains uncompromised as it is primarily determined by the wafer-fabrication process.

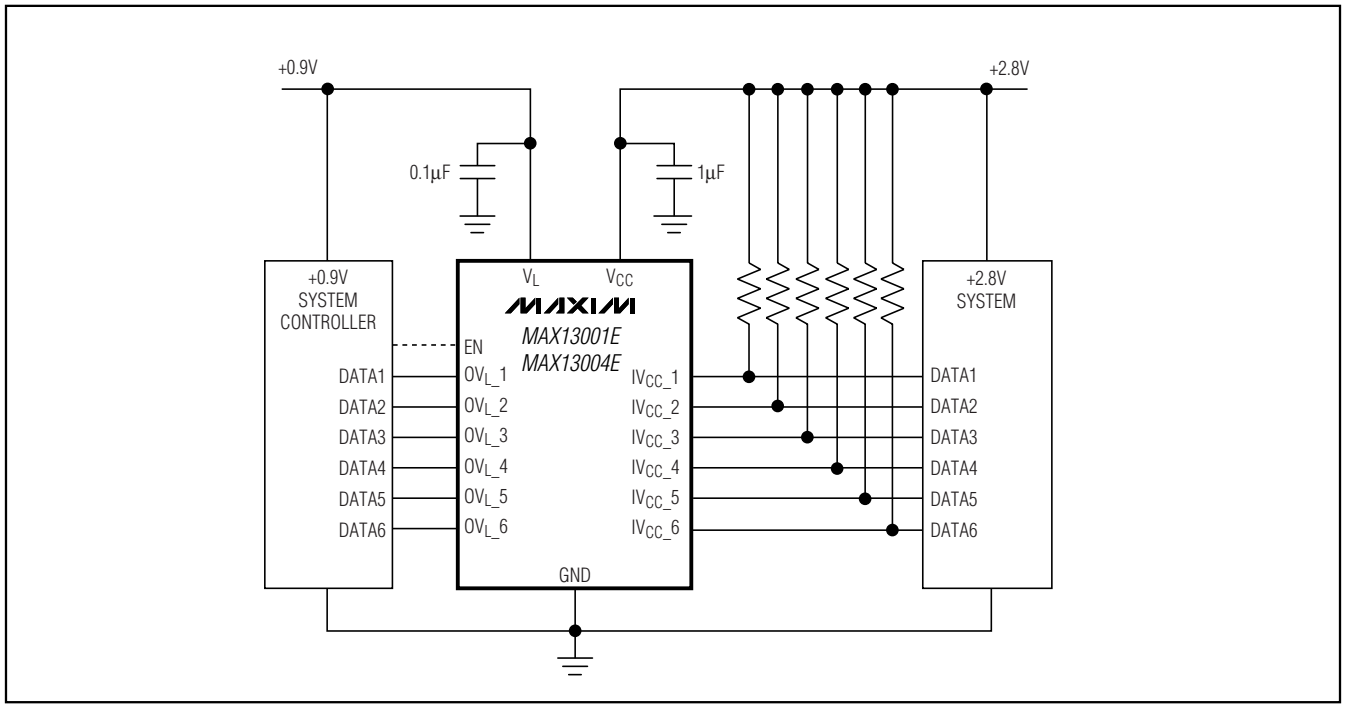
Mechanical stress performance is a greater consideration for a UCSP package. UCSPs are attached through direct solder contact to the user's PC board, foregoing the inherent stress relief of a packaged product lead frame. Solder joint contact integrity must be considered. Information on Maxim's qualification plan, test data, and recommendations are detailed in the UCSP application note, which can be found on Maxim's website at www.maxim-ic.com.

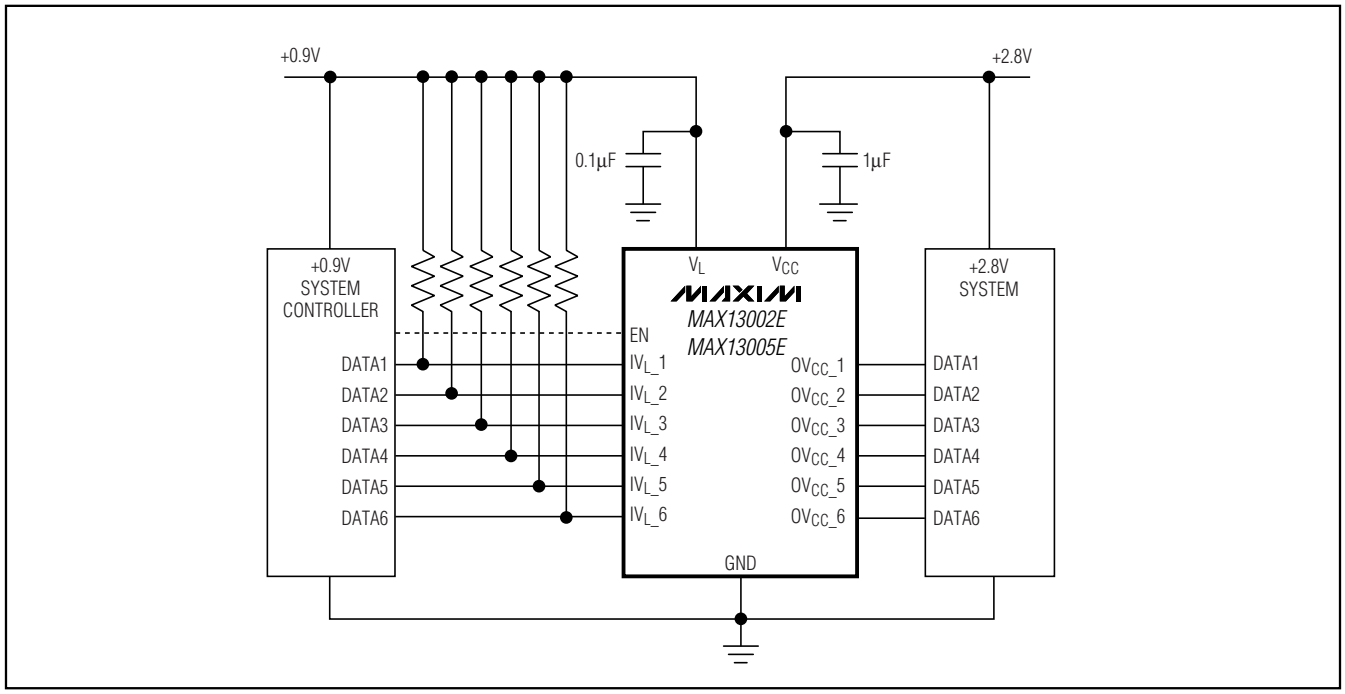
Functional Diagram



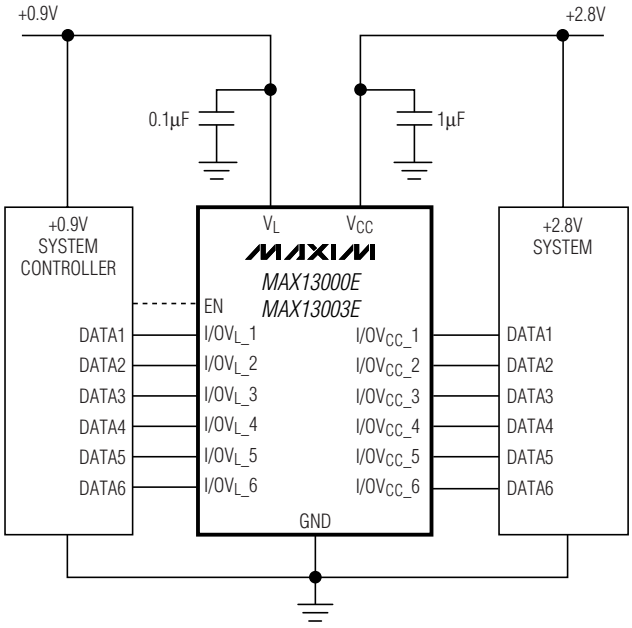
Ultra-Low-Voltage Level Translators

Typical Operating Circuits





Typical Operating Circuits (continued)



Selector Guide

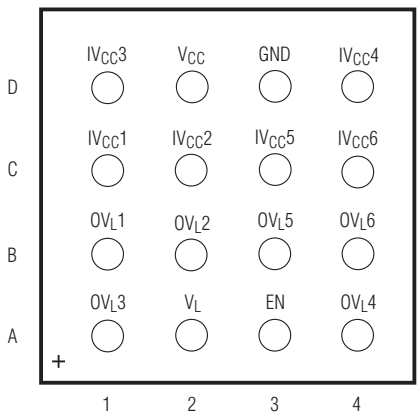
PART	DATA RATE (bps)	NUMBER OF BIDIRECTIONAL TRANSLATORS	NUMBER OF $V_L \rightarrow V_{CC}$ TRANSLATORS	NUMBER OF $V_{CC} \rightarrow V_L$ TRANSLATORS	TRANSLATOR CONFIGURATION
MAX13000E	230k	6	—	—	CMOS-to-CMOS
MAX13001E	230k	—	—	6	OD-to-CMOS
MAX13002E	230k	—	6	—	OD-to-CMOS
MAX13003E	20M	6	—	—	CMOS-to-CMOS
MAX13004E	20M	—	—	6	OD-to-CMOS
MAX13005E	20M	—	6	—	OD-to-CMOS

Ultra-Low-Voltage Level Translators

Pin Configurations (continued)

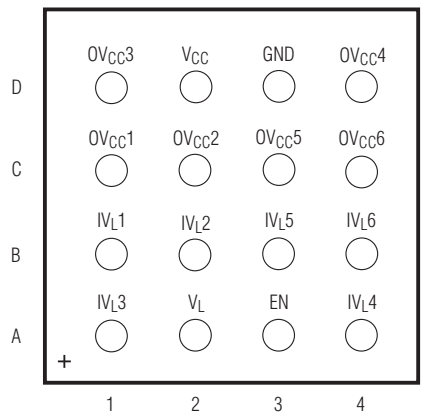
BOTTOM VIEW

MAX13001E/MAX13004E



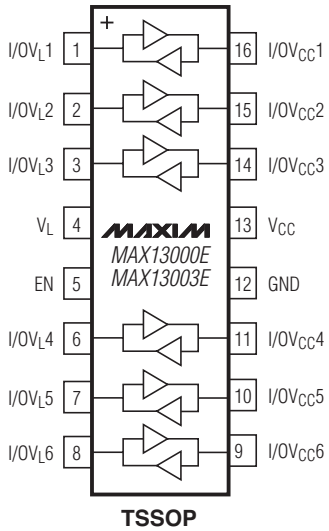
4 X 4 UCSP

MAX13002E/MAX13005E

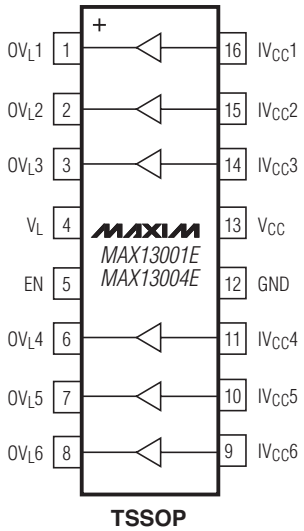


4 X 4 UCSP

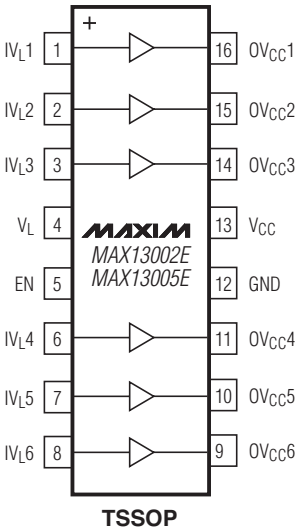
TOP VIEW



TSSOP



TSSOP



TSSOP

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX13000EEBE+T*	-40°C to +85°C	16 UCSP (4mm × 4mm)
MAX13001EEUE+	-40°C to +85°C	16 TSSOP
MAX13001EEBE+T*	-40°C to +85°C	16 UCSP (4mm × 4mm)
MAX13002EEUE+	-40°C to +85°C	16 TSSOP
MAX13002EEBE+T*	-40°C to +85°C	16 UCSP (4mm × 4mm)
MAX13003EEUE+	-40°C to +85°C	16 TSSOP
MAX13003EEBE+T*	-40°C to +85°C	16 UCSP (4mm × 4mm)
MAX13004EEUE+	-40°C to +85°C	16 TSSOP
MAX13004EEBE+T*	-40°C to +85°C	16 UCSP (4mm × 4mm)
MAX13005EEUE+	-40°C to +85°C	16 TSSOP
MAX13005EEBE+T*	-40°C to +85°C	16 UCSP (4mm × 4mm)

**Future Product—contact factory for availability.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
T =Tape and reel.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TSSOP	U16+2	**21-0066**	**90-0117**
16 UCSP	B16+1	**21-0101**	Refer to **Application Note 1891**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/05	Initial release	—
1	5/11	Added lead-free information to the *Ordering Information*	1, 23

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