具有关断保护和 ESD 保护功能的 TMUX154E 低电容双通道 2:1 开关

1 特性

- V_{CC} 工作电压为 3V 至 4.3V
- I/O 引脚可耐受电压高达 5.25V 的电压
- 兼容 1.8V 控制逻辑
- 支持关断保护，当 V_{CC} = 0V 时，I/O 引脚处于高阻抗状态
- R_{ON} = 10Ω（最大值）
- ΔR_{ON} = 0.35Ω（典型值）
- $C_{io(ON)}$ = 7.5pF（典型值）
- 低功耗（最大值为 1uA）
- –3dB 带宽 = 900MHz（典型值）
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范 (1)
- 静电放电 (ESD) 性能测试符合 JESD 22 标准
  - 8000V 人体放电模型（A114-B，II 类）
  - 1000V 充电器件模型 (C101)
- ESD 性能 I/O 端口接地 (2)
  - 15000V 人体放电模型

(1) $\overline{EN}$ 和 SEL 输入除外
(2) 除标准 HBM 测试（A114-B，II 类）外还执行了高压 HBM 测试，仅适用于进行接地测试的 I/O 端口。

2 应用

- 便携式电子产品
- 打印机和其他外设
- 电子销售终端
- 楼宇自动化
- 服务器

3 说明

TMUX154E 是一款高带宽 2:1 开关，专门针对限制 I/O 的应用中的 高速信号开关 进行设计。此开关具有较宽的带宽 (900MHz)，这一特性使得信号传递具有最少的边缘失真和相位失真。此开关为双向开关，高速信号衰减极少或者没有。它能实现低位间偏移和高通道间噪声隔离。

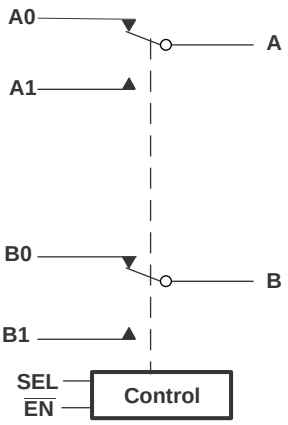
TMUX154E 在所有引脚上集成了 ESD 保护单元，采用微型 UQFN 封装 (1.8mm × 1.4mm) 或 VSSOP 封装，自然通风条件下的工作温度范围为 –40°C 至 85°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TMUX154E	VSSOP (10)	3.00mm × 3.00mm
	UQFN (10)	1.80mm x 1.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

功能方框图



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4 修订历史记录

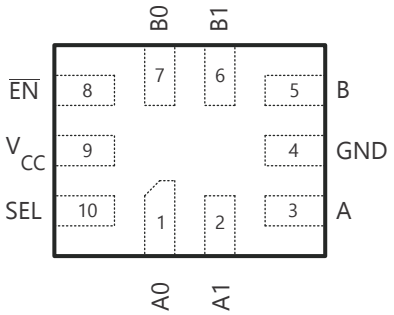
注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2018 年2 月	*	初始发行版。

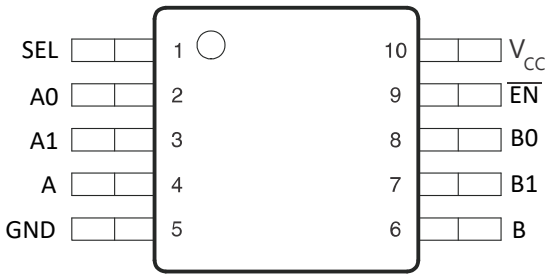
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5 Pin Configuration and Functions

RSW Package
10-PIN UQFN
Top View



DGS Package
10-PIN VSSOP
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	UQFN	VSSOP		
A0	1	2	I/O	signal path port 0
B0	7	8	I/O	
A	3	4	I/O	Common signal path
B	5	6	I/O	
A1	2	3	I/O	signal path port 1
B1	6	7	I/O	
$\overline{EN}$	8	9	I	EN = 0 Enable EN = 1 Disable
SEL	10	1	I	Select input: SEL = 0 A,B to A0,B0 SEL = 1 A,B to A1,B1
GND	4	5	—	Ground
VCC	9	10	—	Voltage supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (see (1) (2))

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_{SEL}, $V_{\overline{EN}}$	Control input voltage		–0.5	7	V
$V_{I/O}$	Signal path I/O voltage	V_{CC} > 0	–0.5	V_{CC} + 0.3	V
		V_{CC} = 0	–0.5	5.25	
I_{IK}	Control input clamp current	V_{IN} < 0		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O}$ < 0		–50	mA
$I_{I/O}$	ON-state switch current			±64	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	All pins	±8000	V
			I/O port to GND	±15000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)		±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See (1).

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	4.3	V
V_{IH}	High-level control input voltage	V_{CC} = 3 V to 3.6 V	1.3	V_{CC}	V
		V_{CC} = 4.3 V	1.7	V_{CC}	
V_{IL}	Low-level control input voltage	V_{CC} = 3 V to 3.6 V	0	0.5	V
		V_{CC} = 4.3 V	0	0.7	
$V_{I/O}$	Data input/output voltage		0	V_{CC}	V
T_A	Operating ambient temperature		–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to *Implications of Slow or Floating CMOS Inputs* (SCBA004).

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6.4 Thermal Information

THERMAL METRIC(1)		TMUX154E		UNIT
		DGS (VSSOP)	RSW (UQFN)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	203.1	114.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	88.7	64.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	123.0	21.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	21.2	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	121.6	21.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
I_{SEL} , I_{EN}	Control inputs	V_{CC} = 4.3 V, 0 V, V_{SEL},V_{EN} = 0 to 4.3 V			±1	µA
I_{OZ}	OFF-state leakage current(3)	V_{CC} = 4.3 V, V_O = 0 to 3.6 V, V_I = 0, Switch OFF			±1	µA
I_{OFF}	Powered off leakage current	V_{CC} = 0 V, $V_{An,Bn}$ = 0 V, $V_{A,B}$ = 0 V to 4.3 V, V_{SEL} , V_{EN} = V_{CC} or GND			±2	µA
I_{CC}	Supply current	V_{CC} = 4.3 V, $I_{I/O}$ = 0, Switch ON or OFF			1	µA
ΔI_{CC} (4)	Difference of supply current due to control input voltage not V_{CC} or GND	V_{CC} = 4.3 V, $V_{SEL}V_{EN}$ = 2.6 V			10	µA
C_{SEL}, C_{EN}	Control inputs digital input capacitance	V_{CC} = 0 V, $V_{SEL}V_{EN}$ = V_{CC} or GND		1		pF
$C_{I/O(OFF)}$	OFF-state input capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 3.3 V or 0, Switch OFF		2		pF
$C_{I/O(ON)}$	ON-state input capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 3.3 V or 0, Switch ON		7.5		pF
R_{ON}	ON-state resistance(5)	V_{CC} = 3 V, V_I = 0.4, I_O = –8 mA		6	10	Ω
ΔR_{ON}	ON-state resistance match between channels	V_{CC} = 3 V, V_I = 0.4, I_O = –8 mA		0.35		Ω
$r_{on(flat)}$	ON-state resistance flatness	V_{CC} = 3 V, V_I = 0 V or 1 V, I_O = –8 mA		2		Ω

(1) V_I, V_O, I_I, and I_O refer to data I/O pins A, B, An, and Bn.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each digital control input that is supplied with a voltage other than V_{CC} or GND.
(5) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

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6.6 Dynamic Electrical Characteristics

over operating range, T_A = –40°C to 85°C, V_{CC} = 3.3 V ± 10%, GND = 0 V

PARAMETER		TEST CONDITIONS	TYP(1)	UNIT
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz, See 图 6	–97	dB
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz, See 图 5	–85	dB
BW	Bandwidth (–3 dB)	R_L = 50 Ω, C_L = 5 pF, See 图 7	900	MHz

(1) For Max or Min conditions, use the appropriate value specified under *Electrical Characteristics* for the applicable device type.

6.7 Switching Characteristics

over operating range, T_A = –40°C to 85°C, V_{CC} = 3.3 V ± 10%, GND = 0 V

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{pd}	Propagation delay(2) (3)	R_L = 50 Ω, C_L = 5 pF, See 图 8		0.25		ns
t_{ON}	Line enable time, SEL to A, B, An, or Bn	R_L = 50 Ω, C_L = 5 pF, See 图 4			30	ns
t_{OFF}	Line disable time, SEL to A, B, An, or Bn	R_L = 50 Ω, C_L = 5 pF, See 图 4			25	ns
t_{ON}	Line enable time, $\overline{OE}$ to A, B, An, or Bn	R_L = 50 Ω, C_L = 5 pF, See 图 4			30	ns
t_{OFF}	Line disable time, $\overline{OE}$ to A, B, An, or Bn	R_L = 50 Ω, C_L = 5 pF, See 图 4			25	ns
$t_{SK(O)}$	Output skew between center port to any other port(2)	R_L = 50 Ω, C_L = 5 pF, See 图 9			50	ps
$t_{SK(P)}$	Skew between opposite transitions of the same output (t_{PHL} – t_{PLH})(2)	R_L = 50 Ω, C_L = 5 pF, See 图 9			20	ps

(1) For Max or Min conditions, use the appropriate value specified under *Electrical Characteristics* for the applicable device type.
(2) Specified by design
(3) The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10-pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

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6.8 Typical Characteristics

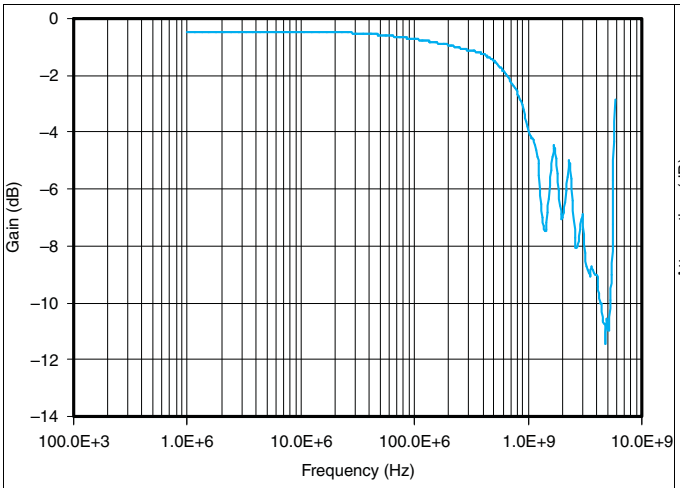


图 1. Bandwidth

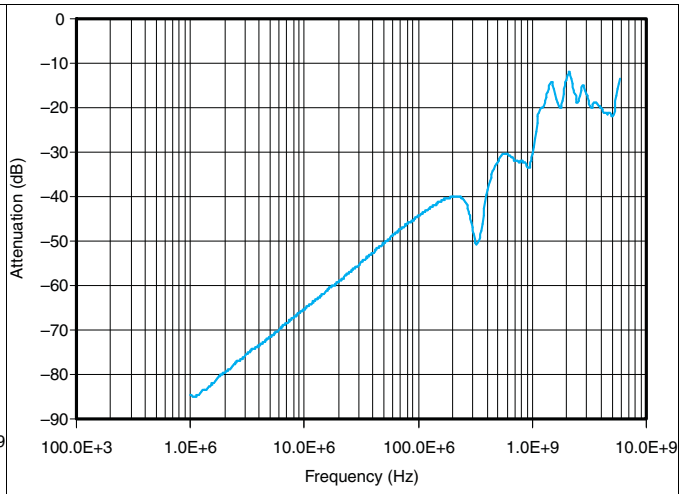


图 2. OFF Isolation

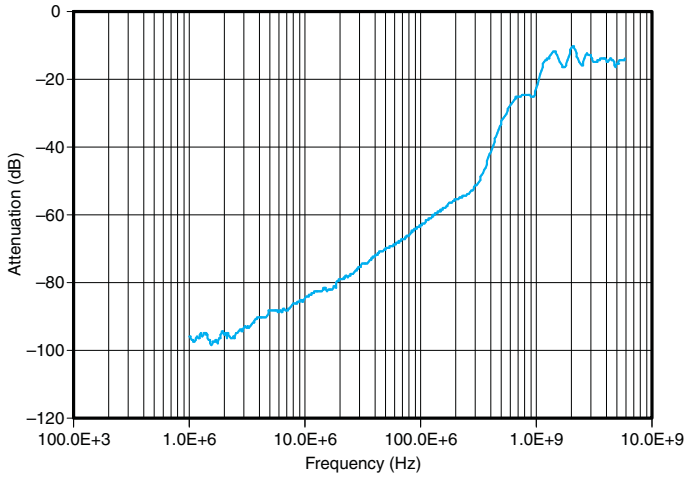
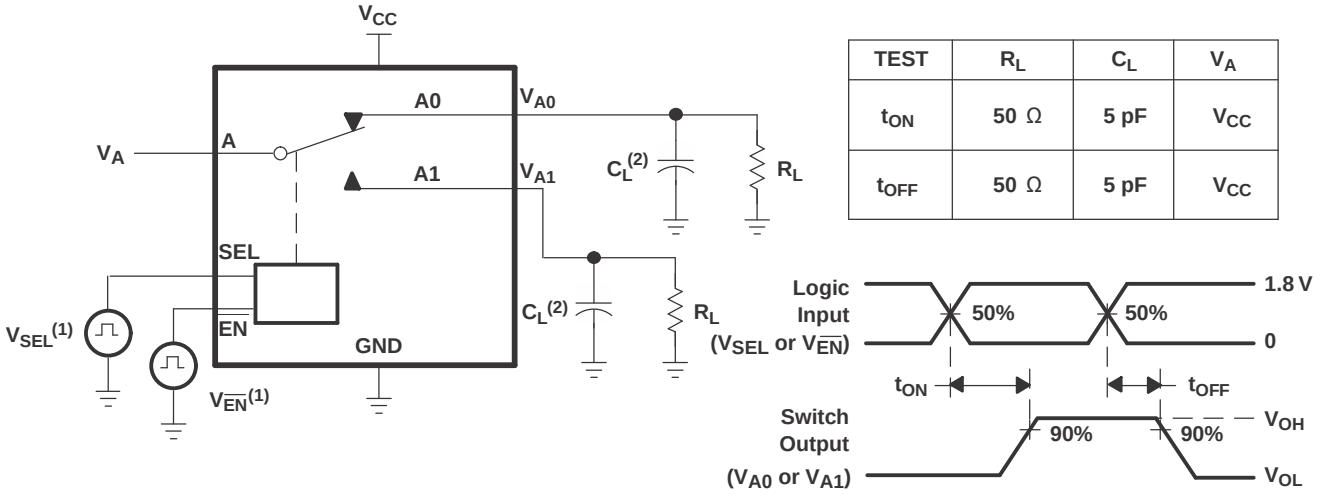


图 3. Crosstalk

7 Parameter Measurement Information



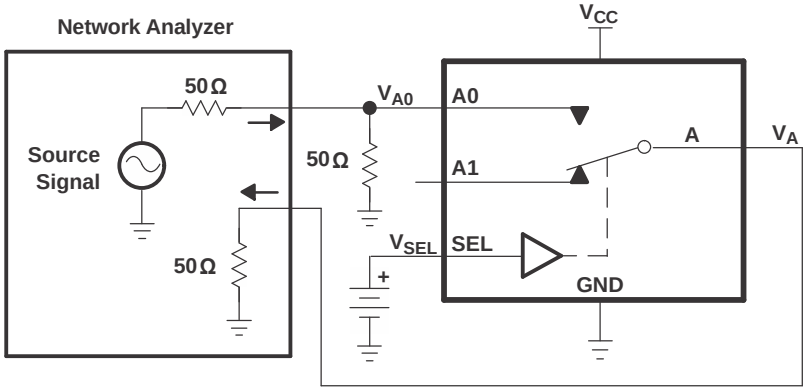
TEST	R_L	C_L	V_A
t_{ON}	50 Ω	5 pF	V_{CC}
t_{OFF}	50 Ω	5 pF	V_{CC}

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(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

图 4. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

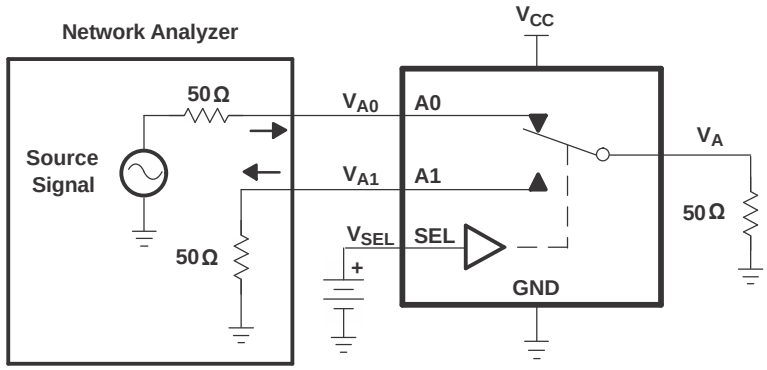


Channel OFF: A to A0
V_{SEL} = V_{CC}

Network Analyzer Setup
Source Power = 0 dBm (632-mV P-P at 50-Ω load)
DC Bias = 350 mV

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图 5. OFF Isolation (O_{ISO})



Channel ON: A0 to A
Channel OFF: A1 to A
V_{SEL} = V_{CC}

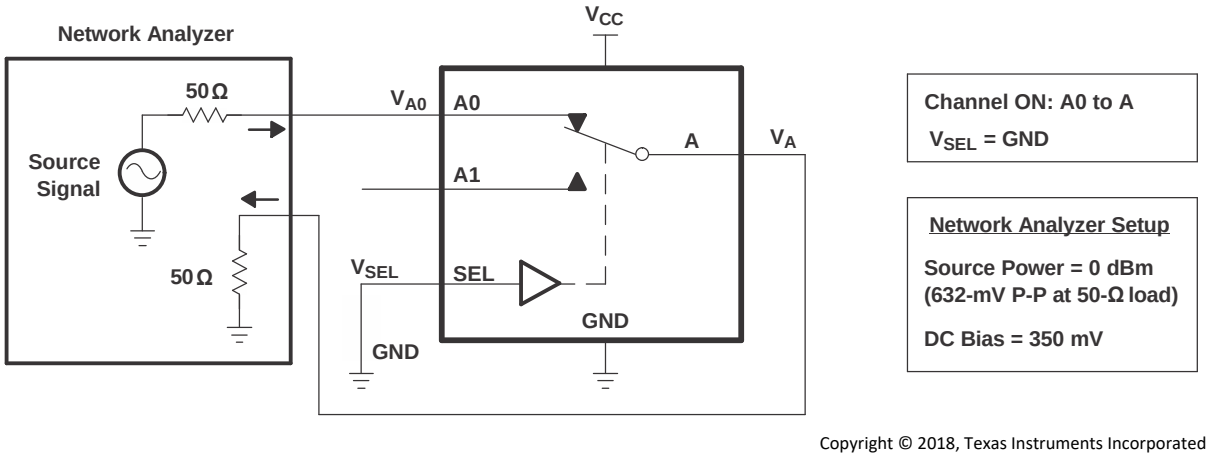
Network Analyzer Setup
Source Power = 0 dBm (632-mV P-P at 50-Ω load)
DC Bias = 350 mV

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图 6. Crosstalk (X_{TALK})

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Parameter Measurement Information (接下页)



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图 7. Bandwidth (BW)

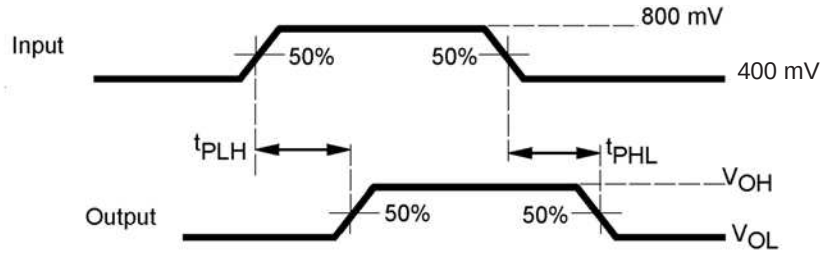
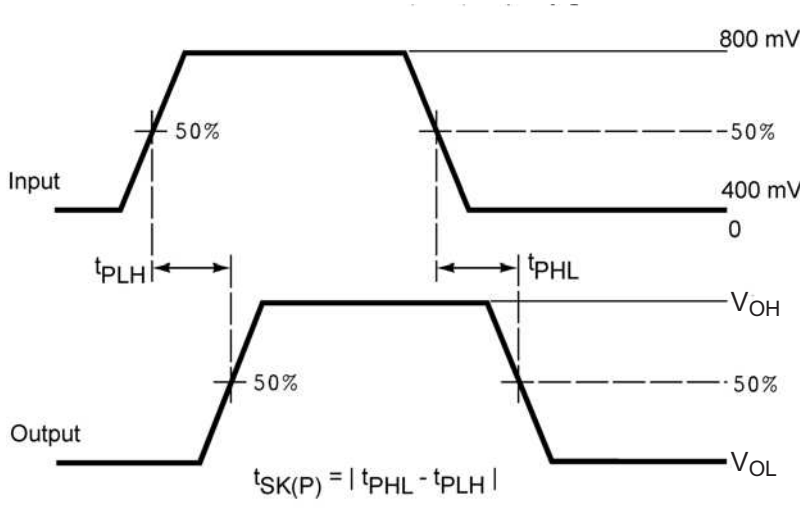
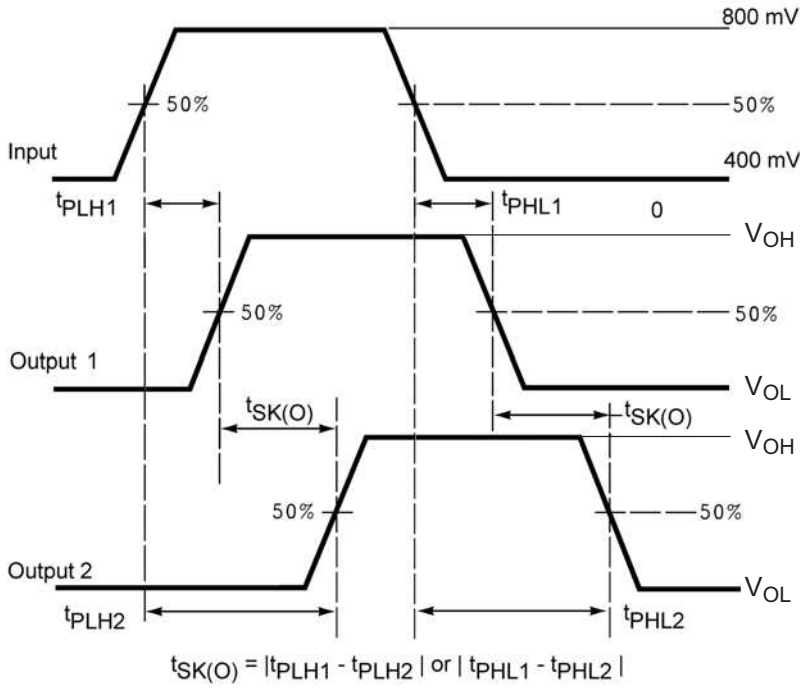


图 8. Propagation Delay

Parameter Measurement Information (接下页)



Pulse Skew $t_{SK(P)}$

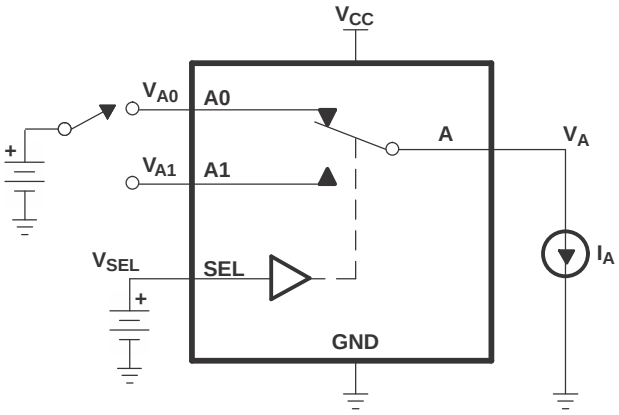


Output Skew $t_{SK(P)}$

图 9. Skew Test

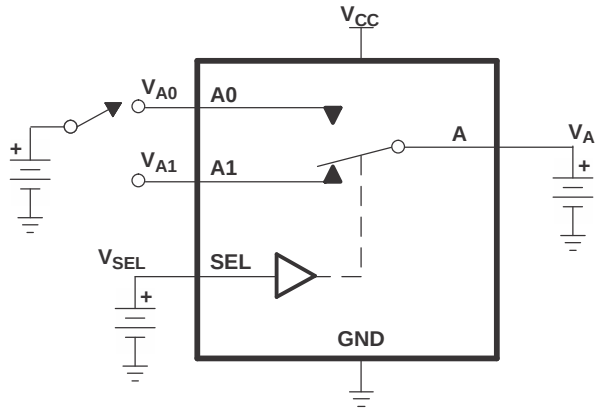
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Parameter Measurement Information (接下页)



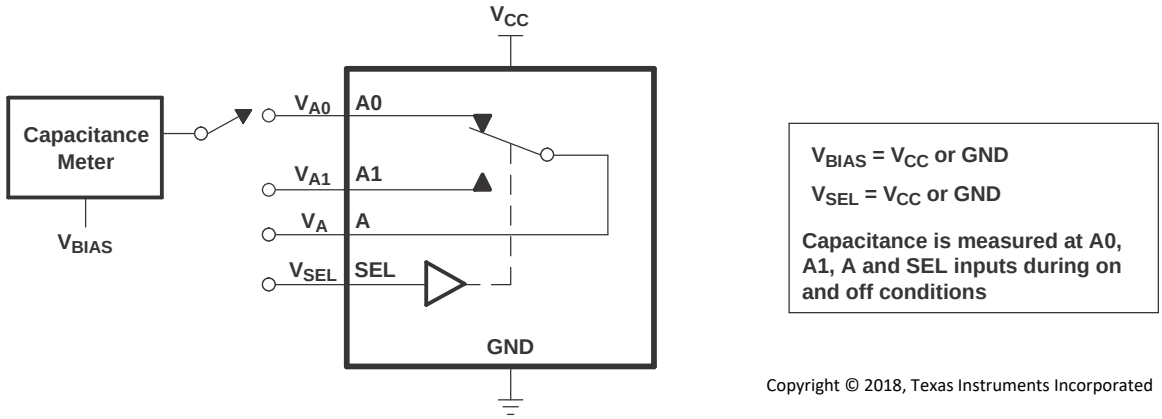
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图 10. ON-State Resistance (R_{ON})



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图 11. OFF-State Leakage Current



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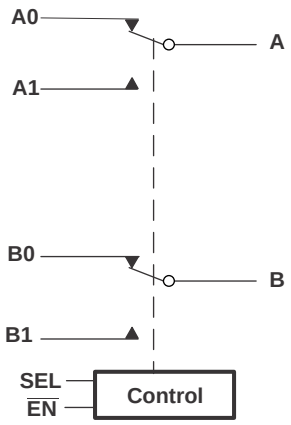
图 12. Capacitance

8 Detailed Description

8.1 Overview

The TMUX154E is a high-bandwidth switch specially designed for the switching and isolating of high-speed signals in systems with limited I/Os. The wide bandwidth (900 MHz) of this switch allows signals to pass with minimum edge and phase distortion. The device multiplexes differential or single ended signals from a single device to one of two corresponding outputs or from two different different devices to one single output. The switch is bidirectional and offers little or no attenuation of the high-speed signals. It is designed for low bit-to-bit skew and high channel-to-channel noise isolation.

8.2 Functional Block Diagram



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8.3 Feature Description

The TMUX154E has an enable pin $\overline{EN}$ that can place the signal paths in high impedance. This allows the user to isolate the signal path when it is not in use and consume less current.

8.4 Device Functional Modes

The device functional modes are shown in 表 1.

表 1. Truth Table

SEL	$\overline{EN}$	FUNCTION
X	H	Disconnect
L	L	A = A0 B= B0
H	L	A = A1 B = B1

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9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

There are many applications in which processors and microcontrollers have a limited number of I/Os. The TMUX154E solution can effectively expand the limited number of I/Os by switching between multiple signal paths in order to interface them to a single processor or microcontroller. TMUX154E can also be used to connect a single microcontroller to two signal paths.

9.2 Typical Application

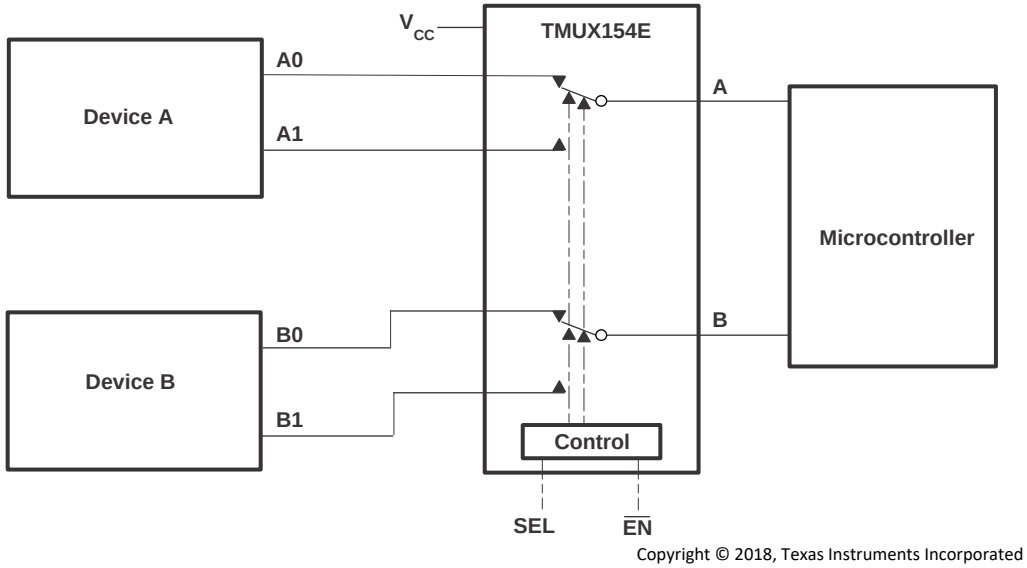


图 13. Application Diagram

9.2.1 Design Requirements

TI recommends that the digital control pins SEL and $\overline{EN}$ be pulled up to V_{CC} or down to GND to avoid undesired switch positions that could result from the floating pin.

9.2.2 Detailed Design Procedure

The TMUX154E can be properly operated without any external components. However, it is recommended that unused pins be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device.

Typical Application (接下页)

9.2.3 Application Curves

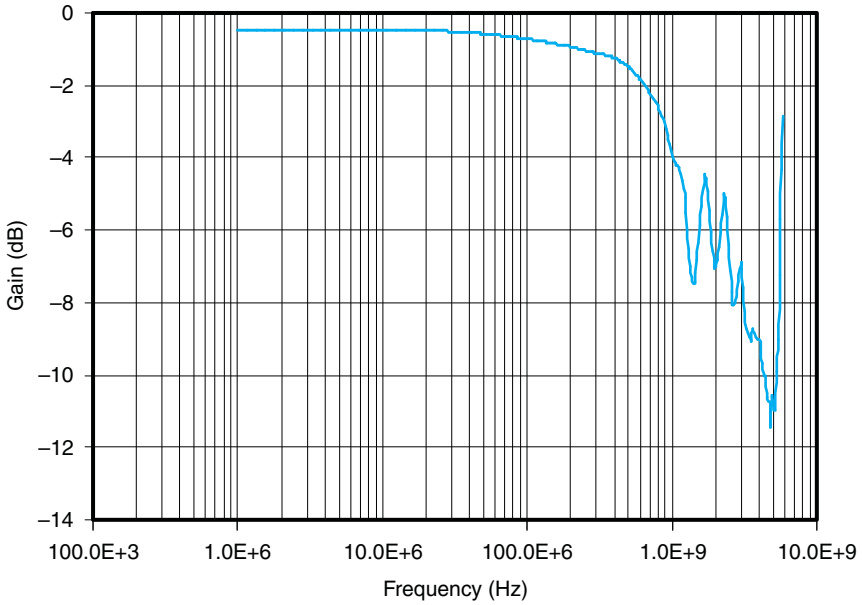


图 14. Bandwidth

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10 Power Supply Recommendations

TI recommends placing a bypass capacitor as close as possible to the supply pin V_{CC} to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

11 Layout

11.1 Layout Guidelines

Place supply bypass capacitors as close to V_{CC} pin as possible and avoid placing the bypass caps near the signal traces.

The high-speed traces should always be of equal length and must be no more than 4 inches; otherwise, the eye diagram performance may be degraded.

Route the high-speed signals using a minimum of vias and corners which will reduce signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the transmission line of the signal and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

Do not route signal traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices, or IC's that use or duplicate clock signals.

Avoid stubs on the high-speed signals because they cause signal reflections.

Route all high-speed signal traces over continuous planes (VCC or GND), with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

For high frequency systems, a printed circuit board with at least four layers is recommended: two signal layers separated by a ground layer and a power layer. The majority of signal traces should run on a single layer, preferably Signal 1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies. For more information on layout guidelines, see *High Speed Layout Guidelines* (SCAA082)

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11.2 Layout Example

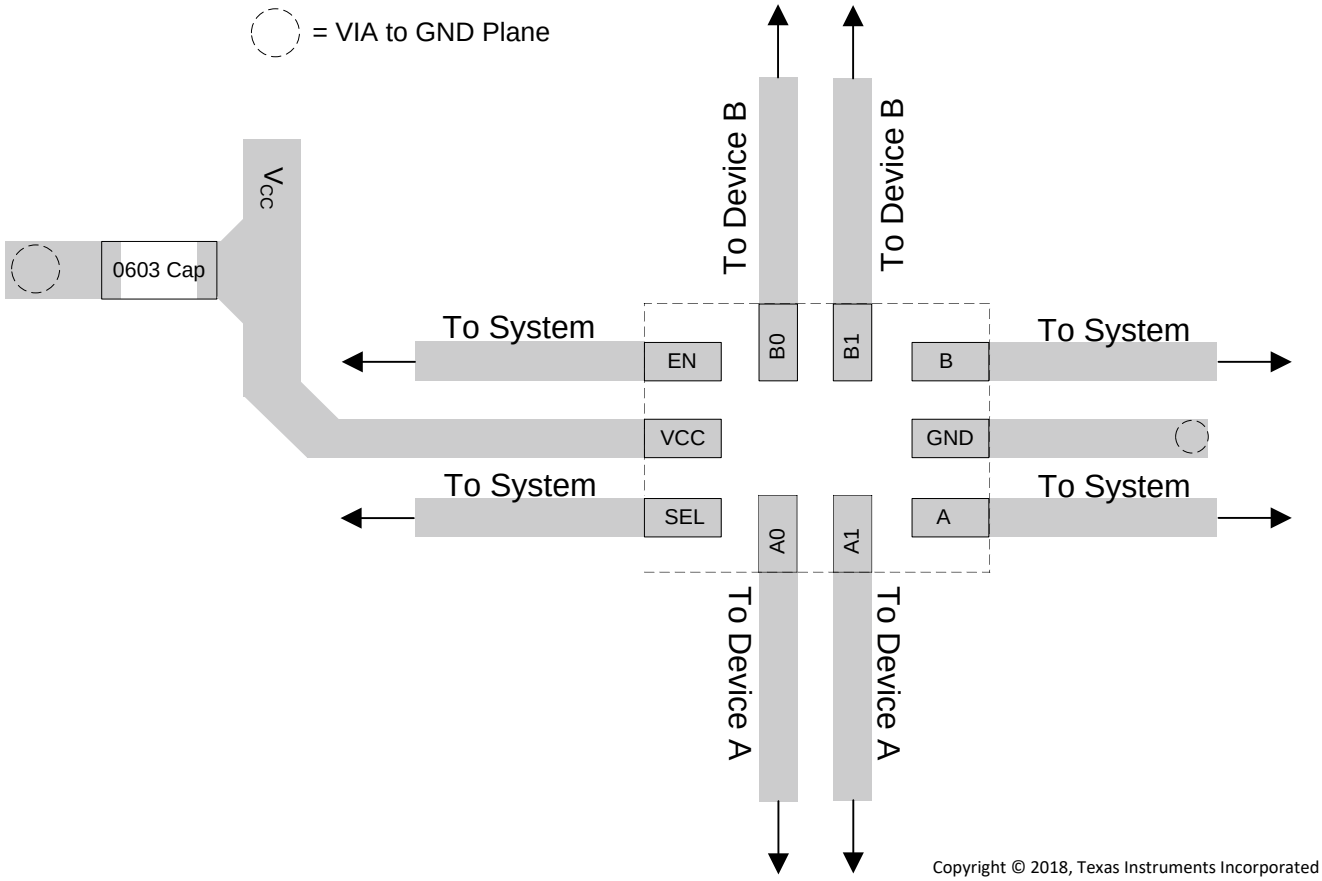


图 15. Layout Recommendation

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12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

如需相关文档，请参阅：

- *《CMOS 输入缓慢变化或悬空的影响》*，SCBA004
- *《高速布局指南》*，SCAA082

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

12.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX154EDGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 85	1A6
TMUX154ERSWR	Active	Production	UQFN (RSW) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BXV

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

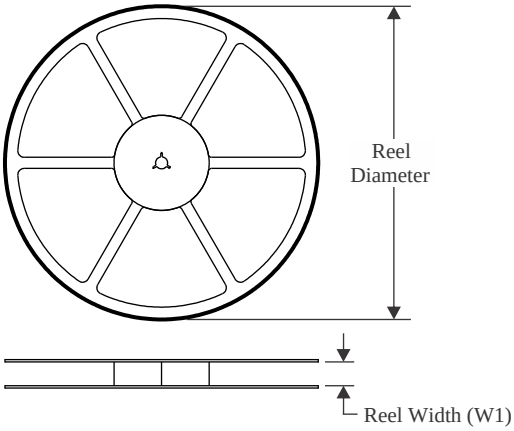
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

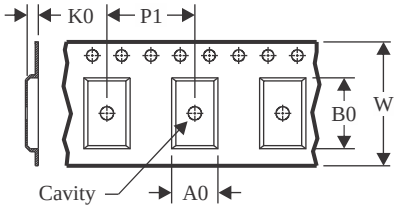
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

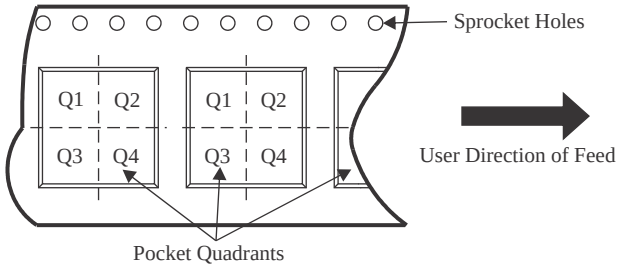


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

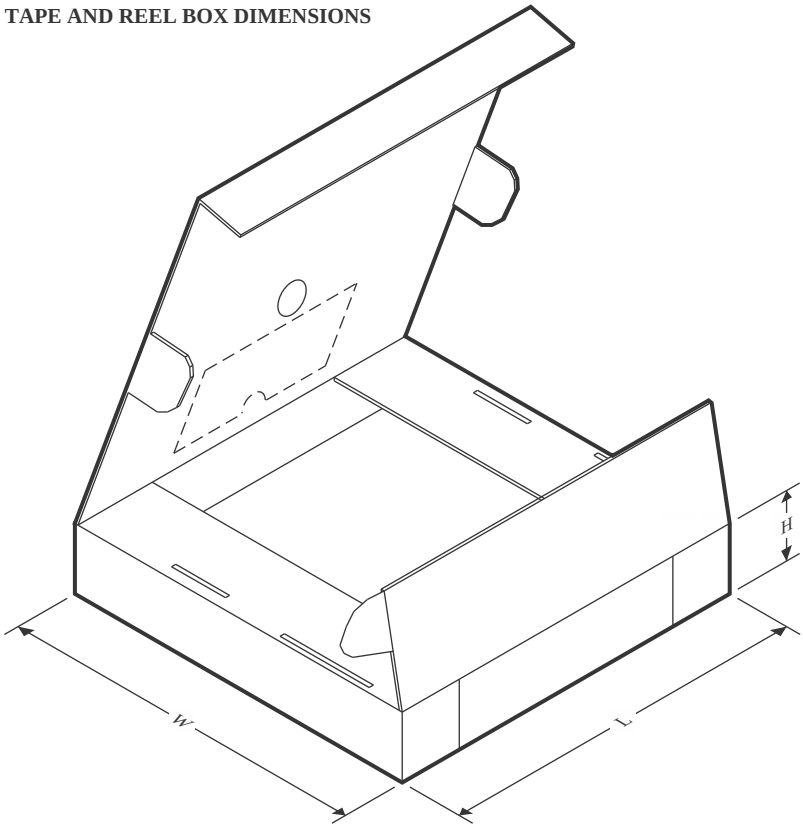
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX154EDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TMUX154ERSWR	UQFN	RSW	10	3000	180.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

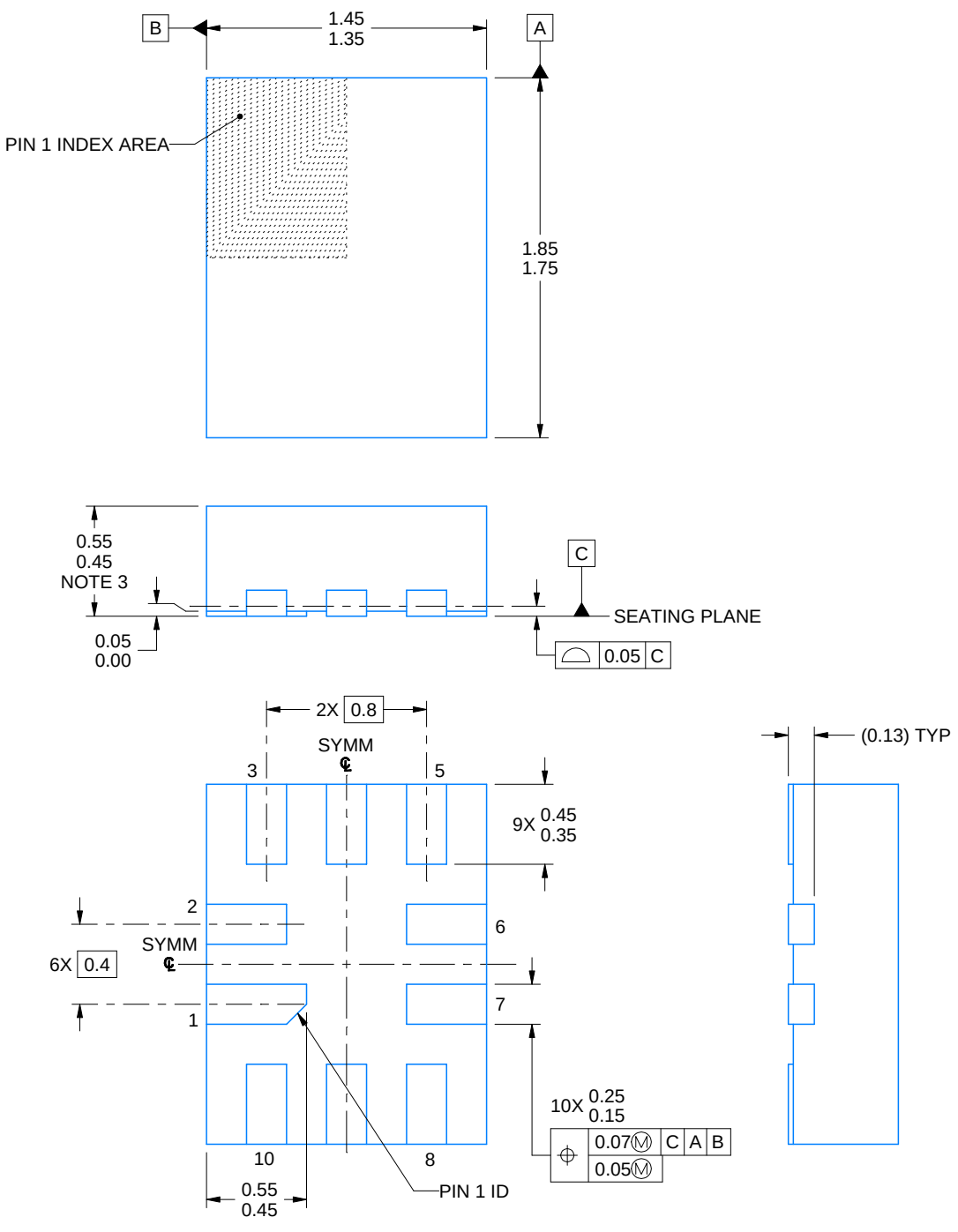
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX154EDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TMUX154ERSWR	UQFN	RSW	10	3000	210.0	185.0	35.0

PACKAGE OUTLINE

RSW0010A

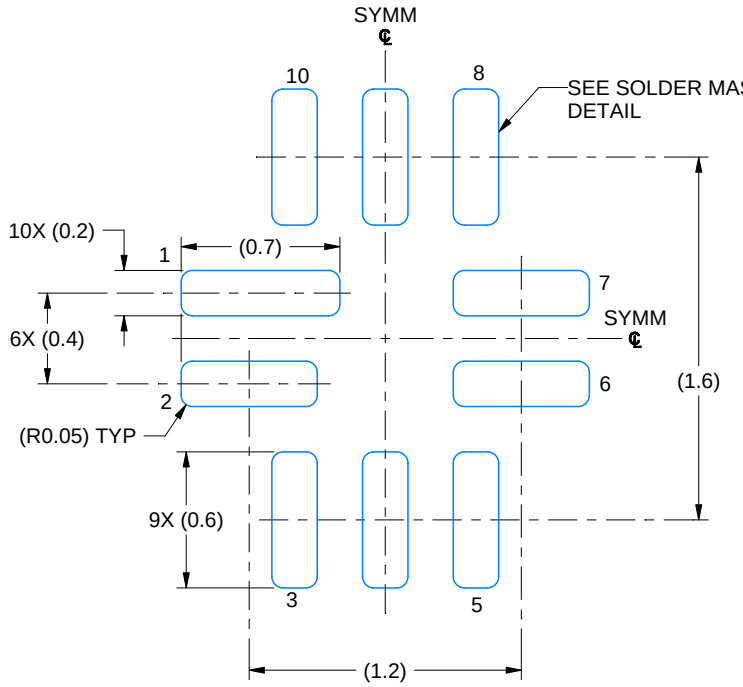
UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

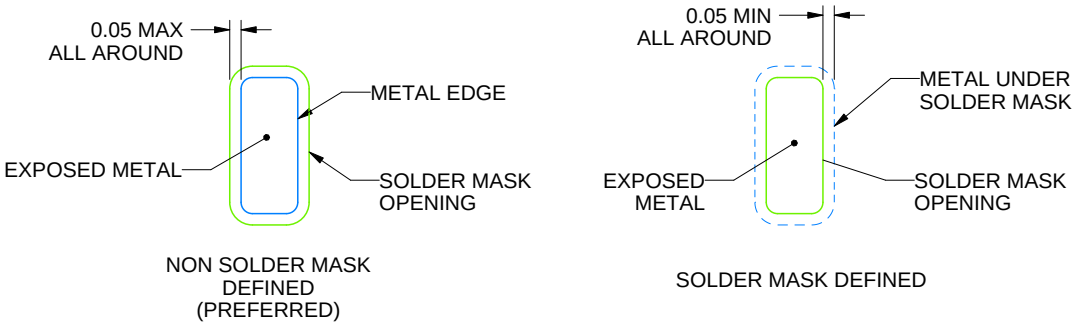


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-288 variation UDEE, except minimum package height.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

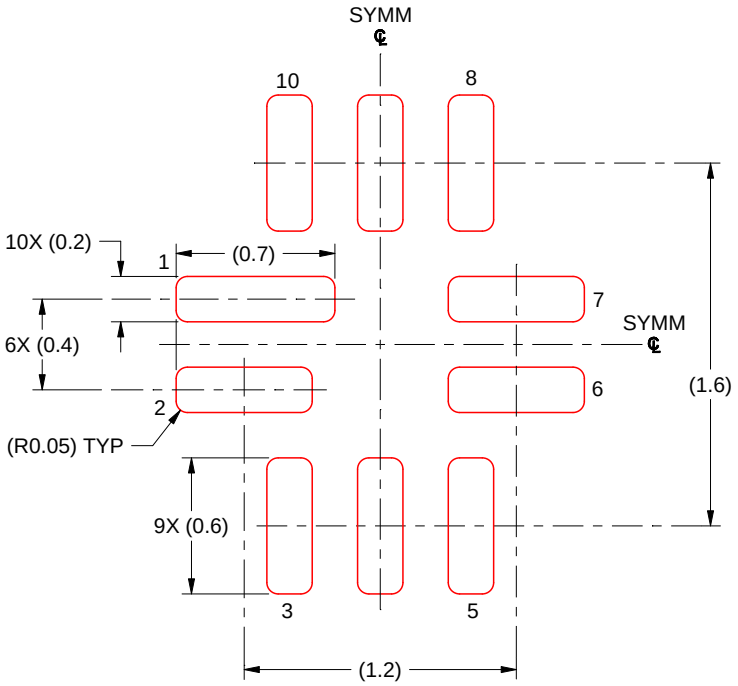


SOLDER MASK DETAILS

4224897/A 03/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

4224897/A 03/2019

NOTES: (continued)

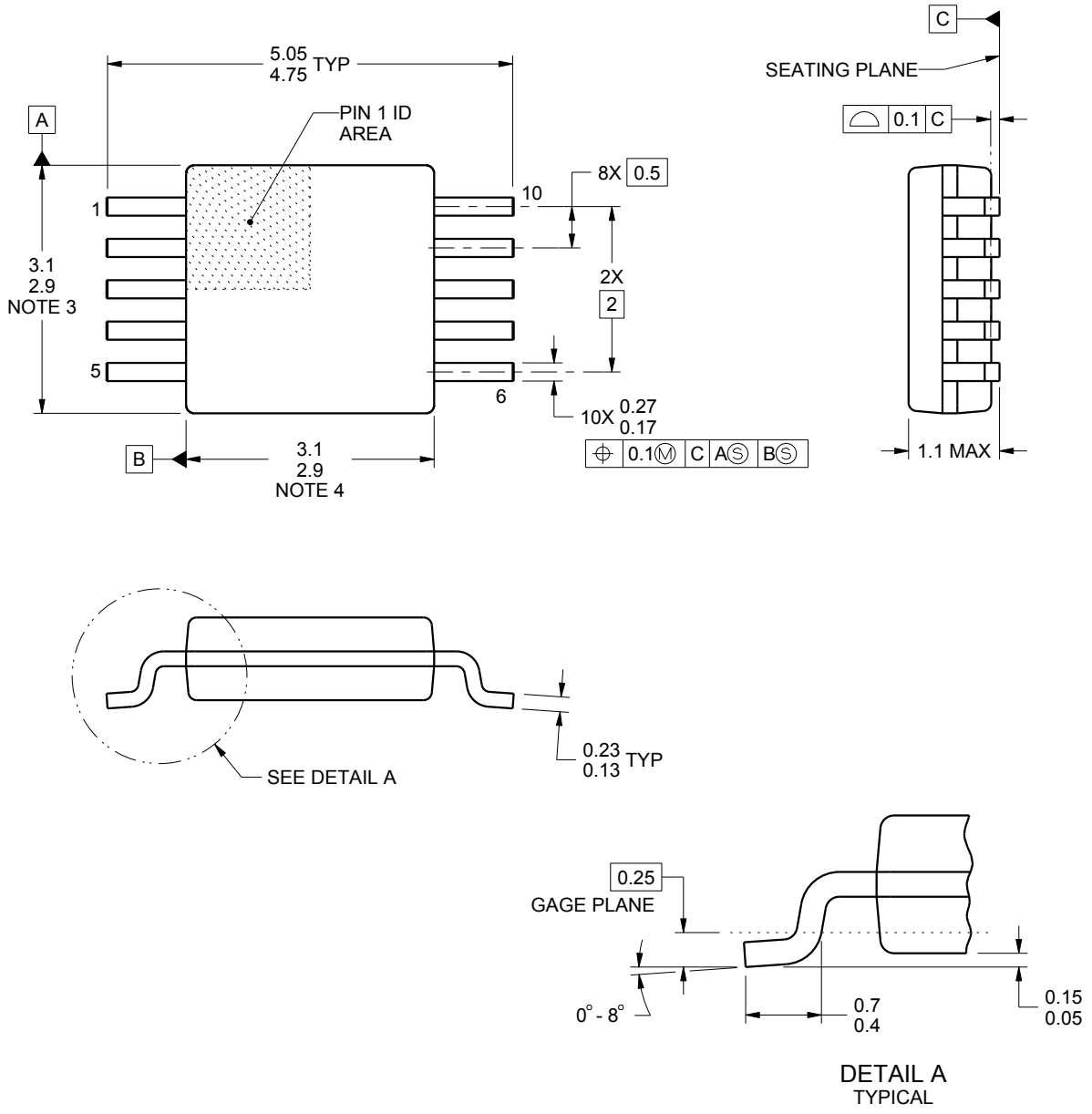
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DGS0010A

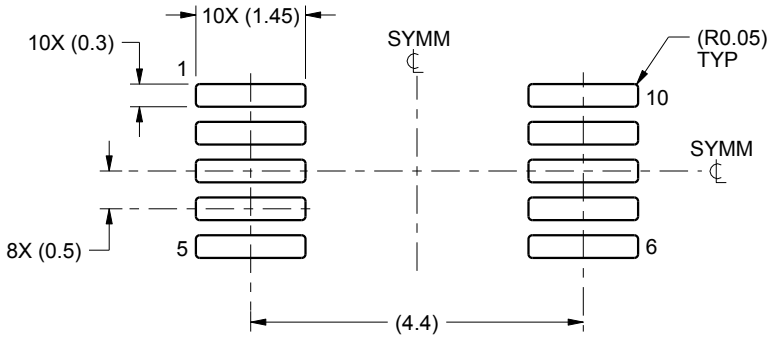
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

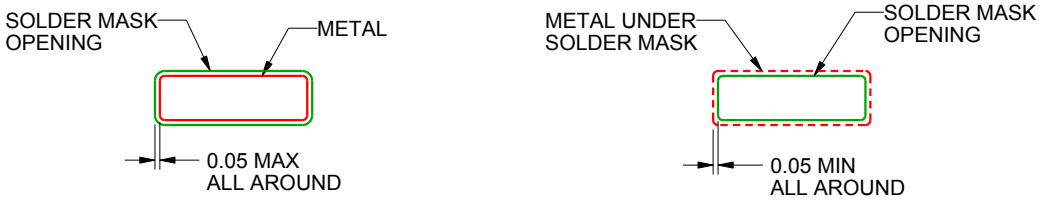


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

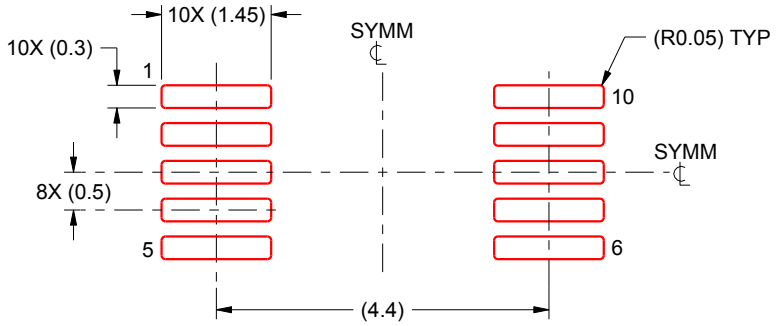


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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