1. Features

- Excellent DC Performance:
  - Low Input Offset Voltage: 25 μV (max)
  - Low Input Offset Drift: 0.2 μV/°C (max)
  - High CMRR: 104 dB, G ⩾ 10 (min)
- Low Input Noise:
  - 9 nV/√Hz at 1 kHz
  - 0.25 μVPP (0.1 Hz to 10 Hz)
- Wide Supply Range:
  - Single Supply: 4 V to 36 V
  - Dual Supply: ±2 V to ±18 V
- Gain Set with a Single External Resistor:
  - Gain Equation: G = 1 + (49.4 kΩ / RG)
  - Gain Error: 0.007%, G = 1
  - Gain Drift: 5 ppm/°C (max) G = 1
- Input Voltage: (V–) + 0.1 V to (V+) – 1.5 V
- RFI-Filtered Inputs
- Rail-to-Rail Output
- Operating Temperature: –40°C to +125°C
- SOP-8, MSOP8 and DFN-8 Packages

2. Applications

- Bridge Amplifiers
- ECG Amplifiers
- Pressure Sensors
- Medical Instrumentation
- Portable Instrumentation
- Weigh Scales
- Thermocouple Amplifiers
- RTD Sensor Amplifiers
- Data Acquisition

3. General Description

The LHAMP188 is a precision instrumentation amplifier that uses auto-zeroing techniques to achieve low offset voltage, near-zero offset and gain drift, excellent linearity, and exceptionally low-noise density (9 nV/√Hz) that extends down to dc.

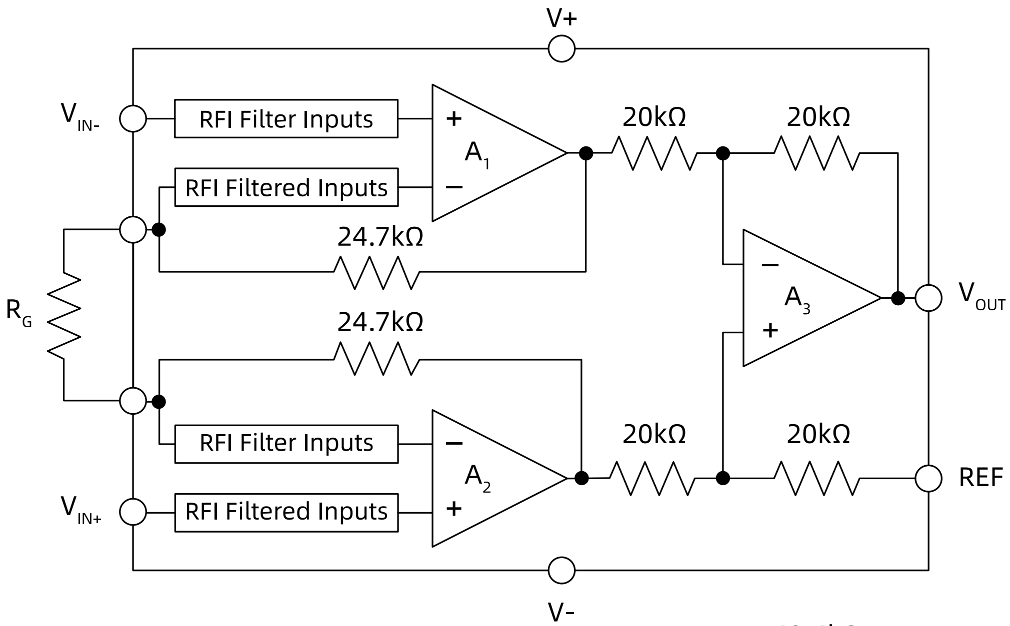
The LHAMP188 is optimized to provide excellent common-mode rejection of greater than 104 dB (G ⩾10). Superior common-mode and supply rejection supports high-resolution, precise measurement applications. The versatile three op-amp design offers a rail-to-rail output, low-voltage operation from a 4-V single supply as well as dual supplies up to ±18 V, and a wide, high-impedance input range. These specifications make this device ideal for universal signal measurement and sensor conditioning (such as temperature or bridge applications).

A single external resistor sets any gain from 1 to 1000. The LHAMP188 is designed to use an industry-standard gain equation: G = 1 + (49.4 kΩ / RG). The reference pin can be used for level-shifting in single-supply operation or for an offset calibration.

The LHAMP188 is specified over the temperature range of –40°C to +125°C .

LHAMP188 is available in SOP8, MSOP8 package.

Simplified Schematic



$$V_{OUT} = (V_{IN+} - V_{IN-}) \times G + V_{REF}$$

$$G = 1 + \frac{49.4k\Omega}{R_G}$$

Table of Contents

4. Revision History

Version number	Date	Update the content
PreA	February 21, 2024	First edition
PreB	March 22, 2024	Add typical characteristics images
	April 8, 2024	Add the small package

5. Pin Configuration and Functions

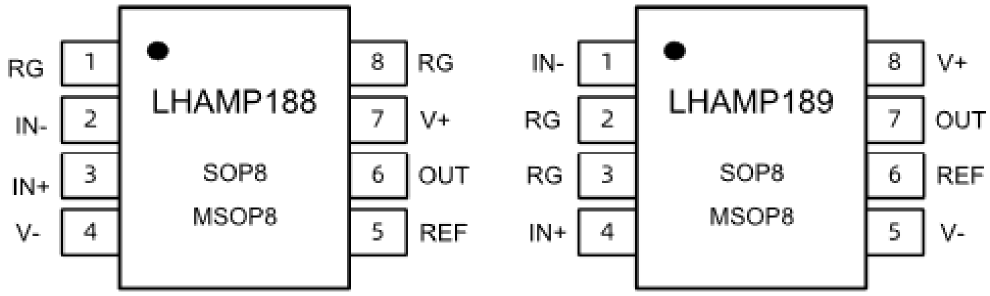


Figure 1. Pin Configuration and Functions

Table 1. Pin Functions

PIN	I/O	DESCRIPTION
REF	I	Reference input. This pin must be driven by low impedance or connected to ground.
RG	—	Gain setting pin. For gains greater than 1, place a gain resistor between two RG pins..
V–	—	Negative supply
V+	—	Positive supply
VIN–	I	Negative input
VIN+	I	Positive input
VOUT	O	Output

6. Specifications

6.1. Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

Table 2. Absolute Maximum Ratings

		MIN	MAX	UNIT
Voltage	Supply		±20	V
			40 (single supply)	
	Current		±10	mA
	Analog input range[2]	(V–) – 0.5	(V+) + 0.5	V
Output short-circuit[3]		Continuous		
Temperature	Operating range, T_A	–55	150	°C
	Junction, T_J		150	
	Storage temperature, T_{stg}	–65	150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails must be current limited to 10 mA or less.

(3) Short-circuit to ground.

6.2. ESD Ratings

Table 3. ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3. Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted).

Table 4. Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_S	Supply voltage	4 (±2)		36 (±18)	V
	Specified temperature	-40		125	°C

6.4. Thermal Information

Table 5. Thermal Information

THERMAL METRIC		LHAMP188 SOP 8 PINS	LHAMP188 MSOP 8 PINS	LHAMP188 DFN 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	125		145	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	80		75	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68		39	°C/W

6.5. Electrical Characteristics: V_S = ±4 V to ±18 V (V_S = 8 V to 36 V)

At T_A = 25°C, R_L = 10 kΩ, V_{REF} = V_S / 2, and G = 1, unless otherwise noted.

Table 6.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT[1]						
V_{OSI}	Input stage offset voltage	At RTI[2]		±5	±40	µV
		At RTI, TA = –40°C to +125°C		±0.08	±0.2	µV/°C
V_{OSO}	Output stage offset voltage	At RTI		±25	±170	µV
		At RTI, TA = –40°C to +125°C		±0.2	±0.35	µV/°C
V_{OS}	Offset voltage	At RTI		±5 ±25 / G	±40 ±170/G	µV
		At RTI, TA = –40°C to +125°C			±0.2 ±0.35/G	µV/°C
PSRR	Power-supply rejection ratio	G = 1, VS = 4 V to 36 V, VCM = VS / 2		±0.7	±2.25	µV/V
		G = 10, VS = 4 V to 36 V, VCM = VS / 2		±0.6		
		G = 100, VS = 4 V to 36 V, VCM = VS / 2		±0.45		
		G = 1000, VS = 4 V to 36 V, VCM = VS / 2		±0.3	±0.8	
	Long-term stability			1[3]		µV
	Turn-on time to specified VOSI			See the Typical Characteristics		
Z_{id}	Differential input impedance			100 || 6		GΩ || pF
Z_{ic}	Common-mode input impedance			100 || 9.5		GΩ || pF
V_{CM}	Common-mode voltage range	The input signal common-mode range can be calculated with this tool	(V–) + 0.1		(V+) – 1.5	V
CMRR	Common-mode rejection ratio	G = 1, at dc to 60 Hz, VCM = (V–) + 1.0 V to (V+) – 2.5 V	84	90		dB
		G = 10, at dc to 60 Hz, VCM = (V–) + 1.0 V to (V+) – 2.5 V	104	110		
		G = 100, at dc to 60 Hz, VCM = (V–) + 1.0 V to (V+) – 2.5 V	124	130		
		G = 1000, at dc to 60 Hz, VCM = (V–) + 1.0 V to (V+) – 2.5 V	130	140		
INPUT BIAS CURRENT						
I_{IB}	Input bias current	TA=25°C		±150	±1500	pA
		TA = –40°C to +125°C		See Figure 2		pA/°C
I_{OS}	Input offset current	TA=25°C		±150	±1500	pA
		TA = –40°C to +125°C		See Figure 3		pA/°C
INPUT VOLTAGE NOISE						
e_{NI}	Input voltage noise	f = 1 kHz, G = 100, RS = 0 Ω		9		nV/√Hz
		f = 0.1 Hz to 10 Hz, G = 100, RS = 0 Ω		0.25		µVPP
e_{NO}	Output voltage noise	f = 1 kHz, G = 100, RS = 0 Ω		57		nV/√Hz
		f = 0.1 Hz to 10 Hz, G = 100, RS = 0 Ω		1.5		$µV_{PP}$
i_N	Input current noise	f = 1 kHz		640		fA/√Hz
		f = 0.1 Hz to 10 Hz		10		pA_{PP}
GAIN						
G	Gain equation			1 + (49.4 kΩ / R_G)		V/V
	Gain range		1		1000	V/V
E_G	Gain error	G=1,(V–)+0.5V≤VO≤(V+)–1.5V		±0.007%	±0.025%	
		G=10,(V–)+0.5V≤VO≤(V+)–1.5V		±0.05%	±0.20%	

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
			G = 100, (V–) + 0.5 V ≤ VO ≤ (V+) – 1.5 V		±0.06%	±0.20%	
			G = 1000, (V–) + 0.5 V ≤ VO ≤ (V+) – 1.5 V		±0.2%	±0.50%	
	Gain versus temperature		G = 1, TA = –40°C to +125°C		1	5	ppm/°C
			G > 1[4], TA = –40°C to +125°C		15	50	
	Gain nonlinearity		G = 1, VO = –10 V to +10 V		3	8	ppm
			G > 1, VO = –10 V to +10 V		See Figure 32, 32		
OUTPUT							
	Output voltage swing from rail[5]		R_L = 10 kΩ[5]		220	250	mV
	Capacitive load drive				0.1		nF
I_{SC}	Short-circuit current		Continuous to common		±32		mA
FREQUENCY RESPONSE							
BW	Bandwidth, –3 dB		G = 1		2200		kHz
			G=10		1000		
			G=100		100		
			G = 1000		10		
SR	Slew rate		G = 1, V_S = ±18 V, V_O = 10-V step		4		V/µs
			G = 100, V_S = ±18 V, V_O = 10-V step		2		
t_S	Settling time	To 0.1%	G=1,V_S=±18V,V_{STEP}=10V		2		µs
			G = 100, V_S = ±18 V, V_{STEP} = 10 V		20		
		To 0.01%	G=1,V_S=±18V,V_{STEP}=10V		3		µs
			G = 100, V_S = ±18 V, V_{STEP} = 10 V		25		
	Overload recovery		50% overdrive		75		µs
REFERENCE INPUT							
R_{IN}	Input impedance				40		kΩ
	Voltage range			V–		V+	V
POWER SUPPLY							
	Voltage range	Single		4		36	V
		Dual		±2		±18	
I_Q	Quiescent current		V_{IN}=V_S/2		2.7	3.3	mA
			T_A = –40°C to +125°C			3.35	
TEMPERATURE RANGE							
	Specified temperature range			–40		125	°C
	Operating temperature range			–55		150	°C

(1) Total V_{OS}, referred-to-input = (V_{OSI}) + (V_{OSO} / G).
(2) RTI = Referred-to-input.
(3) 300-hour life test at 150°C demonstrated a randomly distributed variation of approximately 1 µV.
(4) Does not include effects of external resistor R_G.
(5) See Typical Characteristics curves, Output Voltage Swing vs Output Current.

6.6. Typical Characteristics

At T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1, unless otherwise noted.

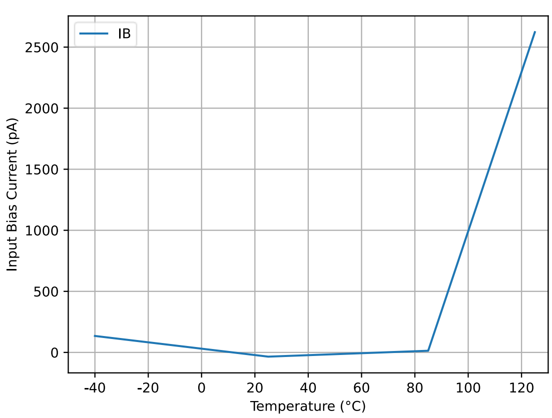


Figure 2. Input Bias Current vs Temperature

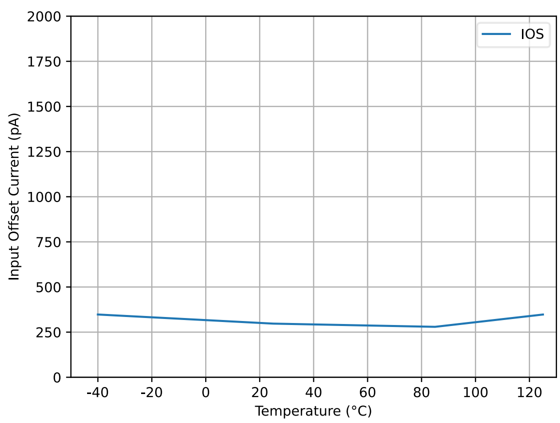
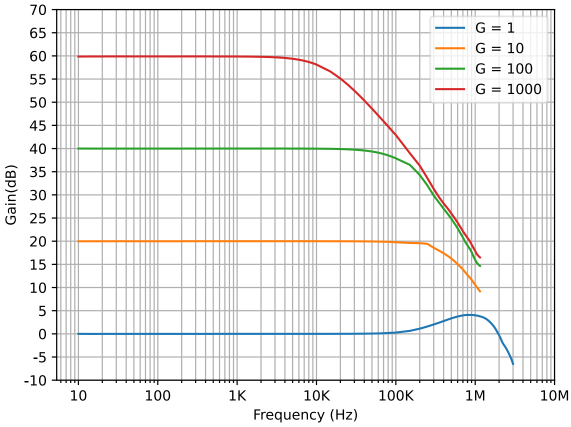


Figure 3. Input Offset Current vs Temperature



At RTI

Figure 4. Gain vs Frequency

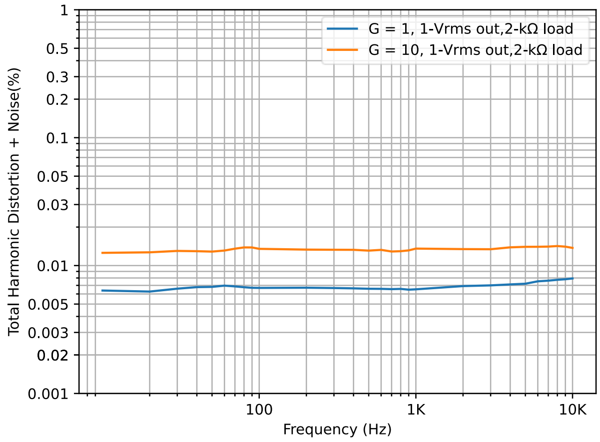
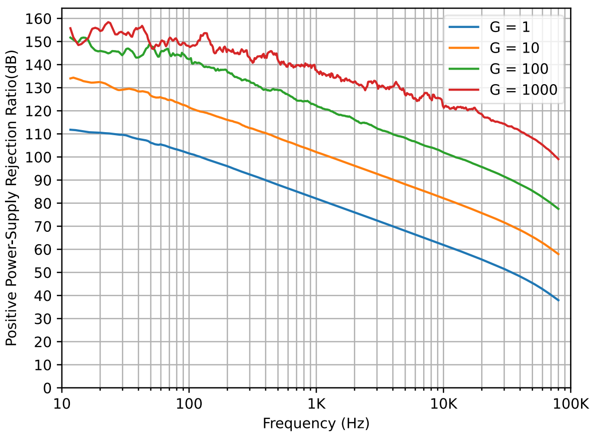
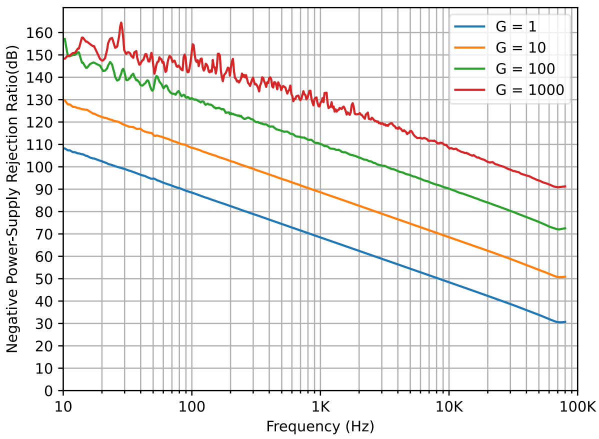


Figure 5. Total Harmonic Distortion + Noise vs Frequency



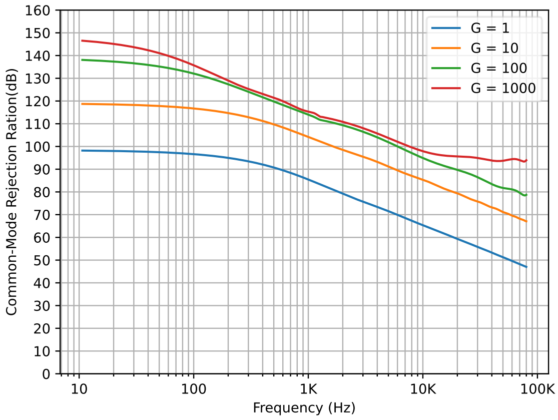
At RTI

Figure 6. Positive PSRR vs Frequency



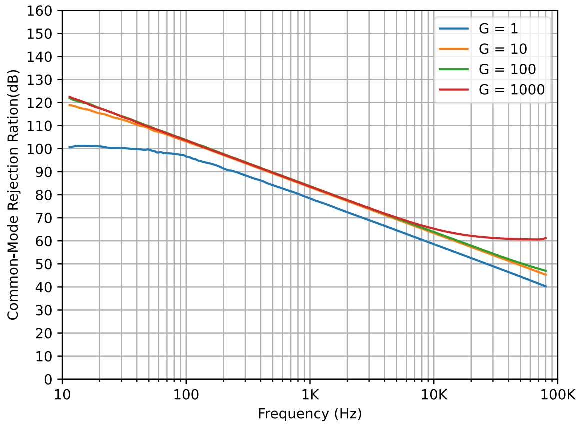
At RTI

Figure 7. Negative PSRR vs Frequency



At RTI

Figure 8. CMRR vs Frequency



At RTI, 1-kΩ Source Imbalance

Figure 9. CMRR vs Frequency

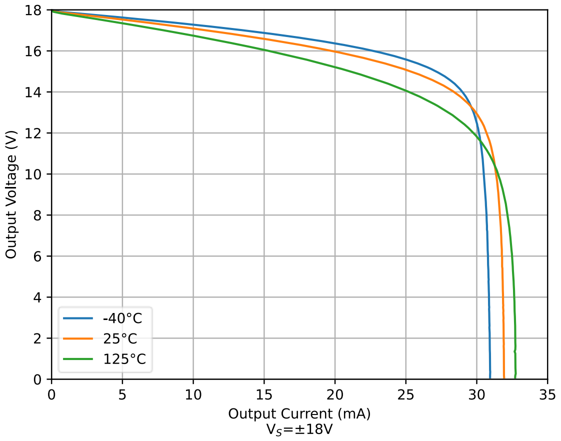


Figure 10. Positive Output Voltage Swing vs Output Current

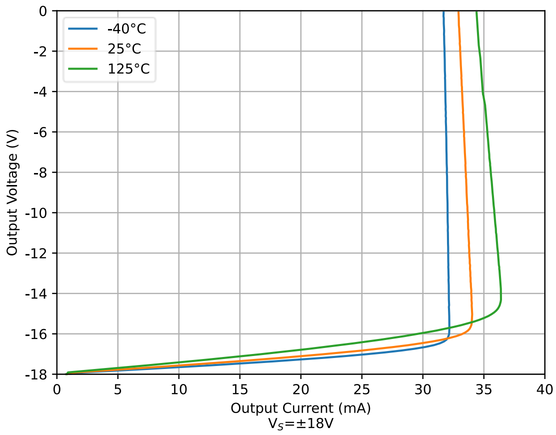


Figure 11. Negative Output Voltage Swing vs Output Current

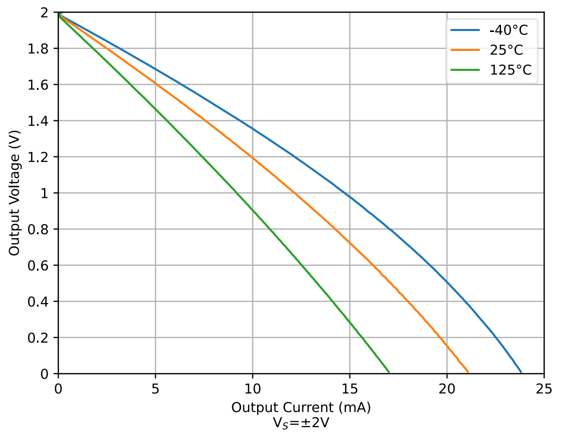


Figure 12. Positive Output Voltage Swing vs Output Current

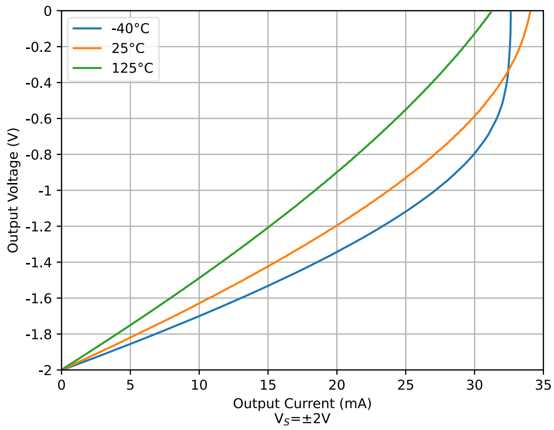


Figure 13. Negative Output Voltage Swing vs Output Current

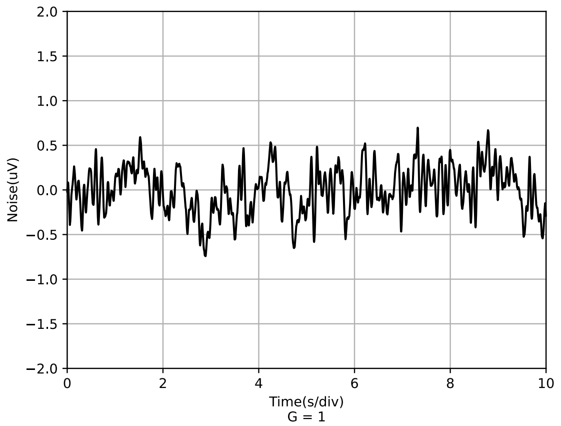


Figure 14. 0.1-Hz to 10-Hz RTI Voltage Noise

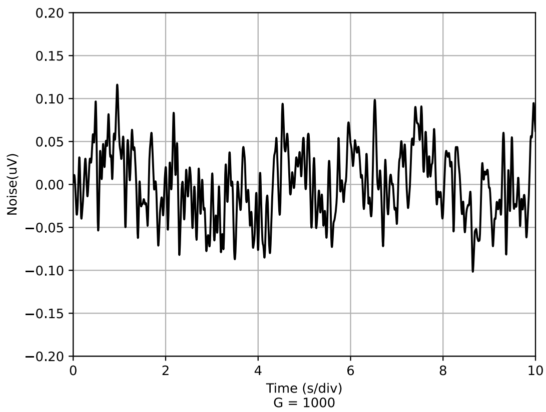
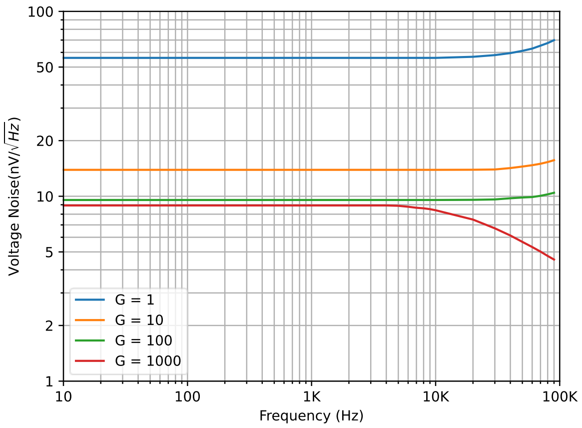


Figure 15. 0.1-Hz to 10-Hz RTI Voltage Noise



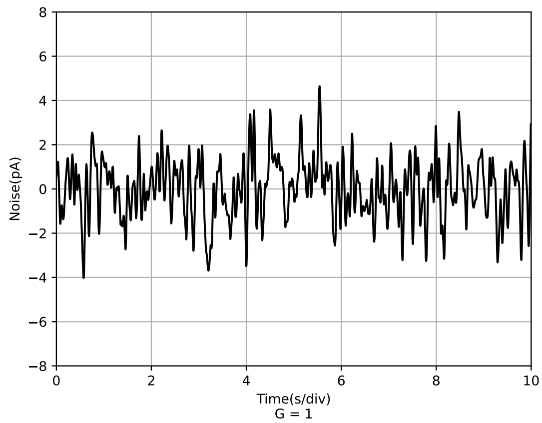
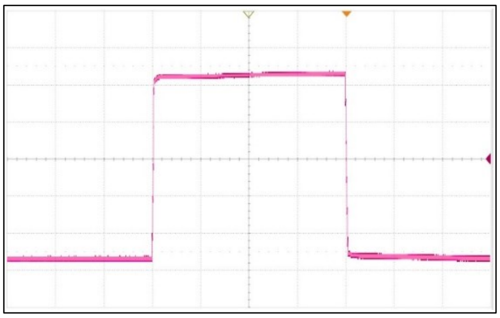


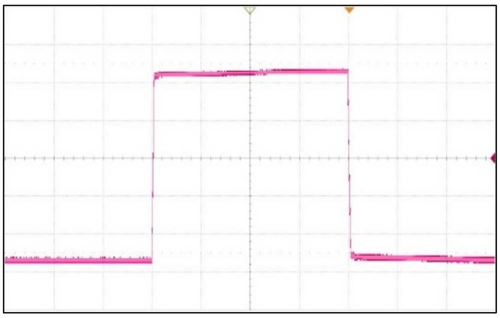
Figure 17. 0.1-Hz to 10-Hz RTI Current Noise

Figure 16. Voltage Noise Spectral Density vs Frequency



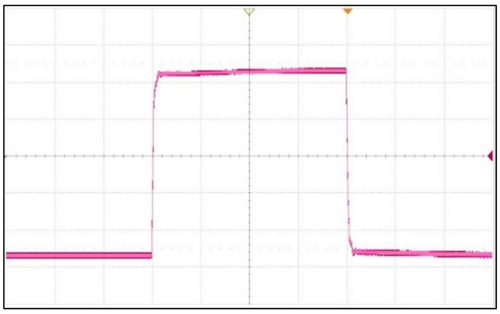
Voltage: 2V/div, Time: 50uS/div, RL= 10kΩ, CL = 100pF, G = 1

Figure 18. Large-Signal Pulse Response



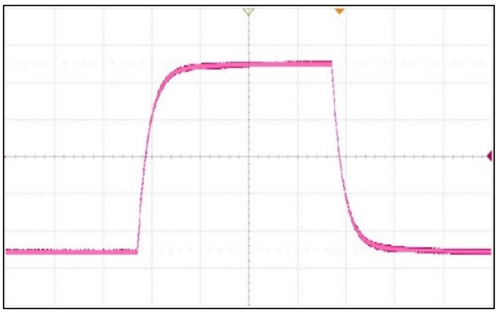
Voltage: 2V/div, Time: 50uS/div, RL= 10kΩ, CL = 100pF, G = 10

Figure 19. Large-Signal Pulse Response



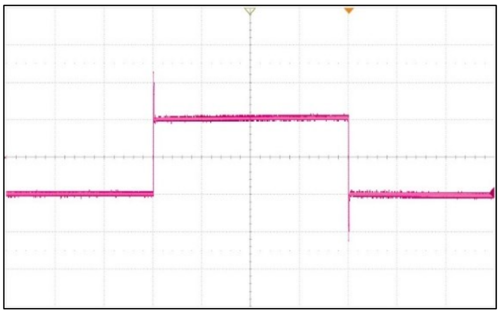
Voltage: 2V/div, Time: 50uS/div, RL= 10kΩ, CL = 100pF, G = 100

Figure 20. Large-Signal Pulse Response



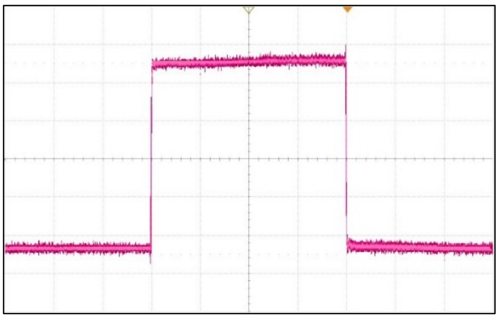
Voltage: 2V/div, Time: 50uS/div, RL= 10kΩ, CL = 100pF, G = 1000

Figure 21. Large-Signal Pulse Response



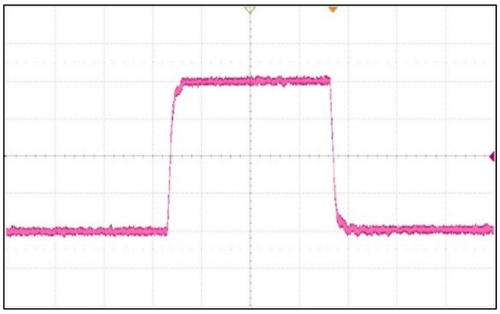
Voltage: 50mV/div, Time: 50uS/div, RL= 10kΩ, CL = 100pF, G = 1

Figure 22. Small -Signal Pulse Response



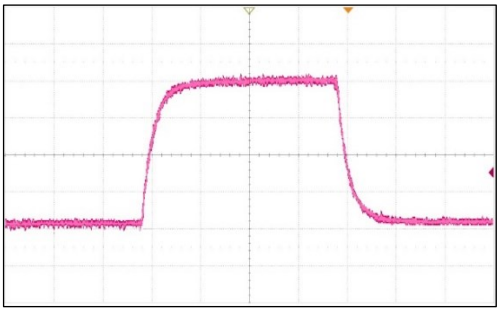
Voltage: 20mV/div, Time: 50uS/div, RL= 10kΩ, CL = 100pF, G = 10

Figure 23. Small -Signal Pulse Response



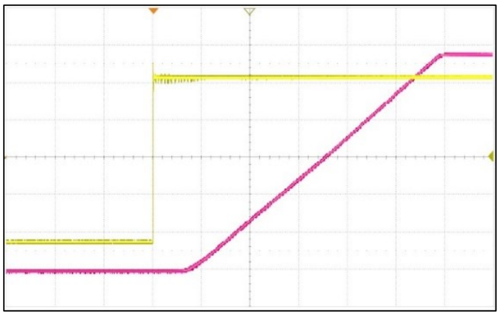
Voltage：50mV/div, Time: 20uS/div, R_L= 10kΩ, C_L = 100pF, G = 100

Figure 24. Small -Signal Pulse Response



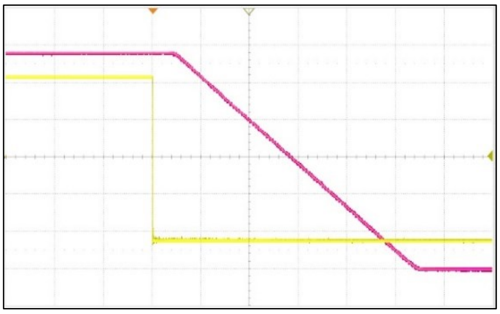
Voltage：50mV/div, Time: 50uS/div, R_L= 10kΩ, C_L = 100pF, G = 1000

Figure 25. Small -Signal Pulse Response



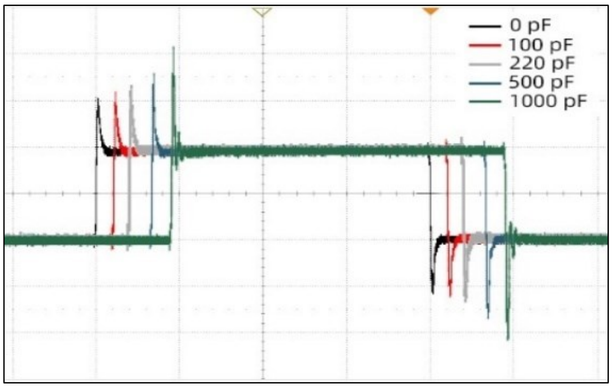
Vin：1V/div, Vout：5V/div, Time: 2uS/div, R_L= 10kΩ, C_L = 100pF, G = 10

Figure 26. Positive Overload Recovery



Vin：1V/div, Vout：5V/div, Time: 2uS/div, R_L= 10kΩ, C_L = 100pF, G = 10

Figure 27. Negative Overload Recovery



Voltage：50mV/div, Time: 10uS/div, G = 1

Figure 28. Small-Signal Response vs Capacitive Load

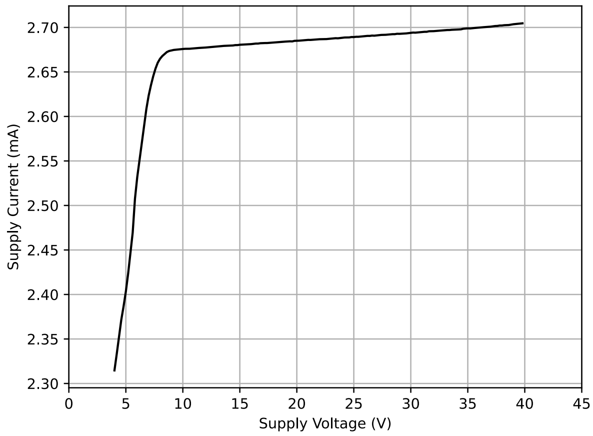


Figure 29. Supply Current vs Supply Voltage

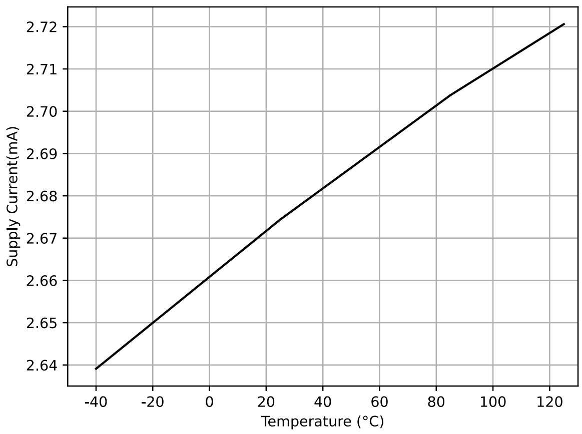


Figure 30. Supply Current vs Temperature

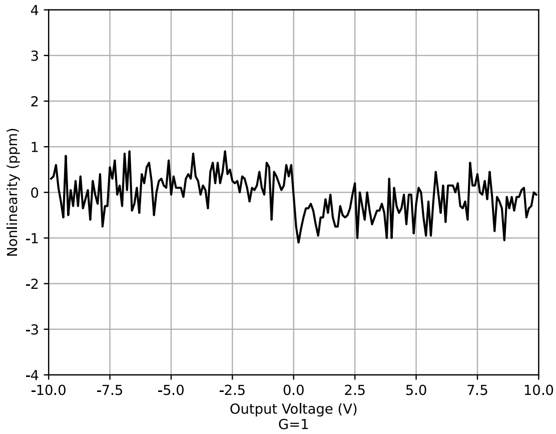


Figure 31. Gain Nonlinearity

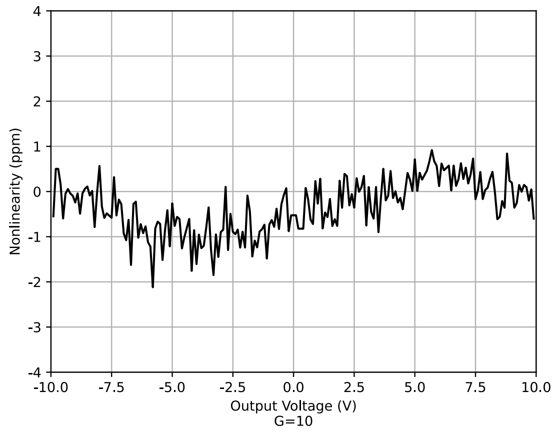


Figure 32. Gain Nonlinearity

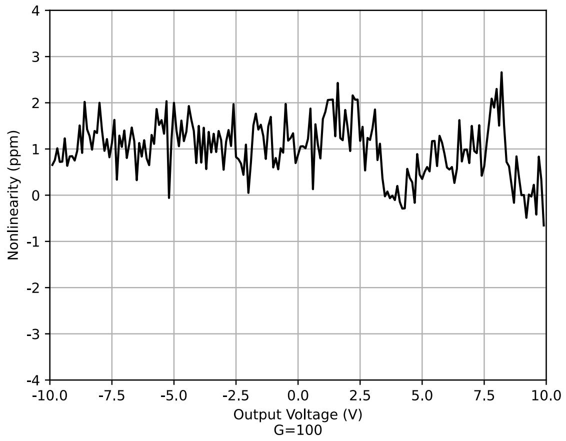


Figure 33. Gain Nonlinearity

7. Detailed Description

7.1. Overview

The LHAMP188 is a monolithic instrumentation amplifier (INA)that integrates laser-trimmed resistors to ensure excellent common mode rejection and low gain error. The combination of the zero-drift amplifier core and the precision resistors allows this device to achieve outstanding dc precision and makes the LHAMP188 ideal for many high-voltage industrial applications.

7.2. Functional Block Diagram

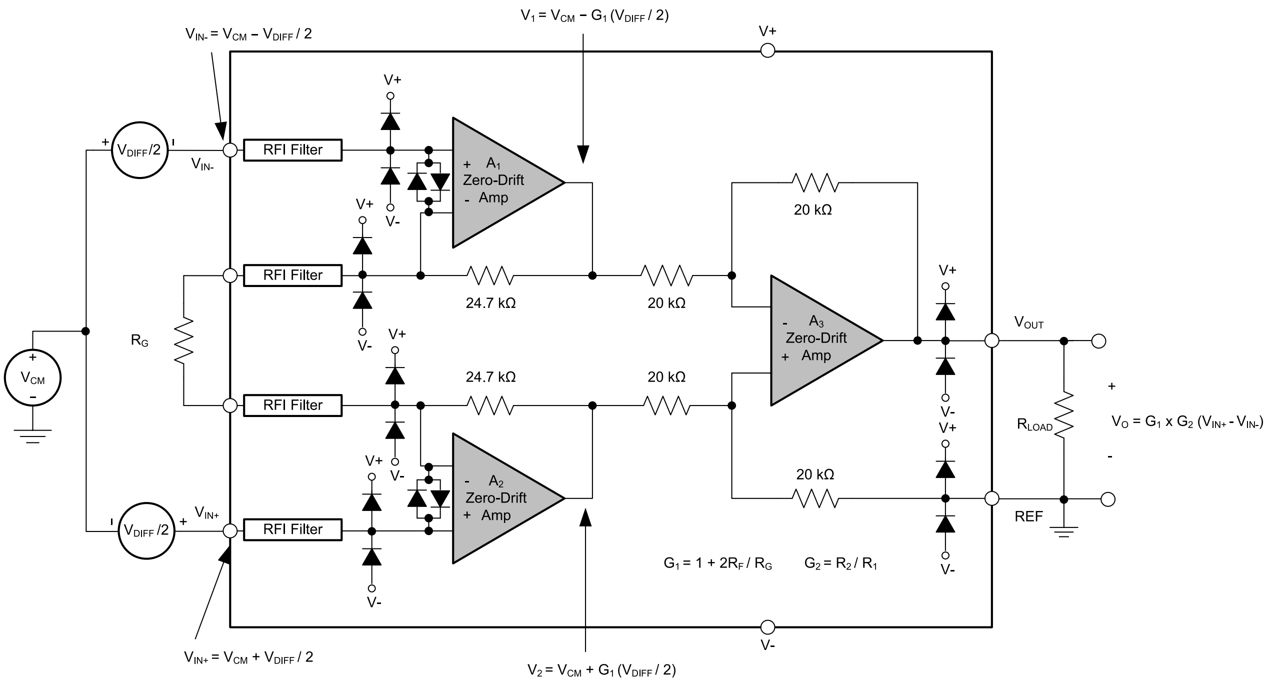


Figure 34. Functional Block Diagram

7.3. Feature Description

7.3.1 Inside the LHAMP188

The Functional Block Diagram section provides a detailed diagram for the LHAMP188, including the ESD protection and radio frequency interference (RFI) filtering. Instrumentation amplifiers are commonly represented in a simplified form, as shown in Figure 35.

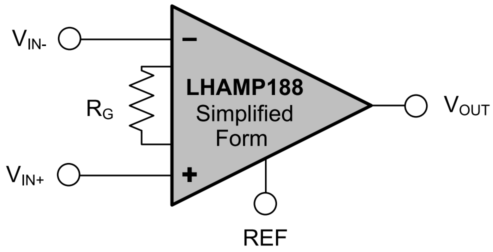


Figure 35. INA Simplified Form

A brief description of the internal operation is as follows:

The differential input voltage applied across R_G causes a signal current to flow through the R_G resistor and both R_F resistors. The output difference amplifier (A_3) removes the common-mode component of the input signal and refers the output signal to the REF pin.

The equations shown in the Functional Block Diagram section describe the output voltages of A_1 and A_2. Understanding the internal node voltages is useful to avoid saturating the device and to ensure proper device operation.

7.3.2 Setting the Gain

The gain of the LHAMP188 is set by a single external resistor, R_G. The value of R_G is selected according to Equation 1:

$$G=1+\frac{49.4\text{k}\Omega}{R_G} \tag{1}$$

Table 7 lists several commonly-used gains and resistor values. The 49.4-kΩ term in Equation 1 comes from the sum of the two internal 24.7-kΩ feedback resistors. These on-chip resistors are laser-trimmed to accurate absolute values. The accuracy and temperature coefficients of these resistors are included in the gain accuracy and drift specifications of the LHAMP188.

Table 7. Commonly-Used Gains and Resistor Values

DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC(1)	NC
2	49.4k	49.9k
5	12.35k	12.4k
10	5.489k	5.49k
20	2.6k	2.61k
50	1.008k	1.02k
100	499	511
200	248.2	249
500	99	100
1000	49.45	49.9

(1) NC denotes no connection.

8. Power Supply Recommendations

The minimum power-supply voltage for the LHAMP188 is ±2 V and the maximum power-supply voltage is ±18 V. This minimum and maximum range covers a wide range of power supplies. However, for optimum performance, ±15 V is recommended. A 0.1-μF bypass capacitor is recommended to be added at the input to compensate for the layout and power-supply source impedance.

9. Layout

9.1. Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Care must be taken to ensure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals. In addition, parasitic capacitance at the gain-setting pins can also affect CMRR over frequency. For example, in applications that implement gain switching using switches relays to change the value of RG, select the component so that the switch capacitance is as small as possible.
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of the device itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 8, keeping R_G close to the pins minimizes parasitic capacitance.
- Keep the traces as short as possible.

9.2. Layout Example

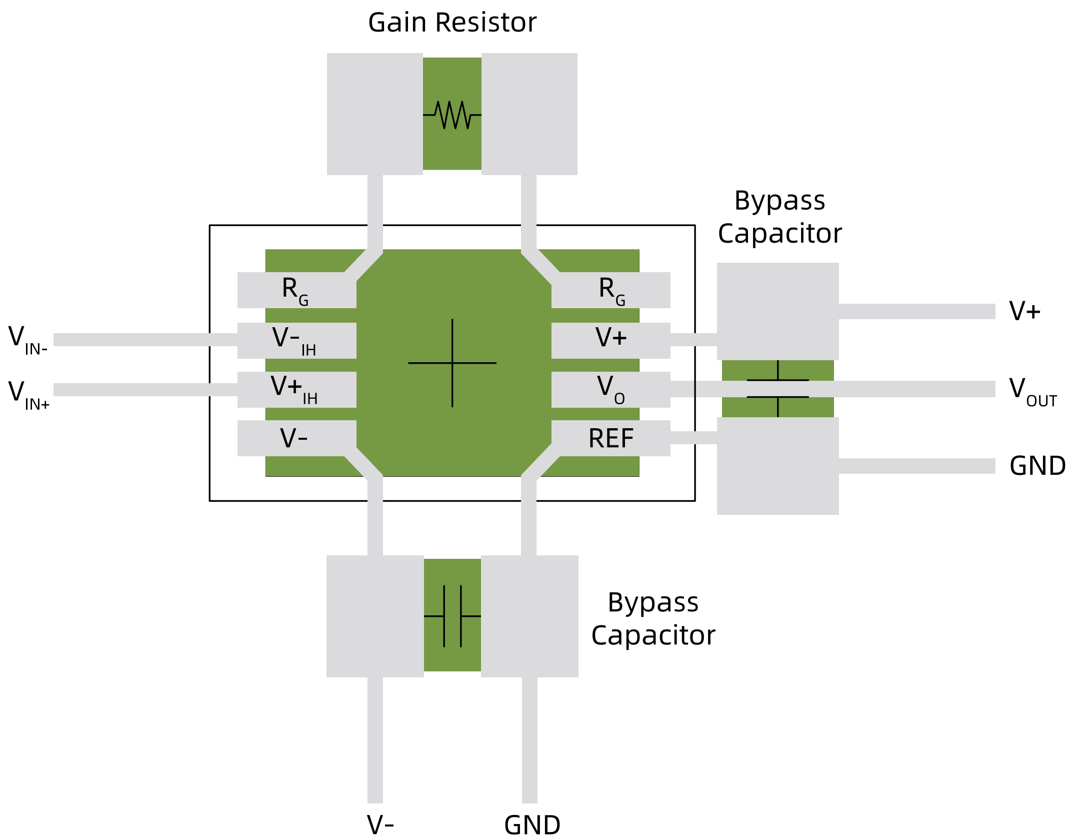
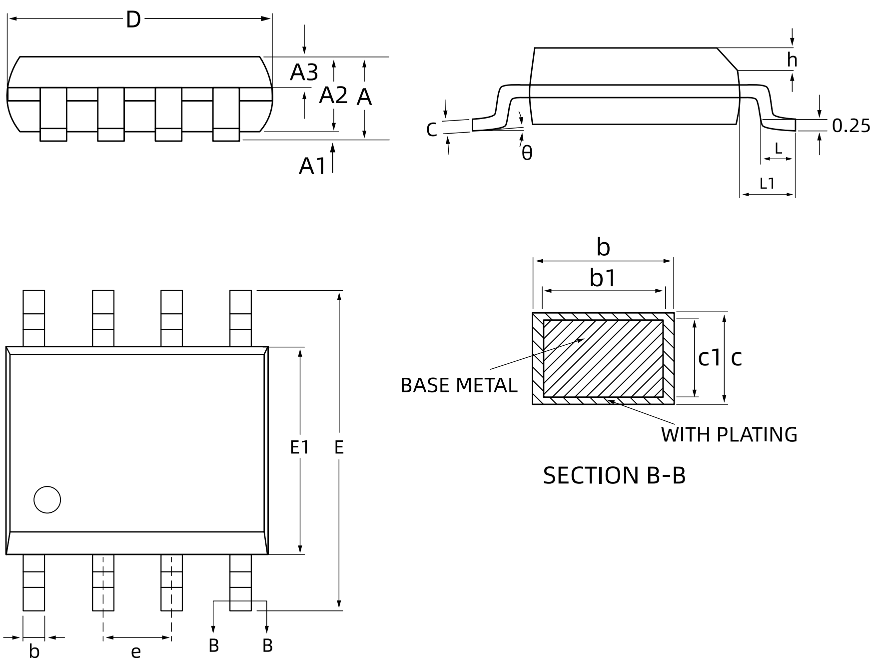


Figure 36. PCB Layout Example

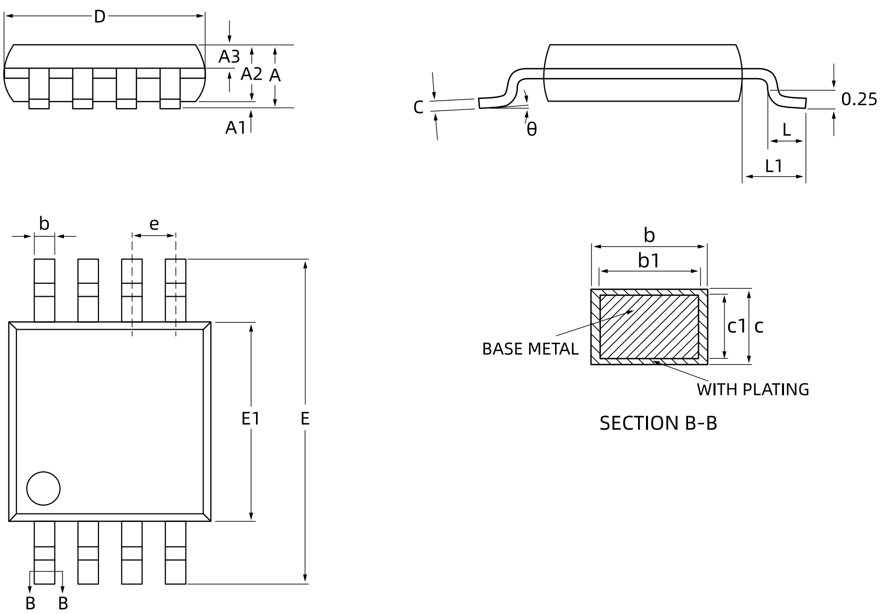
10. Package size

SOP8



	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
	A	—	—	1.75
	A1	0.10	—	0.225
	A2	1.30	1.40	1.50
	A3	0.60	0.65	0.70
△1	b	0.39	—	0.47
△1	b1	0.38	0.41	0.44
△1	c	0.20	—	0.24
	c1	0.19	0.20	0.21
△1	D	4.80	4.90	5.00
	E	5.80	6.00	6.20
△1	E1	3.80	3.90	4.00
	e	1.27BSC		
	h	0.25	—	0.50
	L	0.50	—	0.80
	L1	1.05REF		
	θ	0	—	8°

MSOP8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A1	0.05	—	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.28	—	0.36
b1	0.27	0.30	0.33
c	0.15	—	0.19
c1	0.14	0.15	0.16
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.65BSC		
L	0.40	—	0.70
L1	0.95REF		
θ	0	—	8°

11. Packaging Information

Table 8. Packaging information

Orderable Device	Package Type	Pin number	Op Temp (°C)	MPQ	Remark
LHAMP188FAA	SOP	8	-40 to 125	2500EA/REEL	
LHAMP189FAA	SOP	8	-40 to 125	2500EA/REEL	
LHAMP188FMA	MSOP	8	-40 to 125	3000EA/REEL	
LHAMP189FMA	MSOP	8	-40 to 125	3000EA/REEL	