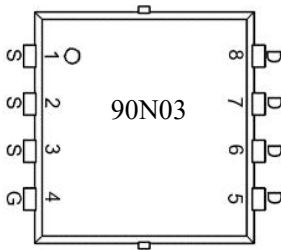
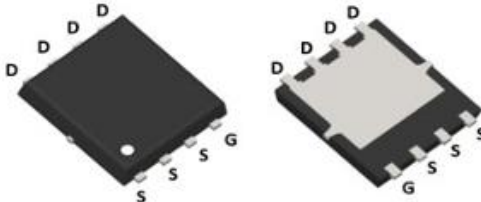
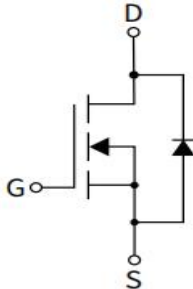


Features ➤ Super Low Gate Charge ➤ 100% EAS Guaranteed ➤ Green Device Available ➤ Excellent CdV/dt effect decline ➤ Advanced high cell density Trench technology	Bvdss	Rdson	ID
	30V	3.5mΩ	90A
	Application ➤ PWM applications ➤ Load Switch ➤ Power management		



Package		
		

Marking and pin assignment

PDFN3*3-8L top view

Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
90N03	90N03D	PDFN3*3-8L	5000

Absolute Maximum Ratings ($T_J=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ¹	I_D	90	A
Continuous Drain Current ¹	I_D	45	A
Pulsed Drain Current ²	I_{DM}	290	A
Single Pulsed Avalanche Energy ³	EAS	196	mJ
Avalanche Current	I_{AS}	36	A
Power Dissipation ⁴	$P_D@T_C=25^{\circ}\text{C}$	46	W
Junction Temperature	T_J	-55 ~ 175	$^{\circ}\text{C}$
Storage Temperature	T_{STG}	-55 ~ 175	$^{\circ}\text{C}$



Thermal Resistance Ratings

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Case ¹	$R_{\theta JC}$	--	1.72	°C/W
Thermal Resistance, Junction-to-Ambient ¹	$R_{\theta JA}$	--	62	°C/W

Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HL90N03D	PDFN3*3-8L	4	5,6,7,8	1,2,3	Tape Reel

Electrical Characteristics (T_J=25°C, unless otherwise specified)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=30V, V_{GS}=0V, T_J=25^\circ C$	-	-	1	μA
		$V_{DS}=30V, V_{GS}=0V, T_J=100^\circ C$	-	-	100	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	1.6	2.5	V
Static Drain-Source On-Resistance ²	$R_{DS(on)}$	$V_{GS}=10V, I_D=30A$	-	3.5	4.6	m Ω
		$V_{GS}=4.5V, I_D=15A$	-	7.8	10	
Forward Transconductance	g_{fs}	$V_{DS}=10V, I_D=30A$	-	80	-	S
Gate Resistance	R_g	$V_{DS}=0V, V_{GS}=0V, f=1MHz$	-	2	-	Ω
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V,$ $f=1.0MHz$	-	2088	-	pF
Output Capacitance	C_{oss}		-	277	-	
Reverse Transfer Capacitance	C_{rss}		-	209	-	
Total Gate Charge	Q_g	$V_{DS}=15V, V_{GS}=4.5V,$ $I_D=30A$	-	20	-	nC
Gate-Source Charge	Q_{gs}		-	5	-	
Gate-Drain Charge	Q_{gd}		-	7.2	-	
Turn-on Delay Time	$T_{d(on)}$	$V_{GS}=10V, V_{DD}=15V,$ $R_G=3\Omega, I_D=30A$	-	9	-	nS
Turn-on Rise Time	t_r		-	16	-	
Turn-Off Delay Time	$T_{d(off)}$		-	43	-	
Turn-Off Fall Time	T_f		-	12	-	
Maximum Continuous Drain to Source Diode Forward Current ^{1,5}	I_S	$V_G=V_D=0V, \text{Force Current}$	-	-	90	A
Maximum Pulsed Drain to Source Diode Forward Current	I_{SM}	--	-	-	-	A
Diode Forward Voltage ²	V_{SD}	$V_{GS}=0V, I_S=1A, T_J=25^\circ C$	-	-	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	--	-	-	-	nS
Body Diode Reverse Recovery Charge	Q_{rr}		-	-	-	nC



Notes:

1. The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
2. The data tested by pulsed, pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
3. The EAS data shows Max. rating. The test condition is $T_J=25^\circ\text{C}$, $V_{DD}=24\text{V}$, $V_{GS}=10\text{V}$, $L=0.1\text{mH}$, $I_{AS}=36\text{A}$.
4. The power dissipation is limited by 150°C junction temperature.
5. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

Typical Characteristics

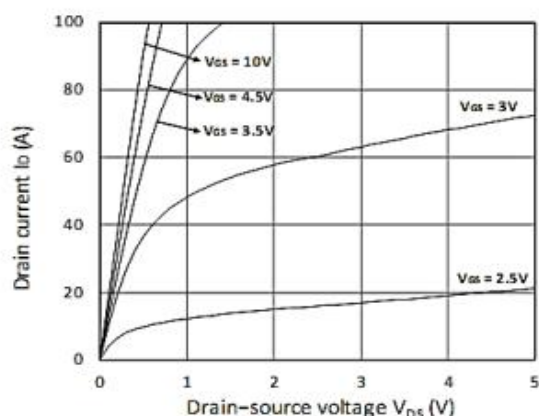


Figure 1. Output Characteristics

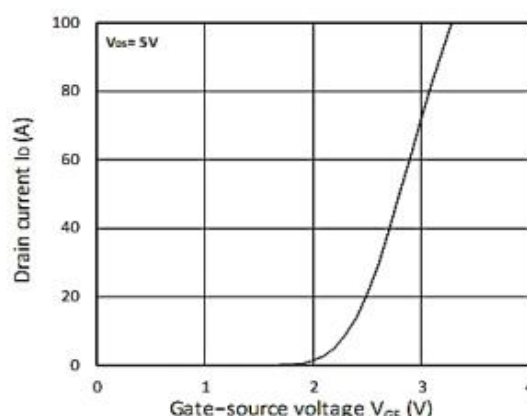


Figure 2. Transfer Characteristics

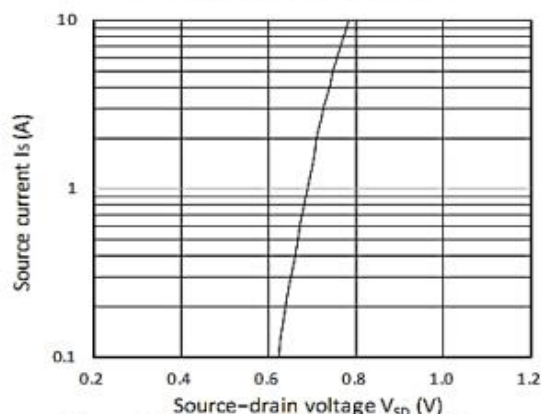


Figure 3. Forward Characteristics of Reverse

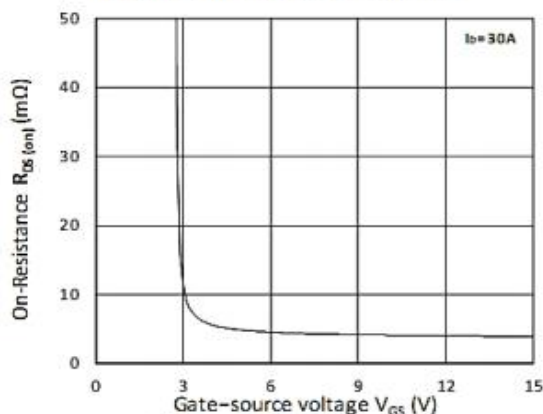


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

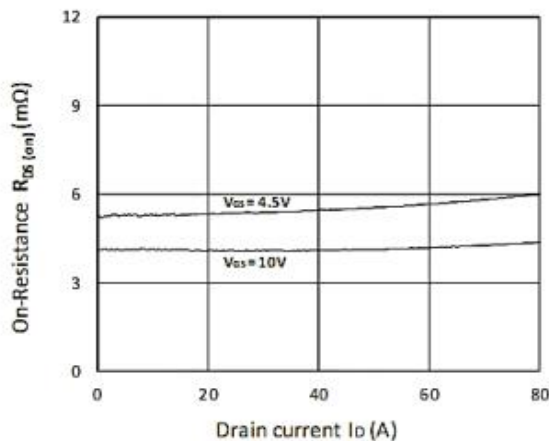


Figure 5. $R_{DS(ON)}$ vs. I_D

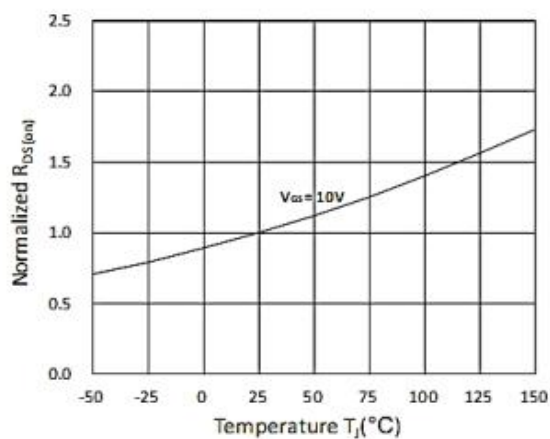


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

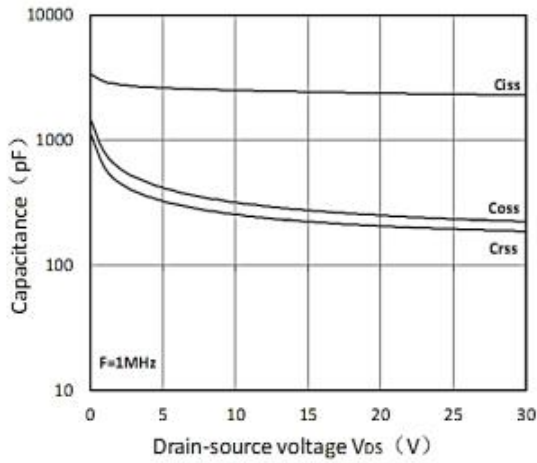


Figure 7. Capacitance Characteristics

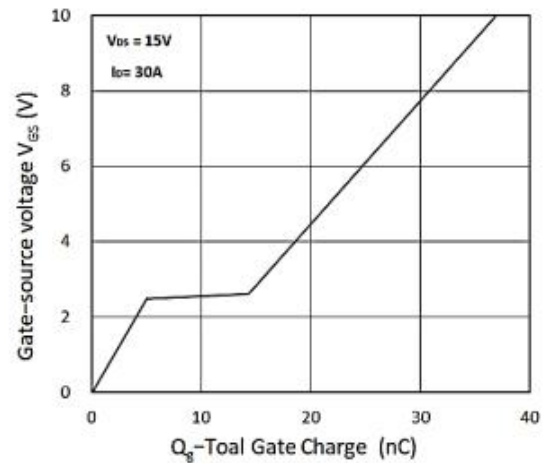


Figure 8. Gate Charge Characteristics

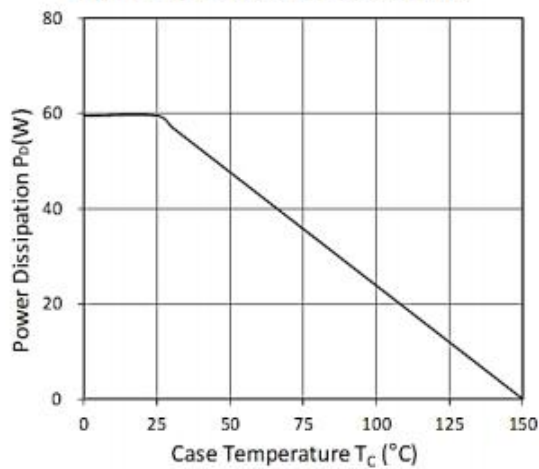


Figure 9. Power Dissipation

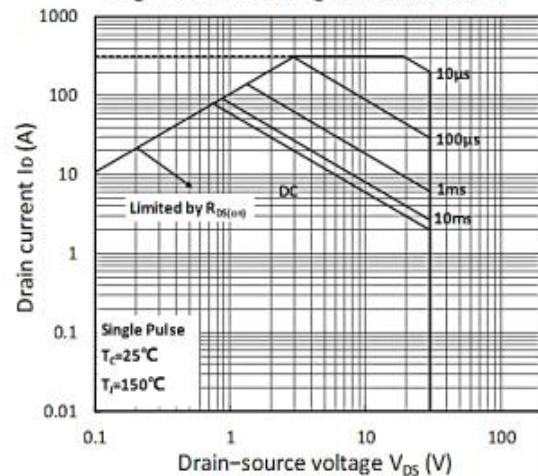


Figure 10. Safe Operating Area

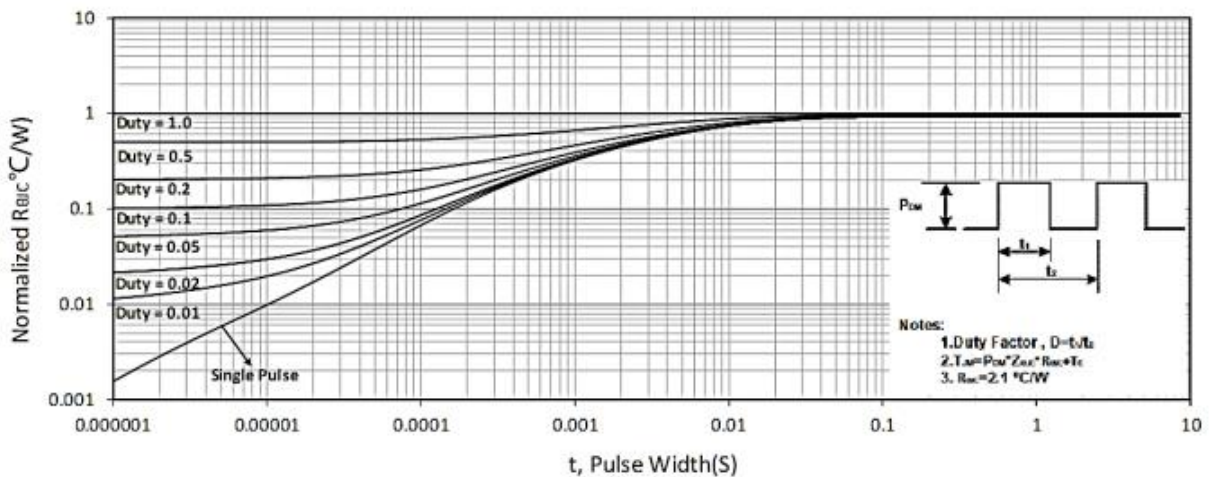
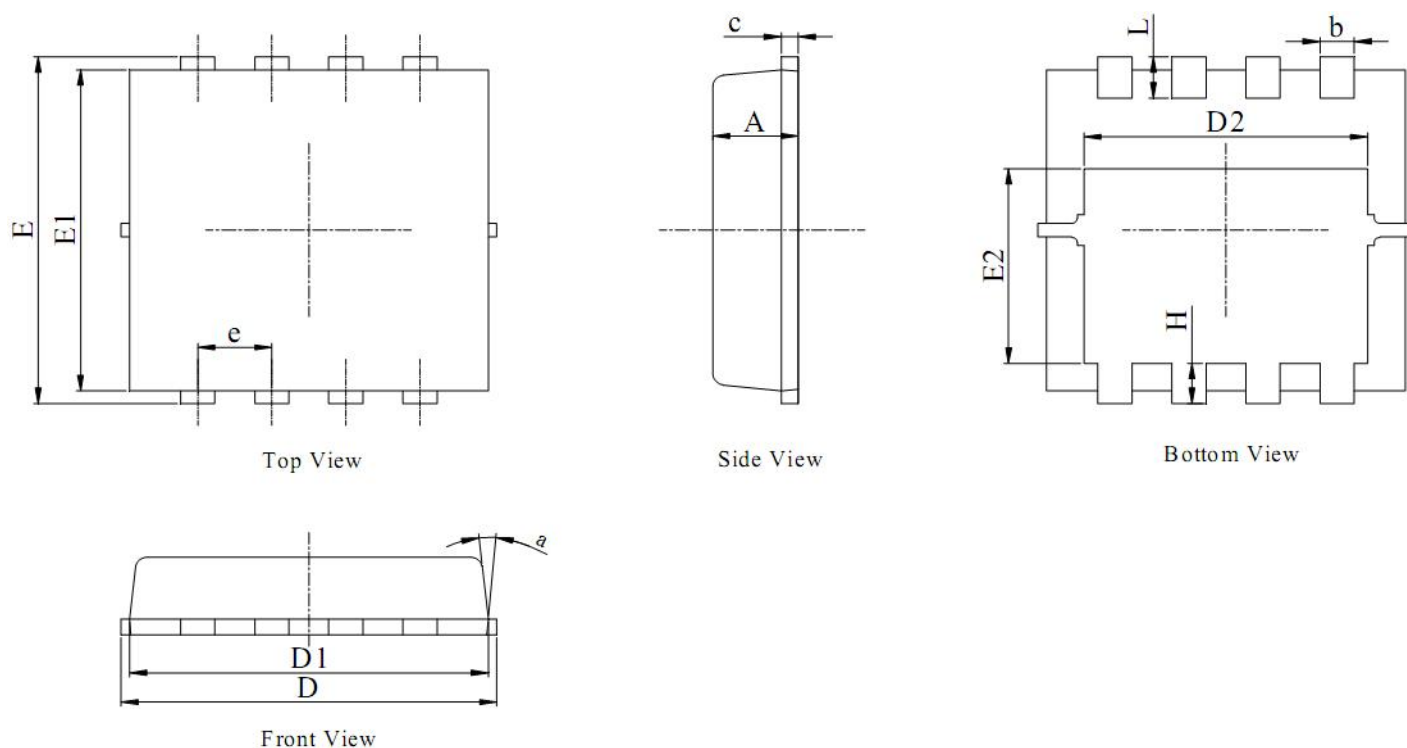


Figure 11. Normalized Maximum Transient Thermal Impedance

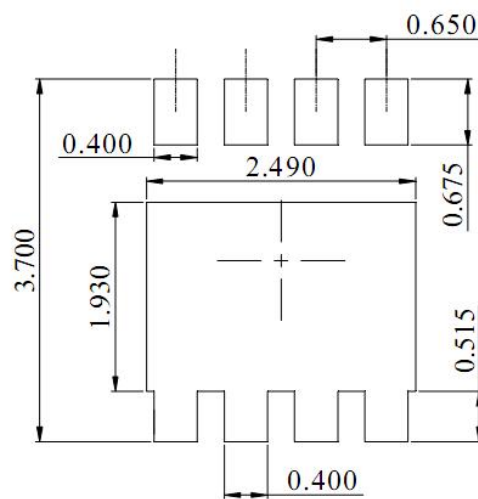
Package Dimensions PDFN3x3-8L



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. ALL DIMNESIONS IN MILLIMETER (ANNGLE IN DEGREE).
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.20	0.25
D	3.00	3.15	3.25
D1	2.95	3.05	3.15
D2	2.39	2.49	2.59
E	3.20	3.30	3.40
E1	2.95	3.05	3.15
E2	1.70	1.80	1.90
e	0.65 BSC		
H	0.30	0.40	0.50
L	0.25	0.40	0.50
a	---	---	15°



DIMENSIONS:MILLIMETERS



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