PRODUCT NOTIFICATION

DEVICE	LITERATURE NO.
TLV320AIC12	SLWS115
TLV320AIC13	SLWS139
TLV320AIC14	SLWS140
TLV320AIC15	SLWS141
TLV320AIC20	SLAS363
TLV320AIC21	SLAS365
TLV320AIC24	SLAS366
TLV320AIC25	SLAS367

Texas Instruments (TI) has recently identified a problem in the product models listed above related to DLL clock-generation. When a clock-generation mode is used that powers up the delay-locked-loop (DLL), the DLL may not startup properly when initiated, resulting in the audio master clock not functioning. This results in the codec in the products not functioning. This issue does not affect applications that do not enable the product's DLL.

Since this issue does not affect operation if the DLL is not enabled, customers are recommended to ensure their system does not enable the product's DLL. The DLL is enabled anytime the *P* value in control register #4 (pertaining to clock generation) is NOT set equal to 8. The DLL is used whenever the part is in *fine* sampling mode, as described in Section 3.1 of the data manual, so the recommended mode to use is the *coarse* sampling mode, which requires P=8.

At present, TI does not have a screening procedure in place to detect product with the DLL issue, but the company also realizes that many customers do not use the DLL in their systems and will be unaffected by this issue.

TI is not confident of the operation of the DLL in this product at this time. To ensure customers have been made aware of this issue, orders for these parts will only be filled upon return of a signed waiver until this issue is resolved. The company has initiated an investigation to fully understand the root cause of this problem and determine what appropriate long-term corrective action should be taken. TI recommends that all customers presently using these parts contact the company immediately, so they can receive updates on this investigation and plans for its resolution.

We apologize for the inconvenience placed upon customers in ordering this product. However, we wish to ensure that our customers are aware of the device shortcomings from the specification. We are working in earnest to remove this waiver requirement.

For further information, please contact

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TEXAS INSTRUMENTS

TLV320AIC15

SMARTDM™ Low-Power, Low-Voltage, 1.1-V to 3.6-V I/O, 16-Bit, 26-KSPS Codec

Data Manual

May 2002

HPA Data Acquisition

SLWS141A

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1 Introduction

The TLV320AIC15 is a true low-cost, low-power, high-performance, highly-integrated voiceband codec designed with new technological advances. The TLV320AIC15 provides high resolution signal conversion from digital-to-analog (D/A) and from analog-to-digital (A/D) using oversampling sigma-delta technology with programmable sampling rate.

1.1 Description

The TLV320AIC15 implements the smart time division multiplexed serial port (SMARTDM™). This is TI's design innovation to optimize DSP performance with its most advanced synchronous serial port in TDM format for glue-free interface to popular DSPs (i.e., C5x, C6x) and microcontrollers. The SMARTDM supports both continuous data transfer mode and on-the-fly reconfiguration programming mode. SMARTDM maximizes the bandwidth of data transfer between the TLV320AIC15 DSP codec and the DSP. In normal operation, it automatically detects the number of codecs in the serial interface and adjusts the number of time slots to match the number of codecs so that no time slot in the TDM frame is wasted. In the turbo mode, it maintains the same number of time slots but maximizes the bit transferred rate to 25 MHz to give the DSP more bandwidth to process other tasks in the same sampling period. The SMARTDM technology allows up to 16 codecs to share a single 4-wire serial bus.

The TLV320AIC15 also provides a flexible host port. The host port interface is a two-wire serial interface that can be programmed to be either an industrial standard I^2C or a simple S^2C (start-stop communication protocol).

The TLV320AIC15 also integrates all of the critical functions needed for most voice-band applications including MIC preamp, handset/headset preamps, antialiasing filter (AAF), input/output programmable gain amplifier (PGA), and selectable low-pass IIR/FIR filters.

The TLV320AIC15 implements an extensive power management; including device power-down, independent software control for turning off ADC, DAC, op-amps, and IIR/FIR filter (bypassable) to maximize system power conservation. The TLV320AIC15 consumes only 10 mW at 3 V.

The TLV320AIC15's low power operation from 2.7-V to 3.6-V for analog and I/O and 1.65 V to 1.95 V for digital core power supplies, along with extensive power management, make it ideal for portable applications including wireless accessories, hands free car kits, VOIP, cable modem, and speech processing. Its low group delay characteristic makes it suitable for single or multichannel active control applications.

The wide range of low-voltage I/O (1.1 V–3.6 V) enables the AIC15 to interface with a single power supply, or with dual power supplies for mixed low-voltage DSP systems such as the TMS320UC54x. This feature eliminates the need for external level-shifting and reduces power consumption.

The TLV320AIC15 is characterized for commercial operation from 0°C to 70°C and industrial operation from –40°C to 85°C.

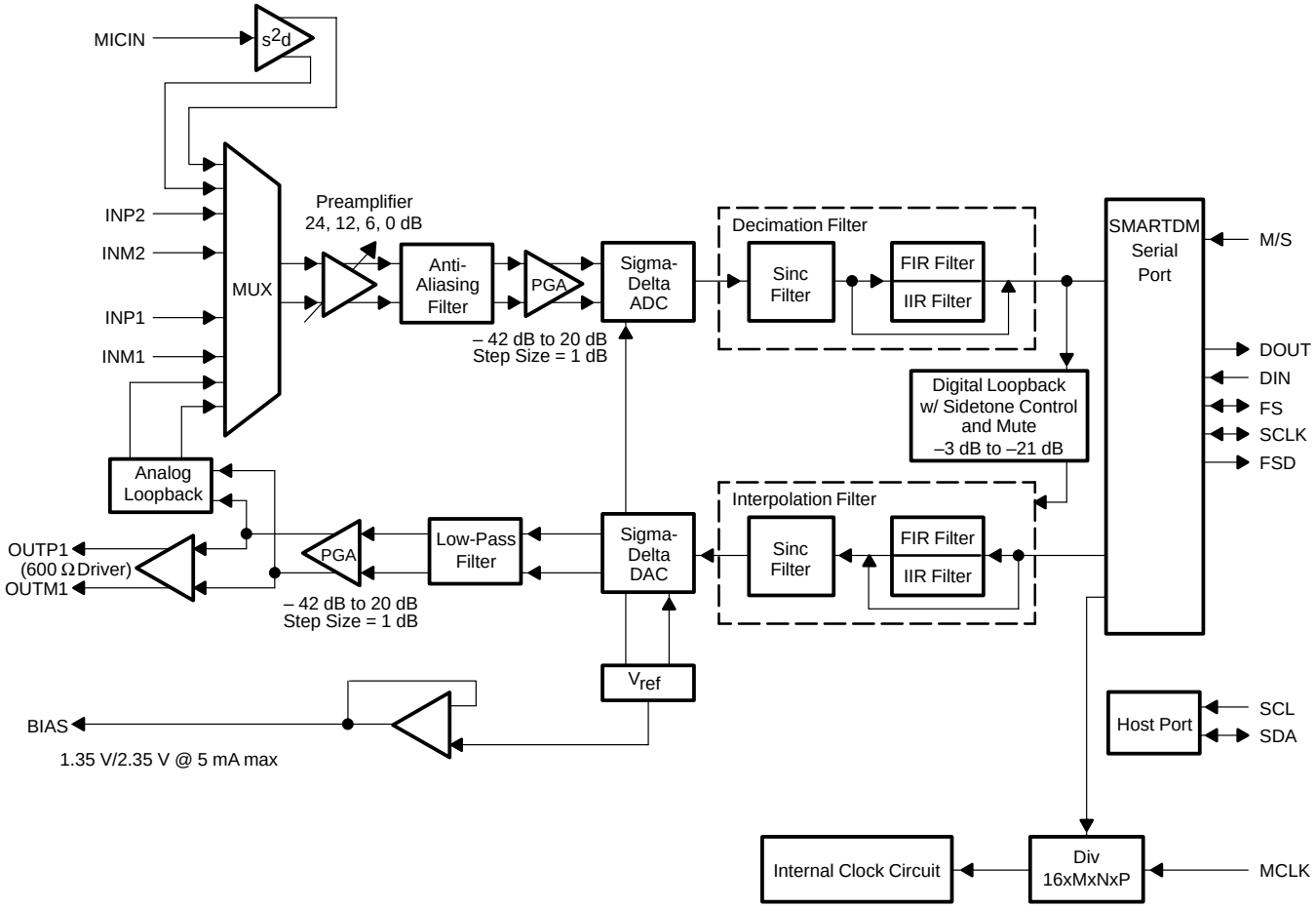
1.2 Features

- C54x Software Driver Available
- 16-Bit Oversampling Sigma-Delta A/D Converter
- 16-Bit Oversampling Sigma-Delta D/A Converter
- Support Maximum Master Clock of 100 MHz to Allow DSPs Output Clock to Be Used as Master Clock
- Selectable FIR/IIR Filter With Bypassing Option

SMARTDM is a trademark of Texas Instruments.

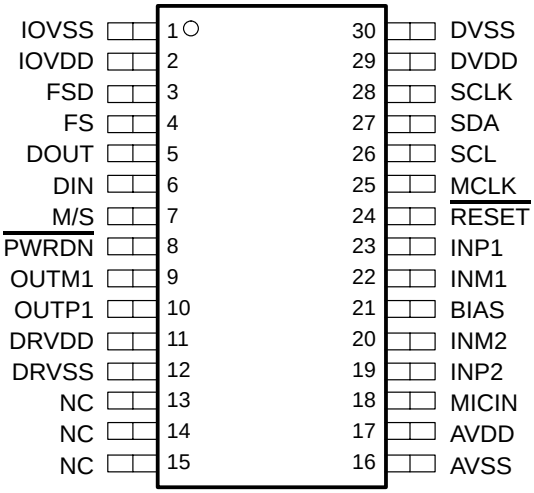
- Programmable Sampling Rate up to:
  - Max 26 KSPS With On-Chip IIR/FIR Filter
  - Max 104 KSPS With IIR/FIR Bypassed
- On-Chip FIR Produced 84-dB SNR for ADC and 91-dB SNR for DAC Over 13-kHz BW
- External DSPs IIR/FIR for a Final Sampling Rate of 8 Ksps (IIR/FIR Bypassed) Produced 87-dB SNR for ADC and 92-dB SNR for DAC.
- Smart Time Division Multiplexed Serial Port (SMARTDM)
  - Glueless 4-Wire Interface to DSP
  - Automatic Cascade Detection (ACD) Self-Generates Master/Slave Device Addresses
  - Programming Mode to Allow On-the-Fly Reconfiguration
  - Continuous Data Transfer Mode to Support DSP's DMA/Autobuffering Mode
  - Turbo Mode to Maximize Bit Clock for Faster Data Transfer and Higher Data Bandwidth
  - Total Number of Time Slots Dynamically Proportional to Number of Codecs in the Cascade to Eliminate Unused Time Slots and Optimize DSP Memory Allocation
  - Allows up to 16 Codecs to Be Connected to a Single Serial Port
- Host Port
  - 2-Wire Interface
  - Selectable I^2C or S^2C
- Differential and Single-Ended Analog Input/Output
- Built-In Functions:
  - Sidetone
  - Antialiasing Filter (AAF)
  - Programmable Input and Output Gain Control (PGA)
  - Microphone Amplifiers
  - Power Management With Hardware/Software Power-Down Modes 30 μW
- Separate Software Control for ADC and DAC Power Down
- Fully Compatible With TI C54x DSP Power Supplies
  - 1.65-V–1.95-V Digital Core Power
  - 1.1-V–3.6-V Digital I/O
  - 2.7-V–3.6-V Analog
- Power Dissipation (P_D) 10 mW at 3 V in Standard Operation
- Internal Reference Voltage (V_{ref})
- 2s Complement Data Format
- Test Mode Which Includes Digital Loopback and Analog Loopback

1.3 Functional Block Diagram



2 Terminal Descriptions

DBT PACKAGE
(TOP VIEW)



2.1 Ordering Information

T_A	30-TSSOP DBT PACKAGE
0°C to 70°C	TLV320AIC15C
–40°C to 85°C	TLV320AIC15I

2.2 Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AVDD	17	I	Analog power supply
AVSS	16	I	Analog ground
BIAS	21	O	Bias output voltage is software selectable between 1.35 V and 2.35 V. Its output current is 5 mA.
DIN	6	I	Data input. DIN receives the DAC input data and register data from the external DSP (digital signal processor) and is synchronized to SCLK and FS. Data is latched at the falling edge of SCLK when FS is low.
DOUT	5	O	Data output. DOUT transmits the ADC output bits and registers data, and is synchronized to SCLK and FS. Data is sent out at the rising edge of SCLK when FS is low. Outside data/control frame, DOUT is put in 3-state.
DRVDD	11	I	Analog power supply for the 600-Ω driver
DRVSS	12	I	Analog ground for the 600-Ω driver
DVDD	29	I	Digital power supply
DVSS	30	I	Digital ground
FS	4	I/O	Frame sync. When FS goes low, DIN begins receiving data bits and DOUT begins transmitting data bits. In master mode, FS is internally generated and is low during the data transmission to DIN and from DOUT. In slave mode, FS is externally generated.
FSD	3	O	Frame sync delayed output. The FSD output synchronizes a slave device to the frame sync of the master device. FSD is applied to the slave FS input and is the same duration as the master FS signal. This pin must be pulled low if AIC15 is a stand-alone slave. It may be pulled high if the AIC15 is a stand-alone master or the last slave in the cascade.
INM1	22	I	Inverting analog input 1. It must be connected to AVSS if not used.
INM2	20	I	Inverting analog input 2. It must be connected to AVSS if not used.
INP1	23	I	Noninverting analog input 1. It must be connected to AVSS if not used.
INP2	19	I	Noninverting analog input 2. It must be connected to AVSS if not used.

2.2 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
IOVDD	2	I	Digital I/O power supply
IOVSS	1	I	Digital I/O ground
MCLK	25	I	Master clock. MCLK derives the internal clocks of the sigma-delta analog interface circuit.
MICIN	18	I	MIC preamplifier input. It must be connected to AVSS if not used.
M/S	7	I	Master/slave select input. When M/S is high, the device is the master, and when low it is a slave.
OUTM1	9	O	Inverting output of the DAC. OUTM1 is functionally identical with and complementary to OUTP1. This differential output can drive a minimum load of 600 Ω. This output can also be used alone for single-ended operation.
NC	13, 14, 15		
OUTP1	10	O	Noninverting output of the DAC. This differential output can drive a minimum load of 600 Ω. This output can also be used alone for single-ended operation.
$\overline{\text{PWRDN}}$	8	I	Power down. When $\overline{\text{PWRDN}}$ is pulled low, the device goes into a power-down mode, the serial interface is disabled, and most of the high-speed clocks are disabled. However, all the register values are sustained and the device resumes full-power operation without reinitialization when $\overline{\text{PWRDN}}$ is pulled high again. $\overline{\text{PWRDN}}$ resets the counters only and preserves the programmed register contents.
$\overline{\text{RESET}}$	24	I	Hardware reset. The reset function is provided to initialize all of the internal registers to their default values. The serial port is configured to the default state accordingly.
SCL	26	I	Programmable host port (I^2C or S^2C) clock input.
SCLK	28	I/O	Shift clock. SCLK signal clocks serial data into DIN and out of DOUT during the frame-sync interval. When configured as an output (M/S high), SCLK is generated internally by multiplying the frame-sync signal frequency by 16 and the number of codecs in cascade in standard and continuous mode. When configured as an input (M/S low), SCLK is generated externally and must be synchronous with the master clock and frame sync.
SDA	27	I/O	Programmable host port (I^2C or S^2C) data line.

2.3 Definitions and Terminology

Data Transfer Interval	The time during which data is transferred from DOUT and to DIN. The interval is 16 shift clocks and the data transfer is initiated by the falling edge of the FS signal in standard and continuous mode.
Signal Data	This refers to the input signal and all of the converted representations through the ADC channel and the signal through the DAC channel to the analog output. This is contrasted with the purely digital software control data.
Frame Sync	Frame sync refers only to the falling edge of the signal FS that initiates the data transfer interval
Frame Sync and Sampling Period	Frame sync and sampling period is the time between falling edges of successive FS signals.
f_S	The sampling frequency
ADC Channel	ADC channel refers to all signal processing circuits between the analog input and the digital conversion result at DOUT.
DAC channel	DAC channel refers to all signal processing circuits between the digital data word applied to DIN and the differential output analog signal available at OUTP1and OUTM.
Dxx	Bit position in the primary data word (xx is the bit number)
DSxx	Bit position in the secondary data word (xx is the bit number)
PGA	Programmable gain amplifier
IIR	Infinite impulse response
FIR	Finite impulse response

3 Functional Description

3.1 Operating Frequencies (see Notes)

The sampling frequency is the frequency of the frame sync (FS) signal whose falling edge starts digital-data transfer for both ADC and DAC. The sampling frequency is derived from the master clock (MCLK) input by the following equations:

- Coarse sampling frequency (default):

  The coarse sampling is selected by programming P = 8 in the control register 4, which is the default configuration of AIC15 on power-up or reset.

  FS = Sampling (conversion) frequency = MCLK / (16 × M × N × 8)

- Fine sampling frequency (see Note 5):

  FS = Sampling (conversion) frequency = MCLK/ (16 × M × N × P)

NOTES:
1. Use control register 4 to set the following values of M, N, and P
2. M = 1,2, . . . ,128
3. N = 1,2, . . . ,16
4. P = 1,2, . . . ,8
5. The fine sampling rate needs an on-chip Delay Lock Loop (frequency multiplier) to generate internal clocks. The DLL requires the relationship between MCLK and P to meet the following condition: 10 MHz ≤ (MCLK/P) ≤ 25 MHz
6. Both equations of FS require that the following conditions should be met:
   • (M × N × P) ≥ (devnum × mode) if the FIR/IIR filter is not bypassed.
   • [Integer(M/4) × N × P] ≥ (devnum × mode) if the FIR/IIR filter is bypassed.
   where
   devnum is the number of devices connecting in cascade
   mode is equal to 1 for continuous data transfer mode and 2 for programming mode
   EXAMPLE:
   The MCLK comes from the DSP C5402's CLKOUT and equals to 20.48 MHz and the conversion rate of 8 kHz is desired. First, set P = 1 to satisfy the condition 5 so that (MCLK/P) = 20.48 MHz/1 = 20.48 MHz. Next, pick M = 10 and N = 16 to satisfy condition 6 and derive 8 kHz for FS. That is,

   FS = 20.48 MHz/ (16 × 10 × 16 × 1) = 8 kHz

3.2 Internal Architecture

3.2.1 Antialiasing Filter

The built-in antialiasing filter is a two-pole filter that has a 20-dB attenuation at 1 MHz.

3.2.2 Sigma-Delta ADC

The sigma-delta analog-to-digital converter is a sigma-delta modulator with 128-x oversampling. The ADC provides high-resolution, low-noise performance using oversampling techniques. Due to the oversampling employed, only single pole R-C filters are required on the analog inputs.

3.2.3 Decimation Filter

The decimation filters are either FIR filters or IIR filters, selected by bit D5 of the control register 1. The FIR filter provides linear-phase output with $17/f_S$ group delay, whereas the IIR filter generates nonlinear phase output with negligible group delay. The decimation filters reduce the digital data rate to the sampling rate. This is accomplished by decimating with a ratio of 1:128. The output of the decimation filter is a 16-bit 2s-complement data word clocking at the sample rate selected for that particular data channel. The BW of the filter is ($0.45 \times$ FS) and scales linearly with the sample rate.

3.2.4 Sigma-Delta DAC

The sigma-delta digital-to-analog converter is a sigma-delta modulator with 128/256/512-x oversampling. The DAC provides high-resolution, low-noise performance using oversampling techniques. The oversampling ratio in DAC is programmable to 256/512 using bits D4–D3 of control register 3, the default being 128. Oversampling ratio of 512 can be used when FS is a maximum of 8 Ksps and an oversampling ratio of 256 can be used when FS is a maximum of 16 Ksps. M should be a multiple of 2 for an oversampling ratio of 256 and 4 for oversampling ratio of 512.

3.2.5 Interpolation Filter

The interpolation filters are either FIR filters or IIR filters selected by bit D5 of the control register 1. The FIR filter provides linear-phase output with $18/f_S$ group delay, whereas the IIR filter generates nonlinear phase output with negligible group delay. The interpolation filter resamples the digital data at a rate of 128/256/512 times the incoming sample rate, based on the oversampling rate of DAC. The high-speed data output from the interpolation filter is then used in the sigma-delta DAC. The BW of the filter is ($0.45 \times$ FS) and scales linearly with the sample rate.

3.2.6 Analog/Digital/Side-Tone Loopback

The analog and digital loopbacks provide a means of testing the data ADC/DAC channels and can be used for in-circuit system level tests. The analog loopback always has the priority to route the DAC low pass filter output into the analog input where it is then converted by the ADC to a digital word. The digital loopback routes the ADC output to the DAC input on the device. Analog loopback is enabled by writing a 1 to bit D2 in the control register 1. Digital loopback is enabled by writing a 1 to bit D1 in control register 1. The side-tone digital loopback attenuates the ADC output and mixes it with the input of the DAC. The level of the side tone is set by DSTG, bits D5–D3 of the control register 5C.

3.2.7 ADC PGA

TLV320AIC15 has a built-in PGA for controlling the signal levels at ADC outputs. ADC PGA gain setting can be selected by writing into bits D5–D0 of register 5A. The PGA range of the ADC channel is 20 dB to –42 dB in steps of 1 dB and mute. To avoid sudden jumps in signal levels with PGA changes, the gains are applied internally with zero-crossovers.

3.2.8 DAC PGA

TLV320AIC15 has a built-in PGA for controlling the analog output signal levels in DAC channel. DAC PGA gain setting can be selected by writing into bits D5–D0 of register 5B. The PGA range of the DAC channel is 20 dB to –42 dB in steps of 1 dB, and mute. To avoid sudden *pop-sounds* with power-up/down and gain changes, the power-up/down and gain changes for DAC channel are applied internally with zero-crossovers.

3.3 Analog Input/Output

The TLV320AIC15 has three programmable analog inputs and three programmable analog outputs. Bits D2–D1 of control register 6 select the analog input source from MICIN, INP1/M1, or INP2/M2. All analog I/O is either single-ended or differential. All analog input signals are self-biased to 1.35 V. The three analog outputs are configured by bits D7, D6, D5, and D4–D3 of control register 6.

3.3.1 MIC Input

TLV320AIC15 supports single-ended microphone input. This can be used by connecting the external single-ended source through ac-coupling to the MICIN pin. This channel is selected by writing 01 or 10 into bits D2–D1 in control register 6. The single ended input is supported in two modes.

Writing 01 into bits D2–D1 chooses self biased MICIN mode. In this mode the device internally self-biases the input at 1.35 V. For best noise performance the user must bias the microphone circuit using the BIAS voltage generated by the device as shown in Figure 5–19.

Writing 10 into bits D2–D1 chooses pseudodifferential MICIN mode. In this mode the single-ended input is connected through ac-coupling to MICIN and the bias voltage used to generate the signal is also ac-coupled to INM1 as shown in Figure 5–20. For best noise performance the MICIN and INM1 lines are routed in similar fashion from the microphone to the device for noise cancellation.

For high quality performance the single-ended signal is converted internally into differential signal before being converted. To improve the dynamic range with different types of microphones the device supports a pre-amplifier with gain settings of 0/6/12/24 dB. This can be chosen by writing into bits D1–D0 of control register 5C.

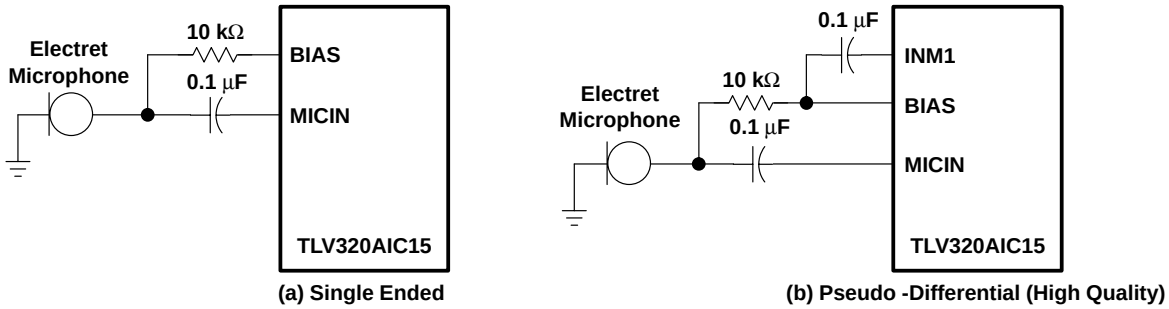


Figure 3–1. Microphone Interface

3.3.2 INP and INM Input

To produce common-mode rejection of unwanted signal performance, the analog signal is processed differentially until it is converted to digital data. The signal applied to the terminals INM1/2 and INP1/2 are differential to preserve device specifications (see Figure 3–2). The signal source driving analog inputs (INP1/2 and INM1/2) should have low source impedance for lowest noise performance and accuracy. To obtain maximum dynamic range, the signal should be ac-coupled to the input terminal.

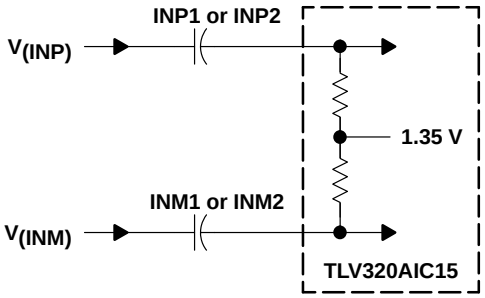


Figure 3–2. INP and INM Internal Self-Biased Circuit

3.3.3 Single-Ended Analog Input

The two differential inputs of (INP1/M1 and INP2/M2) can be configured to work as single-ended inputs by connecting INP to the analog input and INM to ground (see Figure 3–3).

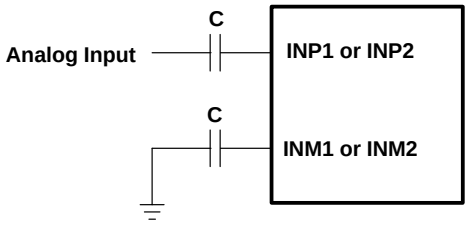


Figure 3–3. Single-Ended Input

3.3.4 Analog Output

The OUTP1 and OUTM1 are differential output from the DAC channel. The OUTP1 and OUTM1 can drive a load of 600-Ω directly and be either differential or single-ended (see Figure 3–4).

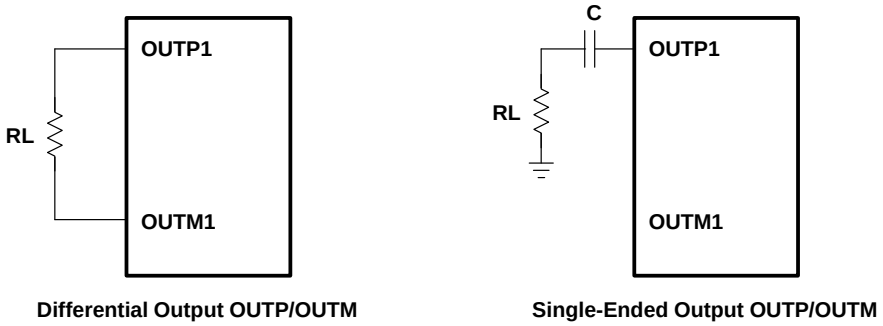


Figure 3–4. OUTP1/OUTM1 Output

3.4 IIR/FIR Control

3.4.1 Overflow Flags

The decimation IIR/FIR filter sets an overflow flag (bit D7) of control register 1 indicating that the input analog signal has exceeded the range of internal decimation filter calculations. The interpolation IIR/FIR filter sets an overflow flag (bit D4) of control register 1 indicating that the digital input has exceeded the range of internal interpolation filter calculations. When the IIR/FIR overflow flag is set in the register, it remains set until the user reads the register. Reading this value resets the overflow flag. These flags need to be reset after power-up by reading the register. If FIR/IIR overflow occurs, the input signal is attenuated by either the PGA or some other method.

3.4.2 IIR/FIR Bypass Mode

An option is provided to bypass IIR/FIR filter sections of the decimation filter and the interpolation filter. This mode is selected through bit D6 of control register 2 and effectively increases the frequency of the FS signal to four times normal output rate of the IIR/FIR-filter. For example, for a normal sampling rate of 8 Ksps (i.e., FS = 8 kHz) with IIR/FIR, if the IIR/FIR is bypassed, the frequency of FS is readjusted to 4×8 kHz = 32 kHz. The sinc filters of the two paths can not be bypassed. A maximum of eight devices in cascade can be supported in the IIR/FIR bypassed mode.

In this mode , the ADC channel outputs data which has been decimated only till 4Fs. Similarly DAC channel input needs to be pre-interpolated to 4Fs before being given to the device. This mode allows users the flexibility to implement their own filter in DSP for decimation and interpolation. M should be a multiple of 4 during IIR/FIR Bypass mode.

3.5 System Reset and Power Management

3.5.1 Software and Hardware Reset

The TLV320AIC15 resets internal counters and registers in response to either of two events:

- A low-going reset pulse is applied to terminal RESET
- A 1 is written to the programmable software reset bits (D5 of control register 3)

NOTE: The TLV320AIC15 requires a power-up reset applied to the RESET pin.

Either event resets the control registers and clears all sequential circuits in the device. The H/W RESET (active low) signal is at least 6 master clock periods long. As soon as the RESET input is applied, the TLV320AIC15 enters the initialization cycle that lasts for 132 MCLKs, during which the DSPs serial port is put in 3-state. For a cascaded system the rise time of H/W RESET needs to be less than the MCLK period and should satisfy setup time requirement of 2 ns with respect to MCLK rise-edge. In stand-alone-slave mode SCLK must be running during RESET. RESET must be synchronized with MCLK in all cases.

3.5.2 Power Management

Most of the device (except the digital interface) enters the power-down mode when D7 and D6, in control register 3, are set to 1. When the $\overline{\text{PWRDN}}$ pin is low, the entire device is powered down. In either case, register contents are preserved and the output of the amplifier is held at midpoint voltage to minimize pops and clicks.

The amount of power drawn during software power down is higher than during a hardware power down because of the current required to keep the digital interface active. Additional differences between software and hardware power-down modes are detailed in the following paragraphs.

3.5.2.1 Software Power-Down

Data bits D7 and D6 of control register 3 are used by TLV320AIC15 to turn on or off the software power-down mode, which takes effect in the next frame FS. The ADC and DAC can be powered down individually. In the software power-down, the digital interface circuit is still active while the internal ADC and DAC channel and differential output OUTP1 and OUTM1 are disabled, and DOUT is put in 3-state in the data frame only. Register data in the control frame is still accepted via DIN, but data in the data frame is ignored. The device returns to normal operation when D7 and D6 of control register 3 are reset.

3.5.2.2 Hardware Power-Down

The TLV320AIC15 requires the $\overline{\text{PWRDN}}$ signal to be synchronized with MCLK. When $\overline{\text{PWRDN}}$ is held low, the device enters hardware power-down mode. In this state, the internal clock control circuit and the differential outputs are disabled. All other digital I/Os are disabled and DIN can not accept any data input. The device can only be returned to normal operation by holding $\overline{\text{PWRDN}}$ high. When not holding the device in the hardware power-down mode, $\overline{\text{PWRDN}}$ must be tied high.

3.6 Digital Interface

3.6.1 Clock Source (MCLK, SCLK)

MCLK is the external master clock input. The clock circuit generates and distributes necessary clocks throughout the device. SCLK is the bit clock used to receive and transmit data synchronously. When the device is in the master mode, SCLK and FS are output and derived from MCLK in order to provide clocking the serial communications between the device and a digital signal processor (DSP). When in the slave mode, SCLK and FS are inputs. In the non-turbo mode (TURBO = 0), SCLK frequency is defined by:

$$\text{SCLK} = (16 \times \text{FS} \times \#\text{Devices} \times \text{mode})$$

Where:

FS is the frame-sync frequency.
#Device is the number of the device in cascade.
Mode is equal to 1 for continuous data transfer mode and 2 for programming mode.

In turbo mode see Section 3.8.3.

3.6.2 Serial Data Out (DOUT)

DOUT is placed in the high-impedance state after transmission of the LSB is completed. In data frame, the data word is the ADC conversion result. In the control frame, the data is the register read results when requested by the read/write (R/W) bit. If a register read is not requested, the low eight bits of the secondary word are all zeroes. Valid data on DOUT is taken from the high-impedance state by the falling edge of frame-sync (FS). The first bit transmitted on the falling edge of FS is the MSB of valid data.

3.6.3 Serial Data In (DIN)

The data format of DIN is the same as that of DOUT, in which MSB is received first on the falling edge of FS. In a data frame, the data word is the input digital signal to the DAC channel. If (15+1)-bit data format is used, the LSB (D0) is set to 1 to switch from the continuous data transfer mode to the programming mode. In a control frame, the data is the control and configuration data that sets the device for a particular function as described in Section 3.9, Control Register Programming.

3.6.4 Frame-Sync FS

The frame-sync signal (FS) indicates the device is ready to send and receive data. FS is an output if the M/S pin is connected to HI (master mode) and an input if the M/S pin is connected to LO (slave mode).

Data is valid on the falling edge of the FS signal.

The frequency of FS is defined as the sampling rate of the TLV320AIC15 and derived from the master clock MCLK as followed (see Section 3.1 Operating Frequencies for details):

$$FS = MCLK / (16 \times P \times N \times M)$$

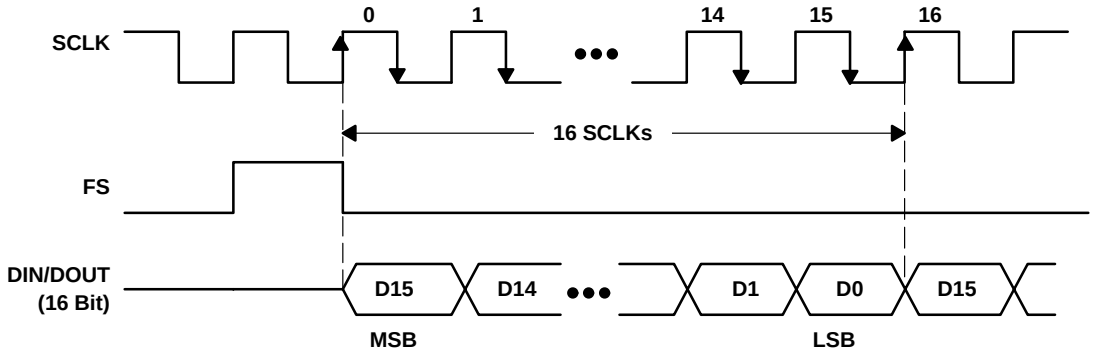


Figure 3–5. Timing Diagram of FS

3.6.5 Cascade Mode and Frame-Sync Delayed (FSD)

In cascade mode, the DSP receives all frame-sync pulses from the master though the master's FS. The master's FSD is output to the first slave and the first slave's FSD is output to the second slave device and so on. Figure 3–7 shows the cascade of 4 TLV320AIC15s in which the closest one to DSP is the master and the rest are slaves. The FSD output of each device is input to the FS terminal of the succeeding device. Figure 3–8 shows the FSD timing sequence in the cascade.

3.6.6 Stand-Alone Slave

In the stand-alone slave connection, the FS and SCLK are input in which they need to be synchronized to each other and programmed according to Section 3.1 (Operating Frequencies). The FS and SCLK input are not required to synchronize to the MCLK input but must remain active at all times to assure continuous sampling in the data converter.

FS is output for initial 132 MCLK and it must be kept low. DSP needs to keep FS low or 3-state for this period to avoid contention on FS.

3.6.7 Asynchronous Sampling (Codecs in cascade are sampled at different sampling frequency)

The AIC15s SMARTDM support different sampling frequency between the different codecs in cascade connecting to a single serial port. In this case, all codecs are required to sample at the same frequency that is the frequency of the FS signal. Then the desired sampling frequency of each codec is calculated by D2–D0 of control register 3. Example: fs1 and fs2 are desired sampling rates for CODEC1 and CODEC2 respectively:

1. FS = MCLK/(16xMxNxP)
2. FS = n1 x fs1 (n1 = 1,2, 0, 8 defined in the control register 3 of CODEC1)
3. FS = n2 x fs2 (n2 = 1,2, 0, 8 defined in the control register 3 of CODEC2)

For validating the conversion data from this operation:

For DAC: DSP need to give same data for n1 samples. CODEC1 picks one of n1 samples.

For ADC: CODEC1 gives same data for n1 samples. DSP should pick one of n1 samples.

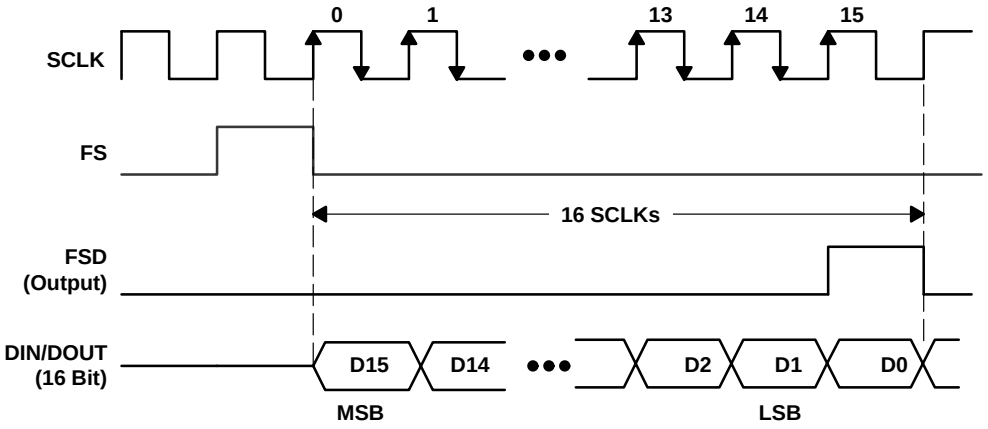


Figure 3–6. Timing Diagram for FSD Output

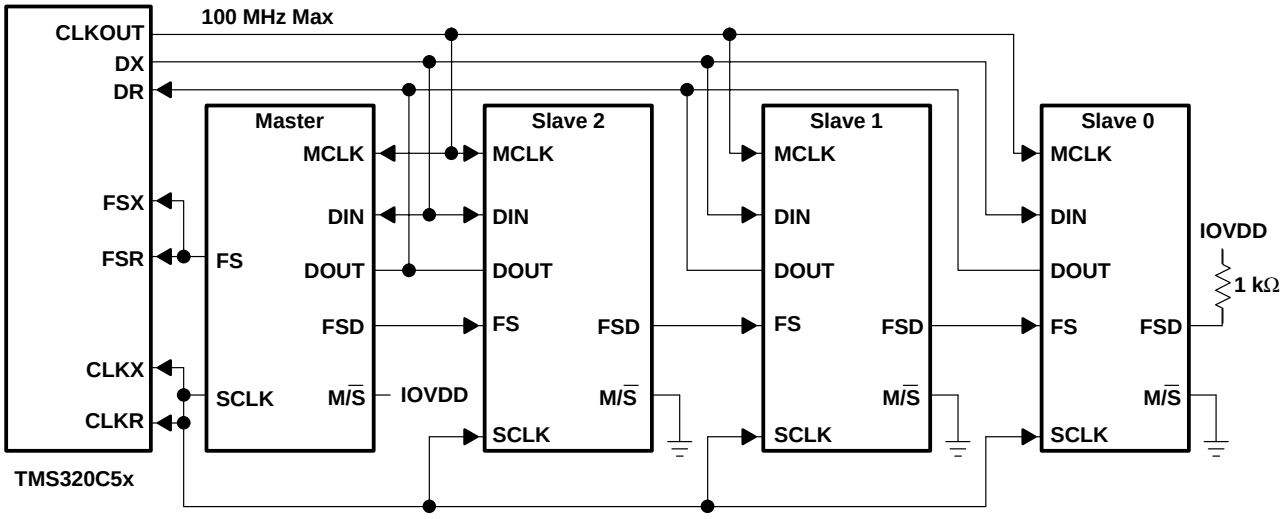
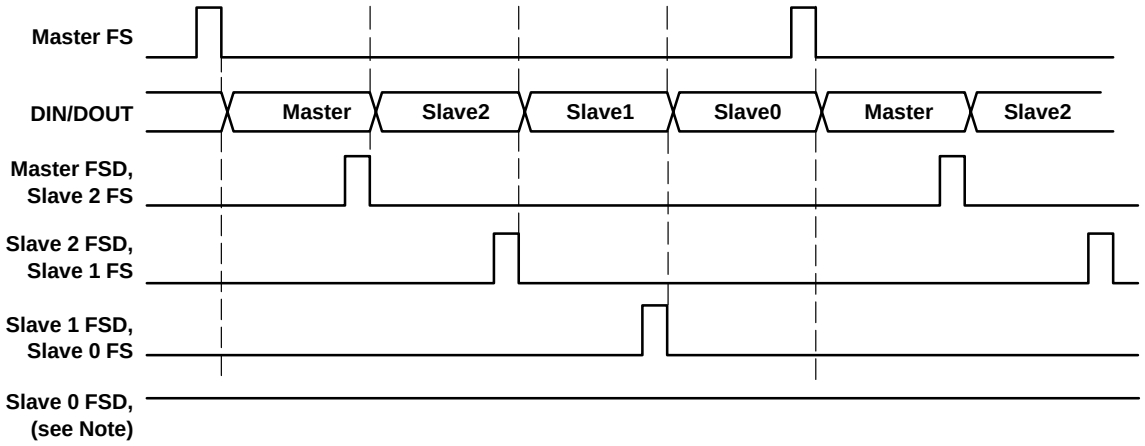


Figure 3–7. Cascade Connection (To DSP Interface)



NOTE: Slave 0 FSD should be pulled high for stand-alone-master or cascade configuration. FSD must be pulled low for stand-alone-slave configuration.

Figure 3–8. Master-Slave Frame-Sync Timing in Continuous Data Transfer Mode

3.7 Host Port Interface

The host port uses a 2-wire serial interface (SCL, SDA) to program the AIC15s six control registers and selectable protocol between S^2C mode and I^2C mode. The S^2C is a write-only mode and the I^2C is a read-write mode selected by setting the bits D1 and D0 of the control register 2 to 00 or 01. If the host interface is not needed, the two pins of SCL and SDA can be programmed to become general-purpose I/Os by setting the bits D1 and D0 of the control register 2 to 10 or 11. If selected to be used as I/O pins, the SDA and SCL pins become output and input pins respectively, determined by D1 and D0.

Both S^2C and I^2C require a SMARTDM device address to communicate with the AIC15. One of SMARTDMs advanced features is the automatic cascade detection (ACD) that enables SMARTDM to automatically detect the total number of codecs in the serial connection and use this information to assign each codec a distinct SMARTDM device address. Table 3–1 lists device addresses assigned to each codec in the cascade by the SMARTDM. The master always has the highest position in the cascade. For example, if there is a total of 8 codecs in the cascade (i.e., one master and 7 slaves), then the device addresses in row 8 are used in which the master is codec 7 with a device address of 0111.

Table 3–1. SMARTDM Device Addresses

TOTAL CODECS	CODECs POSITION IN CASCADE															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1																0000
2															0001	0000
3														0010	0001	0000
4													0011	0010	0001	0000
5												0100	0011	0010	0001	0000
6											0101	0100	0011	0010	0001	0000
7										0110	0101	0100	0011	0010	0001	0000
8									0111	0110	0101	0100	0011	0010	0001	0000
9								1000	0111	0110	0101	0100	0011	0010	0001	0000
10							1001	1000	0111	0110	0101	0100	0011	0010	0001	0000
11						1010	1001	1000	0111	0110	0101	0100	0011	0010	0001	0000
12					1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001	0000
13				1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001	0000
14			1101	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001	0000
15		1110	1101	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001	0000
16	1111	1110	1101	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001	0000

3.7.1 S^{2}C (Start-Stop Communication)

The S^{2}C is a write-only interface selected by programming bits D1-D0 of control register 2 to 01. The SDA input is normally in a high state, pulled low (START bit) to start the communication, and pulled high (STOP bit) after the transmission of the LSB. Figure 3–9 shows the timing diagram of S^{2}C. The S^{2}C also supports a broadcast mode in which the same register of all devices in cascade is programmed in a single write. To use S^{2}Cs broadcast mode, execute the following steps:

1. Write 111 1000 1111 1111 after the start bit to enable the broadcast mode.
2. Write data to program control register as specified in with bits D14–D11 = XXXX (don't care).
3. Write 111 1000 0000 0000 after the start bit to disable the broadcast mode.

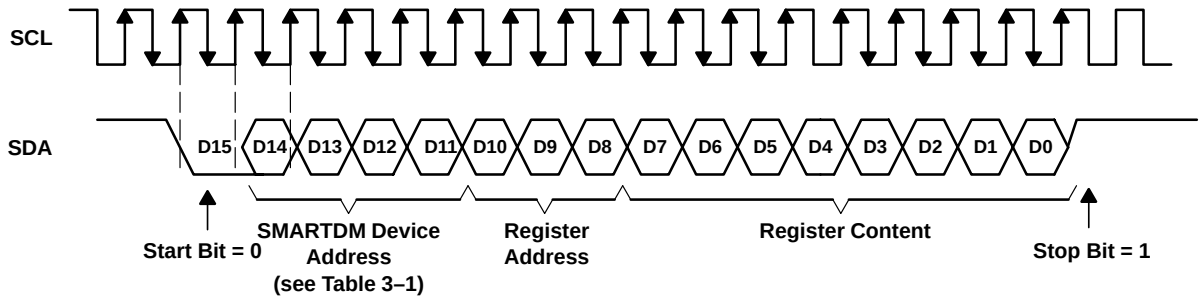


Figure 3–9. S^{2}C Programming

3.7.2 I^{2}C

- Each I^{2}C read-from or write-to AIC15s control register is given by index register address.
- Read/write sequence always starts with the first byte as I^{2}C address followed by 0. During the second byte, default/broadcast mode is set and the index register address is initialized. For write operation control register, data to be written is given from the third byte onwards. For read operation, stop-start is performed after the second byte. Now the first byte is I^{2}C address followed by 1. From the second byte onwards, control register data appears.
- Each time read/write is performed, the index register address is incremented so that next read/write is performed on the next control register.
- During the first write cycle and all write cycles in the broadcast, only the device with address 0000 issues ACK to the I^{2}C.

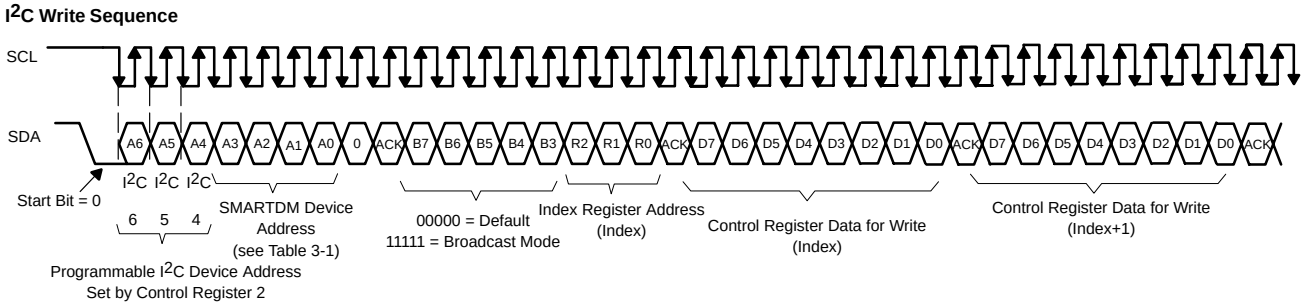


Figure 3–10. I^{2}C Write Sequence

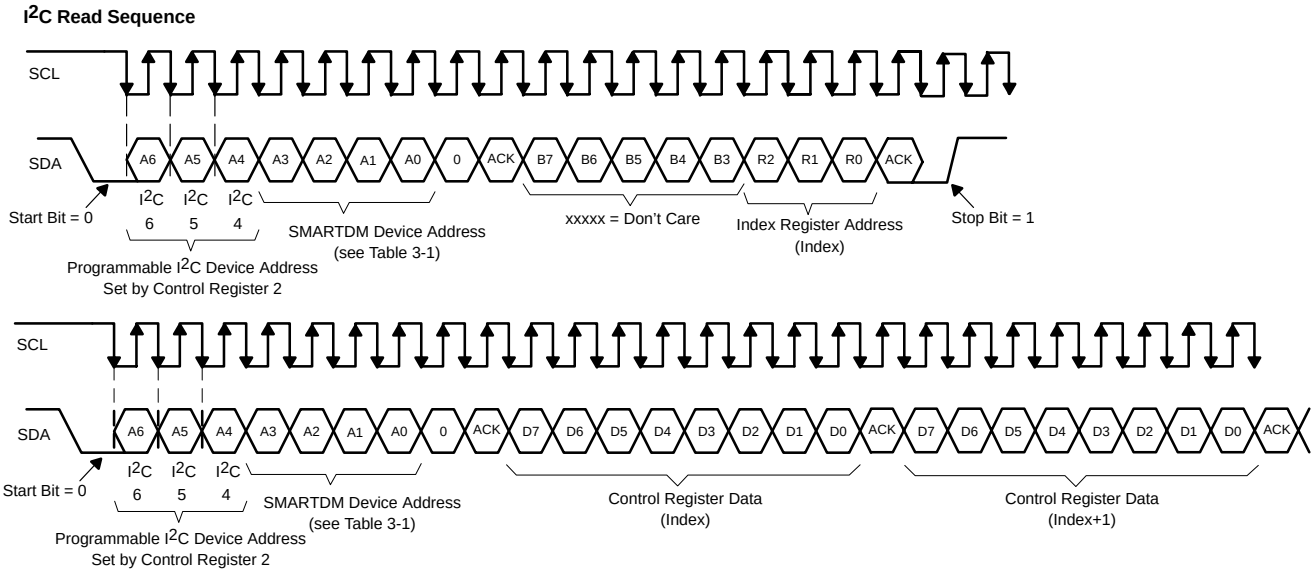


Figure 3–11. I²C Read Sequence

Each AIC has an index register address. To perform a write operation, make the LSB of the first byte as 0 (write) (see Figure 3–12). During the second byte, the index register address is initialized and mode (broadcast/default) is set. From the third byte onwards, write data to the control register (given by index register) and increment the index register until stop or repeated start occurs. For operation, make the LSB of the first byte as 1 (read). From the second byte onwards, AIC starts transmitting data from the control register (given by the index register) and increments the index register. For setting the index register perform operation the same as write case for 2 bytes, and then give a stop or repeated start.

S/Sr –> Start/Repeated Start.

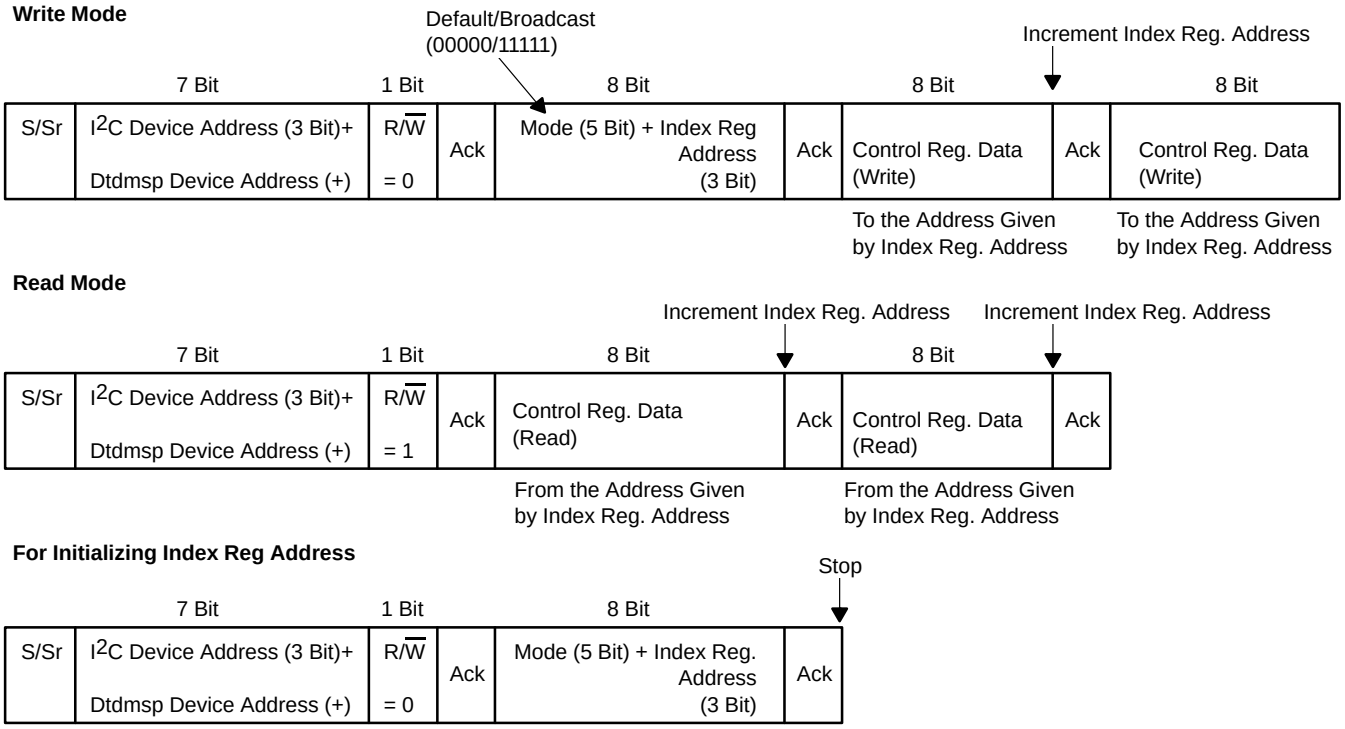


Figure 3–12. Index Register Addresses

3.8 Smart Time Division Multiplexed Serial Port (SMARTDM)

The smart time division multiplexed serial port (SMARTDM) uses the 4 wires of DOUT, DIN, SCLK, and FS to transfer data into and out of the AIC15. The TLV320AIC15s SMARTDM supports three serial interface configurations (see Table 3–2): stand-alone master, stand-alone slave, and master-slave cascade, employing a time division multiplexed (TDM) scheme (a cascade of only-slaves is not supported). The SMARTDM allows for a serial connection of up to 16 codecs to a single serial port. Data communication in these three serial interface configurations can be carried out in either standard operation (default) or turbo operation. Each operation has two modes; programming mode (default mode) and continuous data transfer mode. To switch from the programming mode to the continuous data transfer mode, set bit D6 of control register 1 to 1, which resets after switching back to programming mode. The TLV320AIC15 can be switched back from the continuous data transfer mode to the programming mode by setting the LSB of the data on DIN to 1, only if the data format is (15+1), as selected by bit 0 of control register 1. The SMARTDM automatically adjusts the number of time slots per frame sync (FS) to match the number of codecs in the serial interface so that no time slot is wasted. Both the programming mode and the continuous data transfer mode of the TLV320AIC15 are compatible with the TLV320AIC10. The TLV320AIC15 provides primary/secondary communication and continuous data transfer with improvements and eliminates the requirements for hardware and software requests for secondary communication as seen in the TLV320AIC10. The TLV320AIC15 continuous data transfer mode now supports both master/slave stand-alone and cascade.

Table 3–2. Serial Interface Configurations

TLV320AIC15 CONNECTIONS	M/S PIN		FSD PIN		COMMENTS
	MASTER	SLAVE	MASTER	SLAVE	
Stand-alone master	High	NA	Pull high	NA	
Stand-alone slave	NA	Low	NA	Pull low	
Master-slave cascade	High	Low	Connect to the next slave's FS (see Figure 3–7)		Last slave's FSD pin is pulled high
Slave-slave cascade	NA	NA	NA	NA	Not supported

3.8.1 Programming Mode

In the programming mode, the FS signal starts the input/output data stream. Each period of FS contains two frames as shown in Figures 3–13 and 3–14: data frame and control frame. The data frame contains data transmitted from the ADC or to the DAC. The control frame contains data to program the AIC15s control registers. The SMARTDM automatically sets the number of time slots per frame equal to two times the number of AIC15 codecs in the interface. Each time slot contains 16-bit data. The SCLK is used to perform data transfer for the serial interface between the AIC15 codecs and the DSP. The frequency of SCLK varies depending on the selected mode of serial interface. In the stand-alone mode, there are 32 SCLKs (or two time slots) per sampling period. In the master-slave cascade mode, the number of SLCKs equals 32x(Number of codecs in the cascade). The digital output data from the ADC is taken from DOUT. The digital input data for the DAC is applied to DIN. The synchronization clock for the serial communication data and the frame-sync is taken from SCLK. The frame-sync signal that starts the ADC and DAC data transfer interval is taken from FS. The SMARTDM also provides a turbo mode, in which the FS's frequency is always the device's sampling frequency, but SCLK is running at a much higher speed. Thus, there are more than 32 SCLKs per sampling period, in which the data frame and control frame occupy only the first 32 SCLKs from the falling edge of the frame-sync FS (also see Section 3.6 for more details).

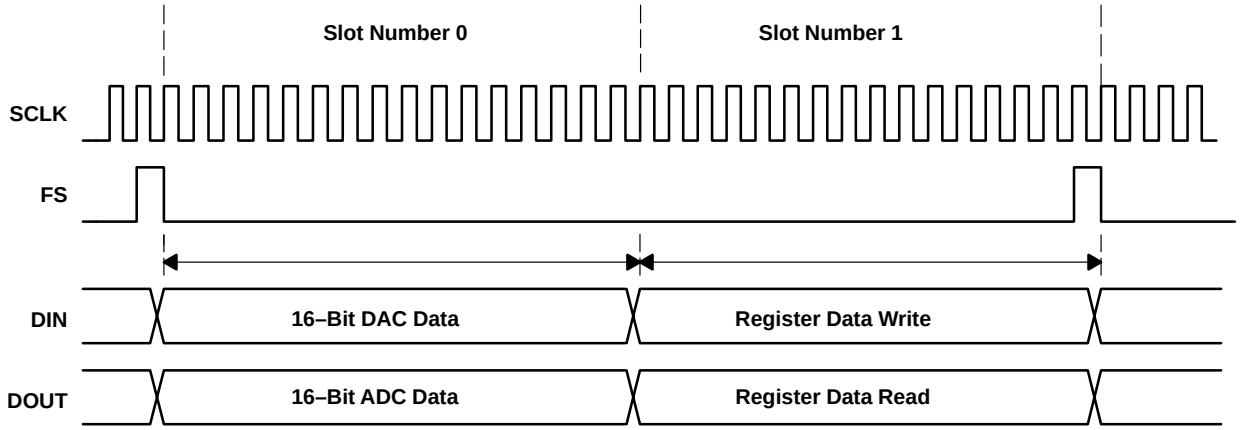
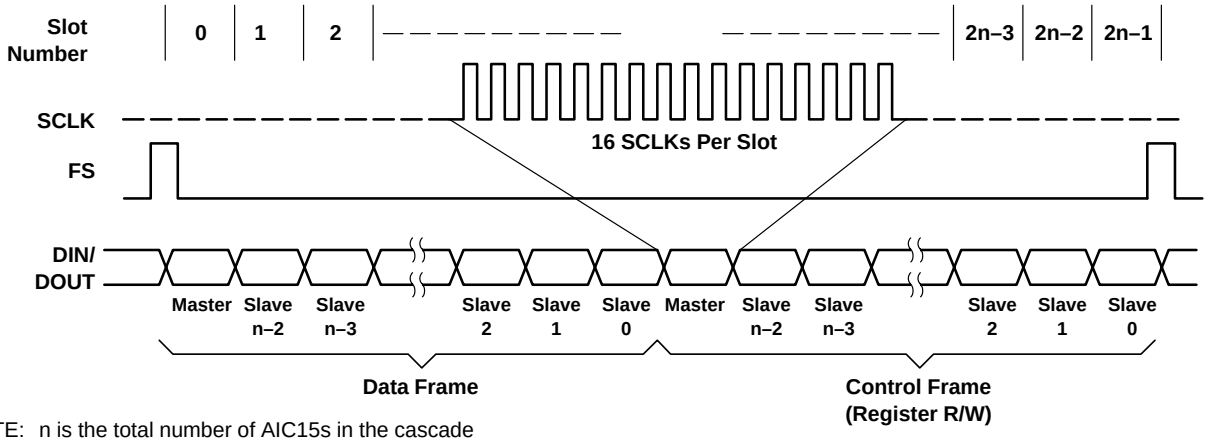


Figure 3–13. Standard Operation/Programming Mode: Stand-Alone Timing



NOTE: n is the total number of AIC15s in the cascade

Figure 3–14. Standard Operation/Programming Mode: Master-Slave Cascade Timing

3.8.2 Continuous Data Transfer Mode

The continuous data transfer mode, selected by setting bit D6 of the control register 1 to 1, contains conversion data only. In continuous data transfer mode, the control frame is eliminated and the period of FS signal contains only the data frame in which the 16-bit data is transferred contiguously, with no inactivity between bits. The control frame can be reactivated by setting the LSB of DIN data to 1 if the data is in the 15+1 format. To return the programming mode in the 16-bit DAC data format mode, write 0 in bit D6 of control register 1 using I^2C or S^2C, or do a hardware reset to come out of continuous data transfer mode. The continuous data transfer mode can support the TI DSP McBSPs autobuffering unit (ABU) operation in which the serial port interrupts are not generated with each word transferred to prevent CPU's ISR overheads.

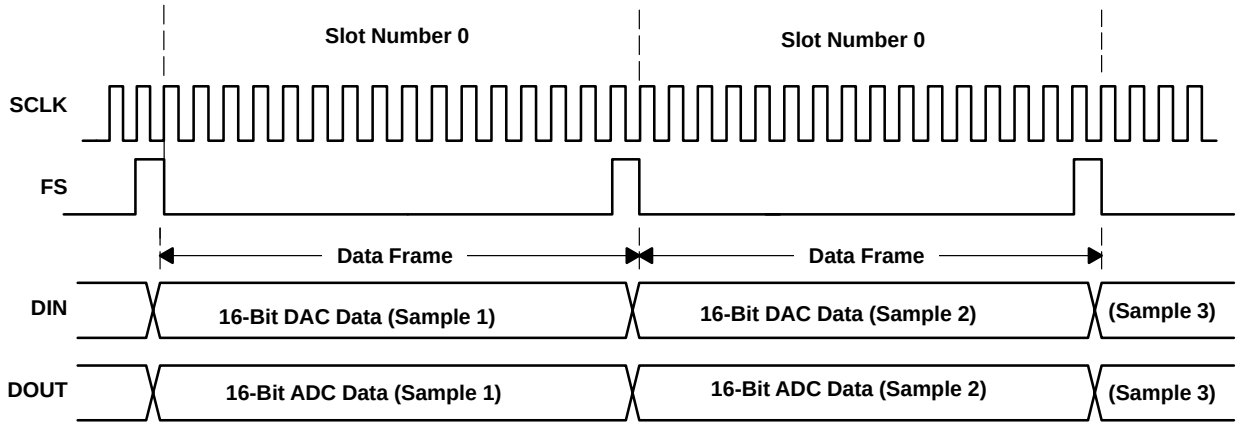
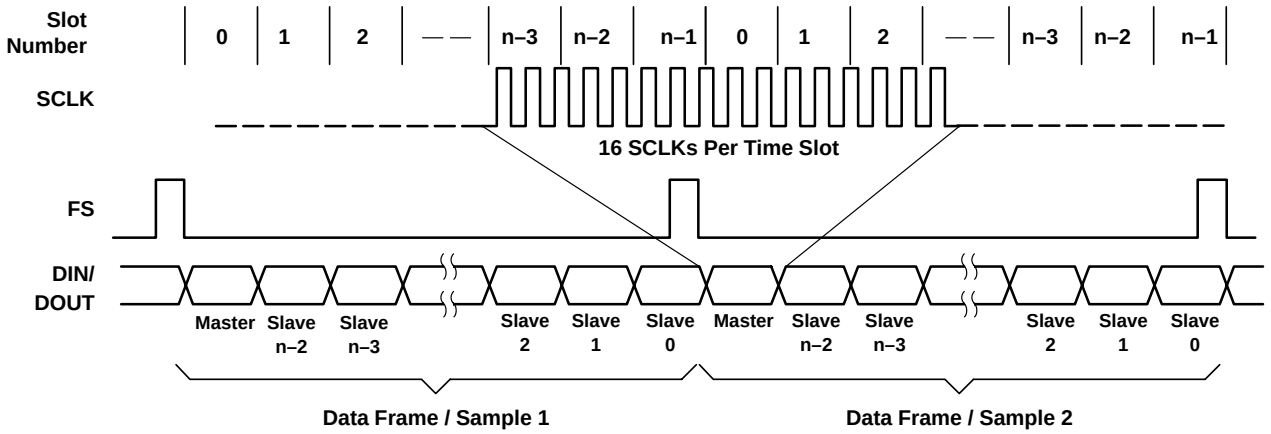


Figure 3–15. Standard Operation/Continuous Data Transfer Mode: Stand-Alone Timing



NOTE: n is the total number of AIC15s in the cascade

Figure 3–16. Standard Operation/Continuous Data Transfer Mode: Master-Slave Cascade Timing

3.8.3 Turbo Mode (SCLK)

Setting TURBO = 1 (bit D7) in control register 2 enables the turbo mode that requires the following condition to be met:

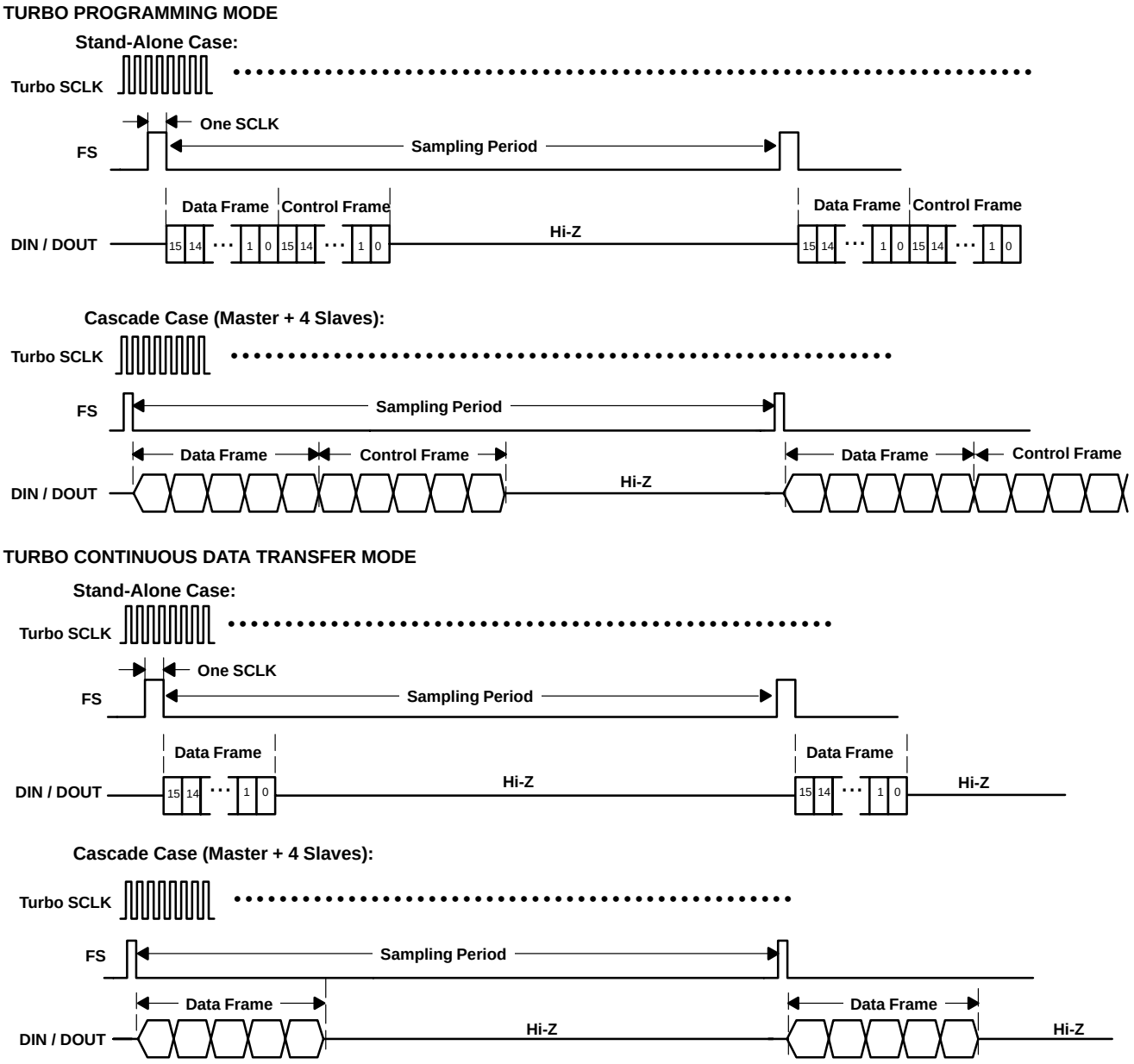
- For master with SCLK as output, M × N > #Devices × mode

Where:

M, N, and P are clock divider values defined in the control register 4.
#Device is the number of the device in cascade.
Mode is equal to 1 for continuous data transfer mode and 2 for programming mode.

- For slave, SCLK is the input with max allowable speed of 25 MHz (no condition is required)

The turbo mode is useful for applications that require more bandwidth for multitasking processing per sampling period. In the turbo mode (see Figure 3–17), the FSs frequency is always the device's sampling frequency but the SCLK is running at much higher speed than that described in Section 3.6.1. The output SCLK frequency is equal to (MCLK/P) in master mode and up to a maximum speed of 25 MHz for both master and slave AIC15. The data/control frame is still 16-SCLK long and the FS is one-SCLK pulse. Therefore, the DSP can maximize its data processing bandwidth by taking advantage of time available between the end of AIC15s control frame and the next frame-sync FS to process other tasks.



NOTE: SCLK is not drawn to scale.

Figure 3–17. Timing Diagram for Turbo Operation

3.9 Control Register Programming

The TLV320AIC15 contains six control registers that are used to program available modes of operation. All register programming occurs during the control frame through DIN. New configuration takes effect after a delay of one frame sync FS except the software reset, which happens after 6 MCLKs from the falling edge of the next frame sync FS. The TLV320AIC15 is defaulted to the programming mode upon power up. Set bit 6 in control register 1 to switch to continuous data transfer mode. If the 15+1 data format of DIN has been selected, the LSB of the DIN to 1 to switch from continuous data transfer mode to programming set mode. Otherwise, either the device needs to be reset or the host port writes 0 to bit D6 of control register 1 during the continuous data transfer mode to switch back to the programming mode.

3.9.1 Data Frame Format

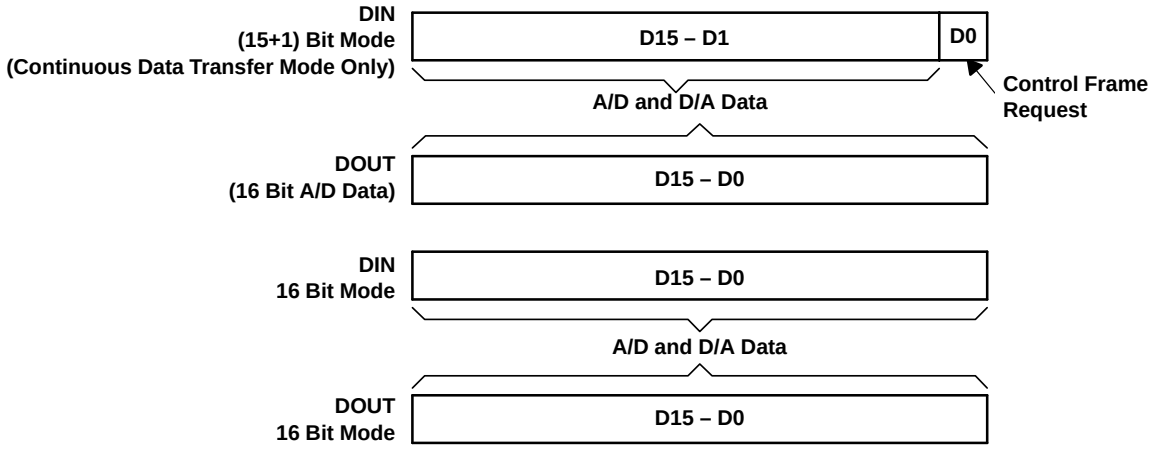


Figure 3–18. Data Frame Format

3.9.2 Control Frame Format (Programming Mode)

During the control frame, the DSP sends 16-bit words to the SMARTDM(TM) through DIN to read or write control registers shown in Table 3–4. The upper byte (Bits D15–D8) of the 16-bit control-frame word defines the read/write command. Bits D15–D13 define the control register address with register content occupied the lower byte D7–D0. Bit D12 is set to 0 for a write or to 1 for a read. Bit D11 in the write command is used to perform the broadcast mode. During a register write, the register content is located in the lower byte of DIN. During a register read, the register content is output in the lower byte of DOUT in the same control frame, whereas the lower byte of DIN is ignored.

3.9.3 Broadcast Register Write

Broadcast operation is very useful for a cascading system of SMARTDM DSP codecs in which all register programming can be completed in one control frame. During the control frame and in any register-write time slot, if the broadcast bit (D11) is set to 1, the register content of that time slot is written into the specified register of all devices in cascade (see Figure 3–20). This reduces the DSP's overhead of doing multiple writes to program same data into cascaded devices.

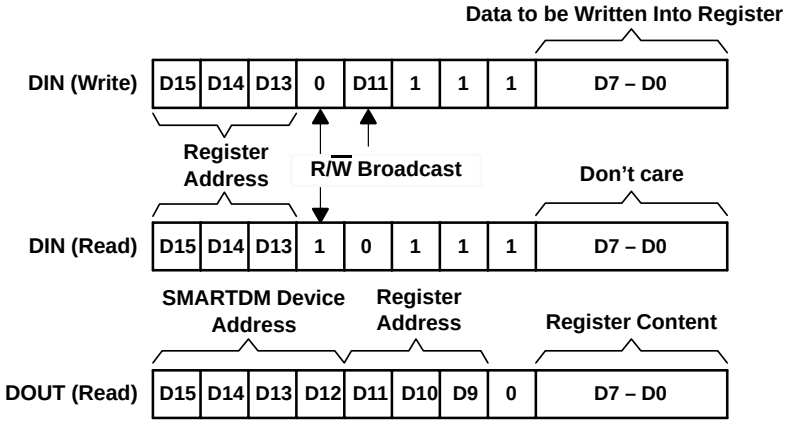
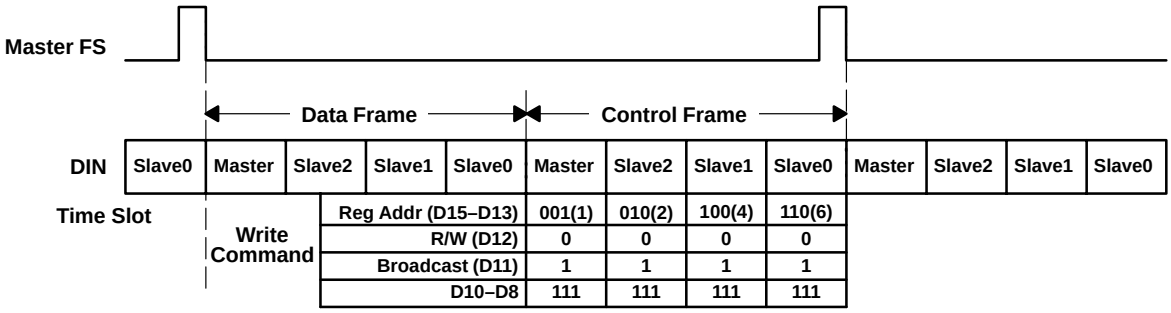


Figure 3–19. Control Frame Data Format



NOTE: In this example, the broadcast operation (D11 = 1) is used to program the four control registers of Reg.1, Reg.2, Reg.4, and Reg.6 in all 4 DSP codecs (Master, Slave2, Slave1, and Slave0) shown in Figure 3–8. These registers are programmed during the same frame.

Figure 3–20. Broadcast Register Write Example

3.9.4 Register Map

Bits D15 through D13 represent the control register address that is written with data carried in D7 through D0. Bit D12 determines a read or a write cycle to the addressed register. When D12 = 0, a write cycle is selected. When D12 = 1, a read cycle is selected. Bit D11 controls the broadcast mode as described above, in which the broadcast mode is enabled if D11 is set to 1. Always write 1s to bits D10 through D8.

Table 3–3 shows the register map.

Table 3–3. Register Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address			RW	BC	1	1	1	Control Register Content							

Table 3–4. Register Addresses

REGISTER NO.	D15	D14	D13	REGISTER NAME
0	0	0	0	No operation
1	0	0	1	control 1
2	0	1	0	control 2
3	0	1	1	control 3
4	1	0	0	control 4
5	1	0	1	control 5
6	1	1	0	control 6

4 Control Register Content Description

4.1 Control Register 1

D7	D6	D5	D4	D3	D2	D1	D0
ADOVF	CX	IIR	DAOVF	BIASV	ALB	DLB	DAC16
R	R/W	R/W	R	R/W	R/W	R/W	R/W

NOTE: R = Read, W = Write

Table 4–1. Control Register 1 Bit Summary

BIT	NAME	RESET VALUE	FUNCTION
D7	ADOVF	0	ADC over flow. This bit indicates whether the ADC is overflow. ADOVF = 0 No overflow. ADOVF = 1 A/D is overflow.
D6	CX	0	Continuous data transfer mode. This bit selects between programming mode and continuous data transfer mode. CX = 0 Programming mode. CX = 1 Continuous data transfer mode.
D5	IIR	0	IIR Filter. This bit selects between FIR and IIR for decimation/interpolation low-pass filter. IIR = 0 FIR filter is selected. IIR = 1 IIR filter is selected.
D4	DAOVF	0	DAC over flow. This bit indicates whether the DAC is overflow DAOVF = 0 No overflow. DAOVF = 1 DAC is overflow
D3	BIASV	0	Bias voltage. This bit selects the output voltage for BIAS pin BIASV = 0 BIAS pin = 2.35V BIASV = 1 BIAS pin = 1.35V
D2	ALB	0	Analog loop back DLB = 0 Analog loopback disabled DLB = 1 Analog loopback enabled
D1	DLB	0	Digital loop back DLB = 0 Digital loopback disabled DLB = 1 Digital loopback enabled
D0	DAC16	0	DAC 16-bit data format. This bit applies to the continuous data transfer mode only to enable the 16-bit data format for DAC input. DAC16 = 0 DAC input data length is 15 bits. Writing a 1 to the LSB of the DAC input to switch from continuous data transfer mode to programming mode. DAC16 = 1 DAC input data length is 16 bit.

4.2 Control Register 2

D7	D6	D5	D4	D3	D2	D1	D0
TURBO	DIFBP	I^2C6	I2C5	I^2C4	GPO	HPC	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

NOTE: R = Read, W = Write

Table 4–2. Control Register 2 Bit Summary

BIT	NAME	RESET VALUE	FUNCTION

D7	TURBO	0	Turbo mode. This bit is used to set the SCLK rate.
			TURBO = 0 SCLK = (16 × FS × #Device × mode)
			TURBO = 1 SCLK = MCLK/P (P is determined in register 4)

D6	DIFBP	0	Decimation/interpolation filter bypass. This bit is used to bypass both decimation and interpolation filters. DIFBP = 0 Decimation/interpolation filters are operated. DIFBP = 1 Decimation/interpolation filters are bypassed.
D5–D3	I^2Cx	100	I^2C device address. These three bits are programmable to define three MSBs of the I^2C device address (reset value is 100). These three bits are combined with the 4-bit SMARTDM device address to form 7-bit I^2C device address.
D2	GPO	0	General-purpose output
D1–D0	HPC	00	Host port control bits. Write the following values into D1–D0 to select the appropriate configuration for two pins SDA and SCL. SDA pin is set to be equal to D2 if D1–D0 = 10. D1–D0 0 0 SDA and SCL pins are used for I^2C interface 0 1 SDA and SCL pins are used for S^2C interface 1 0 SDA pin = D2, input going into SCL pin is output to DOUT 1 1 SDA pin = Control frame flag.

4.3 Control Register 3

D7	D6	D5	D4	D3	D2	D1	D0
PWDN		SWRS	OSR-option		ASRF		
R/W	R/W	R/W		R/W		R/W	

NOTE: R = Read, W = Write

Table 4–3. Control Register 3 Bit Summary

BIT	NAME	RESET VALUE	FUNCTION
D7–D6	PWDN	00	Power down PWDN = 00 No power down PWDN = 01 Power-down A/D PWDN = 10 Power-down D/A PWDN = 11 Software power down the entire device
D5	SWRS	0	Software reset. Set this bit to 1 to reset the device.
D4-D3	OSR option	00	OSR option. D4–D3=X1 OSR for DAC Channel is 512(Max Fs=8Ksps) D4–D3=10 OSR for DAC Channel is 256(Max Fs=16Ksps) D4–D3=00 OSR for DAC Channel is 128(Max Fs=26Ksps)
D2-D0	ASRF	001	Asynchronous sampling rate factor. These three bits define the ratio n between FS frequency and the desired sampling frequency fs (Applied only if different sampling rate between CODEC1 and CODEC2 is desired) ASRF = 001 n = FS/fs = 1 ASRF = 010 n = FS/fs = 2 ASRF = 011 n = FS/fs = 3 ASRF = 100 n = FS/fs = 4 ASRF = 101 n = FS/fs = 5 ASRF = 110 n = FS/fs = 6 ASRF = 111 n = FS/fs = 7 ASRF = 000 n = FS/fs = 8

4.4 Control Register 4

D7	D6	D5	D4	D3	D2	D1	D0
FSDIV	MNP						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

NOTE: R = Read, W = Write

Table 4–4. Control Register 4 Bit Summary

BIT	NAME	RESET VALUE	FUNCTION
D7	FSDIV	0	Frame sync division factor FSDIV = 0 To write value of P to bits D2-D0 and value of N to bits D6-D3 FSDIV = 1 To write value of M to bits D6-D0
D6–D0	MNP	—	Divider values of M,N, and P to be used in junction with the FSDIV bit for calculation of FS frequency according to the formula FS = MCLK / (16xMxNxP) • M = 1,2,…,128 Determined by D6-D0 with FSDIV = 1 D7-D0 = 10000000 M = 128 D7-D0 = 10000001 M = 1 • • D7-D0 = 11111111 M = 127 • N = 1,2,…,16 Determined by D6-D3 with FSDIV = 0 D7-D0 = 00000xxx N = 16 D7-D0 = 00001xxx N = 1 • • D7-D0 = 01111xxx N = 15 • P = 1,2,…,8 Determined by D2-D0 with FSDIV = 0 D7-D0 = 0xxxx000 P = 8 D7-D0 = 0xxxx001 P = 1 • • D7-D0 = 0xxxx111 P = 7

NOTES: 1. It takes 2 sampling periods to update new values of M,N, and P.
2. In register read operation, first read receives N and P values and second read receives M value.
3. M(default) = 16, N(default) = 6, P(default) = 8
4. If P = 8, the device enters the coarse sampling mode as described in Section 3.1 Operating Frequencies

4.5 Control Register 5A

D7	D6	D5	D4	D3	D2	D1	D0
0	0	ADGAIN					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

NOTE: R = Read, W = Write

Table 4–5. Control Register 5A Bit Summary

BIT	NAME	RESET VALUE	FUNCTION
D7-D6	Control Register 5A	00	ADC programmable gain amplifier
D5-D0	ADGAIN	101010	A/D converter gain (see Table 4–6)

NOTES: 5. In register read operation, first read receives ADC gain value, second read receives DAC gain value, third read receives register 5C contents, and fourth read receives register 5D contents.
6. PGA default value = 101010_b (0dB) for both ADC and DAC.

Table 4–6. A/D PGA Gain

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
0	**0**	1	1	1	1	1	1	ADC input PGA gain = MUTE
0	**0**	1	1	1	1	1	0	ADC input PGA gain = 20 dB
0	**0**	1	1	1	1	0	1	ADC input PGA gain = 19 dB
0	**0**	1	1	1	1	0	0	ADC input PGA gain = 18 dB
0	**0**	1	1	1	0	1	1	ADC input PGA gain = 17 dB
0	**0**	1	1	1	0	1	0	ADC input PGA gain = 16 dB
0	**0**	1	1	1	0	0	1	ADC input PGA gain = 15 dB
0	**0**	1	1	1	0	0	0	ADC input PGA gain = 14 dB
0	**0**	1	1	0	1	1	1	ADC input PGA gain = 13 dB
0	**0**	1	1	0	1	1	0	ADC input PGA gain = 12 dB
0	**0**	1	1	0	1	0	1	ADC input PGA gain = 11 dB
0	**0**	1	1	0	1	0	0	ADC input PGA gain = 10 dB
0	**0**	1	1	0	0	1	1	ADC input PGA gain = 9 dB
0	**0**	1	1	0	0	1	0	ADC input PGA gain = 8 dB
0	**0**	1	1	0	0	0	1	ADC input PGA gain = 7 dB
0	**0**	1	1	0	0	0	0	ADC input PGA gain = 6 dB
0	**0**	1	0	1	1	1	1	ADC input PGA gain = 5 dB
0	**0**	1	0	1	1	1	0	ADC input PGA gain = 4 dB
0	**0**	1	0	1	1	0	1	ADC input PGA gain = 3 dB
0	**0**	1	0	1	1	0	0	ADC input PGA gain = 2 dB
0	**0**	1	0	1	0	1	1	ADC input PGA gain = 1 dB
0	**0**	1	0	1	0	1	0	ADC input PGA gain = 0 dB
0	**0**	1	0	1	0	0	1	ADC input PGA gain = -1 dB
0	**0**	1	0	1	0	0	0	ADC input PGA gain = -2 dB
0	**0**	1	0	0	1	1	1	ADC input PGA gain = -3 dB
0	**0**	1	0	0	1	1	0	ADC input PGA gain = -4 dB
0	**0**	1	0	0	1	0	1	ADC input PGA gain = -5 dB
0	**0**	1	0	0	1	0	0	ADC input PGA gain = -6 dB
0	**0**	1	0	0	0	1	1	ADC input PGA gain = -7 dB
0	**0**	1	0	0	0	1	0	ADC input PGA gain = -8 dB
0	**0**	1	0	0	0	0	1	ADC input PGA gain = -9 dB
0	**0**	1	0	0	0	0	0	ADC input PGA gain = -10 dB
0	**0**	0	1	1	1	1	1	ADC input PGA gain = -11 dB
0	**0**	0	1	1	1	1	0	ADC input PGA gain = -12 dB
0	**0**	0	1	1	1	0	1	ADC input PGA gain = -13 dB
0	**0**	0	1	1	1	0	0	ADC input PGA gain = -14 dB
0	**0**	0	1	1	0	1	1	ADC input PGA gain = -15 dB
0	**0**	0	1	1	0	1	0	ADC input PGA gain = -16 dB
0	**0**	0	1	1	0	0	1	ADC input PGA gain = -17 dB
0	**0**	0	1	1	0	0	0	ADC input PGA gain = -18 dB
0	**0**	0	1	0	1	1	1	ADC input PGA gain = -19 dB
0	**0**	0	1	0	1	1	0	ADC input PGA gain = -20 dB
0	**0**	0	1	0	1	0	1	ADC input PGA gain = -21 dB
0	**0**	0	1	0	1	0	0	ADC input PGA gain = -22 dB

Table 4–6. A/D PGA Gain (Continued)

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
0	**0**	0	1	0	0	1	1	ADC input PGA gain = -23dB
0	**0**	0	1	0	0	1	0	ADC input PGA gain = -24 dB
0	**0**	0	1	0	0	0	1	ADC input PGA gain = -25 dB
0	**0**	0	1	0	0	0	0	ADC input PGA gain = -26 dB
0	**0**	0	0	1	1	1	1	ADC input PGA gain = -27 dB
0	**0**	0	0	1	1	1	0	ADC input PGA gain = -28 dB
0	**0**	0	0	1	1	0	1	ADC input PGA gain = -29 dB
0	**0**	0	0	1	1	0	0	ADC input PGA gain = -30 dB
0	**0**	0	0	1	0	1	1	ADC input PGA gain = -31 dB
0	**0**	0	0	1	0	1	0	ADC input PGA gain = -32 dB
0	**0**	0	0	1	0	0	1	ADC input PGA gain = -33 dB
0	**0**	0	0	1	0	0	0	ADC input PGA gain = -34 dB
0	**0**	0	0	0	1	1	1	ADC input PGA gain = -35 dB
0	**0**	0	0	0	1	1	0	ADC input PGA gain = -36 dB
0	**0**	0	0	0	1	0	1	ADC input PGA gain = -37 dB
0	**0**	0	0	0	1	0	0	ADC input PGA gain = -38 dB
0	**0**	0	0	0	0	1	1	ADC input PGA gain = -39 dB
0	**0**	0	0	0	0	1	0	ADC input PGA gain = -40 dB
0	**0**	0	0	0	0	0	1	ADC input PGA gain = -41 dB
0	**0**	0	0	0	0	0	0	ADC input PGA gain = -42 dB

4.6 Control Register 5B

D7	D6	D5	D4	D3	D2	D1	D0
0	1	DAGAIN					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

NOTE: R = Read, W = Write

Table 4–7. Control Register 5B Bit Summary

BIT	NAME	RESET VALUE	FUNCTION
D7-D6	Control Register 5B	NA	
D5-D0	DAGAIN	101010	D/A converter gain (see Table 4–8)

NOTES: 7. In register read operation, first read receives ADC gain value, second read receives DAC gain value, third receives register 5C, and fourth receives register 5D.

8. PGA default value = 101010_b (0dB) for both ADC and DAC.

Table 4–8. D/A PGA Gain

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
0	**1**	1	1	1	1	1	1	DAC input PGA gain = MUTE
0	**1**	1	1	1	1	1	0	DAC input PGA gain = 20 dB
0	**1**	1	1	1	1	0	1	DAC input PGA gain = 19 dB
0	**1**	1	1	1	1	0	0	DAC input PGA gain = 18 dB
0	**1**	1	1	1	0	1	1	DAC input PGA gain = 17 dB
0	**1**	1	1	1	0	1	0	DAC input PGA gain = 16 dB
0	**1**	1	1	1	0	0	1	DAC input PGA gain = 15 dB
0	**1**	1	1	1	0	0	0	DAC input PGA gain = 14 dB

Table 4–8. D/A PGA Gain (Continued)

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
0	**1**	1	1	0	1	1	1	DAC input PGA gain = 13 dB
0	**1**	1	1	0	1	1	0	DAC input PGA gain = 12 dB
0	**1**	1	1	0	1	0	1	DAC input PGA gain = 11 dB
0	**1**	1	1	0	1	0	0	DAC input PGA gain = 10 dB
0	**1**	1	1	0	0	1	1	DAC input PGA gain = 9 dB
0	**1**	1	1	0	0	1	0	DAC input PGA gain = 8 dB
0	**1**	1	1	0	0	0	1	DAC input PGA gain = 7 dB
0	**1**	1	1	0	0	0	0	DAC input PGA gain = 6 dB
0	**1**	1	0	1	1	1	1	DAC input PGA gain = 5 dB
0	**1**	1	0	1	1	1	0	DAC input PGA gain = 4 dB
0	**1**	1	0	1	1	0	1	DAC input PGA gain = 3 dB
0	**1**	1	0	1	1	0	0	DAC input PGA gain = 2 dB
0	**1**	1	0	1	0	1	1	DAC input PGA gain = 1 dB
0	**1**	1	0	1	0	1	0	DAC input PGA gain = 0 dB
0	**1**	1	0	1	0	0	1	DAC input PGA gain = -1 dB
0	**1**	1	0	1	0	0	0	DAC input PGA gain = -2 dB
0	**1**	1	0	0	1	1	1	DAC input PGA gain = -3 dB
0	**1**	1	0	0	1	1	0	DAC input PGA gain = -4 dB
0	**1**	1	0	0	1	0	1	DAC input PGA gain = -5 dB
0	**1**	1	0	0	1	0	0	DAC input PGA gain = -6 dB
0	**1**	1	0	0	0	1	1	DAC input PGA gain = -7 dB
0	**1**	1	0	0	0	1	0	DAC input PGA gain = -8 dB
0	**1**	1	0	0	0	0	1	DAC input PGA gain = -9 dB
0	**1**	1	0	0	0	0	0	DAC input PGA gain = -10 dB
0	**1**	0	1	1	1	1	1	DAC input PGA gain = -11 dB
0	**1**	0	1	1	1	1	0	DAC input PGA gain = -12 dB
0	**1**	0	1	1	1	0	1	DAC input PGA gain = -13 dB
0	**1**	0	1	1	1	0	0	DAC input PGA gain = -14 dB
0	**1**	0	1	1	0	1	1	DAC input PGA gain = -15 dB
0	**1**	0	1	1	0	1	0	DAC input PGA gain = -16 dB
0	**1**	0	1	1	0	0	1	DAC input PGA gain = -17 dB
0	**1**	0	1	1	0	0	0	DAC input PGA gain = -18 dB
0	**1**	0	1	0	1	1	1	DAC input PGA gain = -19 dB
0	**1**	0	1	0	1	1	0	DAC input PGA gain = -20 dB
0	**1**	0	1	0	1	0	1	DAC input PGA gain = -21 dB
0	**1**	0	1	0	1	0	0	DAC input PGA gain = -22 dB
0	**1**	0	1	0	0	1	1	DAC input PGA gain = -23dB
0	**1**	0	1	0	0	1	0	DAC input PGA gain = -24 dB
0	**1**	0	1	0	0	0	1	DAC input PGA gain = -25 dB
0	**1**	0	1	0	0	0	0	DAC input PGA gain = -26 dB
0	**1**	0	0	1	1	1	1	DAC input PGA gain = -27 dB
0	**1**	0	0	1	1	1	0	DAC input PGA gain = -28 dB
0	**1**	0	0	1	1	0	1	DAC input PGA gain = -29 dB
0	**1**	0	0	1	1	0	0	DAC input PGA gain = -30 dB

Table 4–8. D/A PGA Gain (Continued)

D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
0	**1**	0	0	1	0	1	1	DAC input PGA gain = -31 dB
0	**1**	0	0	1	0	1	0	DAC input PGA gain = -32 dB
0	**1**	0	0	1	0	0	1	DAC input PGA gain = -33 dB
0	**1**	0	0	1	0	0	0	DAC input PGA gain = -34 dB
0	**1**	0	0	0	1	1	1	DAC input PGA gain = -35 dB
0	**1**	0	0	0	1	1	0	DAC input PGA gain = -36 dB
0	**1**	0	0	0	1	0	1	DAC input PGA gain = -37 dB
0	**1**	0	0	0	1	0	0	DAC input PGA gain = -38 dB
0	**1**	0	0	0	0	1	1	DAC input PGA gain = -39 dB
0	**1**	0	0	0	0	1	0	DAC input PGA gain = -40 dB
0	**1**	0	0	0	0	0	1	DAC input PGA gain = -41 dB
0	**1**	0	0	0	0	0	0	DAC input PGA gain = -42 dB

4.7 Control Register 5C

D7	D6	D5	D4	D3	D2	D1	D0
1	0	DSTG			Reserved	INBG	
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W

NOTE: R = Read, W = Write

Table 4–9. Digital Sidetone Gain

D5	D4	D3	DSTG
1	1	1	Digital sidetone gain = Mute (Default)
1	1	0	Digital sidetone gain = -21 dB
1	0	1	Digital sidetone gain = -18 dB
1	0	0	Digital sidetone gain = -15 dB
0	1	1	Digital sidetone gain = -12 dB
0	1	0	Digital sidetone gain = -9 dB
0	0	1	Digital sidetone gain = -6 dB
0	0	0	Digital sidetone gain = -3 dB

Table 4–10. Input Buffer Gain

D1	D0	INBG
1	1	Input buffer gain = 24 dB
1	0	Input buffer gain = 12 dB
0	1	Input buffer gain = 6 dB
0	0	Input buffer gain = 0 dB (Default)

4.8 Control Register 5D

D7	D6	D5	D4	D3	D2	D1	D0
1	1	Reserved				Chip Version-ID	
R/W	R/W	R	R	R	R	R	R

NOTE: R = Read, W = Write

4.9 Control Register 6

D7	D6	D5	D4	D3	D2	D1	D0
PSDO	MUTE2	MUTE3	ODRCT		AINSEL		Reserved
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

NOTE: R = Read, W = Write

Table 4–11. Control Register 6 Bit Summary

BIT	NAME	RESET VALUE	FUNCTION
D7–D5	Reserved		
D4–D3	Reserved		
D2–D1	AINSEL	00	Analog input select. These bits select the analog input for the ADC AINSEL = 00 The analog input is INP/M1 AINSEL = 01 The analog input is MICIN self-biased at 1.35 V AINSEL =10 The analog input is MICIN with external common mode AINSEL = 11 The analog input is INP/M2 NOTE: For AINSEL = 10, the external common mode is connected to INM1 via an ac-coupled capacitor.
D0	Reserved		

5 Electrical Characteristics

5.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)

Supply voltage range: DVDD, AV_{DD} (see Note 1) . . . . . –0.3 V to 4 V
DRVDD (see Note 1) . . . . . –0.3 V to 4 V
Output voltage range, all digital output signals . . . . . –0.3 V to DVDD + 0.3 V
Input voltage range, all digital input signals . . . . . –0.3 V to DVDD + 0.3 V
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Case temperature for 10 seconds: Package . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

5.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage for analog, AVDD		2.7	3.3	3.6	V
Supply voltage for analog output driver, DRVDD		2.7		3.6	
Supply voltage for digital core, DVDD		1.65	1.8	1.95	V
Supply voltage for digital I/O, IOVDD		1.1	3.3	3.6	V
Analog single-ended peak-to-peak input voltage, $V_{I(analog)}$				2	V
Output load resistance, R_L	Between OUTP1 and OUTM1 (differential)		600		Ω
Analog output load capacitance, C_L				20	pF
Digital output capacitance				20	pF
Master clock, MCLK	IOVDD = 1.1 V			15	MHz
	IOVDD = 1.8 V			45	
	IOVDD = 2.7–3.6 V			100	
ADC or DAC conversion rate				26	kHz
Operating free-air temperature, T_A		–40		85	°C

5.3 Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, IOV_{DD} = 1.1 V (Unless Otherwise Noted)

5.3.1 Digital Inputs and Outputs, f_S = 8 kHz, Outputs Not Loaded

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, any digital output		0.8 IOVDD			V
V_{OL}	Low-level output voltage, any digital output				0.1 IOVDD	V
I_{IH}	High-level input current, any digital input			0.5		µA
I_{IL}	Low-level input current, any digital input			0.5		µA
C_i	Input capacitance			3		pF
C_o	Output capacitance			5		pF

5.4 ADC Path Digital Filter, f_S = 8 kHz (see Note 2)

5.4.1 FIR Filter

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Filter gain relative to gain at 1020 Hz	0 to 300 Hz	–0.5		0.2	dB
	300 Hz to 3 kHz	–0.5		0.25	
	3.3 kHz	–0.5		0.3	
	3.6 kHz			–3	
	4 kHz			–35	
	≥4.4 kHz			–74	

NOTE 2: Filter gain outside the passband is measured with respect to gain at 1020 Hz. The analog input test signal is a sinewave with 0 dB = 4 $V_{I(PP)}$ as the reference level for the analog input signal. The bandpass is 0 to 3600 Hz for an 8-kHz sample rate. This bandpass scales linearly with the sample rate.

5.4.2 IIR Filter

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Filter gain relative to gain at 1020 Hz	0 to 300 Hz	–0.5		0.2	dB
	300 Hz to 3 kHz	–0.5		0.25	
	3.3 kHz	–0.5		0.3	
	3.6 kHz			–3	
	4 kHz			–20	
	≥4.4 kHz			–60	

NOTE 2: Filter gain outside the passband is measured with respect to gain at 1020 Hz. The analog input test signal is a sinewave with 0 dB = 4 $V_{I(PP)}$ as the reference level for the analog input signal. The bandpass is 0 to 3600 Hz for an 8-kHz sample rate. This bandpass scales linearly with the sample rate.

5.5 ADC Dynamic Performance, f_S = 8 kHz

5.5.1 ADC Signal-to-Noise (see Note 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio (SNR)	V_I = –1 dB	82	88		dB
		V_I = –9 dB	79	82		

NOTE 3: Test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output common mode is 1.35 V.

5.5.2 ADC Signal-to-Distortion (see Note 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	V_I = –1 dB	85	90		dB
		V_I = –9 dB	82	88		

NOTE 3: Test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output common mode is 1.35 V.

5.5.3 ADC Signal-to-Distortion + Noise (see Note 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Signal-to-total harmonic distortion + noise (THD + N)	V_I = –1 dB	79	87		dB
		V_I = –9 dB	73	79		

NOTE 3: Test condition is a 1020-Hz input signal with an 8-kHz conversion rate. Input and output common mode is 1.35 V.

5.5.4 ADC Channel Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I(PP)}$	Single–ended input level	Preamp gain = 6 dB			2	V
V_{IO}	Input offset voltage	MICIN, INPx, INMx		±10		mV
I_B	Input bias current				34	µA
	Common-mode voltage			1.35		V
	Dynamic range	V_I = –1 dB		85		dB
	Mute attenuation	PGA = MUTE		80		dB
	Intrachannel isolation			87		dB
E_G	Gain error	V_I = –1 dB at 1020 Hz		0.6		dB
$E_{O(ADC)}$	ADC converter offset error			±10		mV
CMRR	Common-mode rejection ratio at INMx and INPx	V_I = –100 mV_{pp} at 1020 Hz		50		dB
	Idle channel noise	$V_{INP,INM,MICIN}$ = 0 V		50	100	µVrns
r_i	Input resistance	MICIN, INPx, INMx, T_A = 25°C		30		kΩ
C_i	Input capacitance			2		pF
	Channel delay	IIR		$5/f_S$		s
		FIR		$17/f_S$		s

5.6 DAC Path Digital Filter, f_S = 8 kHz (see Note 4)

5.6.1 FIR Filter

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Filter gain relative to gain at 1020 Hz	0 to 300 Hz	–0.5		0.2	dB
	300 Hz to 3 kHz	–0.25		0.25	
	3.3 kHz	–0.35		0.3	
	3.6 kHz			–3	
	4 kHz			–40	
	≥4.4 kHz			–74	

5.6.2 IIR Filter

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Filter gain relative to gain at 1020 Hz	0 to 300 Hz	–0.5		0.2	dB
	300 Hz to 3 kHz	–0.25		0.25	
	3.3 kHz	–0.35		0.3	
	3.6 kHz			–3	
	4 kHz			–20	
	≥4.4 kHz			–60	

NOTE 4: Filter gain outside of the bandpass is measured with respect to gain at 1020 Hz. The input signal is the digital equivalent of a sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 4 $V_{I(PP)}$. The pass band is 0 Hz to 3600 Hz for an 8-kHz sample rate. This pass band scales linearly with the conversion rate.

5.7 DAC Dynamic Performance

5.7.1 OUTP/OUTM Signal-to-Noise When Load Is 600 Ω (see Note 5)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio (SNR)	V_I = 0 dB	80	92		dB
		V_I = –9 dB	76	83		

NOTE 5: Test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at the output of the application schematic low-pass filter. The test is conducted in 16-bit mode.

5.7.2 OUTP1/OUTM1 Signal-to-Distortion When Load Is 600 Ω (see Note 5)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	V_I = –0 dB	78	85		
		V_I = –9 dB	74	83		

NOTE 5: Test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at the output of the application schematic low-pass filter. The test is conducted in 16-bit mode.

5.7.3 OUTP1/OUTM1 Signal-to-Distortion + Noise When Load Is 600 Ω (see Note 5)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-total harmonic distortion + noise (THD + N)	V_I = –0 dB	75	82		dB
	V_I = –9 dB	70	77		

NOTE 5: Test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at the output of the application schematic low-pass filter. The test is conducted in 16-bit mode.

5.7.4 DAC Channel Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Dynamic range	V_I = 0 dB at 1020 Hz		92		dB
	Interchannel isolation			120		dB
E_G	Gain error, 0 dB	V_O = 0 dB at 1020 Hz		0.5		dB
	Common mode voltage			1.35		V
	Idle channel narrow band noise	0 kHz–4 kHz, See Note 6		80	125	Vrms
V_{OO}	Output offset voltage at OUT1 (differential)	DIN = All zeros		10		mV
V_O	Analog output voltage, (3.3 V)	OUTP1	0.35		2.35	V
P_O	Maximum output power	600 Ω load at 3.3 V between OUTP1 and OUTM1		6.7		mW
IIR	Channel delay			$5/f_S$		s
FIR				$18/f_S$		

NOTE 6: The conversion rate is 8 kHz.

5.8 BIAS Amplifier Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Output voltage		2.2	2.35	2.4	V
	Integrated noise	300 Hz–13 kHz		20		μV
	Offset voltage			10		mV
	Current drive			10		mA
	Unity gain bandwidth			1		MHz
	DC gain			140		dB

5.9 Power-Supply Rejection (see Note 7)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
AVDD	Supply-voltage rejection ratio, analog supply ($f_{(j)}$ = 0 to f_S/2) at 1 kHz		Differential		75		dB
			Single-ended		50		
DVDD	Supply-voltage rejection ratio	DAC channel	$f_{(j)}$ = 0 kHz to 30 kHz		95		dB
		ADC channel			86		

NOTE 7: Power supply rejection measurements are made with both the ADC and DAC channels idle and a 200 mV peak-to-peak signal applied to the appropriate supply.

5.10 Power Supply

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Power dissipation				11.2	16.5	mW
$I_{(t)}$	Total current		Power down		3.4	5	mA
					0.01		mA
I_{DD}	Supply current	Analog	ADC		2		mA
			DAC		1		
			Ref		0.4		
		Digital	All sections on		1.8		mA
			Coarse sampling		1		

5.11 Timing Requirements (see Parameter Measurement Information)

		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{wH}	Pulse duration, MCLK high	C_L = 20 pF	5			ns
t_{wL}	Pulse duration, MCLK low		5			
t_{su1}	Setup time, $\overline{\text{RESET}}$, before MCLK high (see Figure 5–1)		3			
t_{h1}	Hold time, $\overline{\text{RESET}}$, after MCLK high (see Figure 5–1)		2			
t_{d1}	Delay time, SCLK↑ to FS/FSD↓				5	
t_{d2}	Delay time, SCLK↑ to FS/FSD↑				5	
t_{d3}	Delay time, SCLK↑ to DOUT				15	
t_{en}	Enable time, SCLK↑ to DOUT				15	
t_{dis}	Disable time, SCLK↑ to DOUT				15	
t_{su2}	Setup time, DIN, before SCLK↓		10			
t_{h2}	Hold time, DIN, after SCLK↓		10			

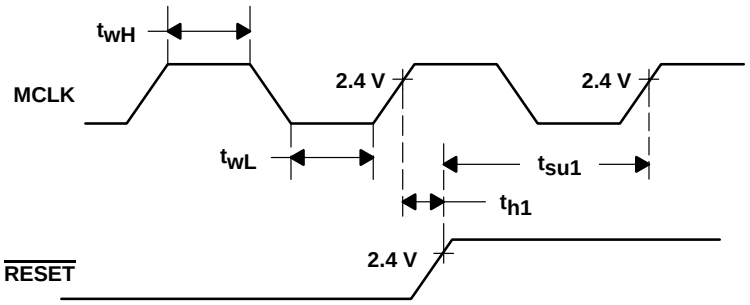


Figure 5–1. Hardware Reset Timing

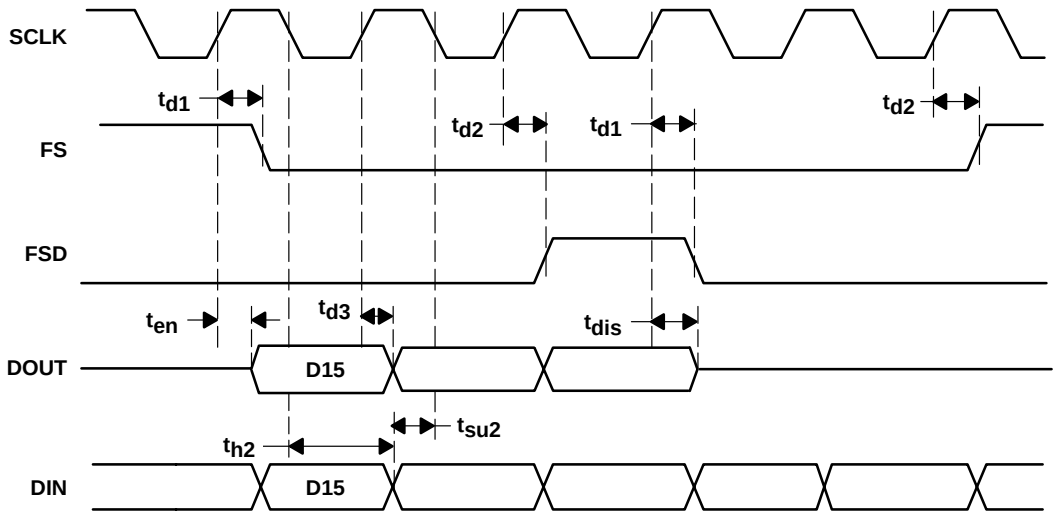


Figure 5–2. Serial Communication Timing

NOTE: Above Figures are meant to show timing delays only.

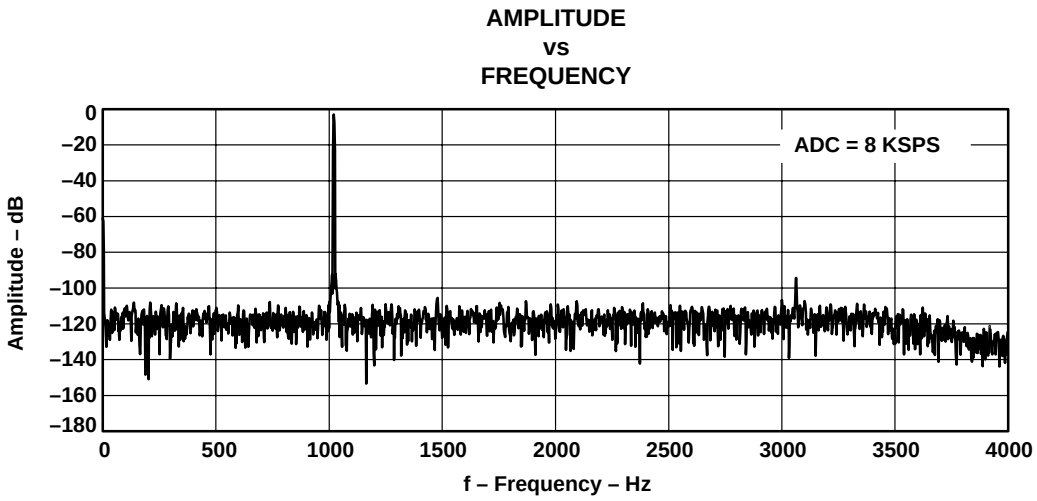


Figure 5–3. FFT—ADC Channel (–3 dB Input)

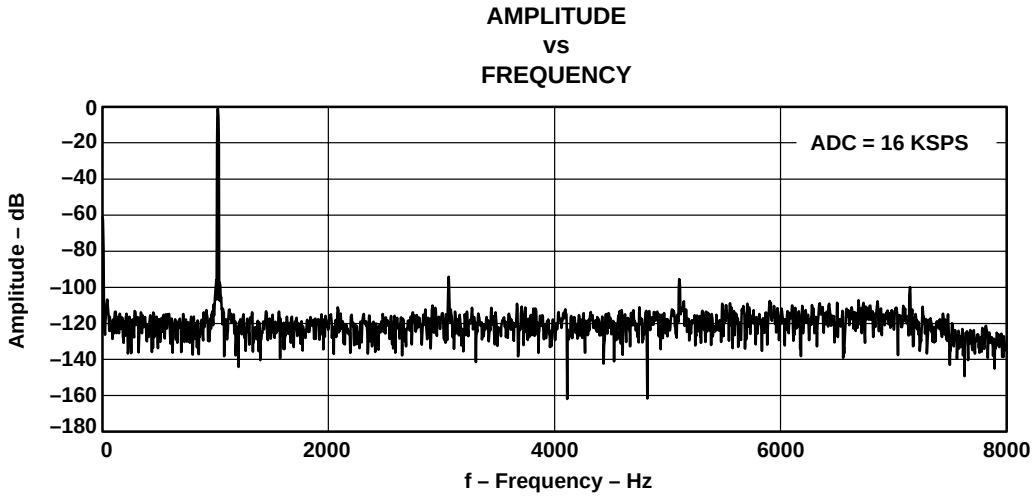


Figure 5–4. FFT—ADC Channel (–1 dB Input)

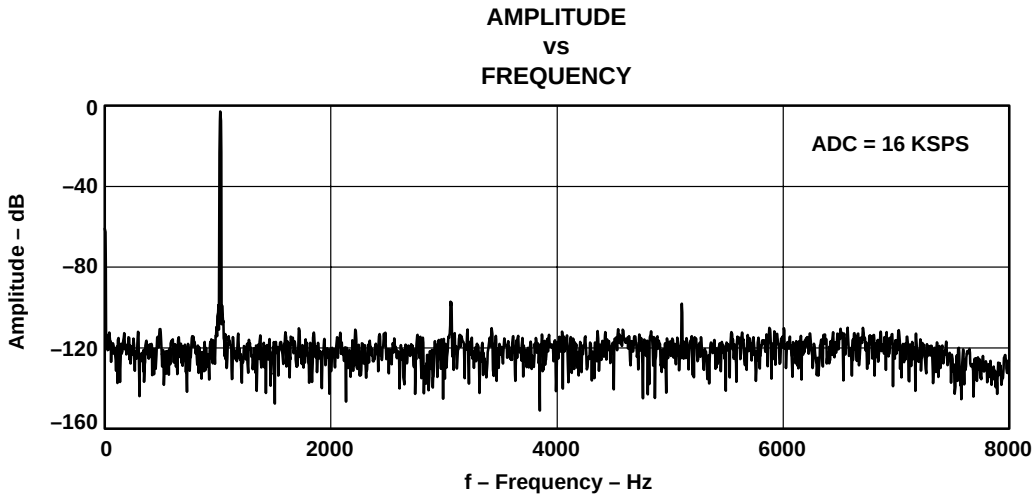


Figure 5–5. FFT—ADC Channel (–3 dB Input)

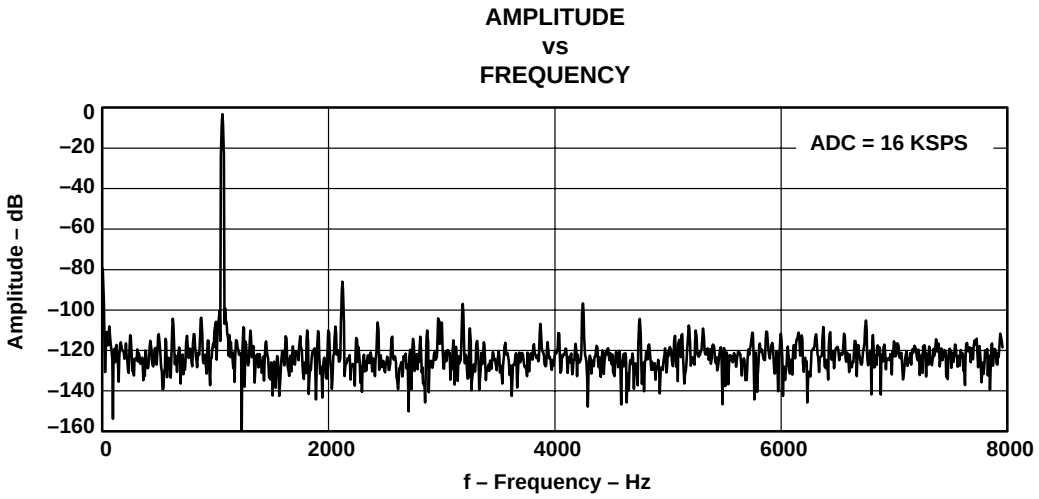


Figure 5–6. FFT—DAC Channel (–3 dB Input)

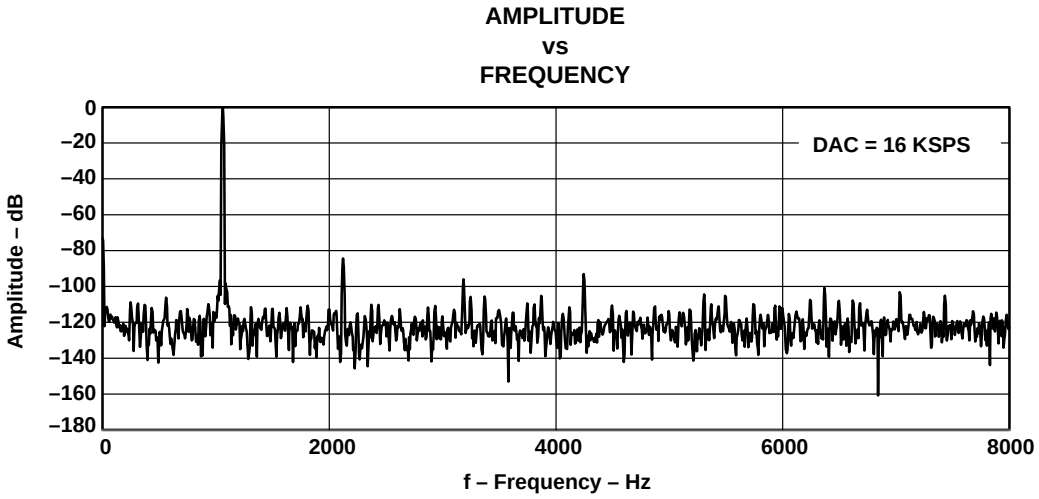


Figure 5–7. FFT—DAC Channel (0 dB Input)

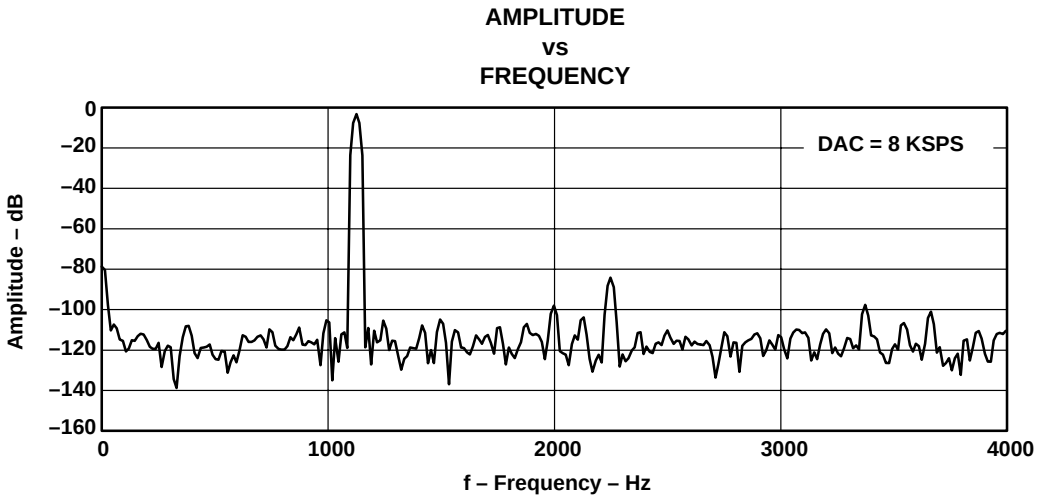


Figure 5–8. FFT—DAC Channel (–3 dB Input)

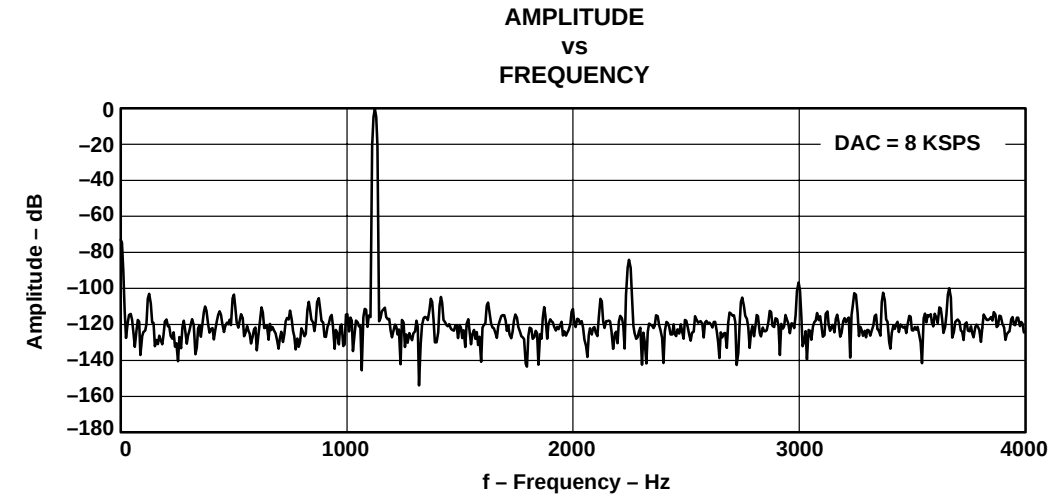


Figure 5–9. FFT—DAC Channel (0 dB Input)

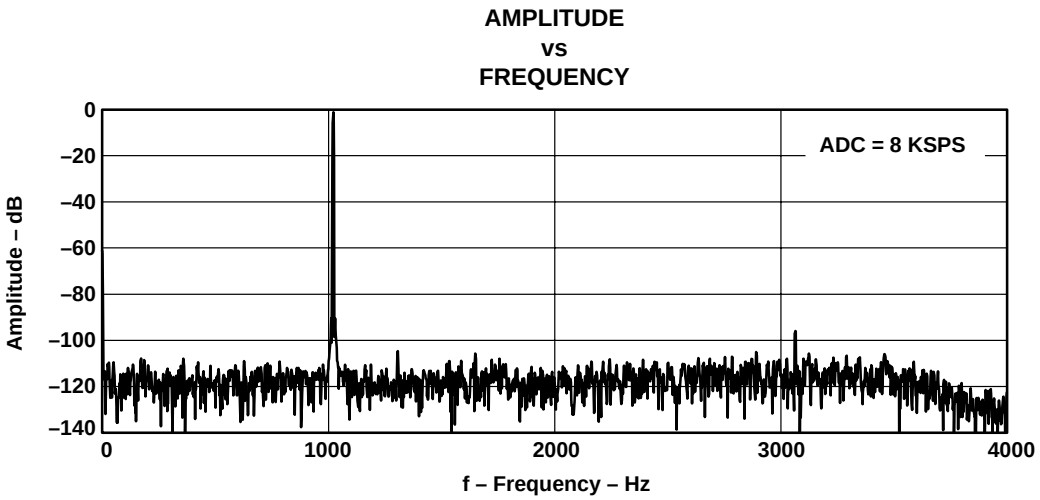


Figure 5–10. FFT—ADC Channel (–1 dB Input)

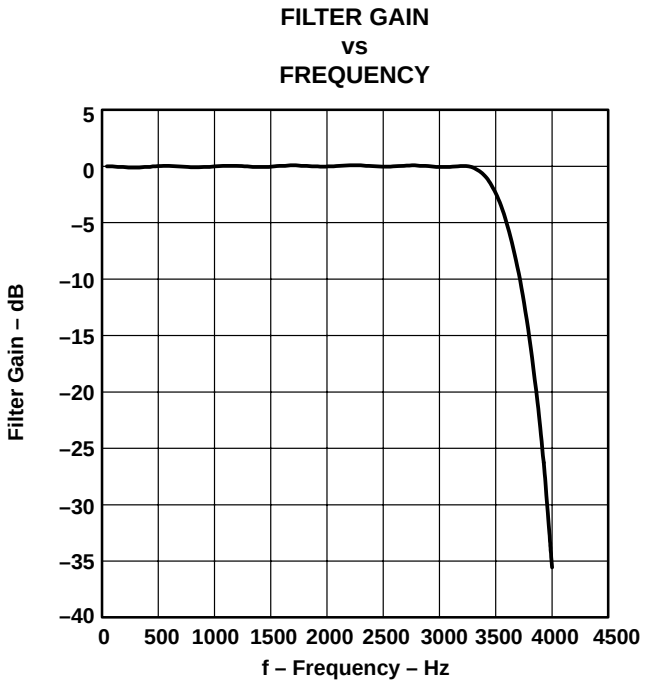


Figure 5–11. ADC FIR Frequency Response

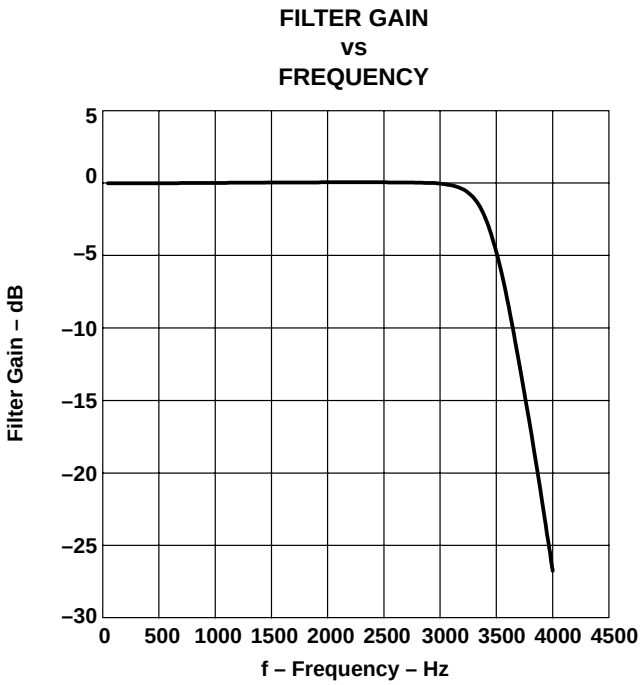


Figure 5–12. ADC IIR Frequency Response

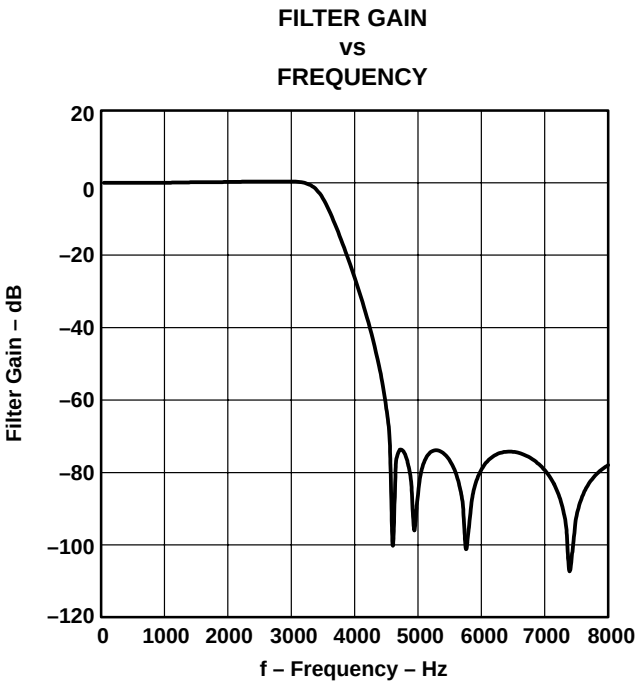


Figure 5–13. DAC IIR Frequency Response (OSR = 512)

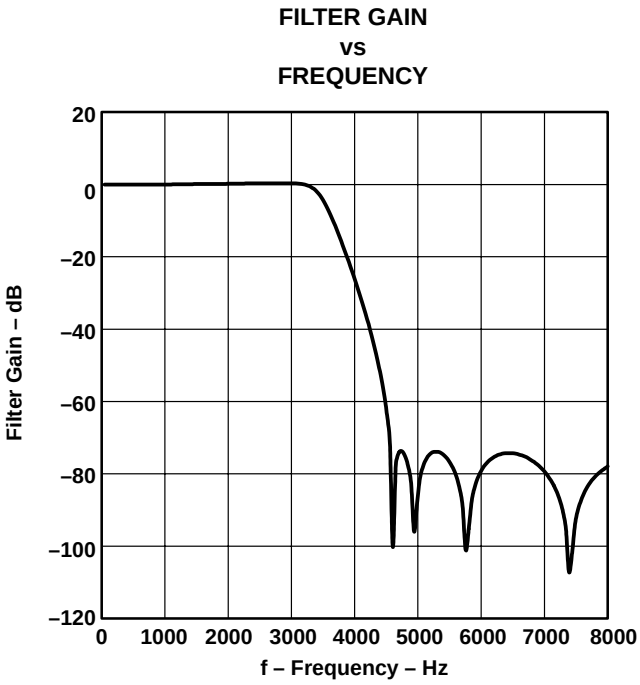


Figure 5–14. DAC IIR Frequency Response (OSR = 256)

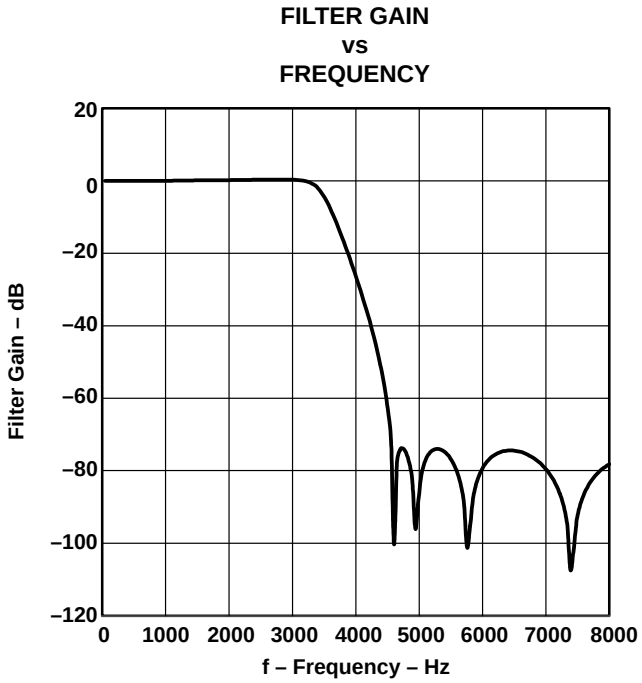


Figure 5–15. DAC IIR Frequency Response (OSR = 128)

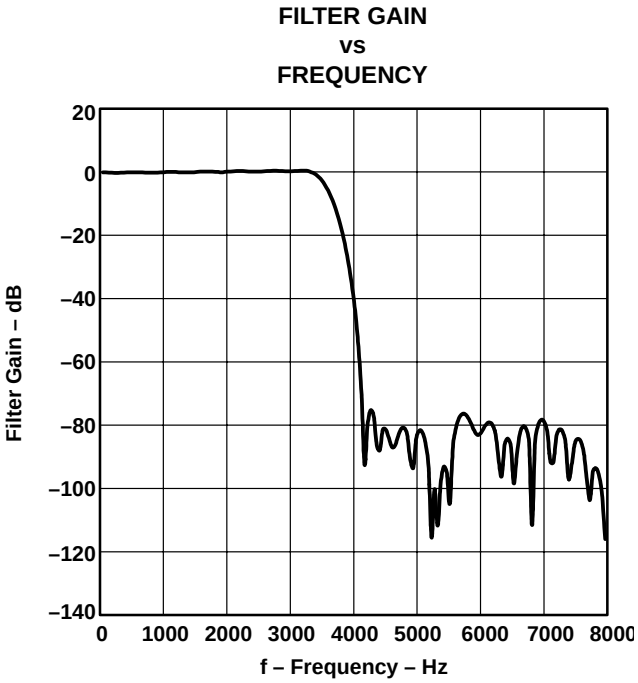


Figure 5–16. DAC FIR Frequency Response (OSR = 512)

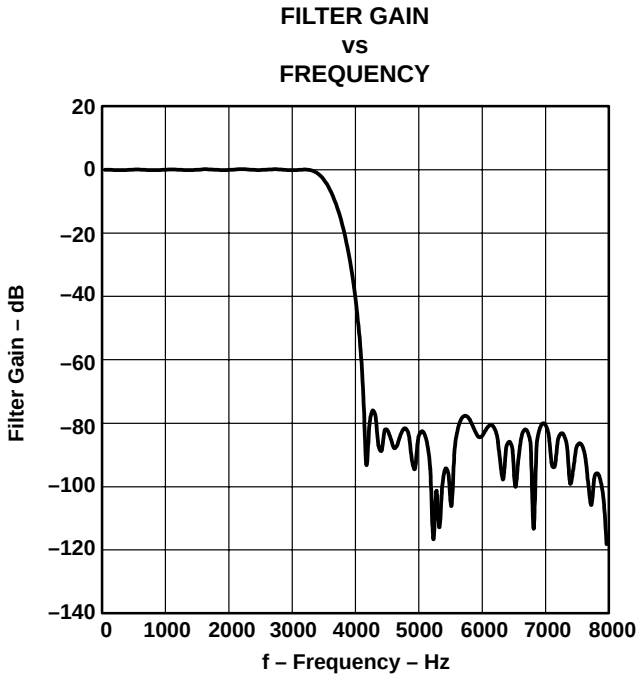


Figure 5–17. DAC FIR Frequency Response (OSR = 256)

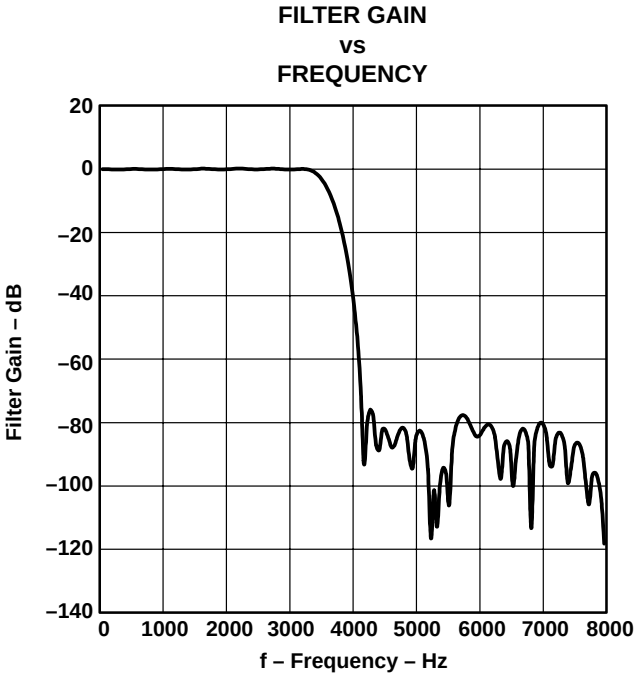


Figure 5–18. DAC FIR Frequency Response (OSR = 128)

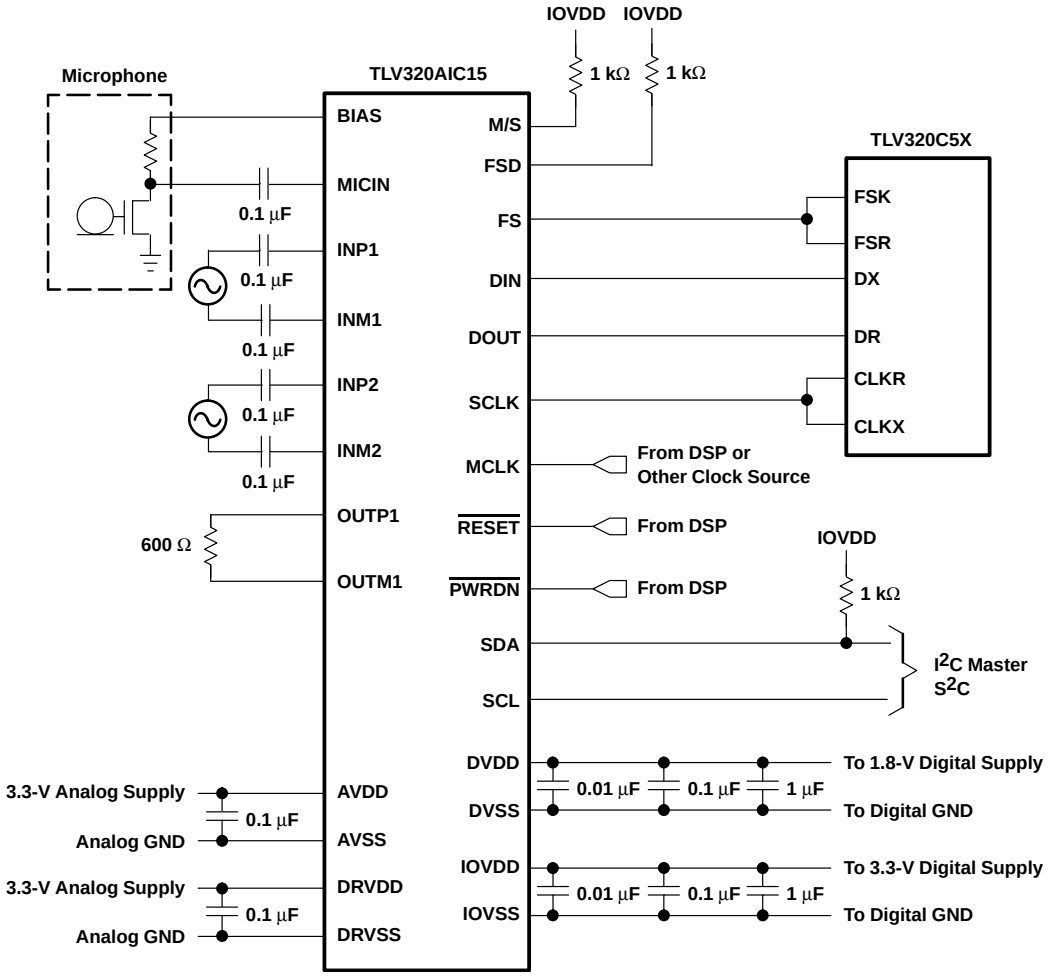


Figure 5–19. Single-Ended Microphone Input (Internal Common Mode)

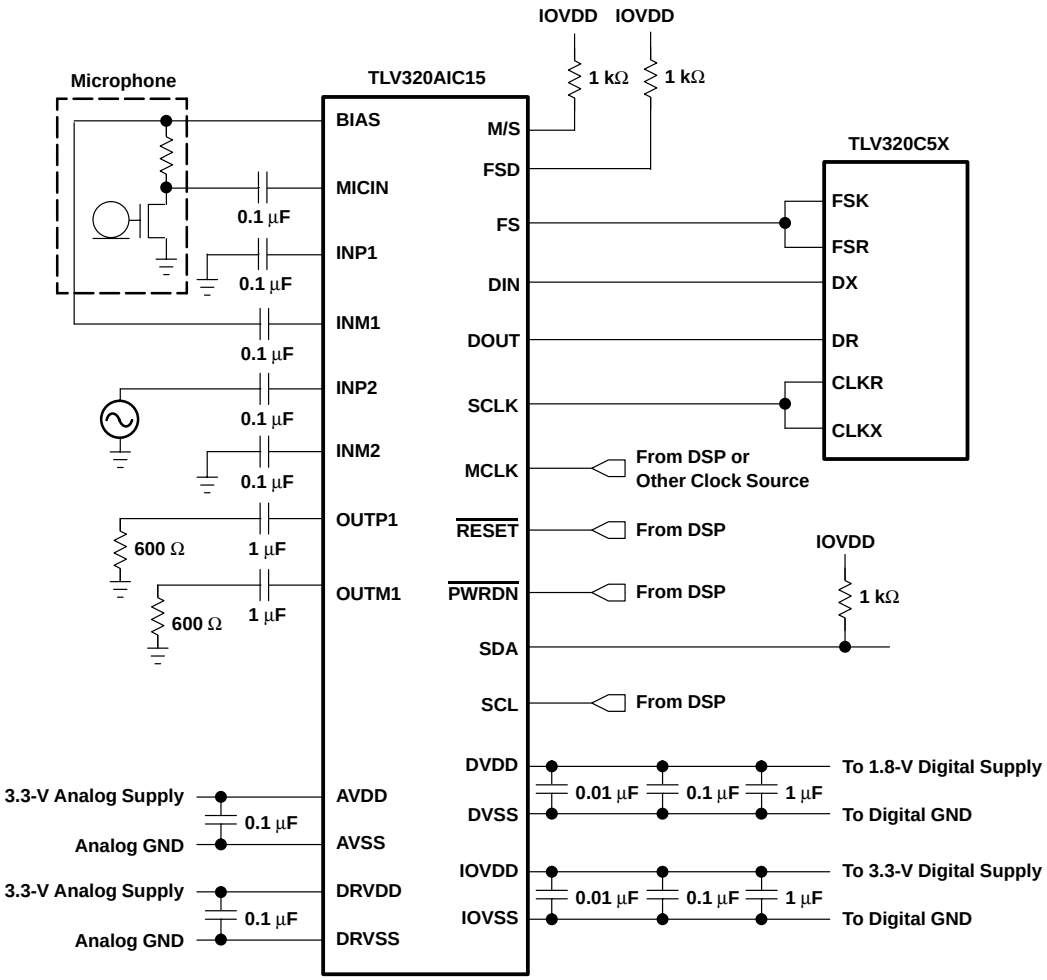


Figure 5–20. Pseudo-Differential Microphone Input (External Common Mode)

5.12 Layout and Grounding Guidelines for TLV320AIC15

TLV320AIC15 has a built-in analog antialias filter, which provides rejection to external noise at high frequencies that may couple into the device. Digital filters with high out-of-band attenuation also reject the external noise. If the differential inputs are used for the ADC channel, then the noise in the common-mode signal is also rejected by the high CMRR of TLV320AIC15. Using external common-mode for microphone inputs also helps reject the external noise. However to extract the best performance from TLV320AIC15, care must be taken in board design and layout to avoid coupling of external noise into the device.

TLV320AIC15 supports clock frequencies as high as 100 MHz. To avoid coupling of fast switching digital signals to analog signals, the digital and analog sections should be separated on the board. In TLV320AIC15 the digital and analog pins are kept separated to aid such a board layout. A separate analog ground plane should be used for the analog section of the board. The analog and digital ground planes should be shorted at only one place as close to TLV320AIC15 as possible. No digital trace should run under TLV320AIC15 to avoid coupling of external digital noise into the device. It is suggested to have the analog ground plane running below the TLV320AIC15. The power supplies should be decoupled close to the supply pins, preferably, with 0.1 μF ceramic capacitor and 10 μF tantalum capacitor following. The ground pin should be connected to the ground plane as close as possible to the TLV320AIC15, so as to minimize any inductance in the path. Since the MCLK is expected to be a very high frequency signal, it is advisable to shield it with digital ground.

For best performance of ADC in differential input mode, the differential signals must be routed close to each other in similar fashion, so that the noise coupling on both the signals is the same and can be rejected by the device.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV320AIC15IDBT	Active	Production	TSSOP (DBT) | 30	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320AIC15I

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

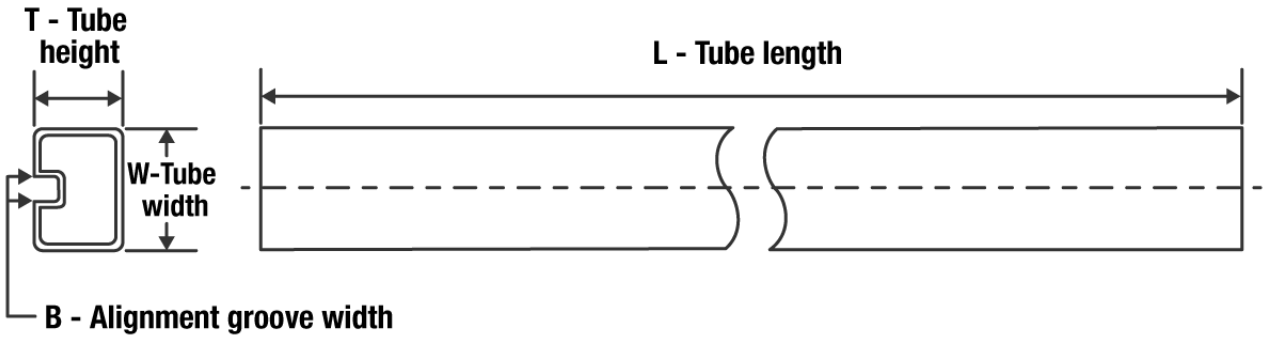
(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE



*All dimensions are nominal

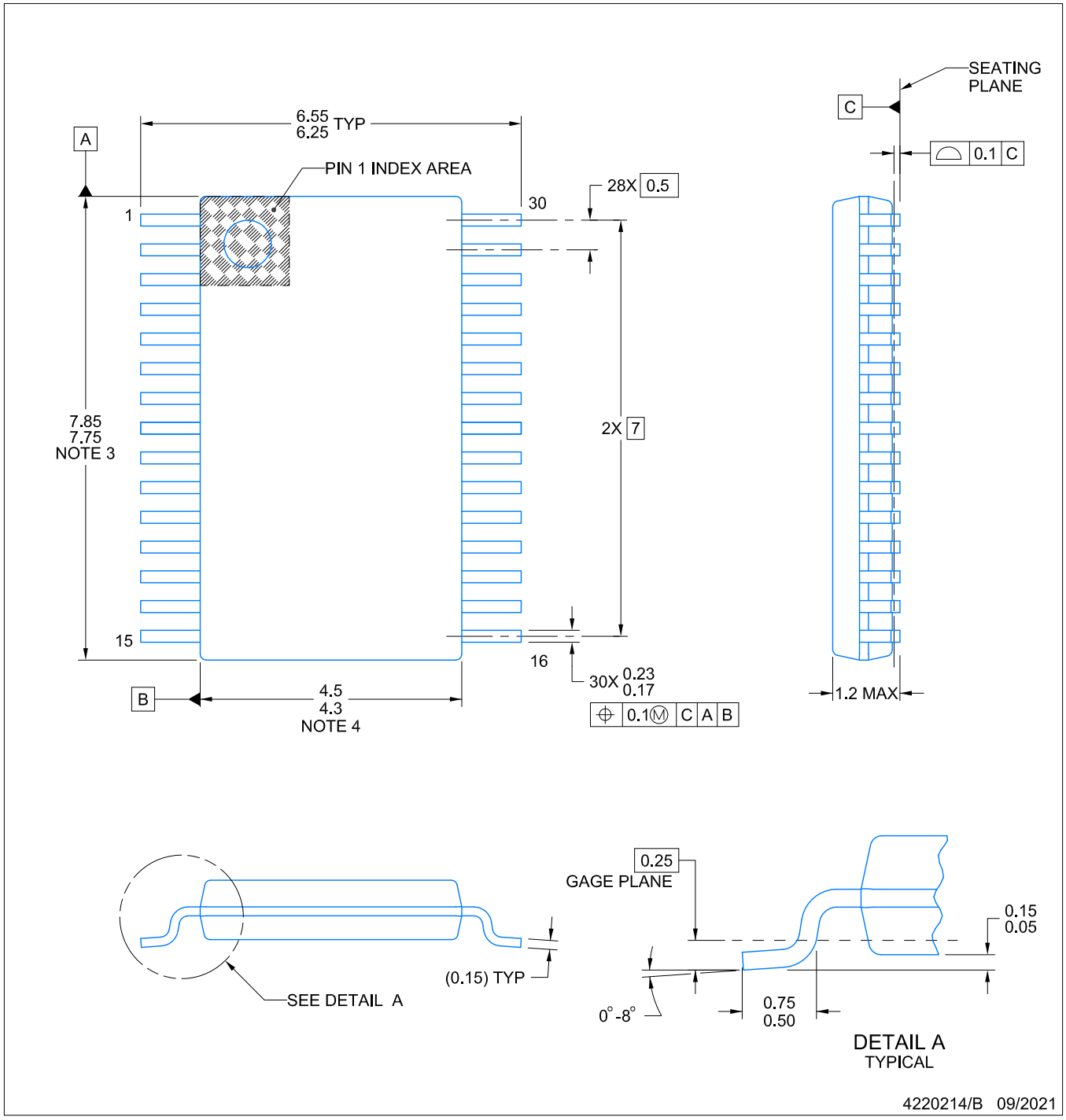
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV320AIC15IDBT	DBT	TSSOP	30	60	530	10.2	3600	3.5

PACKAGE OUTLINE

DBT0030A

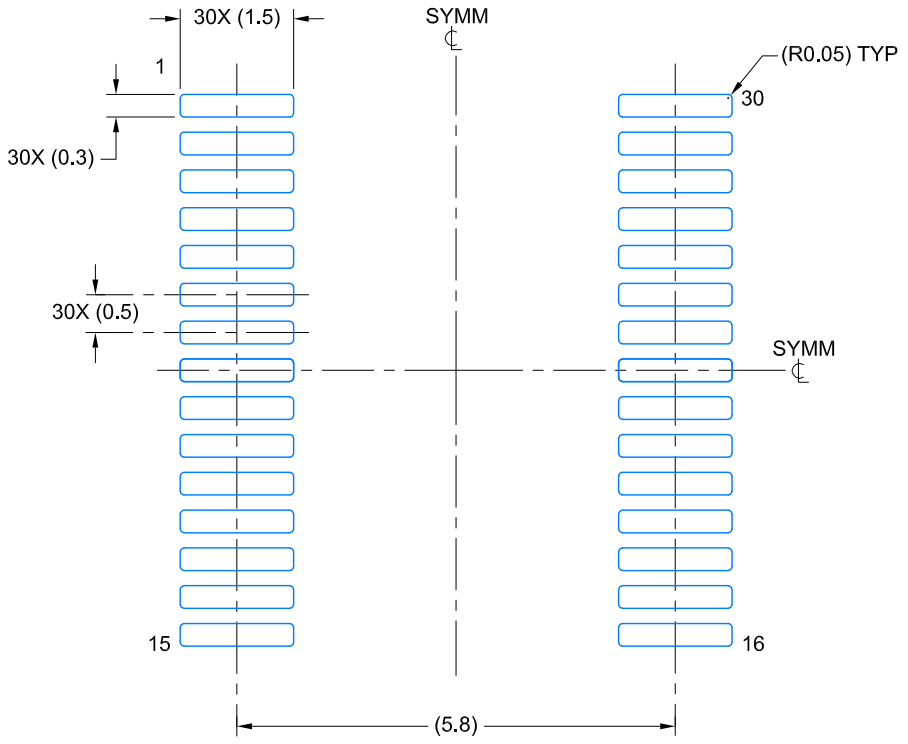
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

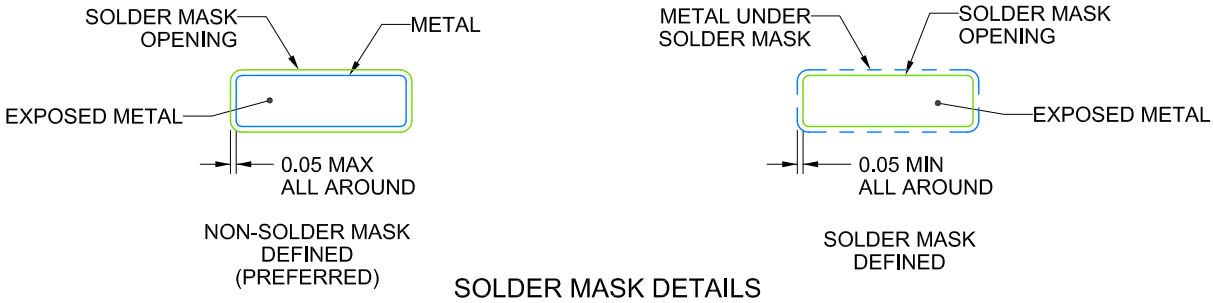


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

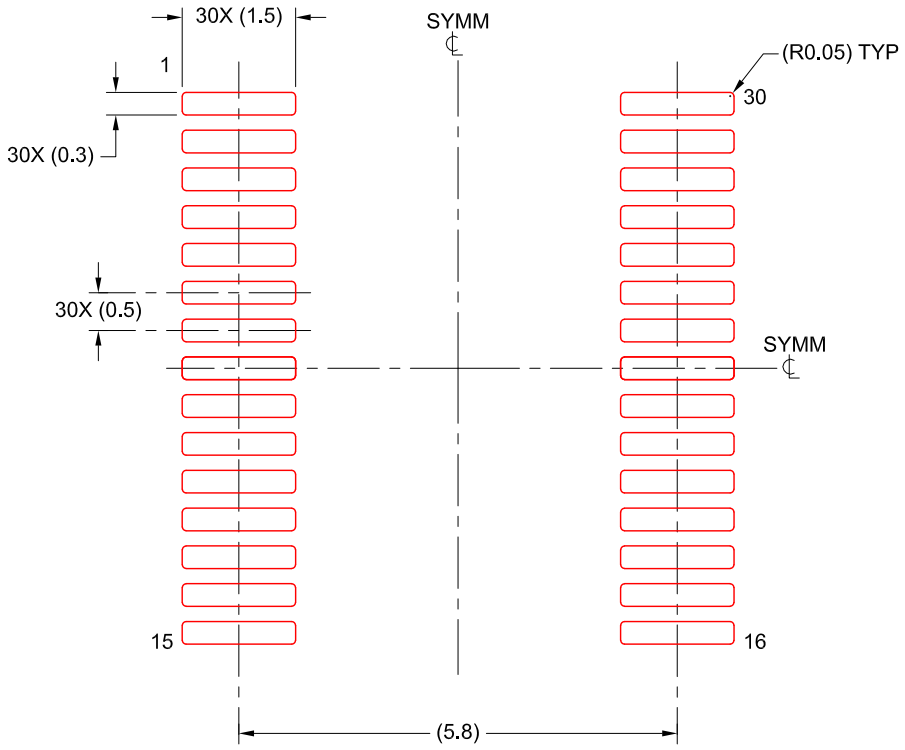


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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