CMX7241/CMX7341
PMR Common Platform Processor

7241/7341FI-2.x: DMR Air Interface Processor

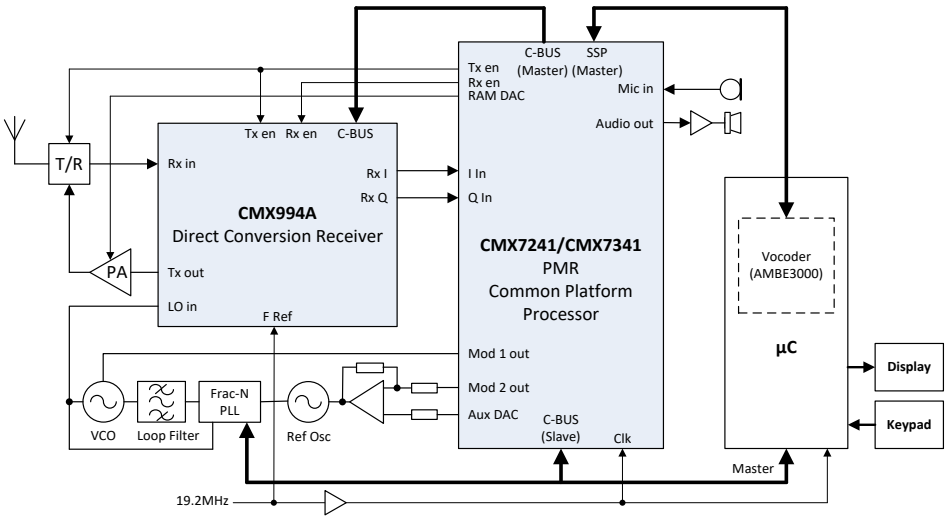
D/7241_7341_FI2.x/14 October 2016 **DATASHEET** Provisional Information

Features

- **Digital DMR Functions:**
- **DMR (ETSI TS 102 361-1) Compliant**
- **Air Interface Physical Layer (Layer 1)**
- **Air Interface Data Link Layer (Layer 2)**
- **Tier 1: peer-to-peer mode (un-licensed)**
- **Tier 2: conventional (licensed) mode**
- **Tier 3: trunked mode support**
- **Status and Data modes**
- **Tx Sequencer**
- **Additional Features**
- **2 Auxiliary ADCs (4 Multiplexed Inputs)**
- **4 Auxiliary DACs**
- **2 Auxiliary System Clock Outputs**
- **Tx Outputs for Two-point or I/Q Modulation**
- **Rx Inputs for Limiter/discriminator or CMX994A Direct Conversion (I/Q) Receiver**
- **C-BUS serial interface to CMX994A transceiver**
- **Voice Codec supports external vocoders (SPI/PCM/I²S compatible - e.g. AMBE+2)**
- **Analogue FM Voice Rx/Tx modes**
- **Analogue FM CTCSS/DCS support**
- **Analogue FM Selcall, DTMF and 1200 baud FFSK support**
- **C-BUS Serial Interface to µC**
- **Flexible Powersave Modes**
- **Low-power (3.3V) Operation**
- **Dedicated hardware reset pin**
- **Single-ended inputs (CMX7241)**
- **Differential inputs (CMX7341)**
- **Available in LQFP or VQFN Packages (CMX7341 – VQFN only)**

Applications

- **Digital Mobile Radio**



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1 Brief Description

The 7241/7341FI-2 Function Image™ (FI) implements a half-duplex 4FSK modem and a large proportion of the DMR Air Interface (physical) layer and Data Link layer. In conjunction with a suitable host and an RF transceiver, a compact, low-cost, low-power digital PMR radio conforming to ETSI's DMR standard TS 102 361-1 can be realised.

Conventional Analogue modes can be supported by re-loading the device with the 7241/7341FI-1 (I/Q Rx mode or LD Rx mode). The CMX7241 and CMX7341 are identical in functionality; the only hardware differences between the two devices are:

- In the input stage: the CMX7241 has single-ended inputs whereas the CMX7341 is a differential input version, allowing for a direct interface to the CMX994.
- The CMX7341 uses two serial ports, one to control the CMX994A in C-BUS mode and the second in SPI-Master mode to provide an audio codec interface to an external vocoder.

The embedded functionality of the 7241/7341FI-2, managing voice and data systems autonomously, including routing audio signals to/from the Vocoder (via the Auxiliary SPI/C-BUS interface), minimises host microcontroller interactions enabling the lowest operating power and therefore the longest battery life for a DMR radio.

From 7241/7341FI-2.3.0.0 onwards, Analogue FM voice and signalling support is available to assist in seamlessly migrating from, or allowing backwards compatibility with, legacy analogue radio modes[1].

The device allows the designer to choose between conventional limiter/discriminator receiver architecture (CMX7241) or an I/Q-based direct conversion architecture (CMX7341) utilising the built-in support for the CMX994A Direct Conversion Receiver.

The device utilises CML's proprietary *FirmASIC®* component technology. On-chip sub-systems are configured by a Function Image™: This is a data file that is uploaded during device initialisation and defines the device's function and feature set. The Function Image™ can be loaded from the host microcontroller over the built-in C-BUS serial interface. The device's functions and features may be enhanced by future Function Image™ releases, facilitating in-the-field upgrades. This document refers specifically to the features provided by Function Image™ 7241/7341FI-2.x.

Other features include two auxiliary ADCs with four selectable inputs and four auxiliary DAC interfaces (with an optional RAMDAC on the first DAC output, to facilitate transmitter power ramping).

The device has flexible powersaving modes and is available in the following packages: VQFN (CMX7241 and CMX7341) and LQFP (CMX7241 only).

Note that text shown in pale grey indicates features that will be supported in future versions of the Function Image™.

This datasheet is the first part of a two-part document comprising datasheet and user manual: the datasheet/user manual combination can be obtained by registering your interest in this product with your local CML representative.

[1] Analogue FM Rx functionality is currently optimised only for Limiter/Discriminator mode.

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History

Version	Changes	Date
14	• Section 6.5.2: Added note on Rx LD signal routing to Input 2 • Section 7.1.4: Added Selcall parametrics • Various clarifications, cross references and editorial corrections	October 2016
13	• Section 5.6.5: Added new Figure 8: RSSI/AGC in I/Q mode • Section 6.6.1: Correct SLC opcode position • Section 8.1.22: Added AGC and RSSI reporting to $9E • Entire document: Added Analogue FM functionality (Rx currently optimised only for LD mode)	June 2016
12	• First public launch of LD mode • Section 5.6.5: Added description for RSSI Measurement (I/Q Mode) • Section 8.1.22: Added description for register $9E (RSSI information now available) • Section 8.1.47: Add I/Q DC tracking re-acquire inhibit and relaxed FS error tolerance to $C2 • Section 8.1.48: Add Tx Symbol Level adjustment to $C3:Dxxx • Section 8.3.7: Setting P6.0:b6 automatically disables RXENA during inactive slots when an MS type channel is being received	May 2016
11	• Section 6.5.17: CMX994E device added to I/Q Calibration description. • Section 6.5.17: Reference to thermal transient during slotted reception. • Section 7.1.3, Operating Characteristics: some figures now added (previously TBA) • Section 8.1.48: $C5 FS reporting register format changed to include slot number • Section 8.3.7: P6.2: Add CMX994 / A / E options • Functionality introduced since FI-2.1.1.0 / FI-2.2.1.0 is now 'un-greyed' within the document • Table 1: Change R20,21 to 47k (was 470k)	November 2015
10	First public release	October 2015

This is Provisional Information; changes and additions may be made to this specification. Parameters marked TBD or left blank will be included in later issues. Items that are highlighted or greyed out should be ignored. These will be clarified in later issues of this document.
Information in this datasheet should not be relied upon for final product design.

2 Block Diagrams

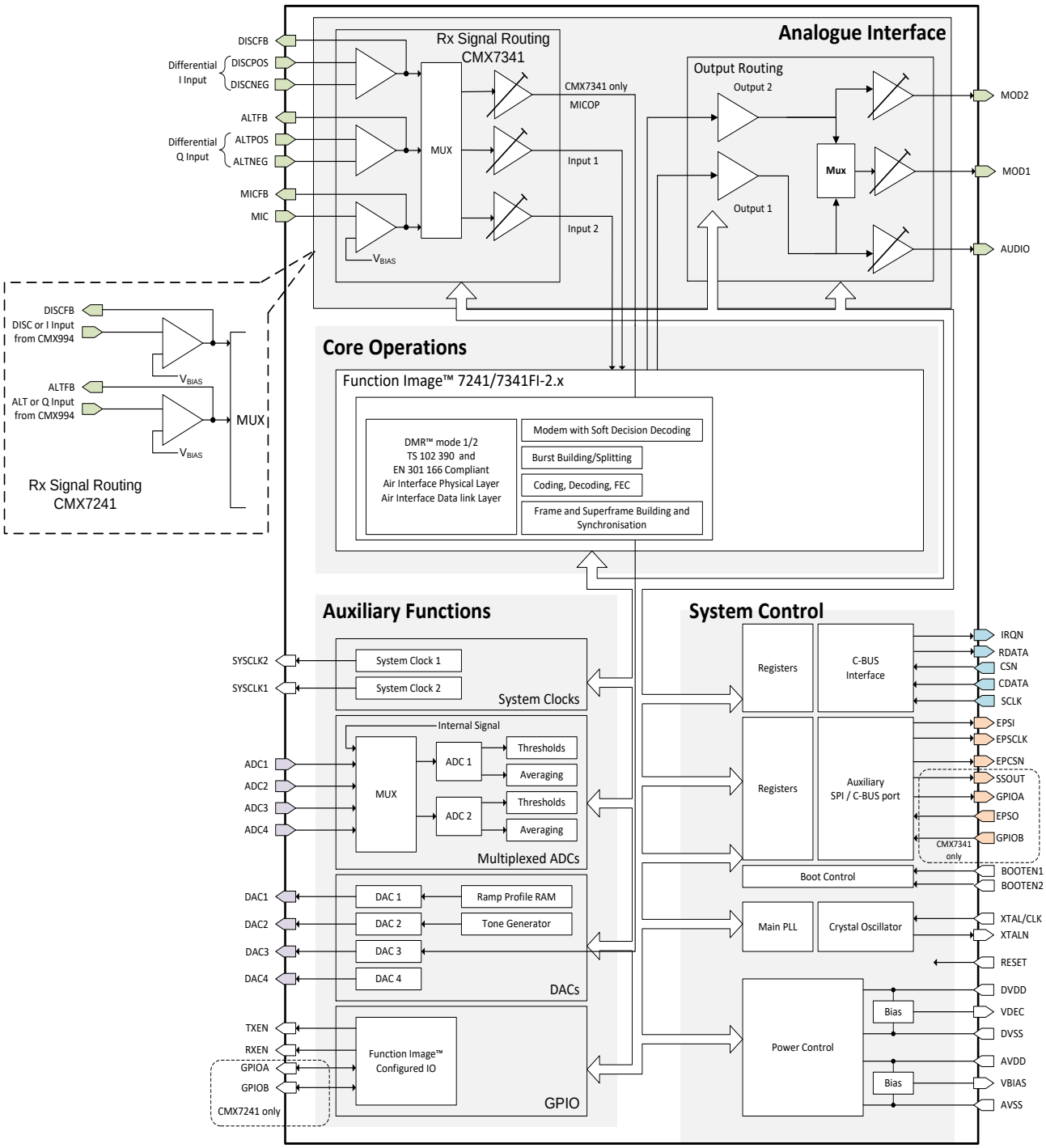


Figure 1 CMX7241/CMX7341 Block Diagram

3 Signal List

CMX7241 48-pin Q3/L4	CMX7341 48-lead Q3	Pin Name	Type	Description	
1	1	EPSI	OP	Serial Data Output	Auxiliary SPI/C-BUS
2	2	EPSCLK	OP	Serial Clock Output	
3	3	EPSO	IP+PD	SPI-Codec Serial Data Input	
4	4	EPCSN	OP	CMX994A Serial Chip Select	
5	5	BOOTEN1	IP+PD	Used in conjunction with BOOTEN2 to determine the operation of the bootstrap program	
6	6	BOOTEN2	IP+PD	Used in conjunction with BOOTEN1 to determine the operation of the bootstrap program	
7	7	RESET	PWR	Dedicated reset function – active high. When asserted has the same effect as a power on reset. If unused, tie to DVSS	
8	8	IRQN	OP	A 'wire-ORable' output for connection to the Interrupt Request input of the host. Pulled down to DV_{SS} when active and is high impedance when inactive. An external pull-up resistor (R1) is required.	Host C-BUS
9	9	VDEC	PWR	Internally generated 1.8V digital supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed. If the device is to be run from a 1.8V external supply then the VDEC pin must be connected directly to the external 1.8V regulated supply.	
10	10	RXENA	OP	Rx Enable – active when in Rx mode	
11		GPIOA	BI		
12		GPIOB	BI		
	11	GPIOA	OP	SPI-Codec Serial Data Output	Auxiliary SPI/C-BUS
	12	GPIOB	OP	SPI-Codec Serial Clock Output	
13		SYSCLK1	OP	Digital System Clock 1 (same as XTAL/CLK at Power-on)	
	13	SYSCLK1	OP	Digital System Clock 1 / External LNA Enable	
14	14	DVSS	PWR	Digital ground	
15	15	TXENA	OP	Tx Enable – active when in Tx mode	
16		DISC	IP	Discriminator inverting input or I input from CMX994	
17		DISCFB	OP	Discriminator input amplifier feedback	
18		ALT	IP	Alternate inverting input or Q input from CMX994	
19		ALTFB	OP	Alternate input amplifier feedback	
	16	DISCPOS	IP	Differential input 1, positive and negative. I input from CMX994	
	17	DISCNEG	IP		
	18	DISCFB	OP	Input 1 amplifier feedback	
	19	ALTPOS	IP	Differential input 2, positive and negative. Q input from CMX994	
	20	ALTNEG	IP		
	21	ALTFB	OP	Input 2 amplifier feedback	

CMX7241 48-pin Q3/L4	CMX7341 48-lead Q3	Pin Name	Type	Description	
20	**22**	MICFB	OP	Microphone input amplifier feedback	
21	**23**	MIC	IP	Microphone inverting input	
22	n/c	AVSS	PWR	Analogue ground	
23	**24**	MOD1	OP	Modulator 1 output	
24	**25**	MOD2	OP	Modulator 2 output	
25	**26**	VBIAS	OP	Internally generated bias voltage of approx. $AV_{DD}/2$, except when the device is in 'Powersave' mode when V_{BIAS} will discharge to AV_{SS}. Must be decoupled to AV_{SS} by a capacitor mounted close to the device pins. No other connections allowed unless buffered.	
26	**27**	AUDIO	OP	Audio Output in SPI-Codec mode	
27	**28**	ADC1	IP	Auxiliary ADC input 1	Each of the two ADC blocks can select its input signal from any one of these input pins, or from the MIC, ALT or DISC input pins. See section 6.16 for details.
28	**29**	ADC2	IP	Auxiliary ADC input 2	
29	**30**	ADC3	IP	Auxiliary ADC input 3	
30	**31**	ADC4	IP	Auxiliary ADC input 4	
31	**32**	AVDD	PWR	Analogue +3.3V supply rail. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AV_{SS} by capacitors mounted close to the device pins.	
32	**33**	DAC1	OP	Auxiliary DAC output 1 / RAMDAC	
33	**34**	DAC2	OP	Auxiliary DAC output 2 / Tone Generator output	
34	n/c	AVSS	PWR	Analogue ground	
35		DAC3	OP	Auxiliary DAC output 3	
	35	DAC3/MICOP	OP	Auxiliary DAC output 3 / MICOP (see note 1)	
36	**36**	DAC4	OP	Auxiliary DAC output 4	
37	**37**	DVSS	PWR	Digital Ground	
38	**38**	VDEC	PWR	Internally generated 1.8V supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed.	
39	**39**	XTAL/CLK	IP	Input from the external clock source or Xtal	
40	**40**	XTALN	OP	The output of the on-chip Xtal oscillator inverter. NC if external clock used.	
41	**41**	DVDD	PWR	Digital +3.3V supply rail. This pin should be decoupled to DV_{SS} by capacitors mounted close to the device pins.	
42	**42**	CDATA	IP	Command Data input from the µC	Host C-BUS
43	**43**	RDATA	TS OP	Reply Data tri-state output to the µC (high impedance when not sending data to the µC).	
44	**44**	SSOUT	OP	SPI-Codec Frame Sync	Auxiliary SPI/C-BUS
45	**45**	DVSS	PWR	Digital ground	
46	**46**	SCLK	IP	Serial clock input from the µC	Host C-BUS
47	**47**	SYSCLK2	OP	Digital System Clock 2 - used for Internal SlotClock	

CMX7241 48-pin Q3/L4	CMX7341 48-lead Q3	Pin Name	Type	Description	
48	**48**	CSN	IP	Chip Select input from the µC (no internal pullup on this input)	Host C-BUS
Exposed Metal Pad	**Exposed Metal Pad**	SUBSTRATE	~	The central metal pad (which is exposed on Q3 package only) must be connected to analogue ground (AV_{SS}). **No other electrical connection is permitted.**	

Note 1: In CMX7341 only, this is a dual purpose pin (function defined by $A0:b3. When used in a system which uses the CMX994A with Reverse Channel signalling or Duplex Speech, this should be allocated as MICOP and routed to ADC4 input to allow Microphone -> SPI-Codec operation in parallel with I/Q Rx operation for the duration of the Reverse Channel burst.

Colour Definitions:

= Aux SPI/C-BUS

= Host C-BUS

= Analogue Inputs/Outputs

= ADCs/DACs

Notes: IP = Input (+ PU/PD = internal pullup / pulldown resistor)
OP = Output
BI = Bidirectional
TS OP = 3-state Output
PWR = Power Connection
NC = No Connection - should NOT be connected to any signal.

3.1 Signal Definitions

Signal Name	Pins	Usage
AV_{DD}	AVDD	Power supply for analogue circuits
DV_{DD}	DVDD	Power supply for digital circuits
V_{DEC}	VDEC	Power supply for core logic, derived from DVDD by on-chip regulator
V_{BIAS}	VBIAS	Internal analogue reference level, derived from AVDD
AV_{SS}	AVSS	Ground for all analogue circuits
DV_{SS}	DVSS	Ground for all digital circuits

4 Component and PCB Recommendations

4.1 Recommended External Components

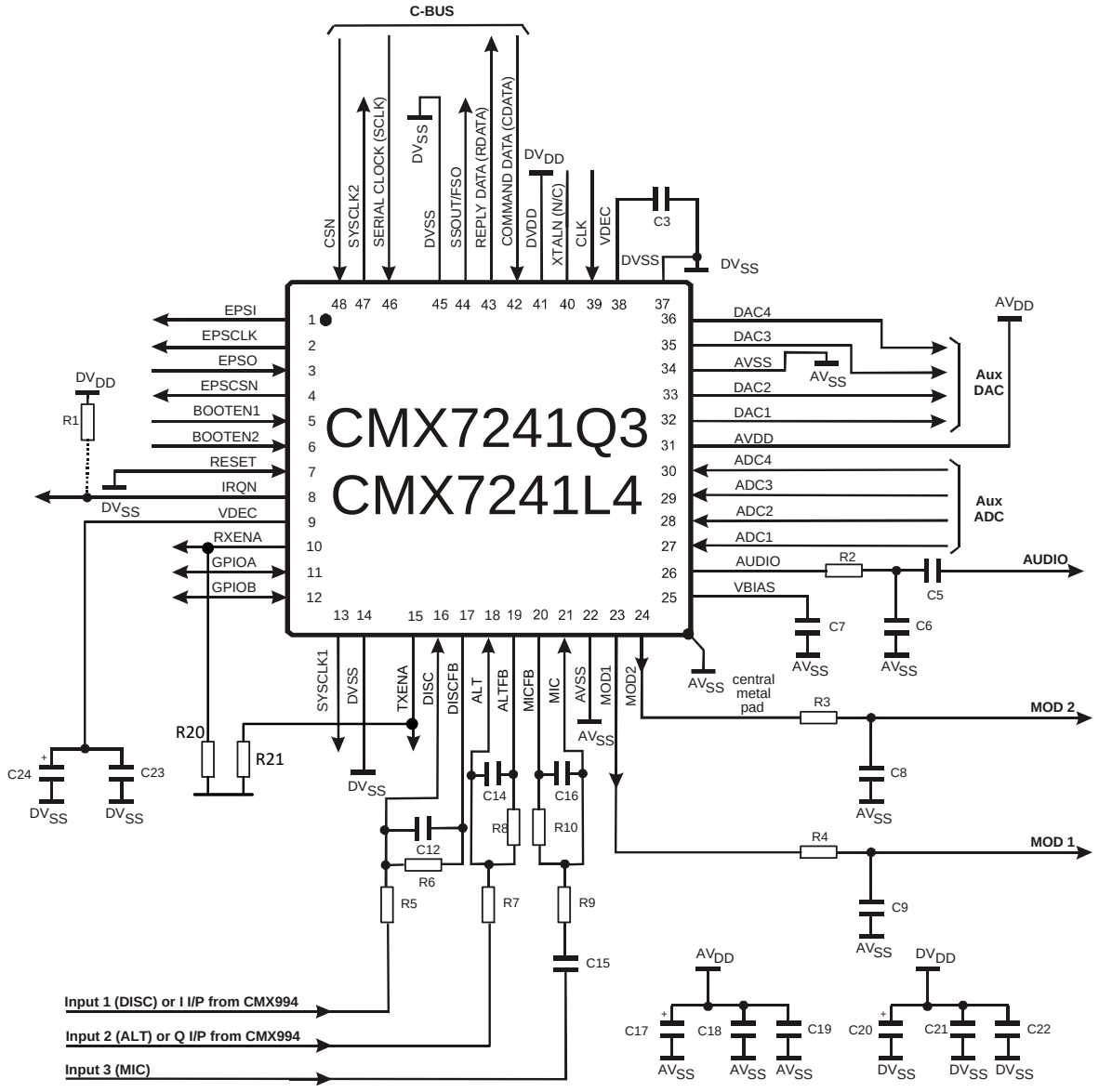


Figure 2 CMX7241 (L4 and Q3) Recommended External Components

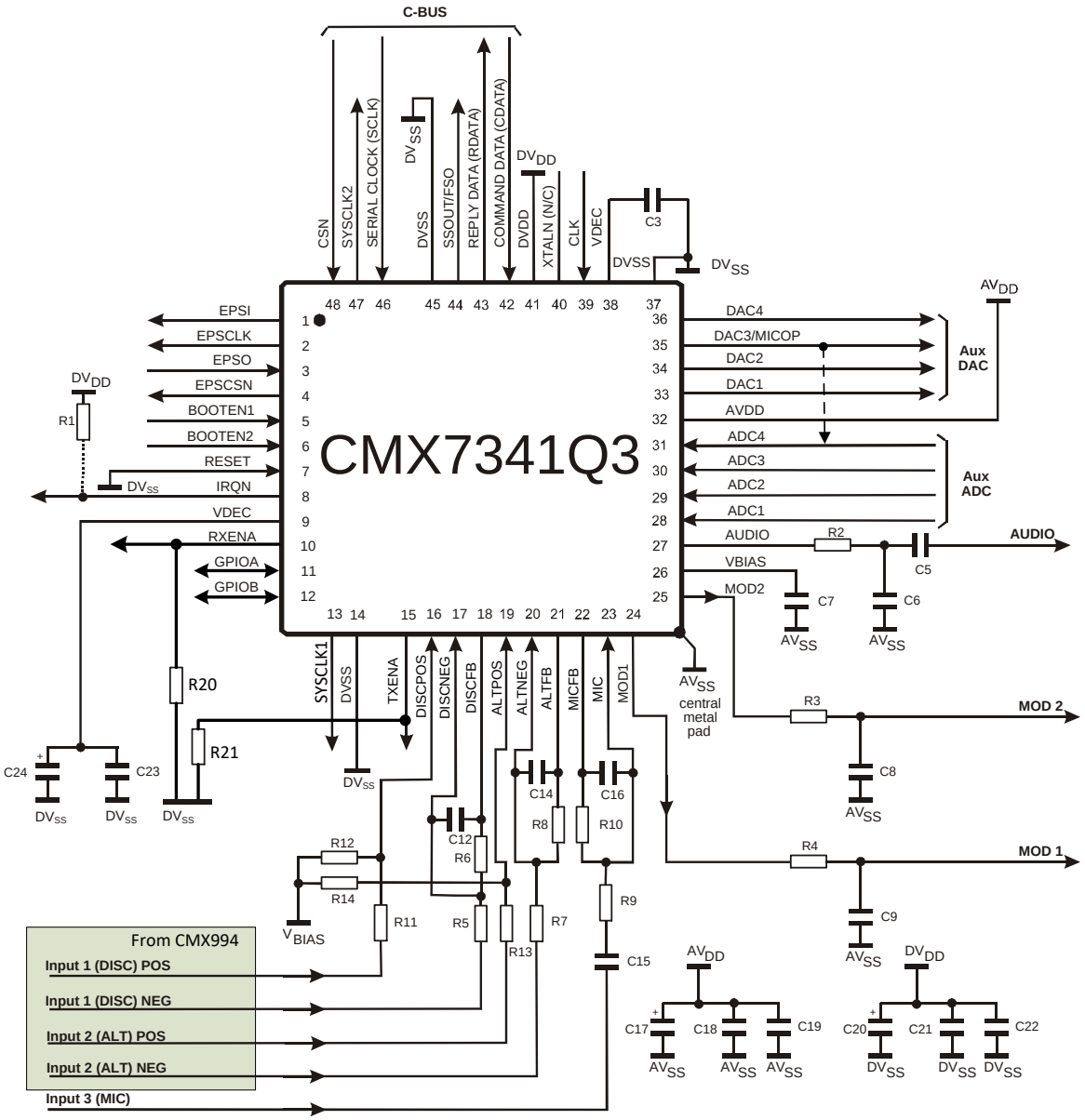


Figure 3 CMX7341 (Q3) Recommended External Components

Table 1 Recommended External Components

R1	100kΩ	C3	10nF	C11	not used	C21	10nF
R2	20kΩ	C4	not used	C12	100pF	C22	10nF
R3	20kΩ	C5	1nF	C13	not used	C23	10nF
R4	20kΩ			C14	100pF	C24	10µF
R5	100kΩ (note 2)			C15	note 5		
R6	100kΩ	C6	100pF	C16	200pF		
R7	100kΩ (note 3)	C7	1µF	C17	10µF		
R8	100kΩ	C8	100pF	C18	10nF		
R9	See note 4	C9	100pF	C19	10nF		
R10	100kΩ	C10	not used	C20	10µF		
R11	100kΩ						
R12	100kΩ	R20	47kΩ				

R13	100kΩ	R21	47kΩ
R14	100kΩ		

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Notes:

1. The CLK input must be an external 19.2MHz source. The tracks between the external clock and the device pins should be as short as possible to achieve optimum performance. By default, a 19.2MHz oscillator is assumed, other values could be used if the internal clock dividers are set to appropriate values.

2. For CMX7241 operation, R5 should be selected to provide the desired dc gain of the discriminator input, as follows:

   $|GAIN_{DISC}| = 100k\Omega / R5$

   The gain should be such that the resultant output at the DISCFB pin is within the DISC input signal range specified in 6.19.2. For 4FSK modulation, this signal should be dc coupled from the Limiter/Discriminator output.

3. For CMX7241 operation, R7 should be selected to provide the desired dc gain of the alternative input as follows:

   $|GAIN_{ALT}| = 100k\Omega / R7$

   The gain should be such that the resultant output at the ALTFB pin is within the alternative input signal range specified in 6.19.

4. R9 should be selected to provide the desired dc gain (assuming C15 is not present) of the microphone input as follows:

   $|GAIN_{MIC}| = 100k\Omega / R9$

   The gain should be such that the resultant output at the MICFB pin is within the microphone input signal range specified in 6.19.1. For optimum performance with low signal microphones, an additional external gain stage may be required.

5. C15 should be selected to maintain the lower frequency roll-off of the MIC input as follows:

   $C15 \geq 30nF \times |GAIN_{MIC}|$

6. When used with a Limiter/Discriminator Receiver, ALT and ALTFB connections allow the user to have a second discriminator or microphone input. Component connections and values are as for the respective DISC and MIC networks. If this input is not required, the ALT pin should be connected to AV_{SS}.

7. AUDIO output is used when SPI-Codec mode has been selected.

8. A single 10µF electrolytic capacitor (C24, fitted as shown) may be used for smoothing the power supply to both VDEC pins, providing they are connected together on the pcb with an adequate width power supply trace. Alternatively, separate smoothing capacitors should be connected to each VDEC pin. High frequency decoupling capacitors (C3 and C23) must always be fitted as close as possible to both VDEC pins.

9. TxENA and RxENA should be pulled down by an external resistor (R20, R21) to be directly compatible with the CMX994A (active high signals) or pulled up to DV_{DD} to be compatible with CMX7141 legacy implementations.

4.2 PCB Layout Guidelines and Power Supply Decoupling

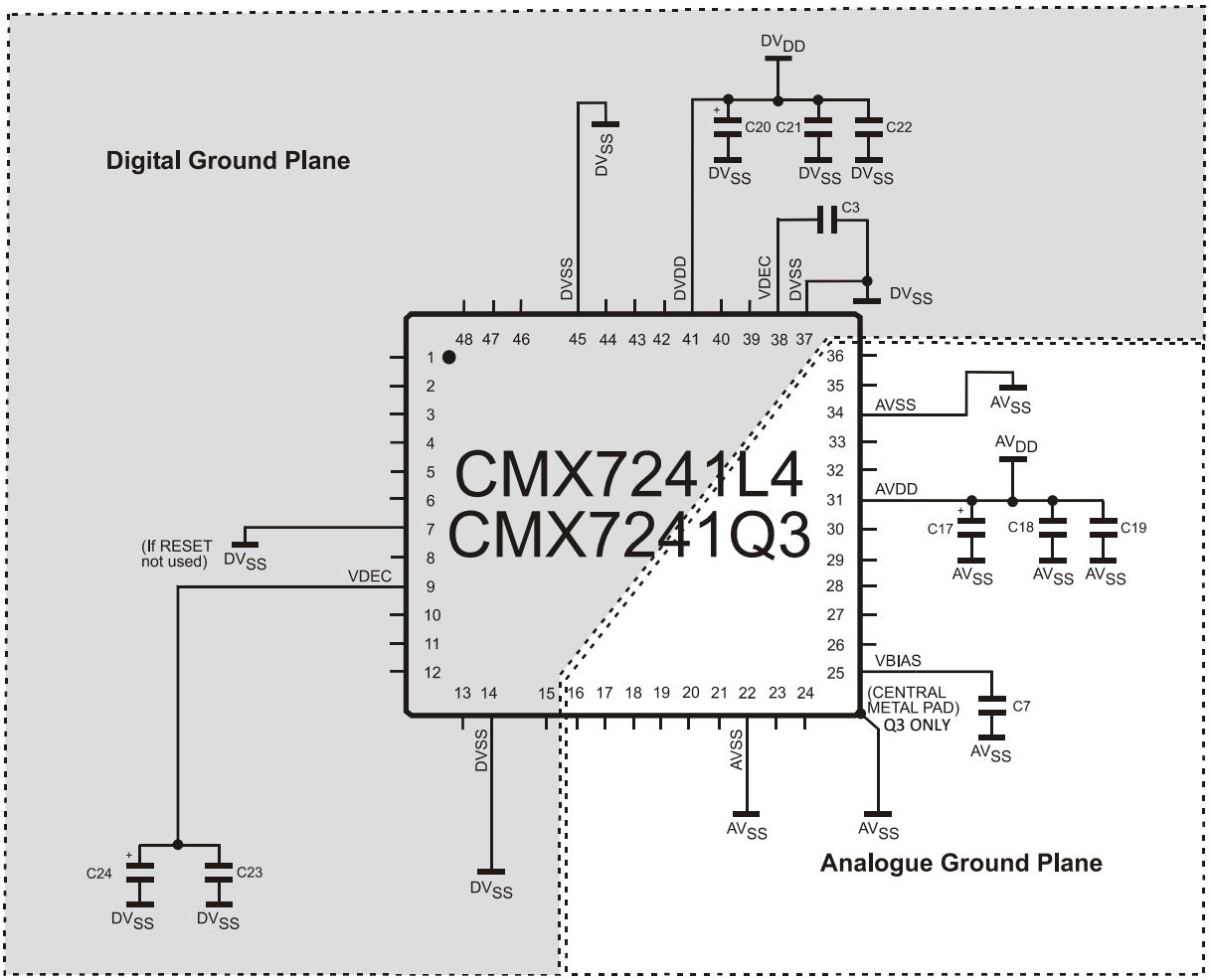


Figure 4 CMX7241 (L4/Q3) Power Supply and De-coupling

Component Values as per Figure 2

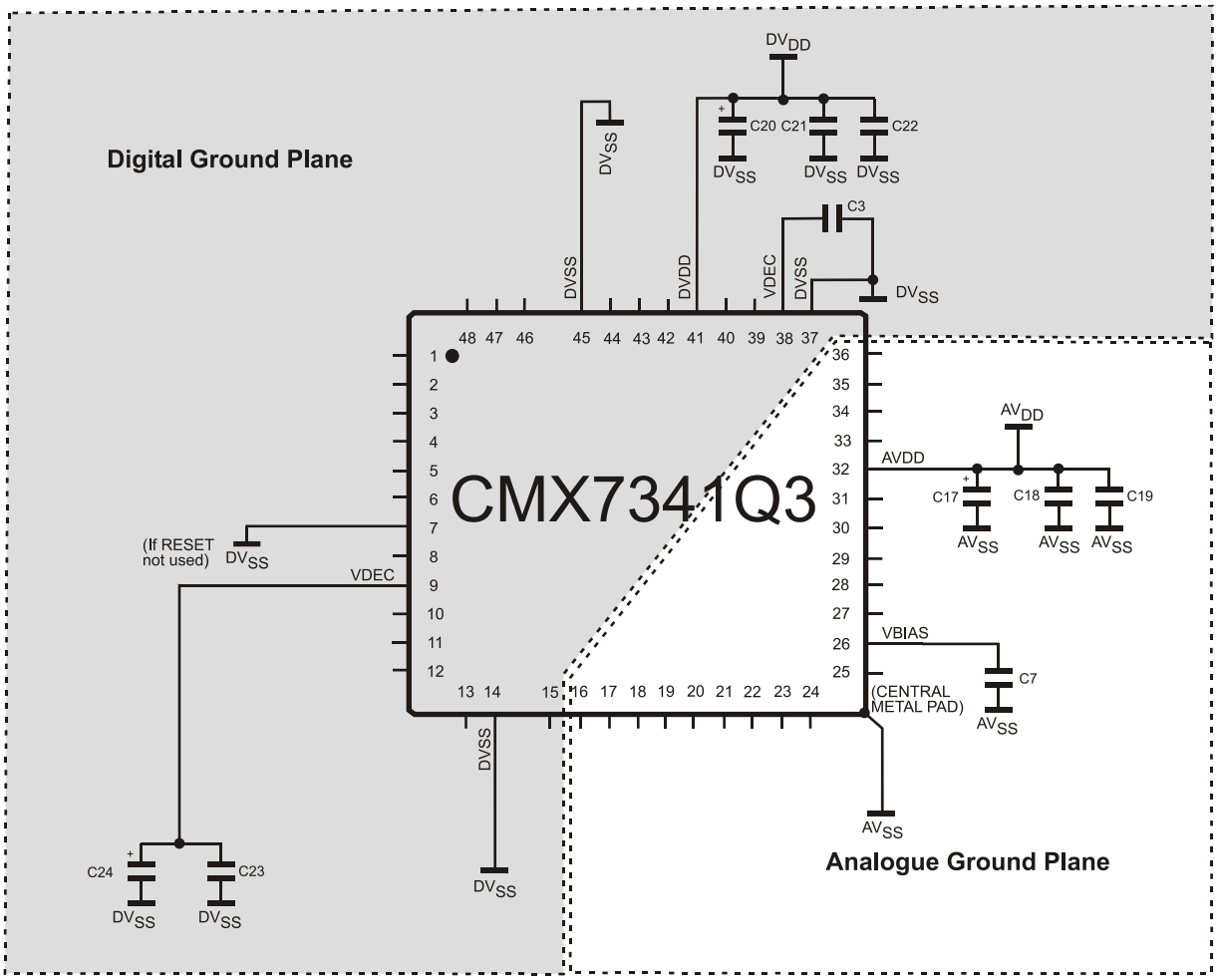


Figure 5 CMX7341 (Q3) Power Supply and De-coupling

Component Values as per Figure 3

Notes:

It is important to protect the analogue pins from extraneous inband noise and to minimise the impedance between the CMX7241/7341 and the supply and bias de-coupling capacitors. The de-coupling capacitors C3, C7, C18, C19, C21, C22 and C24 should be as close as possible to the CMX7241/7341. It is therefore recommended that the printed circuit board is laid out with separate ground planes for the AV_{SS} and DV_{SS} supplies in the area of the device, with provision to make links between them, close to the device. Use of a multi-layer printed circuit board will facilitate the provision of ground planes on separate layers.

V_{BIAS} is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled, to ensure its integrity, so apart from the decoupling capacitor shown, no other loads should be connected. If V_{BIAS} needs to be used elsewhere in the design, it should be buffered with a high input impedance buffer.

The single ended microphone input and audio output must be ac coupled (as shown), so that their return paths can be connected to AV_{SS} without introducing dc offsets. Further buffering of the audio output is advised.

The crystal, X1, should be replaced with an external clock source, usually a VCTXCO, running at 19.2MHz.

The device executes an internal scheduler running at 4.8kHz, which may result in current “spikes” on the DVDD line, which must be taken into account when designing the power supply circuitry.

4.3 CMX994A /CMX994E Interface

The CMX7341 is designed to be used in I/Q mode connected to a CMX994A (or CMX994E) as shown in Figure 6. Component values are shown in Table 2. Where values are not shown refer to the CMX994A Datasheet. Note: Resistors R20 and R21 (see Figure 3) are required to ensure that the TxENA and RxENA signals are kept in an inactive state during FI loading, and inform the FI that these signals should be implemented active high.

The CMX994A and the CMX7341 may share the same 19.2MHz reference (however note that the CMX7341 requires a CMOS logic compatible signal).

AuxADC1 is configured to sense the Adjacent/Alternate channel power levels and so improve the performance of the CMX994A AGC system in situations where high levels of interference may be encountered on alternate channels.

The CMX994A should be connected to the Auxiliary SPI/C-BUS using EPCSN as the chip select (see sections 4.4 and 5.6.3).

Where an external LNA is used (instead of the CMX994's internal LNA), the SYSCLK1 pin can be re-programmed to act as an external LNA enable to aid AGC operation however automatic gain control of the CMX994A by the CMX7341 will not function correctly in this case so should be disabled.

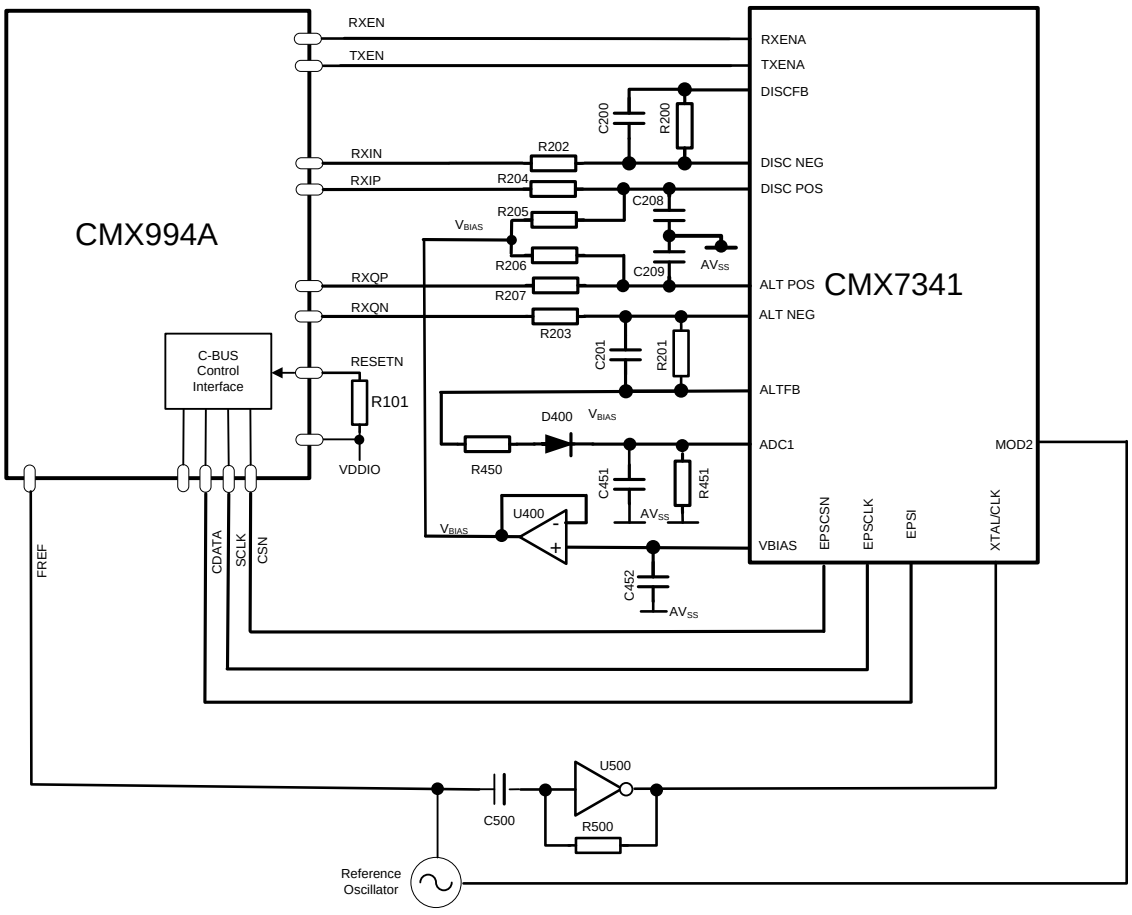


Figure 6 CMX7341/CMX994A Interface

Table 2 Recommended External Components when using CMX994

R101	100kΩ	C200	220pF	C208	220pF
R200 to R207	100kΩ	C201	220pF	C209	220pF
R450	22kΩ	C400	100nF		
R451	1MΩ	C451	1nF	D400	MMBD1503A
R500	100kΩ	C452	100nF	U400	e.g. LMV931MG
		C500	1nF	U500	e.g. SN74AHC1G04DRL

4.4 Serial Port Interfaces

Two serial ports are available on the device to interface to a CMX994A and provide an audio SPI-codec interface. On the 7241FI-1 these can be multiplexed together (with separate CSN signals) or entirely separate, whilst on the 7241/7341FI-2 they must be kept separate. Refer also to Table 10.

Table 3 shows the options available and includes the CMX7141 to show where backwards compatibility is feasible.

Table 3 Serial Port Assignments

configuration	pin name	7141	7241-FI1	7241-FI2 Limiter/discriminator	7341-FI2 I/Q demod
default	EPCSN	CMX994A	CMX994A	SPI-Codec	CMX994A
	EPSCLK				
	EPSI	SPI-Codec or CMX 618/7262	SPI-Codec or CMX 618/7262		SPI-Codec
	EPSO				
	SSOUT				
	GPIOA				
	GPIOB				
alternate	EPCSN		CMX994A		
	EPSCLK				SPI-Codec
	EPSI				
	EPSO		SPI-Codec or CMX 618/7262	SPI-Codec	
	SSOUT				
	GPIOA				
	GPIOB				

4.5 RESET Pin

This pin (pin 7) provides a dedicated reset function when connected to a suitable host microprocessor. To use reset the pin must be held high for a minimum of 100ns and then released. When the state of reset changes from 1 to 0, the same effect as a power-on reset is achieved.

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5 General Description

5.1 7241/7341FI-2 Features

The 7241/7341FI-2 Function Image™ is intended for use in half-duplex digital PMR terminal equipment using 4FSK modulation at 4.8 ksymbols/s (9.6 kbps) suitable for 12.5kHz RF channels. This document should be read in conjunction with the following ETSI standards:

- TR 102 398 DMR Designers Guide
- TS 102 361-1 DMR Air Interface Protocol

A flexible power control facility allows the device to be placed in its optimum powersave mode when not actively processing signals.

The device includes a clock generator, with buffered output, to provide a common system clock if required. At power-on, the SYSCLK1 pin will output the same signal presented at the XTAL input, and so can be used to drive the host controller if required.

A block diagram of the device is shown in

Figure 1. The signal processing blocks can be routed from any of the three DISC/ALT/MIC input pins.

5.2 Digital Features

Much of the DMR ETSI TS 102 361-1 standard air interface protocol is embedded in the 7241/7341FI-2 Function Image™ operation namely:

Air Interface Physical Layer 1

- 4FSK modulation and demodulation
- Bit and symbol definition
- Frequency and symbol synchronisation
- Sync detection (MS/BS/Direct/Voice/Data)
- Slot timing
- Transmission burst building and splitting
- Burst timing/scheduling

Air Interface Data Link Layer 2

- Channel coding and decoding (FEC, CRC)
- Interleaving, de-interleaving and bit ordering
- Frame and superframe building and synchronising
- Burst and parameter definition
- Interfacing of voice applications (voice data) with the Physical Layer
- Data bearer services
- Exchanging signalling and/or user data with the Call Control Layer

Tier 1 – Unlicensed peer-to-peer direct communication network (without repeaters or infrastructure), using a single frequency channel, unlicensed (limited RF power).
Tier 2 – Licensed operation (allowing higher RF powers) using either Direct mode (peer-to-peer) or Conventional repeater mode (note that this FI is designed for implementation in terminal devices only).
Tier 3 – Trunked operation, using multiple channels and/or repeaters.

5.3 Analogue Features

Voice processing for 12.5kHz channel operation including:

- 300Hz HPF
- Pre-emphasis / de-emphasis
- Tx limiter and Voice AGC
- Channel filter

Analogue signalling:

- CTCSS encode / decode
- Selcall encode / decode
- 1200 baud FFSK encode / decode (MPT1327, MDC1200 compatible)
- DTMF encode / decode

5.4 Auxiliary Functions

- Automatic Tx sequencer simplifies host control
- RAMDAC operation with level adjustment for PA control
- TXENA and RXENA hardware signals
- Two-point or I/Q modulation outputs[2]
- Hard or soft data output options
- Two programmable system clock outputs (SYSCLK1 active at power-on)
- Two auxiliary ADCs with four selectable external input paths
- Four auxiliary DACs, one with built-in programmable RAMDAC

5.5 Interface

- Optimised C-BUS (4-wire, high-speed synchronous serial command/data bus) interface to host for control and FIFOs for data transfer
- Open drain IRQ to host
- Auxiliary SPI/C-BUS for direct control of CMX994A I/Q Receiver (CMX7341 only)
- Auxiliary SPI-Codec interface for PCM speech codec to support third-party vocoders, e.g. AMBE+2
- Fast, streaming C-BUS (host) boot mode.

5.6 System Design

5.6.1 General

A number of system architectures can be supported by the device. The most significant architectural decisions are:

RF receiver:

- Limiter/Discriminator (CMX7241) or
- I/Q using the CMX994A Direct Conversion Receiver (CMX7341)

[2] If Tx I/Q mode is enabled, SPI-Codec functionality will be limited: no output on the AUDIO pin will be available during Tx.

Vocoder:

External/host based: all encoded data is transferred over the host C-BUS interface. The SPI/C-BUS interface may be used as an Audio Codec for PCM data (this is appropriate for use with the DVSI AMBE devices). In this mode the host must issue all control commands to the vocoder, and also transfer coded data packets between the vocoder and device. Unlike previous CMX7141 devices, in the CMX7341, the auxiliary SPI/C-BUS may NOT be shared with the CMX994, so, in Rx I/Q mode, an additional serial port becomes operational, re-using the GPIOA and GPIOB pins.

The configuration of the auxiliary SPI/C-BUS port is controlled by the Program Register P6.1. In SPI-Codec mode 16-bit PCM audio samples are transferred at 8 ksamples/s. When this mode is selected:

in Tx: the MIC input should be routed from MIC to Input 1. The input signal is lowpass filtered, converted to 16-bit linear PCM at 8 ksamples/s and then output on the EPSI/GPIOA pin of the SPI-Codec port for the external vocoder to process.
in Rx: the AUDIO output should be routed from Output 1. 16-bit linear PCM samples are read from the EPSO pin of the SPI-Codec port, then filtered and output via the Audio Output Attenuator. This mode can also be used for voice annunciations/warnings etc.

All payload data (including voice traffic channel data) is routed through the main C-BUS to the host. The host can then transfer it to/from the third party vocoder over a suitable port supported by the chosen vocoder. This architecture is shown in Figure 7. See also Section 6.4. Note that the vocoder functionality could also be implemented inside the host micro in this mode.

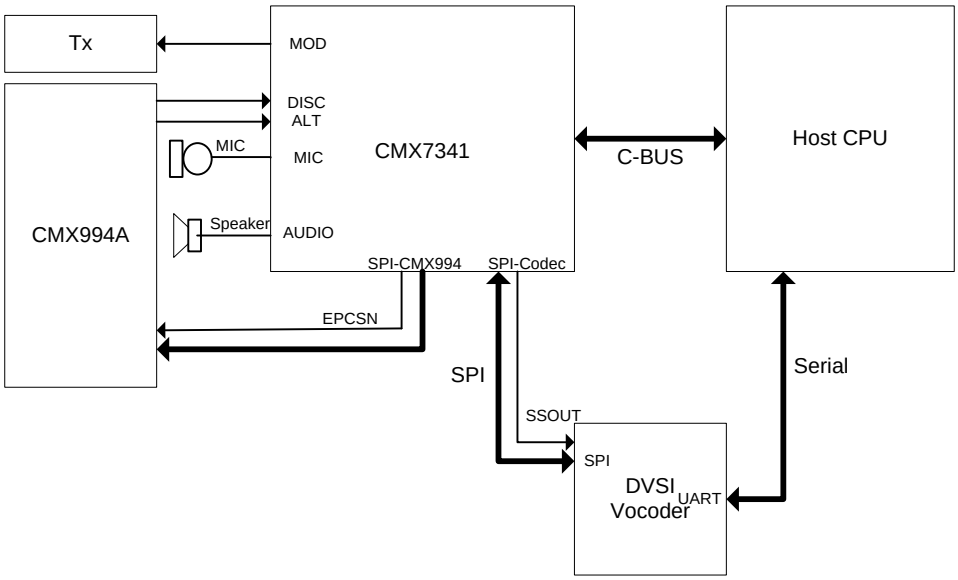


Figure 7 CMX994A and DVSI Vocoder Connection

5.6.2 Data Transfer

When transmitting, an initial block of payload or control channel data will need to be loaded from the host into the C-BUS TxData FIFO registers. The device can then format and transmit that data while at the same time loading in the following data blocks from the host or vocoder.

When receiving, the host needs to consider that when a signal is received over the air there will be a processing delay while the device filters, demodulates and decodes the output data before presenting it to the host or vocoder. For best performance, voice payload data is output in soft-decision (4-bit log-likelihood ratio) format compatible with third-party vocoders, although this mode increases the data transfer rate over C-BUS by a factor of four.

5.6.3 CMX994A Connection (I/Q Mode)

The CMX994A can be connected via the auxiliary C-BUS connection (Table 4). This allows the CMX994A to be used along with the DVSI vocoder or other third party vocoder.
Note that the data and clock connections to the CMX994A are not common with the SPI-Codec interface.

Table 4 CMX994A Connections

CMX7241/7341 Pin	CMX994A Pin
EPCSN	CSN
EPSI	CDATA
EPSCLK	SCLK

The operation of the CMX994A is generally automatic, however specific data may be written to CMX994A registers using the pass-through mode available using the Program Block write mechanism (Programming register $C8). For example if the CMX994A PLL and VCO are used in the radio design then it is necessary to program the appropriate frequency data to the CMX994A PLL-M Divider, PLL N-Divider and VCO Control registers using the pass-through mode before attempting reception.

The SYSCLK1 pin may be reconfigured using Program Block P6.0:b5 as an external LNA Enable/ gain control as part of the I/Q receiver AGC system where the CMX994's own internal LNA is bypassed. Note that at power-on, this pin will output the XTAL clock signal until the host has completed the re-configuration. This may be disabled to save power using $AB:b15.

5.6.4 Hardware AGC – AuxADC1 Connection

In I/Q mode the AuxADC1 input can be used to improve the adjacent/alternate channel rejection with the addition of suitable external components (shown in Figure 6). This function provides a broadband signal detector which is used in the AGC process. This is used to prevent the DISC/ALT ADC inputs limiting internally in the presence of strong alternate channel signals, which are attenuated by the inherent filtering of the ADC. This functionality is enabled by setting:

- Program Block P2.0:b8=1 (enable hardware AGC)
- $C0:b6 = 1 (enable BIAS)
- $93 = $xx3C (AuxADC1 Enabled, averaging = 3, Routed from AuxADC input 1)
- $95 = $0185 (hi threshold)
- $94 = $0180 (lo threshold)

Note that threshold levels may need adjustment to suit particular hardware implementations.

5.6.5 RSSI Measurement (I/Q Mode)

In I/Q mode the RSSI is calculated from the signal levels present at the I and Q inputs and the AGC levels currently in use. Figure 8 shows a typical response. The RSSI value is used to control the AGC of the I/Q system, automatically adjusting both the gain of the CMX994A and the Input 1 / Input 2 stages of the 7241/7341. The input signal level is averaged continuously over a half-slot duration and reported as a dB value (8-bit unsigned) in C-BUS register $9E:b7-0. A typical response taken from a DE9945 Evaluation board is shown in Figure 8.

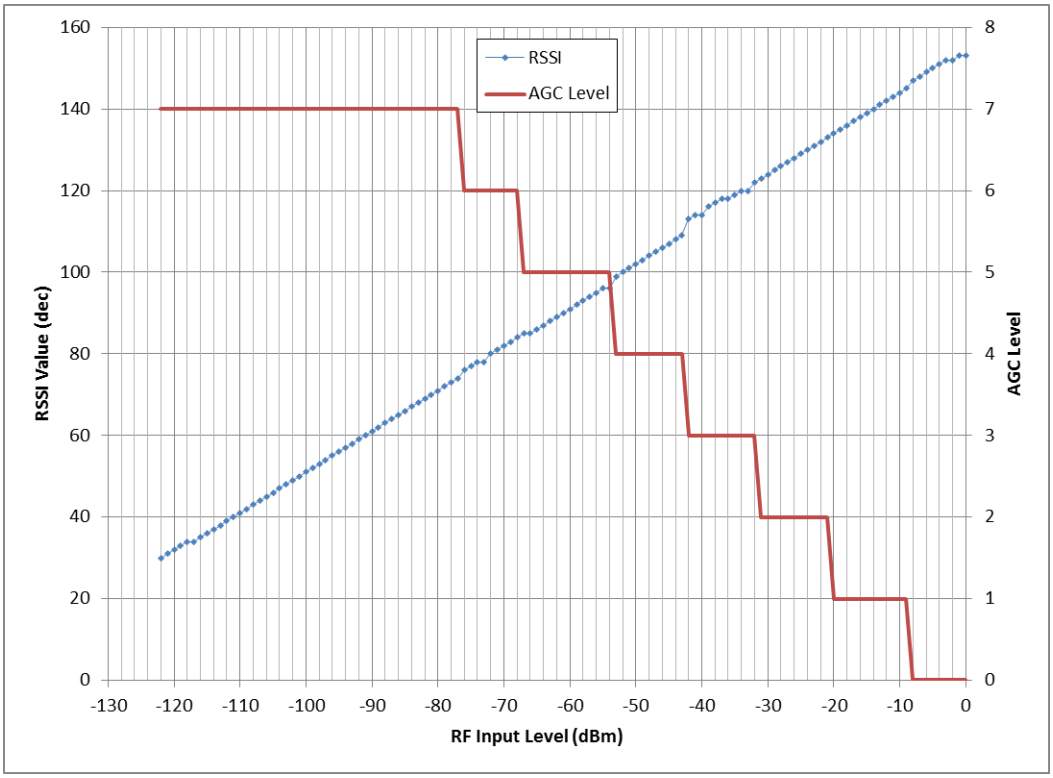


Figure 8 RSSI/AGC in I/Q Mode

5.6.6 RSSI Measurement (LD mode)

The AuxADC provided by the device can be used to detect the Squelch or RSSI signal from the RF section while the device is in Rx or Tx Off/Rx Off mode. This allows a significant degree of powersaving within the device and avoids the need to wake the host up unnecessarily. The host-programmable AuxADC thresholds allow for user selection of squelch threshold settings.

5.7 DMR Modem Description

This modem is designed to be compatible with the ETSI TS 102 361-1 DMR standard (www.etsi.org) for Tier 1, Tier 2 and Tier 3 terminals:

Symbol rate:	4.8 ksymbols/s (9.6 kbps)
Modulation:	4FSK
Channel spacing:	12.5kHz
Mode:	2-slot TDMA, 60 ms frame

It has been designed such that, when combined with suitable RF, host controller, vocoder and appropriate control software, it meets the requirements of the EN 300 113 standard.
This document should be read in conjunction with the ETSI standards; TS 102 361-1 (Air interface) and TR 102 398 (Designers Guide).

The ETSI standard does not specify a voice coding algorithm, but the DMR Association has standardised on the AMBE+2 vocoder from DVSI Inc. which is available in hardware form as the AMBE-3000 or as software modules for various microcontrollers.

Note that the TS 102 361-1 DMR standard is NOT compatible with the TS 102 658 or TS 102 490 (dPMR) 6.25kHz/4800 baud FDMA system.

5.7.1 Modulation

4FSK modulation details:

RRC alpha: 0.2

RRC filters are implemented in both Tx and Rx. The CMX7241/7341 can adapt to the maximum time-base clock drift of 2ppm over the duration of a 180-second burst.

Information bits		Symbol	4FSK deviation
Bit 1	Bit 0		
0	1	+3	+1.944kHz
0	0	+1	+0.648kHz
1	0	-1	-0.648kHz
1	1	-3	-1.944kHz

$$|F(f)| = 1 \quad \text{for} \quad |f| \le 1\,920\ Hz$$

$$|F(f)| = \left|\cos\left(\pi f / 1\,920\right)\right| \quad \text{for} \quad 1\,920\ Hz < |f| \le 2\,880\ Hz$$

$$|F(f)| = 0 \quad \text{for} \quad |f| > 2\,880\ Hz$$

where $|F(f)|$ = magnitude response of the Square Root Raised Cosine Filter.

NOTE: f = frequency in hertz.

Figure 9 DMR Modulation Characteristics

5.7.2 Format

The DMR signal format differs from most existing PMR systems in that it is a 2-slot TDMA system with the sync placed at the centre of the slot. Each frame is 60 ms long and holds two 30 ms slots. Voice superframes consist of 6 TDMA frames, labelled A to F, with the Voice Sync appearing in Frame A, and embedded signalling or reverse channel bursts (to provide late entry or transmit interrupt facilities) appearing in subsequent frames. This scheme allows for two different conversations to be in progress on the same radio channel, one occupying Slot 1, the other Slot 2. In peer-to-peer / direct mode, either one slot is used (12.5kHz mode) or both (TDMA 6.25kHz equivalent mode), however the latter scheme imposes additional constraints on frequency accuracy and timing. There is no requirement for a terminal to Tx in an adjacent Rx slot, except for the case of Reverse Channel signalling, where a special shortened burst is used to allow the hardware sufficient time to change modes.

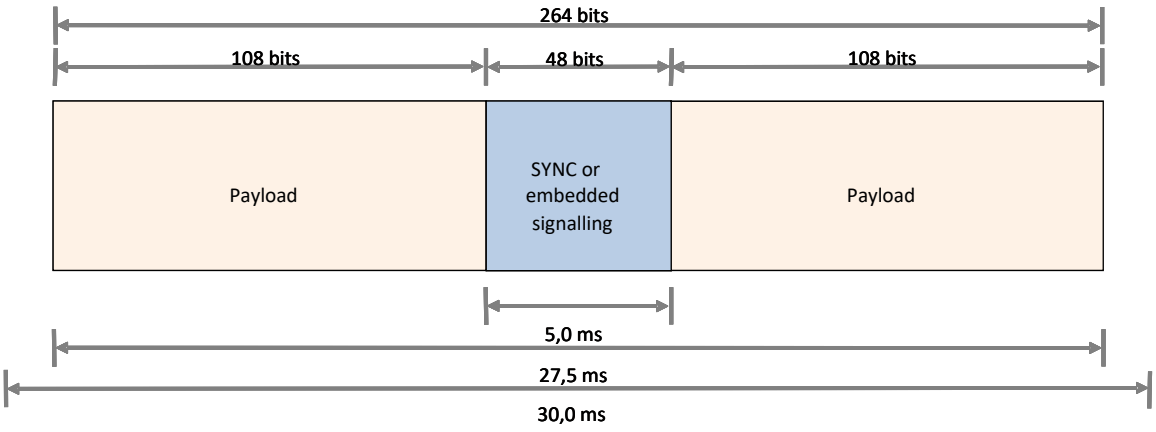


Figure 10 Generic Burst Structure

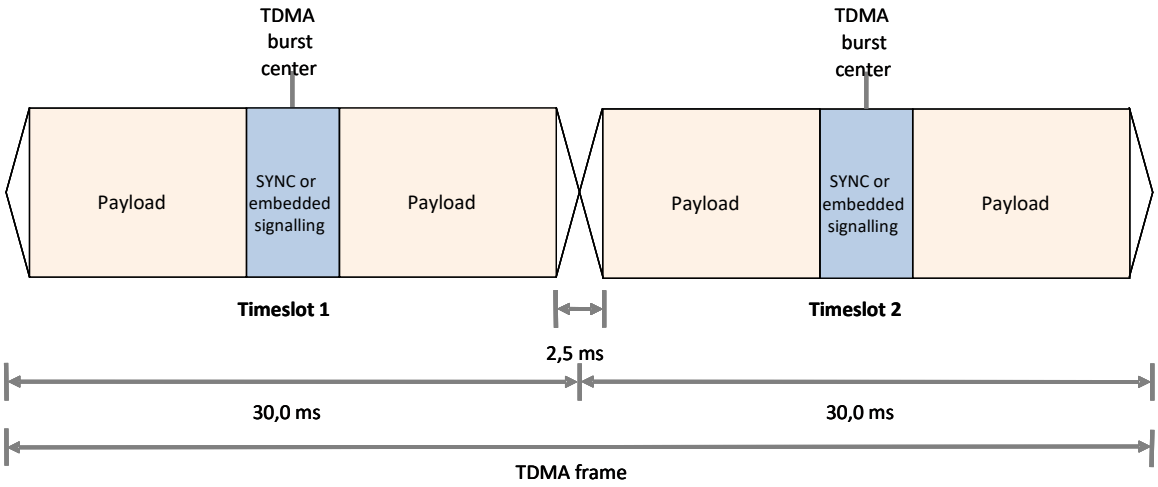


Figure 11 MS Sourced TDMA Frames

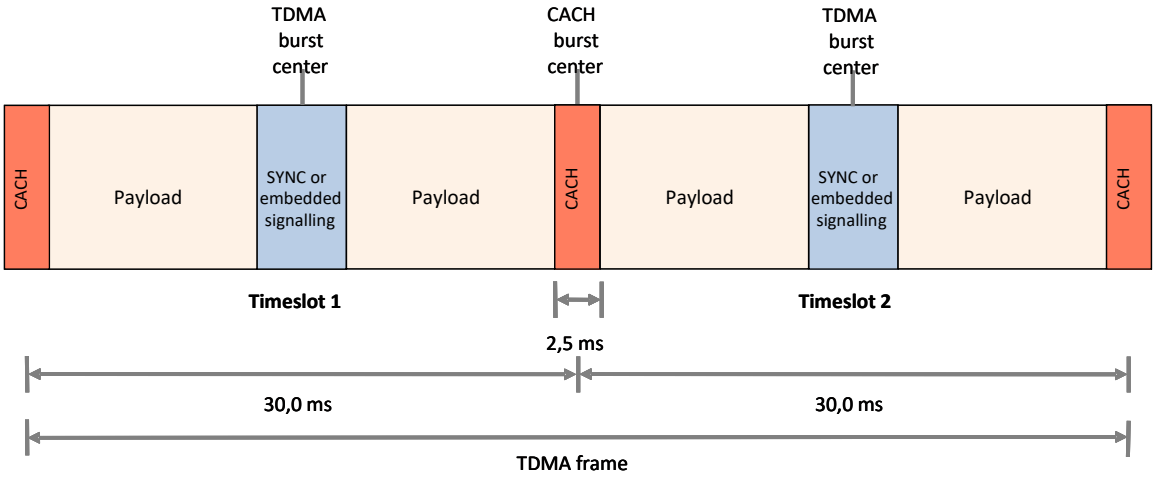


Figure 12 BS Sourced TDMA Frame

5.7.3 Internal Data Processing

The device operates as a half-duplex device, either receiving signals from the RF circuits in Rx mode, or sourcing signals to the RF circuits in Tx mode. It also has a Tx Off/Rx Off (powersave) mode to support battery saving protocols. Due to the TDMA nature of the protocol and the inherent processing delays associated with it, the internal data processing is designed to be essentially duplex in operation with Tx and Rx processes running concurrently. However the RF hardware itself can only operate in a half-duplex mode.

The internal data processing blocks for Tx and Rx modes are illustrated in Figure 13. In addition, when connected to the CMX994A Direct Conversion receiver, the FI will automatically control the dc removal, frequency compensation and AGC algorithms.

Considering Figure 13 it can be observed that the signal level measurement takes place before and after the I/Q filtering. This information is used to control input gain stages in the CMX7231/7341 as well as the gain of the CMX994A/CMX994E via the C-BUS interface. The standard AGC algorithm controls AGC correctly in the majority of usage cases but is not necessarily optimum is some scenarios such as TDMA direct mode initial acquisition. The advanced AGC algorithm ensures AGC is set during acquisition of a TDMA direct mode signal and also optimises adjacent / alternate channel performance including using the hardware AGC signal (section 5.6.4).

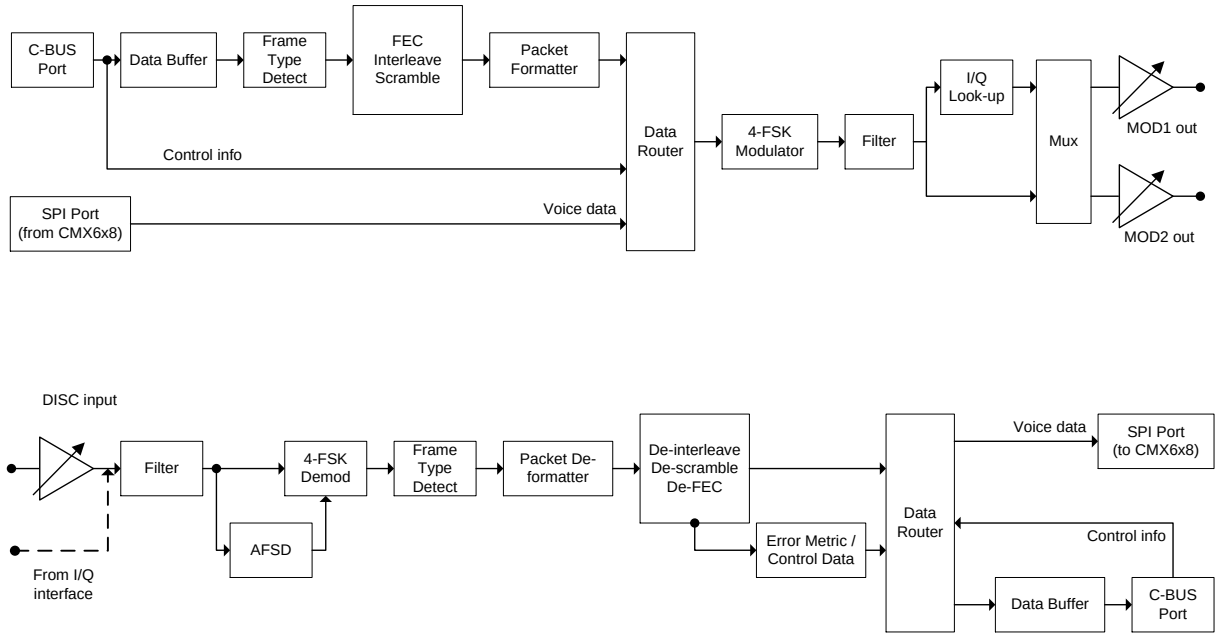


Figure 13 Internal DMR Data Processing Blocks

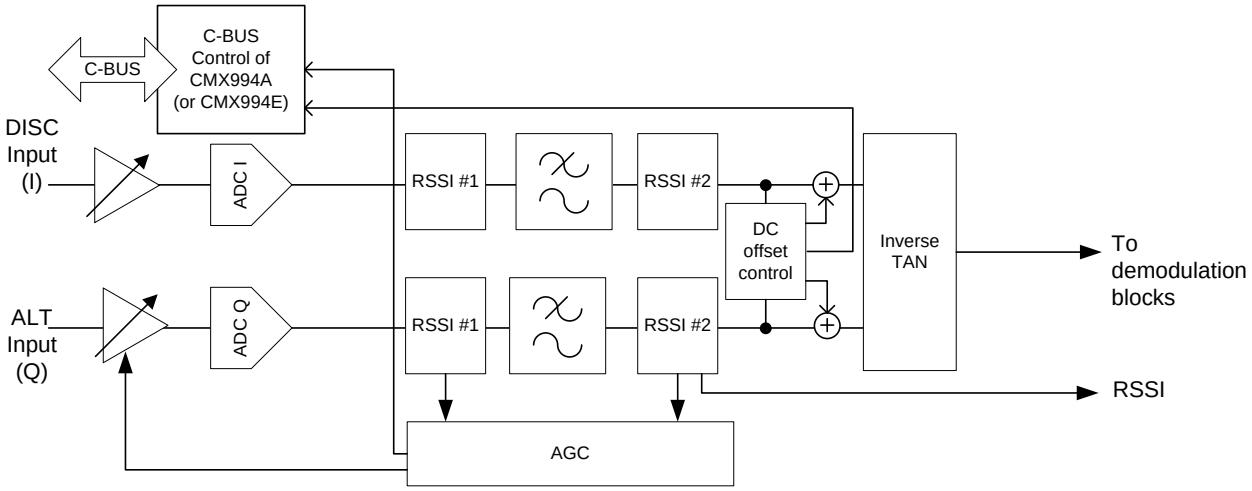


Figure 14 Additional Internal Data Processing in I/Q Mode

5.7.4 Automated Frame Sync Detector and Demodulation

The analogue signal from the receiver may be from either a CMX994A I/Q interface (CMX7341) or a limiter/discriminator (LD) output (CMX7241). The signal(s) from the RF section should be applied to the CMX7241/7341 input(s) (normally the DISC input for LD Rx and DISC and ALT inputs for I/Q Rx).

In LD mode, the signals can be adjusted to the correct level either by selection of the feedback resistor(s) or using the CMX7241/7341 Input Gain settings.

In I/Q mode, filtering is applied to the input signals and dc offsets are removed before an inverse tan function performs the FM demodulation function. The output of this stage has an offset depending on the frequency error of the received signal compared to the nominal frequency of the receiver. This offset is removed before RRC filtering and Inverse Rx Sinc filter matching the filters applied in the transmitter.

From this point onwards, the processing is essentially the same for LD and I/Q mode. The signal is passed to the AFSD (Automated Frame Sync Detector) block which extracts symbol and Frame synchronisation derived from the sync field in the centre of each burst. Any combination of the ten defined sync patterns can be scanned and detected in parallel. On detection of a valid Frame Sync the AFSD process establishes the slot boundary and timing, and updates the internal system slot clock which will be used for subsequent Tx bursts to ensure that the radio remains synchronised to other stations in the overall radio system.

During search, the 4FSK demodulator and the data-processing sections that follow are dormant to minimise power consumption. Once frame synchronisation has been achieved the AFSD section is powered down, and the timing and symbol-level information is passed to the 4FSK demodulator which is now enabled. The input signal is saved in an internal buffer which allows the demodulator to start decoding data from the beginning of the slot in which the Frame Sync was detected, followed by data from all subsequent slots. Symbol timing information is carried forward and subsequent Frame Syncs are used to track and adjust for small timing variations.

To be detected as a valid FS pattern, AFSD allows for a tolerance of up to two bit errors in the detection process (see P1.0:b1-0). Subsequent FS or EMB fields are detected by the layer 2 process, which will continue to be reported to the host along with the associated data (even if there is no longer any valid data - during a fade or if the terminator has been lost, for instance). Alternatively, the confidence level field in P1.1 may be programmed to automatically reject any bursts that may be considered to be invalid and so inhibit the data being reported to the host. The default state of P1.1 is set to allow all bursts, so as to enable BER testing etc. in poor signal conditions, but is made available so that the host can adjust it to suit its own requirements..

To allow flexibility (especially in TDMA Direct Mode), two control bits are provided to force the modem to reset AFSD and re-acquire sync for every Rx slot / superframe.

A slot edge signal is output on the SYSCLK2 pin whenever the device is in an active Rx or Tx mode. This corresponds to the internal timing that the device will use for its next Tx operation, and it can be used by the host to synchronise its process to the incoming data stream (e.g. PLL programming) in conjunction with reading the value of the C-BUS Internal Slot Counter register $CC.

In I/Q mode the CMX7241/7341 also provides measurements of frequency error and RSSI (which are not available in LD mode). This data is also used to drive the CMX994A AGC process.

Table 5 SYNC Patterns

Frame Sync	Index	BS sourced													
FS1	0001	Voice	Hex	7	5	5	F	D	7	D	F	7	5	F	7
FS2	0010	Data	Hex	D	F	F	5	7	D	7	5	D	F	5	D
		MS sourced													
FS3	0011	Voice	Hex	7	F	7	D	5	D	D	5	7	D	F	D
FS4	0100	Data	Hex	D	5	D	7	F	7	7	F	D	7	5	7
FS5	0101	Reverse	Hex	7	7	D	5	5	F	7	D	F	D	7	7
		TDMA direct mode time Slot 1													
FS6	0110	Voice	Hex	5	D	5	7	7	F	7	7	5	7	F	F
FS7	0111	Data	Hex	F	7	F	D	D	5	D	D	F	D	5	5
		TDMA direct mode time Slot 2													
FS8	1000	Voice	Hex	7	D	F	F	D	5	F	5	5	D	5	F
FS9	1001	Data	Hex	D	7	5	5	7	F	5	F	F	7	F	5

		Reserved SYNC pattern													
FS10	1010		Hex	D	D	7	F	F	5	D	7	5	7	D	D

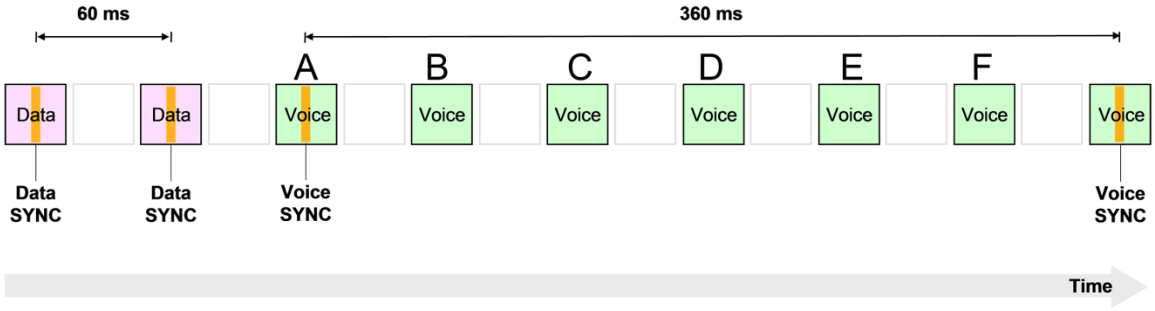


Figure 15 DMR MS Voice Frame Format

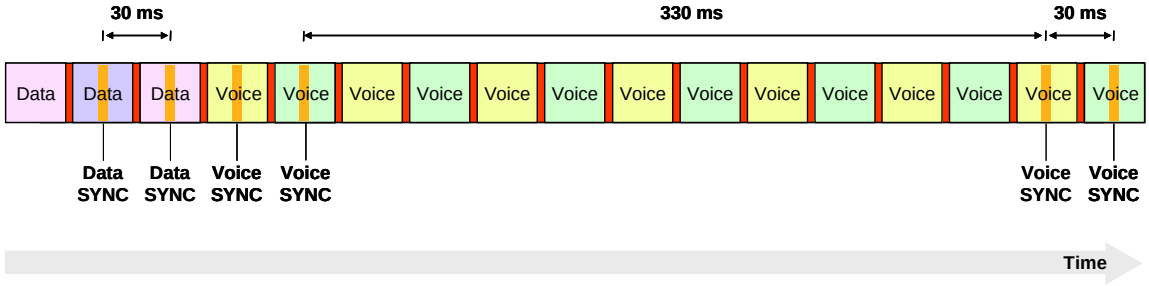


Figure 16 DMR BS Downlink Frame Format

Note that, as the Frame Sync is positioned in the middle of the burst, when the receiver is first enabled, Frame Sync detection is delayed to ensure that the first payload section is not missed.

The Voice and Data Sync patterns are the inverse of one another; care should be taken in the hardware design so that the signal polarity is maintained throughout the signal path to avoid potential “false” detections. If required, the Tx and Rx signal polarities can be inverted using Analogue Output Gain - $B0 write, bits 11 and 7 to compensate for different hardware configurations.

5.7.5 FEC and Coding

The CMX7241/7341 implements all checksums, CRCs, Coding schemes, interleaving etc. required by the standard as shown in Table 6. Any checksum or CRC failures are indicated when transferring the decoded fields to the host. This relieves the host of a substantial processing load and has the added advantage of reducing the complexity and timing constraints of interfacing between the host, vocoder and CMX7241/7341. The FEC/CRC information can be used by the host to decide if the current signal is still suitable, or whether a new channel with a better signal should be scanned for.

Table 6 FEC and CRC Schemes

Field	FEC code	Checksum
EMB field	Quadratic Residue (16,7,6)	none
Slot Type	Golay (20,8)	none
CACH TACT bits	Hamming (7,4)	none
Embedded signalling	Variable length BPTC	5-bit CheckSum (CS)
Reverse Channel (RC) Signalling	Variable length BPTC	defined as part of RC message
Short LC in CACH	Variable length BPTC	8-bit CRC
PI Header	BPTC(196,96)	CRC-CCITT
Voice LC header	BPTC(196,96)	(12,9) Reed-Solomon
Terminator with LC	BPTC(196,96)	(12,9) Reed-Solomon
CSBK	BPTC(196,96)	CRC-CCITT
Idle message	BPTC(196,96)	none
Data header	BPTC(196,96)	CRC-CCITT
Rate ½ data continuation	BPTC(196,96)	Unconfirmed: none
		Confirmed: CRC-9
Rate ½ last data block	BPTC(196,96)	Unconfirmed: 32-bit CRC
		Confirmed: 32-bit CRC and CRC-9
Rate ¾ data continuation	Rate ¾ Trellis	Unconfirmed: none
		Confirmed: CRC-9
Rate ¾ last data block	Rate ¾ Trellis	Unconfirmed: 32-bit CRC
		Confirmed: 32-bit CRC and CRC-9
Rate 1 non-last data block	Rate 1 coded	Unconfirmed: none
		Confirmed: CRC-9
Rate 1 last data block	Rate 1 coded	Unconfirmed: 32-bit CRC
		Confirmed: 32-bit CRC and CRC-9
Response header block	BPTC(196,96)	CRC-CCITT
Response data block	BPTC(196,96)	32-bit CRC
MBC header	BPTC(196,96)	CRC-CCITT
MBC continuation	BPTC(196,96)	none
MBC last block	BPTC(196,96)	CRC-CCITT
UDT header	BPTC(196,96)	CRC-CCITT
UDT continuation	BPTC(196,96)	none
UDT last block	BPTC(196,96)	CRC-CCITT

5.7.6 Timing

The device maintains its own internal clock which determines the slot and frame boundaries which is active when an Rx or Tx mode is selected and output on the SYSCLK2 pin. This is updated by the AFSD process in order to maintain accurate synchronisation over time and temperature variations. This internal clock is used to schedule transmissions so that they maintain accurate timing for the duration of the call.

A Tx sequencer is used to time the hardware actions (TxENA, RAMDAC, Modulation start/end etc.) to relieve the host of the need to maintain its own accurate timer section. The basic hardware operations are defined to a resolution of 1/6 symbol to ensure compliance with TS 102 361-1.

6 Detailed Descriptions

6.1 Xtal Frequency

The CMX7241/7341 is designed to work with an external frequency source of 19.2MHz. Other frequencies maybe possible, contact CML Customer Support for details. This signal should be provided by a VCTCXO device connected to the XTAL/CLK pin. This may be shared with the CMX994A clock signal to minimise the number of clock sources in the equipment design to reduce cost and limit potential interference issues, however note that the CMX7241/7341 requires a CMOS logic level signal, whereas the CMX994A only needs a 0.5 Vpp signal.

6.2 Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX7241/7341 and the host microcontroller; this interface is compatible with microwire and SPI. Interrupt signals notify the host microcontroller when a change in status has occurred and the µC should read the status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set. See section 8.1.59

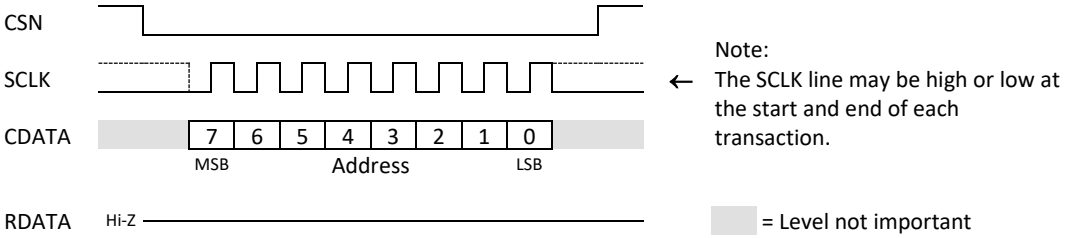
6.2.1 C-BUS Operation

This block provides for the transfer of data and control or status information between the CMX7241/7341's internal registers and the host µC over the C-BUS serial interface. Each transaction consists of a single address byte sent from the µC which may be followed by one or more data byte(s) sent from the µC to be written into one of the CMX7241/7341's Write Only Registers, or one or more data byte(s) read out from one of the CMX7241/7341's Read Only Registers, as shown in Figure 17.

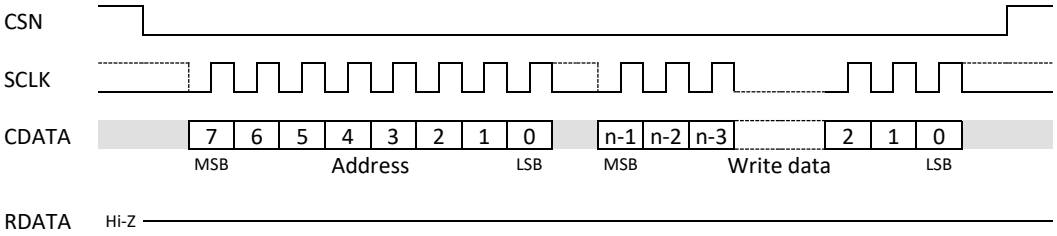
Data sent from the µC on the CDATA (Command Data) line is clocked into the CMX7241/7341 on the rising edge of the SCLK (Serial Clock) input. RDATA (Reply Data) sent from the CMX7241/7341 to the µC is valid when the SCLK is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine.

The number of data bytes following an address byte is dependent on the value of the Address byte. The most significant bit of the address or data is sent first. For detailed timings see section 7.2. Note that, due to internal timing constraints, there may be a delay of up to 208 µs between the end of a C-BUS write operation and the device reading the data from its internal register.

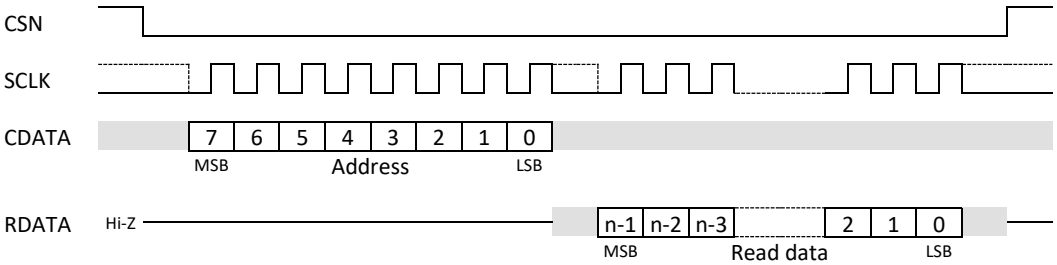
C-BUS single byte command (no data)



C-BUS n-bit register write



C-BUS n-bit register read



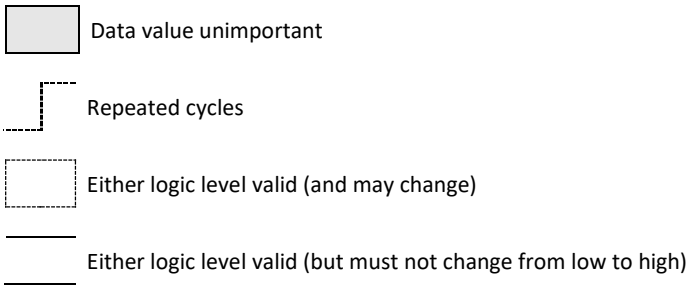


Figure 17 C-BUS Transactions

Notes:

1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset).
2. For single byte data transfers only the first 8 bits of the data are transferred.
3. The CDATA and RDATA lines are never active at the same time. The Address byte determines the data direction for each C-BUS transfer.
4. The SCLK input can be high or low at the start and end of each C-BUS transaction.
5. The gaps shown between each byte on the CDATA and RDATA lines in the above diagram are optional, the host may insert gaps or concatenate the data as required.
6. For the CMX7241/7341, n is either 8 or 16 bits depending on the register being addressed.

6.2.2 C-BUS FIFO operation

The 7241/7341 implements Rx and Tx FIFOs to buffer the incoming and outgoing data. To maximise data bandwidth across the C-BUS interface, the FIFO registers are also capable of data-streaming operation. This allows a single address byte to be followed by the transfer of multiple read or write data words, all within the same C-BUS transaction. This can significantly increase the transfer rate of large data blocks, as shown in Figure 18.

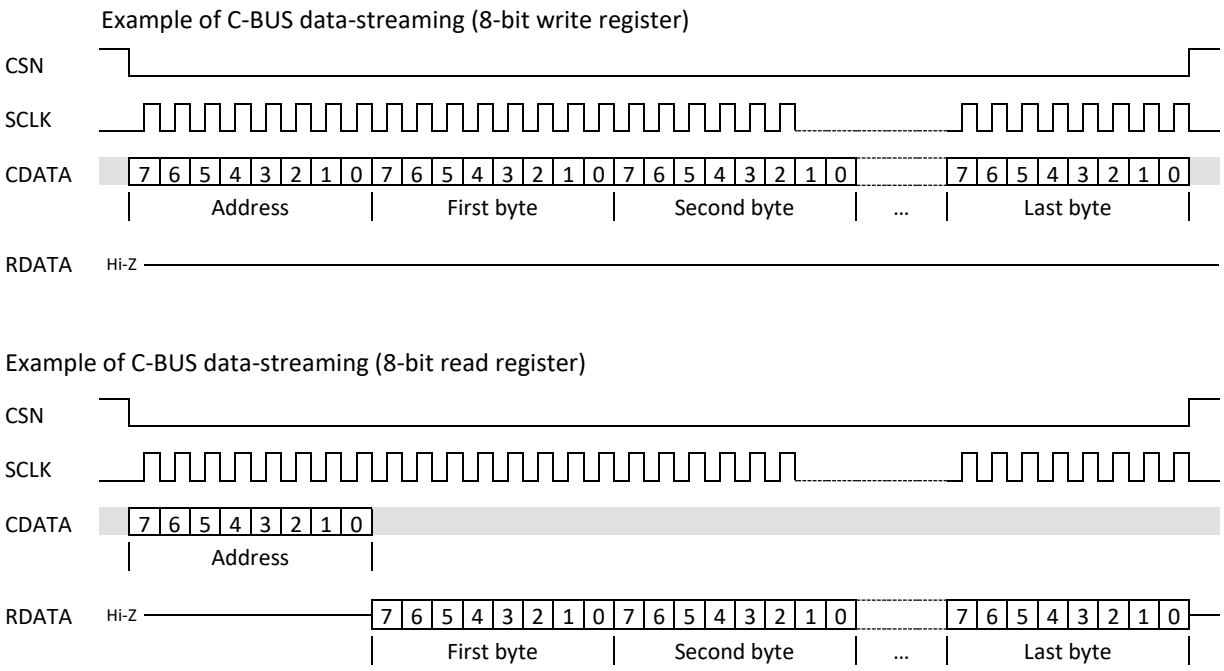


Figure 18 C-BUS Data-Streaming Operation

The Tx and Rx FIFOs are implemented as two separate 256 x 16-bit arrays. Each row of the arrays can be accessed as a 16-bit word ($79 and $7D) or an 8-bit byte ($78 and $7C - which accesses the lower byte of each row). The number of rows of each array currently in use can be read using the $7B and $7F registers.

Table 7 C-BUS FIFO Registers

C-BUS Address	Function		C-BUS Address	Function
$78 (write)	Tx FIFO data byte		$7C	Rx FIFO data byte
$79 (write)	Tx FIFO data word		$7D	Rx FIFO data word
$7B (read)	Tx FIFO level		$7F	Rx FIFO Level

The Tx FIFO can be flushed by putting the Tx modem into Tx Off (powersave) ($C1=$xx0x).

6.2.3 C-BUS IRQ Operation

The device will issue an interrupt on the IRQN line when the IRQ bit (bit 15) of the IRQ Status register ($C6) and the IRQ enable bit (bit 15) of the C-BUS Interrupt Mask ($CE) register are both set to '1'. The IRQ bit is set when the state of any interrupt flag bits in the C-BUS Status register change from a '0' to '1' and the corresponding enable bit(s) in the C-BUS Interrupt Mask register is (are) set. Enabling an interrupt by setting a C-BUS Interrupt Mask bit (0→1) after the corresponding C-BUS Status register bit has already been set to 1 will also cause the IRQ bit to be set.

The Interrupt Request flag (bit 15) in the C-BUS Status register is cleared to 0 following the address phase of a C-BUS read of the C-BUS Status register, thus releasing the interrupt request.

6.3 Function Image™ Loading

The Function Image™ (FI), which defines the operational capabilities of the device, may be obtained from the CML Technical Portal, following registration. This is in the form of a 'C' header file which can be included into the host controller software. The maximum possible size of Function ImageTM is 96 kbytes, although a typical FI will be less than this. Note that the BOOTEN pins are only read at power-on or following a C-BUS General Reset or reset via the RESET pin and must remain stable throughout the FI loading process. Once the FI load has completed, the BOOTEN pins are ignored by the CMX7241/7341 until the next power-up or C-BUS General Reset.

The BOOTEN pins are both fitted with internal low current pull-down devices. For C-BUS load operation, both pins should be pulled high by connecting them to DVDD either directly or via a 220 kΩ resistor (see Figure 19). Once the FI has been loaded, the CMX7241/7341 will report the following information:

- $C5 = Product Ident Code ($7241 or $7341)
- $C9 = FI version code ($2xxx)
- $A9, $AA = Block 2 Checksum
- $B8, $B9 = Block 1 Checksum

The host should verify the checksum values with those published with the Function Image file downloaded from the CML Technical Portal.

The device waits for the host to load the 32-bit Device Activation Code through C-BUS register $C8.
Once activated, the device initialises fully, enters Tx Off/Rx Off mode and becomes ready for use, and the Programming flag (bit 0 of the Status register) will be set.

Once the FI has been activated, the checksum, product identification and version code registers are cleared and these values are no longer available. If an invalid activation code is loaded, the device will report the value $DEAD in register $A9 and must be power-cycled before an attempt is made to re-load the FI and re-activate.

Both the Device Activation Code and the checksum values are available from the CML Technical Portal.

Table 8 BOOTEN Pin States

	BOOTEN2	BOOTEN1	Notes
C-BUS Host load	1	1	FIFO mode (or single word mode)
Multi-Serial Memory load	1	0	Flexible address mode
Serial Memory load	0	1	Compatible with CMX7141
No FI load	0	0	

Note: Following a reset, the contents of the device should be verified using the CRC check facility, and re-loaded if required.

6.3.1 FI Loading from Host Controller

The Function Image™ can be included with the host controller software for download into the CMX7241/7341 at power-up over the C-BUS interface. This is done by writing the FI data into the Tx FIFO Data register, which supports streaming operation. The BOOTEN1/2 pins must first be set to the C-BUS load configuration and the device then powered up or Reset before the FI data is sent over C-BUS.

When using the recommended 19.2MHz clock source for XTALIN, the device can accommodate the host continuously streaming data to the Tx FIFO at the maximum SCLK rate of 10MHz; therefore it is not necessary to monitor the FIFO level registers during this operation. FI download time is limited only by the clock frequency of the C-BUS. With a 10MHz SCLK it should take less than 250ms to complete, even when loading the largest possible Function Image™.

The CMX7241/7341 memory can be protected against brownout or other forms of corruption. This protection is applied automatically in the 7241/7341 FIs, however when using legacy 7141/7131 FIs, this should be applied during the process of FI loading. To apply protection, the host must write the value $007F to C-BUS register $A0 after the last data block is loaded and before sending the activation block which ends the loading of the FI.

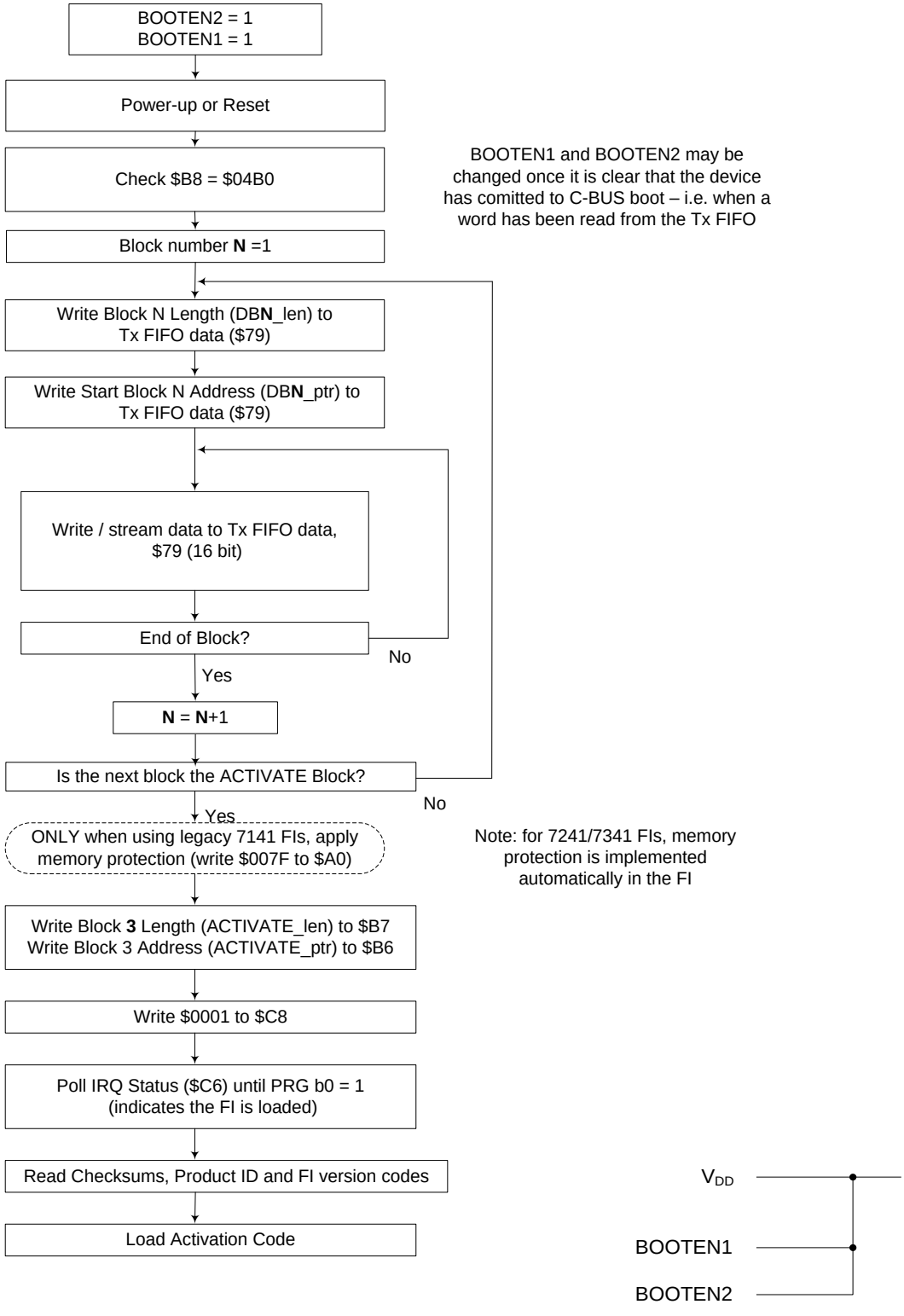


Figure 19 FI Loading from Host

If the main clock frequency (at the XTALIN pin) is slower than the C-BUS clock then the host will need to manually increase the internal MainCLK speed (contact CML Customer Support for details). The device does not take any action until BOTH length and address have been written to the FIFO, so writing the length and then polling for 'FIFO level = 0' will NOT work.

Support for the legacy mode, as used in the CMX7141 and CMX7041 series, is provided but not recommended. Contact CML Customer Support for details.

Block 3 (Activate) may also be loaded using the Tx FIFO mechanism. However, in this case, the PRG flag will not be set when the operation has completed, so the host must implement a fixed delay or poll the $C5 register until the Device Ident Code appears, before the checksum values can be read.

6.4 External Vocoder Support

6.4.1 DVSI Vocoder Interface

If the DVSI vocoder (or other third-party vocoder) is used all radio channel data will need to be transferred over the main C-BUS through the host.

The connections for the AMBE3000 vocoder from DVSI to enable it to use the CMX7241/7341 as the PCM audio codec in SPI mode are shown in Table 9 and Table 10.

Table 9 DVSI Vocoder Connections – I/Q mode

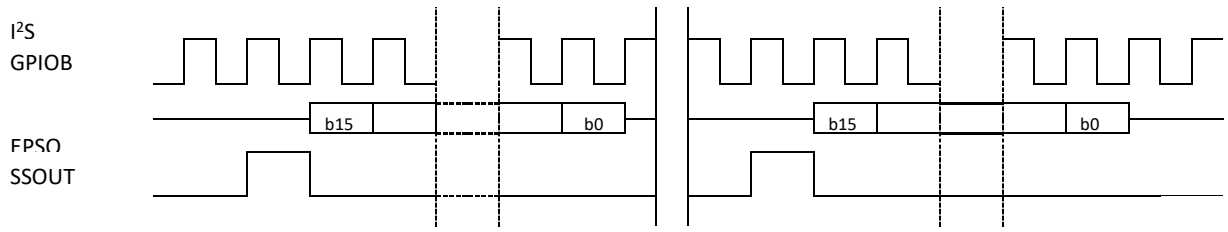
CMX7241/7341 Pin	AMBE3000 pin
SSOUT	SPI_STE
GPIOA	SPI_RX_DATA
EPSO	SPI_TX_DATA
GPIOB	SPI_CLK and SPI_CLK_IN.

Table 10 DVSI Vocoder Connections – LD mode

CMX7241/7341 Pin	AMBE3000 pin
SSOUT	SPI_STE
EPSI	SPI_RX_DATA
EPSO	SPI_TX_DATA
EPSCLK	SPI_CLK and SPI_CLK_IN.

6.4.2 Support for I²S Mode

The device can support I2S interfaces in mono, 16-bit mode only, for transmitting and receiving audio codec data using the SPI bus. This mode is selected in the Programming register (see Section 8.3.7). The diagram below shows typical transmit waveforms.



6.5 Device Control

The CMX7241/7341 can be set into the relevant mode to suit its environment. These modes are described in the following sections and are programmed over the C-BUS: either directly to operational registers or, for parameters that are not likely to change during operation, via the Programming register ($C8).
For basic operation:

(1) Enable the relevant hardware sections via the Power Down Control register

(2) Set the appropriate mode registers to the desired state

(3) Select the required signal routing and gain

(4) Use the Modem Control register to issue the required Rx or Tx commands

(5) Either:

a. Send Data packets to the device

b. Wait for the appropriate Rx IRQ and read Data packets from the device.

To conserve power when the device is not actively processing a signal, place the device into Tx Off/Rx Off mode. Additional powersaving can be achieved by disabling any unused hardware blocks, however, care must be taken not to disturb any sections that are automatically controlled. Note that the BIAS block must be enabled to allow any of the Input or output blocks to function.
See:

- Modem Control - $C1 write

6.5.1 General Notes

In normal operation, the most significant registers, in addition to the TxData and RxData FIFOs, are:

- Modem Control - $C1 write
- IRQ Status - $C6 read (note: reading this register will automatically clear any pending IRQs)
- Analogue Output Gain - $B0 write
- Input Gain and Signal Routing - $B1 write

Issuing an Rx or Tx command will automatically increase the internal clock speed to its operational speed, whilst issuing the Tx Off/Rx Off command will place the device in its powersaving configuration. To access the Program Blocks (through the Programming register, $C8) the device MUST be in Tx Off/Rx Off mode. In I/Q Rx mode, the Input 1 and Input 2 gain stages are automatically controlled by the internal AGC system and so cannot be changed by the host.

6.5.2 Signal Routing

The CMX7241/7341 offers a flexible routing architecture, with three signal inputs, a choice of two modulator configurations (to suit two-point modulation or I/Q schemes) and a single audio output.
See Figure 27 and:

- Input Gain and Signal Routing - $B1 write
- Analogue Output Gain - $B0 write
- Modem Control - $C1 write

For use with the CMX994A Rx and two-point modulation Tx, the following routing is recommended:

Rx:

I Channel -> DISC -> Input 1	Output 1 -> AUDIO
Q Channel -> ALT -> Input 2	Output 2 -> MOD2 or V_{BIAS}
	VBIAS -> MOD1

Tx:

Mic	-> MIC -> Input 1	Output 1 -> AUDIO
V_{BIAS}	-> Input 2 (not used)	Output 2 -> MOD1
		Output 2 -> MOD2

This configuration allows the AUDIO output to be available in both Rx and Tx modes for both voice call and annunciations/warnings etc. This feature is not available if Tx I/Q mode is selected as Output 1 is then used to provide the I modulation signal to MOD1, and Output 2 provides the Q signal to MOD2.

For Rx LD mode, the following is recommended:

Rx:

V_{BIAS} -> Input 1	Output 1 -> AUDIO
LD signal -> DISC -> Input 2	Output 2 -> MOD2
	V_{BIAS} -> MOD1

Notes:

1. In Tx two-point mode, Output 2 is used to feed both MOD1 and MOD2 pins, so it is not possible to selectively invert MOD1 whilst leaving MOD2 un-inverted. See Analogue Output Gain - $B0 write
2. In Rx mode, MOD2 may be routed to V_{BIAS}.
3. In Rx LD mode, the LD signal must be routed to Input 2.

The analogue gain/attenuation of each input and output can be set individually, with additional Fine Attenuation control available via the C-BUS registers in the CMX7241/7341.
See:

- Input Gain and Signal Routing - $B1 write
- Analogue Output Gain - $B0 write and MOD1 and MOD2 Fine Level Control - $80 write (byte)

6.5.3 Internal Timing

When the CMX7241/7341 is switched into an active Tx / Rx mode an internal slot timer is started. Initially this will be on an arbitrary time base but it will become aligned to the external over-air timing when a Frame sync is received. In BS mode all received Frame Syncs come from the same source, so the CMX7241/7341 will automatically align the slot timer to the first received Frame Sync, but in Direct mode the host can elect to use whichever FS is deemed to have come from the timing master. A slot clock signal is output on the SYSCLK2 pin which provides an alternating rising/falling edge on each slot boundary, along with a modulo-255 slot counter which is reported in the Internal Slot Counter register, $CC. The appropriate slot number is also reported back with each block of received data from the modem. The host can use the slot counter value as a basis to determine and specify which slots it will subsequently wish to transmit into.
In TDMA Direct Mode, the receive timings of signals on each slot may be significantly different, due to propagation delays and variations in reference oscillators, so the host must determine which is to be used by the modem as the reference and instruct the modem appropriately using the Tx Timing Control - $CA write register.

Some examples of timing scenarios are shown below:

- $C2=$4080 (Auto Re-acquire on, TDMA Slot 2 on)
- $C2=$40A0 (Auto Re-acquire on, TDMA Slot 2, TDMA Slot 1 on)
- $C2=$00A0 (Auto Re-acquire off, TDMA Slot 2, TDMA Slot 1 on)

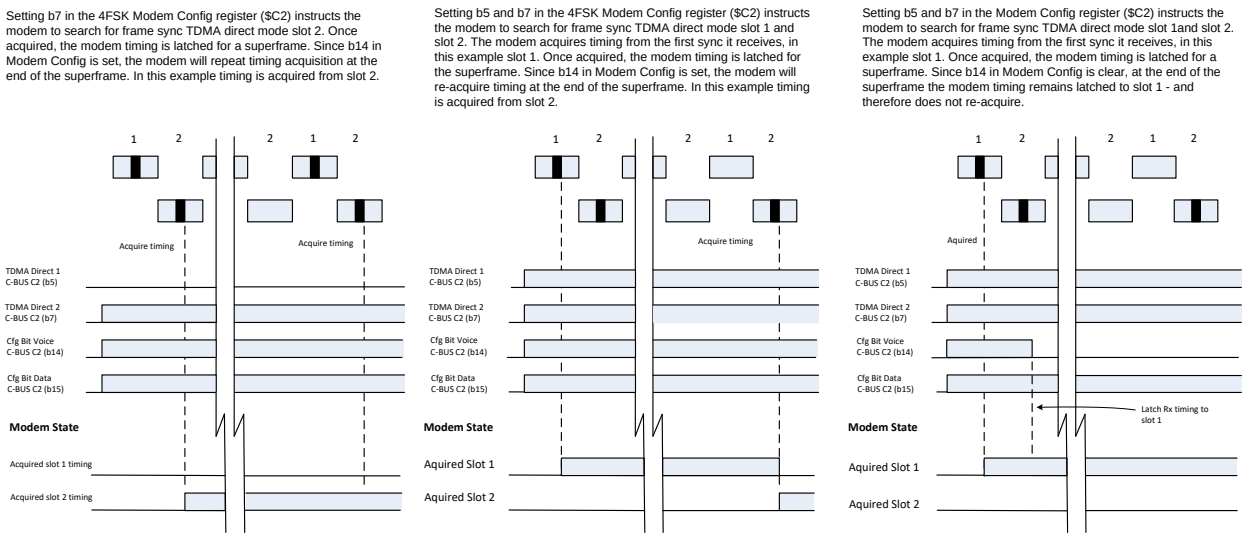


Figure 20 Timing Scenarios

6.5.4 Modem Control

Modem operation is primarily controlled by writing to the Modem Control register, $C1. Although the CMX7241/7341 is a half-duplex device, the timing constraints of receiving and transmitting in a slotted

system may require both Rx and Tx operating modes to be enabled concurrently by the host, allowing the CMX7241/7341 to synchronise hardware control and schedule data processing based on the current internal slot timer reference. During active Transmit slots the Tx sequencer will automatically override the RxENA state to ensure that the RF hardware always operates in half-duplex mode.

At power-on or following a Reset, the device will automatically enter Tx Off/Rx Off (powersave) mode, which allows maximum power saving whilst still retaining the capability of monitoring the AuxADC inputs (if enabled). It is only possible to write to the Programming register whilst in Tx Off/Rx Off mode. When the device is in Tx Off/Rx Off mode, a write to the Modem Control register setting the device into an active Tx and/or Rx mode will be executed immediately. Subsequent commands are executed on slot boundaries.

Receive modes automatically enable Rx hardware and begin scanning the incoming channel for a valid Frame Sync sequence. Once an FS has been acquired the receiver will begin demodulating slot data and processing it as required before passing it to the host through the Rx FIFO. Each Rx data block carries the slot number in which the data was received.

Frame Sync search can be re-started at any time by re-writing the receive mode command. When receiving from mobile sources in 12.5kHz Direct Mode this will be necessary after the end of each incoming call as there is no defined timing relationship from one transmitting mobile source to another.
Transmit modes will not activate the internal data modulator or external hardware until a data block is supplied by the host for transmission. Each Tx data block also carries a slot number and the CMX7241/7341 will wait before sending the data in the specified slot. During active Tx slots the receiver hardware and internal Rx processing are automatically suppressed and then re-enabled in the next slot. Note that Tx data blocks must be loaded 10ms before the target slot in order for the required burst formatting and FEC to complete.

See:

- Modem Control - $C1 write.

Table 11 TxENA and RxENA Signals

Device Mode	R20, R21 connected to DVdd		R20, R21 connected to DVss	
	TXENA	RXENA	TXENA	RXENA
Tx off, Rx off – Powersave / Configuration Mode ($C1 = $xxxx xxxx 0000 0000_b)	1	1	0	0
Rx active ($C1:b3-0 non-zero)	1	0	0	1
Tx active ($C1:b7-4 non-zero)	0	1	1	0

Control of CMX994A directly (to program the PLL, for instance) is accomplished by using the Program Block write mechanism (see Section 8.1.53). This cannot be accessed if the CMX7241/7341 is in Rx or Tx modes.

Table 12 Modem Control Selection

Tx ($C1) b7-4	Tx Task	Rx ($C1) b3-0	Rx Task
0000	Tx Off (powersave)	0000	Rx Off (powersave)
0001	Tx Idle	0001	Rx Idle
0010	Tx 4FSK Raw	0010	Rx 4FSK Raw
0011	Tx 4FSK DMR	0011	Rx 4FSK DMR
0100	reserved	0100	*reserved*
0101	Tx Analogue	0101	Rx Analogue
0110	*reserved*	0110	Rx 4FSK Raw and Analogue
0111	*reserved*	0111	Rx 4FSK DMR and Analogue
1000	*reserved*	1000	*reserved*
1001	Tx 4FSK PRBS	1001	*reserved*
1010	Tx 4FSK Test	1010	*reserved*
1011	*reserved*	1011	*reserved*
1100	*reserved*	1100	*reserved*
1101	Pass-through Output with LPF	1101	*reserved*
1110	4FSK Eye Output	1110	*reserved*
1111	Pass-through Output	1111	CMX994A Full Calibration

Table 13 Analogue Mode Selection

Analogue ($C1) b15-8	Function
b15	Enable Voice Processing
b14	Enable Audio Tone
b13	Enable Sub-Audio Processing
b12	*reserved*
b11	*reserved*
b10	Enable Selcall Processing
b9	Enable DTMF Processing
b8	Enable FFSK Processing

Table 14 Standard Operating Values in $C1

Description	Value	Notes
Tx Off/Rx Off	$0000	Powersave mode
Tx + Rx Raw Mode	$0022	
Tx + Rx DMR	**$0033**	**Slot 1, Slot 2 and CACH active (normal operation)**
Tx PRBS	$009x	
Tx Test signal	$00Ax	
Pass-through with 300Hz LPF Output	$00Dx	
4FSK Eye	$00Ex	
Pass-through	$00Fx	"Public Address" mode, MIC in -> AUDIO out selected by: $B1=$0070, $B0=$000F
CMX994A Full Calibration	$000F	Calibrate CMX994A for DC offset removal

6.5.5 Tx Idle

In this mode transmit processing is disabled.

6.5.6 Tx 4FSK Raw

This mode allows raw data to be transmitted directly from the C-BUS Tx FIFO without any data formatting, FEC or CRC processing. Data is sent exactly as presented in the FIFO and the host should insert Frame Sync sequences as required. General operation is the same as for Tx 4FSK DMR mode but Tx Raw data blocks may be 33 bytes or 36 bytes, and if 36-byte blocks are loaded in consecutive slots the data will be sent as a continuous transmission. Format is the same as that shown in Figure 24 for Rx.

6.5.7 Tx 4FSK DMR

This mode arms the modem so that it is ready to send 33-byte slots with CRC/FEC processing and data formatting for DMR. The data for each Tx burst data block is encoded and Frame Syncs are automatically inserted as required.
In normal operation the host should set this mode and then write Tx burst data blocks to the C-BUS Tx FIFO with appropriate slot number values, as required, for transmission. The Layer 2 process interrogates the Tx FIFO approximately half-way through each slot to check if the slot number of the burst matches the up-coming internal slot number. If it does, then the data block will be read, processed and the TxFIFO RDY IRQ will be asserted to inform the host that the device is able to receive more data. During active Tx slots the Tx Sequencer automatically executes its START and END tasks to control RF hardware and the receiver is automatically suppressed - so there is no requirement for the host to change the Modem Control - $C1 write register for every transmit burst.

Tx burst data blocks generate 33-byte slots for transmission and appropriate scheduling is always required. It is possible to pre-load multiple bursts into the Tx FIFO but care should be taken not to overflow the 256-byte limit and to ensure that the slot number values always remain consistent. In this case, a TxFIFO_RDY IRQ will be asserted for each data block as and when it is processed. If the TxDone IRQ is enabled (by setting b2 of the Tx Burst first word), then the following TxDone IRQ will indicate the end of the transmission.

It is recommended that the Internal Slot Counter - $CC read register be interrogated before loading any Tx burst data into the FIFO to ensure that the slot numbering is consistent. An example of sending a short data transmission is shown in section 9.3.

6.5.8 Tx Analogue

Transmit the Analogue signals as selected by b15-8. Note that making this selection will override any Rx selection or DMR Tx selection as the analogue processing is simplex only.

6.5.9 Tx 4FSK PRBS

In PRBS mode a PRBS test pattern conforming to ITU-T O.153 (Para. 2.1) is modulated and transmitted continuously giving a 511-bit repeating sequence.

6.5.10 Tx 4FSK Test

In Test mode any simple repeating test pattern can be defined using the Tx Test Pattern register ($CB) to be modulated and transmitted continuously. This mode can be used to facilitate transmitter alignment and set-up. The host may write any 16-bit data sequence to the register which is then extended to 32 bits in length by repeating the MSB and LSB. For example, if the register is set to $55FF the transmitted pattern will be $5555FFFF, resulting in a filtered square waveform at 300Hz with a deviation of +/-1.944kHz. Alternatively $0033 would result in a similar square wave but with a deviation of +/-648Hz.

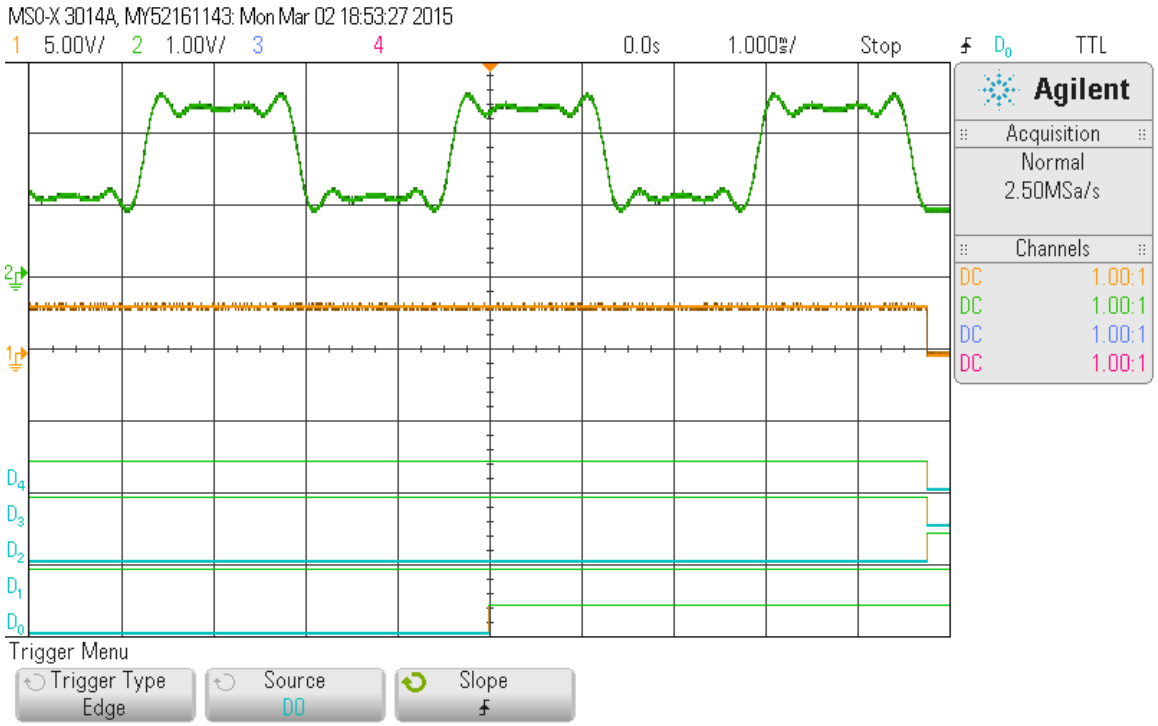


Figure 21 Tx Test Pattern

Green: MOD2 output
Yellow: RAMDAC output

D4:	GPIOB	D3:	GPIOA
D2:	TxENA	D1:	RxENA
D0:	SLTCLK		

6.5.11 Pass-through with 300Hz LPF

The received signal from Input 2 is low-pass filtered to remove signals above 300Hz, and passed to Output 2. The typical frequency response is shown in Figure 22. Output level can be adjusted using $C3:3xxx.

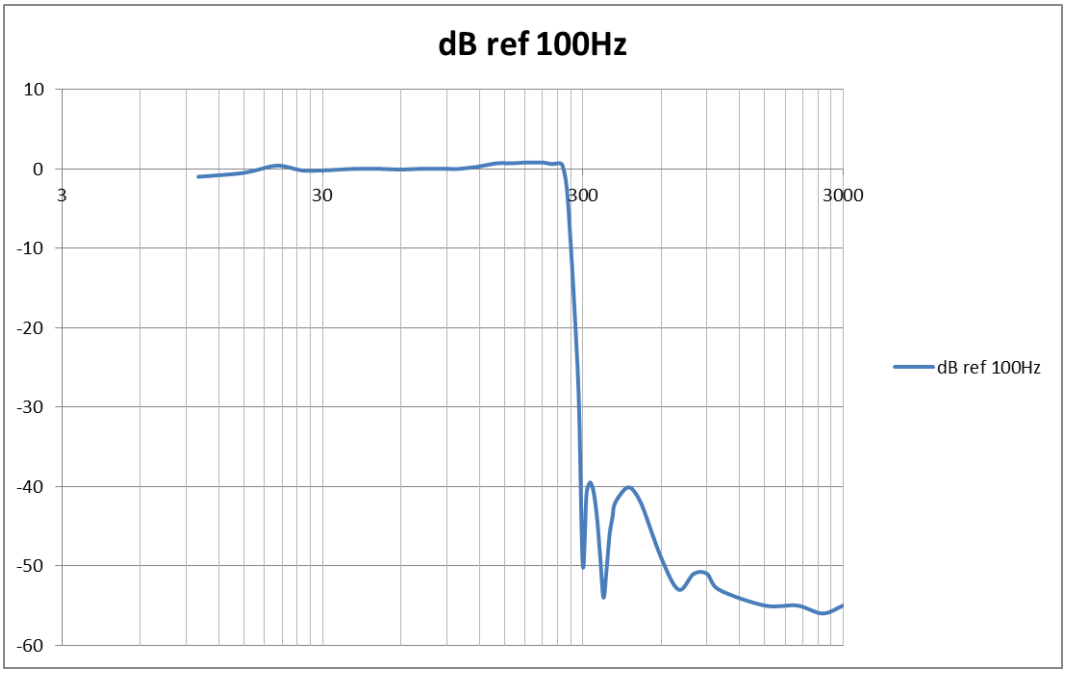


Figure 22 300Hz Pass-through filter

6.5.12 4FSK Eye

The received signal is demodulated, passed through the RRC filter and presented on Output 1. An internal synchronisation pulse is available on Output 2. This mode can be used for analysing the Rx signal path hardware. Note that in I/Q mode the quality of the received eye will vary depending on whether I/Q DC offsets have been properly acquired. Also note that the synchronisation pulse is derived from the local clock, not from the received signal, so a small amount of timing drift may be observed.

6.5.13 Pass-through

The received signals from Input 1 and 2 are passed to Output 1 and 2, with level adjustment provided in Analogue Level Control - $C3 write: $3xxx. This mode can be used for analysing the Rx signal path hardware or for a “public address” mode. The typical frequency response is shown in Table 15. Inputs 1 and 2 may be routed from any of MIC, ALT or DISC inputs under control of Input Gain and Signal Routing - $B1 write and outputs controlled by Analogue Output Gain - $B0 write.

Table 15 Frequency Response for Pass-through Operation

300Hz	-0.6 dB
1kHz	0 dB (reference)
2kHz	-0.7 dB
2.5kHz	-1.4 dB
3kHz	-2.4 dB
4kHz	-4.9 dB
6kHz	-12.2 dB

6.5.14 Tx Sequencer

The Tx Sequencer automates external hardware control and internal modulation timing, thus reducing timing constraints placed on the host. It automatically executes START and END tasks for every active Tx slot when data has been supplied for transmission by the host.

The time for each action relative to the nominal slot boundary can be set using the Programming register, P3.0 to P3.12. The minimum timing increment is 1/6 of a 4FSK symbol at 4800 baud = 34.7 us.

The RAMDAC ramping time (up and down) is set by P3.13 (RAMDAC scan time configuration). RAMDAC operation is only available whilst TxENA is active so it is important that the RAMDAC ramp down completes before TxENA becomes inactive. When TxENA becomes active, the RAMDAC output is enabled, so the initial value of the RAMDAC table (P7.0) will be output at this time, but the ramping will only start at the expiry of the RAMDAC ramp up timer (P3.3). For this reason, it is recommended that the initial value of the RAMDAC table always be cleared to zero.

The TxDone IRQ ($C6:b2) will be triggered when the TxENA signal goes to its inactive state,(if it has been enabled by the Tx burst word, b2).

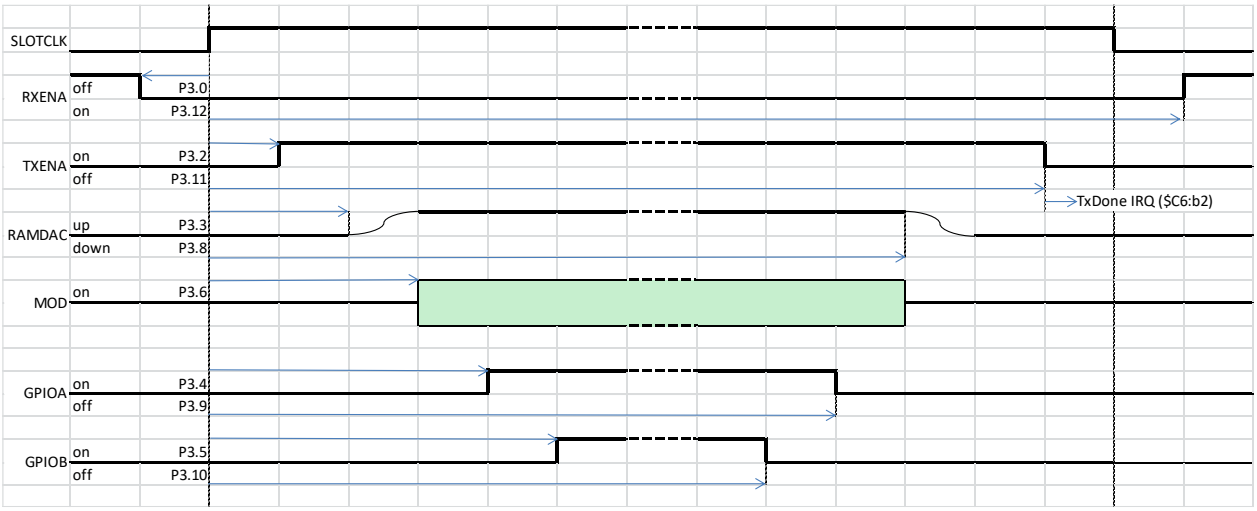


Figure 23 Tx Sequencer Delay Timers

6.5.15 Rx Idle

In this mode receiver processing is disabled but the received I/Q or LD input signal remains available for 4FSK Eye or Pass-through modes. In addition the AFSD Frame Sync search process is reset and will be re-started when the device is placed into an active Rx mode again. The RxENA signal will be active in this mode.

6.5.16 Rx 4FSK Raw

This mode allows continuous data to be received and presented to the host in its raw state with no data de-formatting, FEC or CRC processing. This may be useful for BER testing or for diagnostic purposes.

When placed into this mode the CMX7241/7341 will automatically start searching for a valid Frame Sync sequence. When one is found a Frame Sync IRQ is asserted. The device will automatically align its internal slot timing reference to the received channel, and then output the received data from the current slot and all following slots to the host in 36-byte Rx Raw data blocks using the C-BUS Rx FIFO. Each block contains the slot number in which the data was received and is accompanied with an Rx FIFO IRQ. The host must be able to service the Rx FIFO IRQs and registers promptly in order to avoid overflow.

The Frame Sync search may be re-started by the host re-sending the Rx 4FSK Raw command over the C-BUS.
If a Tx 4FSK Raw mode is also selected and the host loads a Tx data block to be transmitted, then the receiver is automatically suppressed during the active Tx slot. A dummy 0-byte sized Rx data block is returned to the host for that slot.

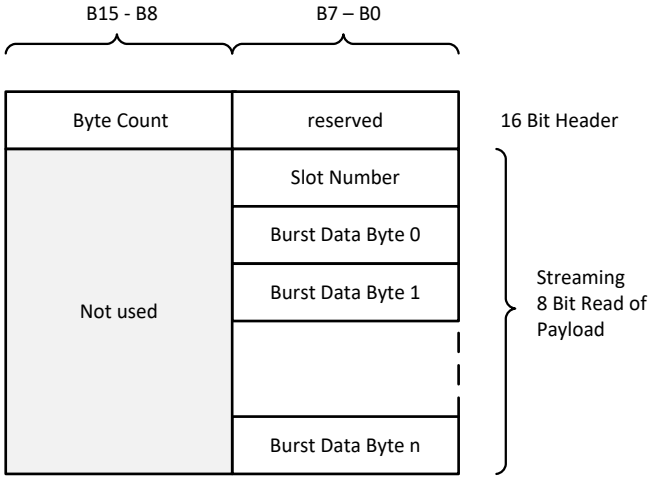


Figure 24 Rx 4FSK Raw Data Block Format

The data returned in the FIFO represents (in order):

- First half-slot Payload data
- Frame Sync
- Second half-slot Payload data
- CACH data

6.5.17 Rx 4FSK DMR

This mode allows continuous or slotted DMR data to be received and presented to the host after DMR data de-formatting, FEC and CRC processing.

When placed into this mode the CMX7241/7341 will automatically start searching for a valid Frame Sync sequence. When one is found a Frame Sync IRQ is asserted. Depending on which Frame Sync is received the device will automatically distinguish between a continuous (base station source) channel and a slotted (mobile source) channel. The device will automatically align its internal slot timing reference to the received channel, and then output the data from the current slot and all following active slots to the host in Rx Burst data blocks. The type and sequence of data blocks will depend on the channel contents. Each block contains the internal slot number in which the data was received and is accompanied with an Rx FIFO IRQ. The host must be able to service the Rx FIFO IRQs and registers promptly in order to avoid overflow.

Frame Sync search can be re-started at any time by re-writing the Rx 4FSK DMR command to the Modem Control - $C1 write register. When receiving from mobile sources in 12.5kHz Direct Mode this will be necessary after the end of each incoming call as there is no defined timing relationship from one transmitting mobile source to another. This action will also reset the internal slot counter value to zero, so any pending Tx bursts in the Tx FIFO will no longer have valid slot counter values and should be flushed.

If Tx 4FSK DMR mode is also selected, the receiver is automatically suppressed during all active Tx slots for which the host has loaded data blocks to be transmitted, and is then re-activated afterwards. It is not necessary for the host to manually disable the receiver. Slot and symbol timing references are maintained while the receiver is suppressed so the receiver can immediately continue receiving and processing data from a continuous (base station source) channel after brief interruptions without re-acquiring Frame Sync, although it may be necessary to do so after making a longer call.

When receiving in I/Q Mode the device will control its internal analogue gain and the gain of the CMX994A in order to keep the received I/Q signals within an acceptable dynamic range. This AGC feature may be disabled using Program Block P6.0:b2 (I/Q AGC Disable), in which case any setup that the host has made of the

CMX994A will determine its gain, with the input gain of the device being controlled using the Input Gain and Signal Routing - $B1 write register.

It is important to ensure that the DC offset on the I/Q signals is small, otherwise the AGC function will interpret the DC as a large received signal and never select maximum gain. This problem can be addressed by calibrating the CMX994A as described in Section 6.5.21.

6.5.18 Rx Analogue

Enable Analogue Rx processing as determined by b15-8.

6.5.19 4FSK Raw with Rx Analogue

Enable both the 4FSK modem in raw mode and the Analogue processing.

6.5.20 4FSK DMR with Analogue

Enable both the 4FSK DMR modem in formatted mode and the Analogue processing. Once a valid signal has been found, the device will automatically disable the other mode.

6.5.21 CMX994A / CMX994E I/Q Calibration (I/Q Mode only)

When receiving, the device will estimate and remove the dc error present in the I/Q signals from a CMX994A (or CMX994E) receiver. However, it is necessary to calibrate the CMX994A so that the magnitude of the initial dc offsets present is as small as possible. Selecting this mode ($C1, Modem Control = $000F) causes the device to switch the CMX994A LNA off to isolate the input3, and then measure the dc offset on the DISC and ALT input pins and to control the CMX994A receiver to minimise the dc offsets. When returned to normal Rx Mode ($C1=$xxx3), the device will then begin to receive normally – correcting the remaining dc offset internally. This mode should be executed during production test / re-calibration and the values stored by the host, or at power-on.

In addition to the static dc offsets the CMX994A exhibits a small thermal transient which can be problematic during slotted reception, for further details please consult the CMX994/CMX994A/CMX994E datasheet. The 7241/7341FI-2.x can correct for the transient as long as the calibration mode is run before reception.

Important note: when calibrating I/Q it is important that the I/Q signals are not swapped when interfacing to the CMX994A. This can be corrected by using bits 2 to 5 of the Input Gain and Routing register ($B1).

If the CMX994A is poorly calibrated, a loss of headroom when receiving signals will result. In extreme cases, when large dc offsets are amplified, the result can be big enough to prevent the AGC from reaching maximum gain as it interprets the dc offset itself as a large signal.

The parameters returned are:

- DC Offset value that the calibration process has applied to the I/Q channels
- A scaling factor calculated for the transient response of the I/Q channels (may vary with temperature)

These are returned in the registers $B9, $BA, $BB. An Event IRQ is raised when the calibration is completed, and the status reported in the 4FSK Modem Status register, $C9.

This means that, having calibrated the CMX994A on a receive channel, the calibration result may be stored by the host microcontroller and restored at a later time using Program Blocks P6.3-5.

6.6 Layer 2 Logical Burst Interface

Logical bursts are transferred from/to the host using Rx and Tx FIFO 8/16-bit C-BUS registers, allowing a full burst to be transferred in one operation. In Rx, the device will indicate to the host that burst(s) are available

[3] In some high input level situations, this may not provide sufficient isolation to determine the offset levels accurately, in which case, additional isolation would be required – see the CMX994A Data Sheet for more information.

to be read by asserting the RxFIFO_RDY flag in the IRQ Status register ($C6). In Tx, the device will indicate to the host that the FIFO is available by asserting the TxFIFO_RDY flag in the IRQ Status register ($C6).

The device detects that new data from the host is available by the host write to the C-BUS Tx FIFO register. The Tx burst data block consists of both a logical burst to be transmitted and control information to allow the 7241/7341 to encode, burst build, include the appropriate Frame Sync and select the slot to send it in. This process takes a finite time, so the data must be loaded 10ms in advance of the slot that it is expected to be transmitted in. If the data is not presented in time, it will be discarded and a data underrun error flagged in the 4FSK Modem Status - $C9 read.

The Rx Burst Data Block supplies both the decoded data received as well as timing information for the slot in which it was received and the condition of the error correction / detection process.

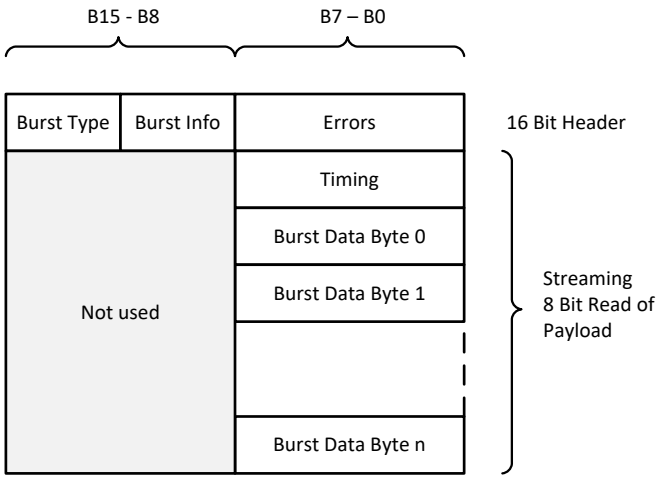


Figure 25 Logical Burst Overview

A logical burst consists of a 16-bit header followed by 8-bit payload bytes as shown in Figure 25. The Burst Type in the header implies the number of payload bytes that follow, with the exception of the Data Burst, where the payload length depends on the format and coding scheme in use, which is determined from the Data Type field. The Burst Info field may contain data, the colour code or the Frame Sync information as appropriate. The first payload byte provides slot and timing information. Exceptions to this are the CACH logical burst types, which do not have timing information, therefore their first payload byte is logical burst information. The data received in the embedded fields is combined from the separate bursts of the superframe and presented as the Embedded LC logical burst. The logical bursts are detailed in Table 18.

The format of the data within the bursts has been made common across Tx and Rx wherever possible. The most significant difference is in the handling of the Voice Payload block, which expects single bit fields in Tx, but will produce 4-bit LLR codes in Rx (compatible with the AMBE+2 Vocoder).

In a similar manner, in Tx mode, the host should write the first word of the Tx FIFO to indicate the type of burst and coding required, with the error fields cleared to zero, and the first payload byte with the slot number in which the data should be transmitted.

The CACH bursts are not applicable in Tx mode as these are not supported in terminal devices.

The logical embedded signalling burst will be populated automatically using the data already supplied in the LC Voice Header format block. However the embedded signalling, if required, can be updated in Tx on a superframe basis. The update can take place at any time in the superframe and will become current when physical burst B is transmitted.

Table 16 Burst Type

		Burst Type	Notes
0000	0		
0001	1	Analogue FFSK	Used for 1200/2400 baud FFSK
0010	2	CACH TACT	BS - every frame
0011	3	CACH SLC	BS – every four frames
0100	4		
0101	5		
0110	6		
0111	7	LC embedded	BS/MS – every superframe
1000	8	LC Voice Header	BS/MS
1001	9	LC Terminator	BS/MS
1010	A	Voice Payload	BS/MS
1011	B	Data (CSBK, Idle etc)	BS/MS
1100	C		
1101	D		
1110	E	Embedded Data	BS/MS – every superframe
1111	F		

The Burst Info field holds TACT data, Colour Code or Frame Sync information:

Table 17 Frame Sync Values in Burst Info field

Burst Info field		Frame Sync
0000	0	undefined
0001	1	BS Sourced Voice
0010	2	BS Sourced Data
0011	3	MS Sourced Voice
0100	4	MS Sourced Data
0101	5	Reverse Channel
0110	6	TDMA Direct Mode Slot 1 Voice
0111	7	TDMA Direct Mode Slot 1 Data
1000	8	TDMA Direct Mode Slot 2 Voice
1001	9	TDMA Direct Mode Slot 2 Data
1010	A	*reserved for FS10*
1011	B	*reserved*
1100	C	*reserved*
1101	D	EMB - LC data
1110	E	EMB - non-LC data
1111	F	*reserved*

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Also see TS 102 361-1 section 9.1.1 and Table 9.2

Where the Burst Info field holds Colour Code information, it is in the same format as defined in TS 102 361-1 section 9.3.1.

The lower byte of the Header word contains the error correction / detection appropriate to the burst. In receive, when an error-free burst has been detected, this will always return zero. When a CRC field is set, then the data in the burst should be treated as suspect. The BPTC coding scheme will attempt to correct a significant number of errors, which are reported for the host to evaluate the quality of the incoming signal.

The TACT status field reports the results of the Hamming code check:

00	No errors, or 1 error corrected
01	More than 1 error detected
10	*reserved*
11	*reserved*

SLC CRC field reports the result of the CRC process:

00	CRC OK, data is valid
01	CRC failed, data is invalid
10	*reserved*
11	*reserved*

EMB Error field reports the result of the Quadratic Residue process:

00	Data matched a valid code word
01	Data had 1 bit different from a valid code word
10	Data had 2 bits different from a valid code word
11	Data had 3 bits different from a valid code word

Slot Error field reports the result of the Golay process:

00	Data matched a valid code word
01	Data had 1 bit different from a valid code word
10	Data had 2 bits different from a valid code word
11	Data had 3 or more bits different from a valid code word

BPTC Error count reports the number of bits corrected, 0 to 15 (or more). The validity of the data depends on the length of the BPTC code used in each case, but for the BPTC 192,96 case, any value greater than 14 indicates that the data may be invalid, but most of the bursts that use this scheme also use a CRC which can also be checked to confirm the integrity of the data.

In Transmit, these fields should be cleared to zero, except in the case where a TxDone IRQ is required (on the final burst of a transmission), when b2 should be set.

6.6.1 Logical Burst Types

Table 18 Logical Burst Detail

Analogue FFSK (1 word):

0	0	0	1	0000	B7	B6	B5	B4	B3	B2	B1	B0

CACH TACT format (1 word):

0	0	1	0	TACT bits	0	0	0	0	0	0	TACT status

CACH SLC format (1 word + 4 bytes):

0	0	1	1	TACT bits				BPTC Error Count				SLC CRC		TACT status	
0	0	0	0	0	0	0	0	0	0	0	0	SLC Op Code			
0	0	0	0	0	0	0	0	B23	B22	B21	B20	B19	B18	B17	B16
0	0	0	0	0	0	0	0	B15	B14	B13	B12	B11	B10	B9	B8
0	0	0	0	0	0	0	0	B7	B6	B5	B4	B3	B2	B1	B0

LC Embedded format (1 word + 11 bytes):

0	1	1	1	0000				BPTC Error Count		0	0	0	CRC
0	0	0	0	0	0	0	0	Internal Slot Count					
0	0	0	0	0	0	0	0	Colour Code				PI	0	0	0
0	0	0	0	0	0	0	0	B71							
0	0	0	0	0	0	0	0								
0	0	0	0	0	0	0	0								B0

LC Voice Header format (1 words + 11 bytes):

1	0	0	0	Frame Sync				BPTC Error Count				Slot Errors		0	CRC
0	0	0	0	0	0	0	0	Internal Slot Count							
0	0	0	0	0	0	0	0	Colour Code				Data Type (0001_b)			
0	0	0	0	0	0	0	0	B71							
0	0	0	0	0	0	0	0								
0	0	0	0	0	0	0	0								B0

LC Voice Terminator format (1 words + 11 bytes):

1	0	0	1	Frame Sync				BPTC Error Count				Slot Errors		0	CRC
0	0	0	0	0	0	0	0	Internal Slot Count							
0	0	0	0	0	0	0	0	Colour Code				Data Type (0010_b)			
0	0	0	0	0	0	0	0	B71							
0	0	0	0	0	0	0	0								
0	0	0	0	0	0	0	0								B0

Voice Payload format (1 words + 109 bytes in Rx):

1	0	1	0	See Note 1				0	0	0	0	EMB Errors	0	0
0	0	0	0	0	0	0	0	Internal Slot Count						
0	0	0	0	0	0	0	0	LLR215				LLR214		
0	0	0	0	0	0	0	0	LLR213				LLR212		
0	0	0	0	0	0	0	0							
0	0	0	0	0	0	0	0	LLR3				LLR2		
0	0	0	0	0	0	0	0	LLR1				LLR0		

Voice Payload format (1 words + 28 bytes in Tx):

1	0	1	0	See Note 1				0	0	0	0	0	TxDone ENA	0	0
0	0	0	0	0	0	0	0	Internal Slot Count							
0	0	0	0	0	0	0	0	B215							
0	0	0	0	0	0	0	0								B0

Note 1: Burst Info Field can be SYNC, EMB or Reverse Channel.

Note 2: In Rx operation, the data returned is in 4-bit LLR format (LLR215-000), In Tx operation, host should supply single-bit values (b215-000).

Non - LC Embedded format (1 word + 4 bytes):[4]

1	1	1	0	Embedded (1110_2)				BPTC Error Count				EMB Errors		0	0
0	0	0	0	0	0	0	0	Internal Slot Count							
0	0	0	0	0	0	0	0	Colour Code				PI	LCSS		0
0	0	0	0	0	0	0	0	0	0	0	0	0	B10	B9	B8
0	0	0	0	0	0	0	0	B7	B6	B5	B4	B3	B2	B1	B0

Note: This logical burst type returns the data that would normally be contained in Frame F to allow for reverse channel or encrypted operation. Normally this would be a “null” field.

Standalone Inbound Reverse format (1 words + 4 bytes):

1	1	1	0	Frame Sync (0101_2)				BPTC Error Count				EMB Errors		0	0
0	0	0	0	0	0	0	0	Internal Slot Count							
0	0	0	0	0	0	0	0	Colour Code				PI	LCSS		0
0	0	0	0	0	0	0	0	0	0	0	0	0	B10	B9	B8
0	0	0	0	0	0	0	0	B7	B6	B5	B4	B3	B2	B1	B0

Standalone Outbound Reverse format (1 words + 4 bytes):

[4] This function is liable to change following discussions at ETSI TGDMR meeting #49, CR48v5

1	1	1	0	Frame Sync (0101_2)				BPTC Error Count				EMB Errors		0	0
0	0	0	0	0	0	0	0	Internal Slot Count							
0	0	0	0	0	0	0	0	Colour Code				PI		LCSS	0
0	0	0	0	0	0	0	0	0	0	0	0	0	B10	B9	B8
0	0	0	0	0	0	0	0	B7	B6	B5	B4	B3	B2	B1	B0

Data format (1 words + xx bytes):

1	0	1	1	Frame Sync				BPTC Error Count				SLOT Errors		CRC32	CRC
0	0	0	0	0	0	0	0	Internal Slot Count							
0	0	0	0	0	0	0	0	Colour Code				Data Type			
0	0	0	0	0	0	0	0								

The Data burst is different to the others in that the payload coding and length is decided by the setting of the Data Type field as shown in Table 19. (Note that the Frame Sync field may be replaced by Reverse Channel information in some Base Station downlink circumstances).

Table 19 Data Types

$b_3 – b_0$	Data Type	Size	Notes
0000_2	PI Header	1 word + 12 bytes	payload 10 bytes
0001_2	Voice LC Header	1 word + 11 bytes	*reserved* – Sent / Received as burst type 8
0010_2	Terminator with LC	1 word + 11 bytes	*reserved* – Sent / Received as burst type 9
0011_2	CSBK	1 word + 12 bytes	payload 10 bytes
0100_2	MBC Header	1 word + 12 bytes	payload 10 bytes
0101_2	MBC Continuation	1 word + 14 bytes	payload 12 bytes / payload 10 bytes + 2 bytes CRC
0110_2	Data Header	1 word + 14 bytes	payload 10 bytes + 2 bytes CRC
0111_2	Rate ½ Data	1 word + 14 bytes	payload 12 bytes
1000_2	Rate ¾ Data	1 word + 20 bytes	payload 18 bytes
1001_2	Idle	1 word + 14 bytes	payload 12 bytes
1010_2	Rate 1 Data	1 word + 26 bytes	payload 24 bytes
1011_2	*reserved*		Treated as CSBK
1100_2	*reserved*		
1101_2	*reserved*		
1110_2	*reserved*		
1111_2	*reserved*		

Note that “Voice LC Header” and “Terminator with LC” are special cases of this generic format and are handled separately.
Note: “MBC Continuation” covers both MBC Intermediate **and** MBC Last Block formats – see TS 102-361-1 section 7.4

6.6.2 Confirmed and Unconfirmed Data Bursts

Both confirmed and non-confirmed data transfers are supported, the content of the Data Header determining how the subsequent data bursts are processed, with the device applying the 9-bit CRC for confirmed mode, and the 32-bit Fragment CRC for both modes where appropriate (see TS 301 361-1 Section 8.2.2).

Types of data header are distinguished by the DPF field (Data Packet Format), which is the lowest 4 bits in the first header byte (see TS 102 361-1 section 8.2.1.1 and 8.2.1.2 and 9.3.17). Any of the defined types can be sent and received, but the FI uses the DPF values for 'Data packet with unconfirmed delivery - 0010_2' and 'Data packet with confirmed delivery - 0011_2' to determine how to calculate CRCs for the subsequent data blocks. In other formats, the unconfirmed / confirmed operation is determined by the state of the "Response Requested" info ("A") field of the data header (see TS 102 361-3 section 6.1.2 and TS 102 361-1 section 8.2.1).

A confirmed data burst consists of a confirmed data header followed by a number of Rate ½, ¾ or Rate 1 data blocks. The first two payload bytes in a confirmed data block consist of a 7-bit serial number and the 9-bit CRC.

In Tx, the host must load the 7-bit serial number in the first byte of the payload, aligned to the 7 MSBs and a null field for the 9-bit CRC, where appropriate. The host should provide the data followed by sufficient padding bytes to reach the message boundary, including 4 bytes of null 32-bit CRC (where appropriate, both 9-bit and 32-bit CRC fields will be overwritten with the CRC's calculated by the device before transmission).
In Rx, the FI will report the serial number and CRC as part of the payload. If there is a CRC9 error, bit 0 of the PDU Error status field will be set. The values of the 9-bit CRC in the payload are reported after the appropriate CRC bit mask (as shown in TS 102 361-1 Appendix B, 3.12.) has been applied; other CRC values are reported without the mask.

An unconfirmed data burst consists of an unconfirmed data header followed by a number of Rate ½, ¾ or Rate 1 data blocks. The host should provide the data followed by sufficient padding bytes to reach the message boundary, including 4 bytes of null CRC (which will be overwritten with the CRC calculated by the device before transmission). The last block is identified by reading the 'Blocks to Follow' field in the header block, and counting subsequent data blocks.

In Tx, the FI will replace the null CRC field provided by the host with one calculated by the device.
In Rx, the FI will report the CRC as part of the payload. If there is a CRC32 error, bit 1of the PDU Error status field will be set.

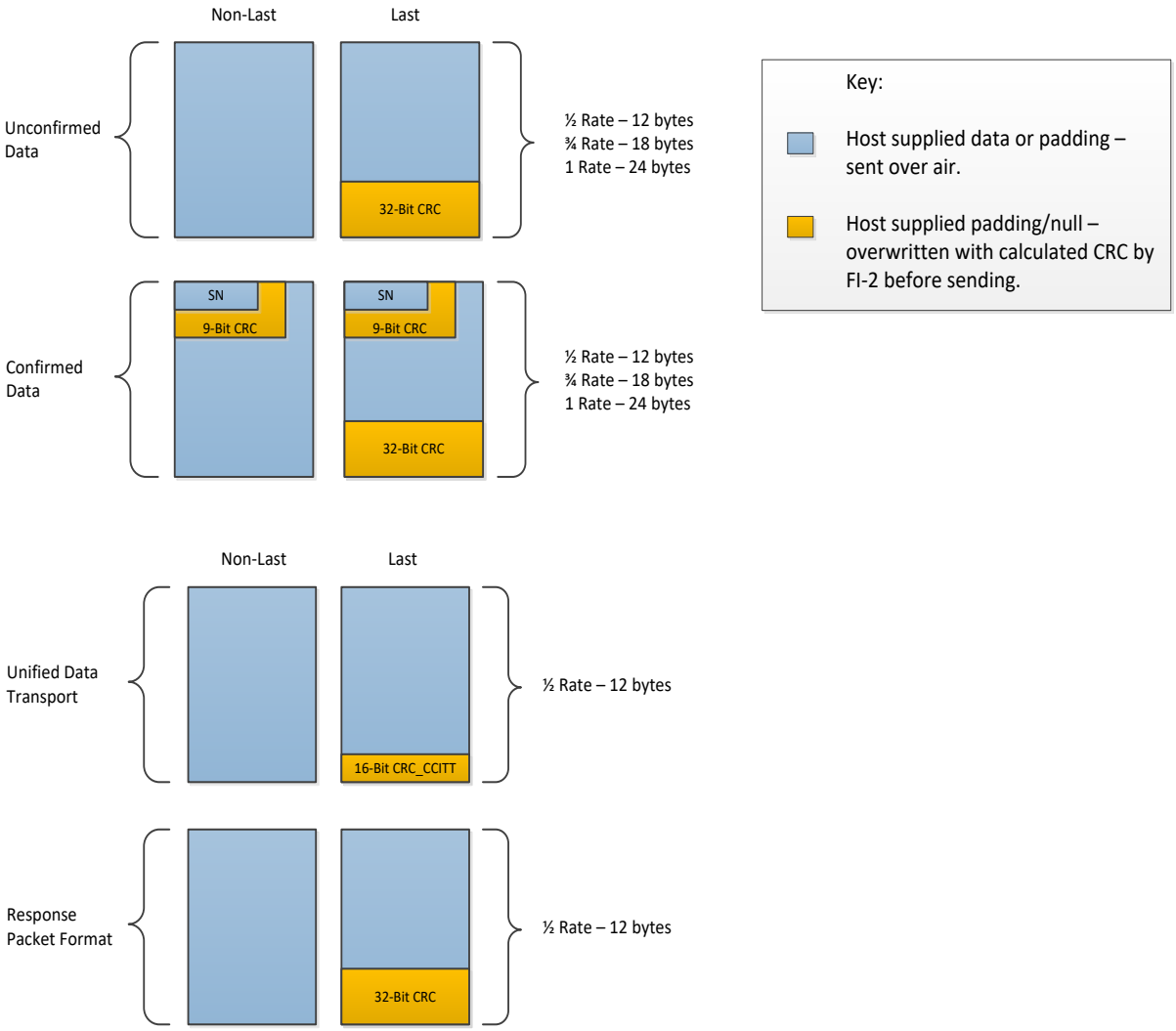


Figure 26 Data Format

6.6.3 Voice Call Example

An example where a MS receives a Voice call from a BS is shown in Table 20:

Table 20 Burst Sequence

Burst Type	Burst Info Field Content	Internal Slot Count Value	DMR Slot	Burst / Frame Type	Notes
LC Voice Header	Frame Sync - BS Sourced Data	23	1	81	Assume received on slot 23
CACH TACT	TACT			2x	
Idle	Frame Sync - BS Sourced Data	24	2	B1	
CACH TACT	TACT			2x	
Voice Payload	Frame Sync - BS Sourced Voice	25	1	A2	Voice Frame A
CACH TACT	TACT			2x	
Idle	Frame Sync - BS Sourced Data	26	2	B1	
CACH SLC	TACT			3x	
Voice Payload	Embedded	27	1	AD	Voice Frame B
CACH TACT	TACT			2x	
Idle	Frame Sync - BS Sourced Data	28	2	B1	
CACH TACT	TACT			2x	
Voice Payload	Embedded	29	1	AD	Voice Frame C
CACH TACT	TACT			2x	
Idle	Frame Sync - BS Sourced Data	30	2	B1	
CACH SLC	TACT			3x	
Voice Payload	Embedded	31	1	AD	Voice Frame D
CACH TACT	TACT			2x	
Idle	Frame Sync - BS Sourced Data	32	2	B1	
CACH TACT	TACT			2x	
Voice Payload	Embedded	33	1	AD	Voice Frame E
LC embedded	Colour Code = 1		1	71	Used for late entry
CACH TACT	TACT			2x	
Idle	Frame Sync - BS Sourced Data	34	2	B1	
CACH SLC	TACT			3x	
Voice Payload	Reverse	35	1	AE	Voice Frame F
Non-LC embedded	Embedded			EE	Data Content of Embedded Frame F – normally null.
CACH TACT	TACT			2x	
Idle	Frame Sync - BS Sourced Data	36	2	B1	

Note that the DMR slot number (1 or 2) is not known to the modem, this information is contained within the CACH logical burst. Using the CACH information, the host may determine the relationship between the internal slot counter value and the actual DMR slot number.

6.6.4 CACH SLC and Embedded Signalling Handling:

The CACH SLC logical burst is mapped across 4 consecutive physical bursts received from a BS. The embedded signalling logical burst is mapped across 4 frames of a Voice burst (superframe) received from either another MS or a BS, so cannot be handled on a physical burst basis.

Instead, they will be presented as Logical Channels, when they become available, interspersed with the burst data.

In Tx the logical embedded signalling burst will be populated automatically using the data already supplied in the LC Voice Header format block. However the embedded signalling, if required, can be updated in Tx on a superframe basis. The update can take place at any time in the superframe and will become current when physical burst B is transmitted.

CACH transmission is not supported in this device (This is a BS function).

6.6.5 Burst Error / FEC reporting

All bursts that implement error detection or correction (or both) can report the success / failure using the error status fields of the burst data. Two fields are provided as most bursts implement different schemes for different sections of the burst. Where a parity or CRC check is implemented, the success or failure of this process is reported in LSB's of the Error status field, Where an FEC is implemented, the number of bits that required correction is indicated in the higher order bits. If no errors were detected or corrected, the Error status field will return all zeros. This information may be used by the host to evaluate the quality of the communication channel in use, and if necessary, try and find a better one. Note that the time to decode received bursts will vary with the degree of error correction required, especially with BPTC schemes, which may execute the BPTC decode multiple times to maximise the error correction capabilities.

The layer 2 FS decode evaluates this field for both FS or embedded data by evaluating the confidence levels for a FS decode against the Embedded data QR decode result. The most confident result will be reported. This scheme enhances the ability of the device to correctly decode the field in poor signal conditions.

6.7 CMX994A / CMX994E Pass-through Mode

To allow the host to communicate directly with the CMX994A / CMX994E for test and configuration purposes, a pass-through mode is available which allows any CMX994A / CMX994E C-BUS register to be written).
To write to the CMX994A / CMX994E:

- Set the device to Tx Off/Rx Off mode ($C1=$0000)
- Wait for the Program Flag to be set ($C6 b0)
- Write the CMX994A address value and select Program Block $0F in the Program Block Address register ($C7)
- Write the CMX994A C-BUS data to the Programming register ($C8)
- Wait for the Program Flag to be set ($C6 b0).

Note that it is NOT possible to read data back from the CMX994A using this interface.

6.8 Addressing

Addressing is handled by the host. Both Link Control and Short Link Control bursts are supported to allow for normal and late-entry calls.

6.9 SPI-Codec Control

If SPI-Codec mode has been enabled, the host should set the device into an active (Rx or Tx) mode, enable the Audio Codec and deliver audio PCM samples to the SPI-Codec port. At the end of all DMR transmissions the host should determine when it is safe for shut down the SPI-Codec port and the Vocoder.

The SPI-Codec is controlled using C-BUS register SPI Codec Control - $A0 write. The SPI-Codec interface may be configured for either SPI style operation (SSOUT is active for the duration of the PCM data word) or I^2S

mode (SSOUT is active for one SCLK cycle at the start of each PCM word). The SCLK rate is fixed at 3.2MHz to be compatible with the AMBE 3000 device from DVSI Inc.

Configuration of the SPI-Codec is enabled in Program Block P6.1

6.10 Analogue PMR Description

6.10.1 Sub-Audio Processing

The DCS 4-pole Bessel filter used in the sub-audio path can be set by Program Block 2.12. A 260Hz Chebyshev is selected automatically for CTCSS operation.
An internal generator/detector is available for the 51 CTCSS tones shown in Table 22 and the 83 DCS codes shown in Table 21. Squelch-tail elimination is provided by inverting the MOD outputs or executing a phase change in CTCSS mode or a 134Hz “turn-off tone” in DCS mode. The tone/code to be generated is set by the value in the Analogue Mode register ($B5) in Tx mode and read from the Analogue Status / Pon Checksum 1 Hi register ($B8) in Rx mode (see section 8.1.39).

6.10.2 Voice Processing

A set of Audio Processing blocks are available for use in Analogue mode:

- 300Hz HPF
- 12.5kHz channel filter or 25kHz channel filter
- Hard limiter with anti-splatter filter
- Pre-emphasis and De-emphasis
- Voice AGC
- Level adjust
- In–band audio generator/s in both Rx and Tx paths

The 12.5kHz channel filter (narrow) will be selected by default, the 25kHz filter (wide) can be enabled by setting P2.0:b0. Note that selecting 25kHz mode operation in I/Q mode will automatically inhibit DMR operation due to the difference in receiver bandwidths. Parallel analogue / digital mode is only available in 12.5kHz mode.

6.10.3 300Hz HPF

This is designed to reject signals below 300Hz from the voice path so that sub-audio signalling can be inserted (in Tx) or removed (in Rx) as appropriate. It should be enabled whenever sub-audio signalling is required.

6.10.4 12.5kHz/25kHz Channel Filters

These are designed to meet the requirements of ETSI 300 296 for Voice signal processing and feature an upper roll-off at 2.55kHz and 3.0kHz respectively.

6.10.5 Hard Limiter

This is provided to limit the peak deviation of the radio signal to meet the requirements of ETSI EN 300 296. An anti-splatter filter is included to reduce the effects of any harmonic signals generated in the process. The limiter threshold can be set using P2.3.

6.10.6 Voice AGC

An automatic gain control system is provided in the MIC path, utilising the programmable gain settings of the Input 1 amplifier. When used in conjunction with the hard limiter function, this can compensate for large variations in the MIC input signal without introducing significant distortion. The AGC threshold is programmable using P2.1 whilst the maximum gain setting and the decay timeout can be set using P2.2. When this feature is enabled, the host should not attempt to directly control the Input 1 gain setting.

6.10.7 Level Adjust

Independent level adjustments are provided using $C3 register for the voice, in-band and sub-audio signals as shown in Figure 27 Tx & Rx Routing and Control.

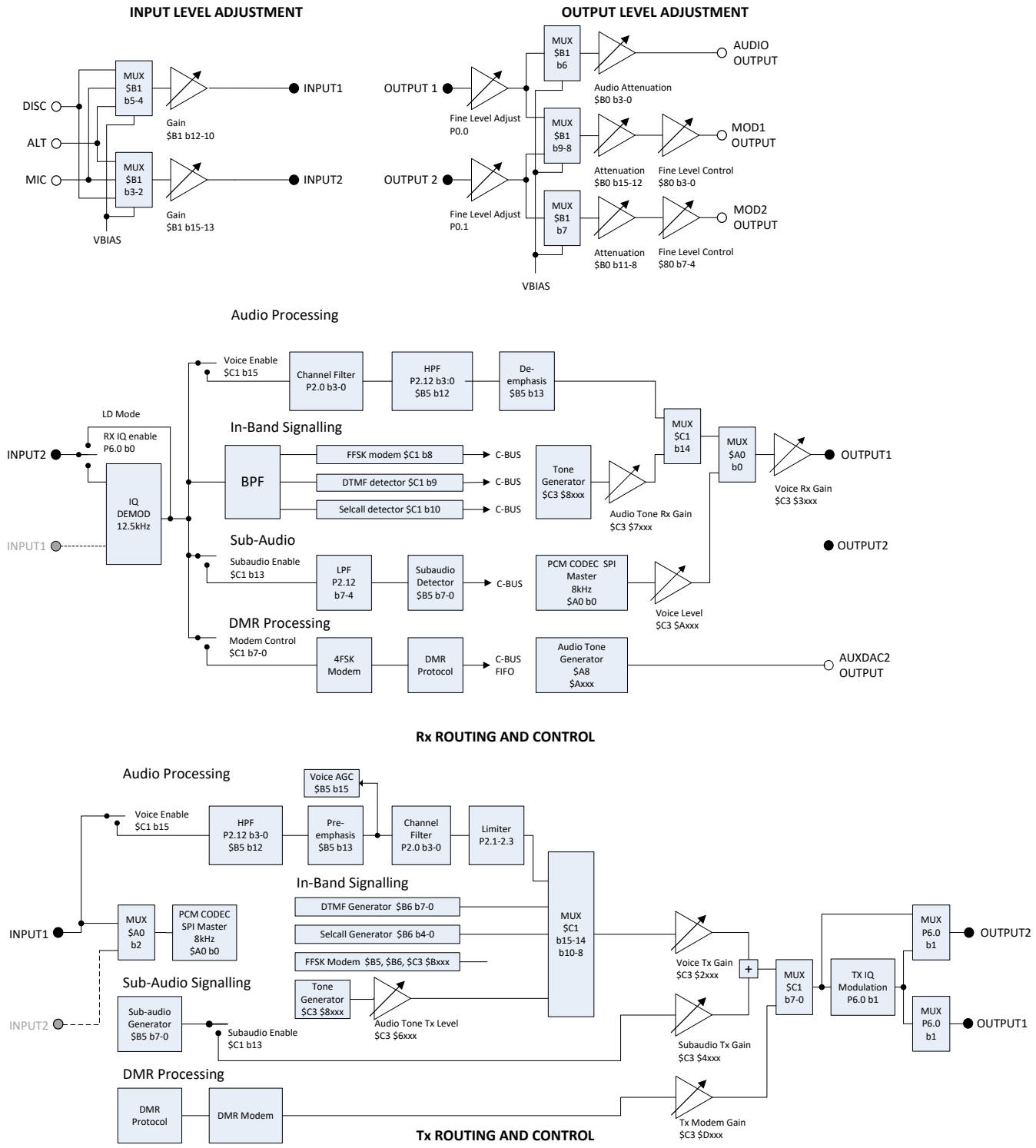


Figure 27 Tx & Rx Routing and Control

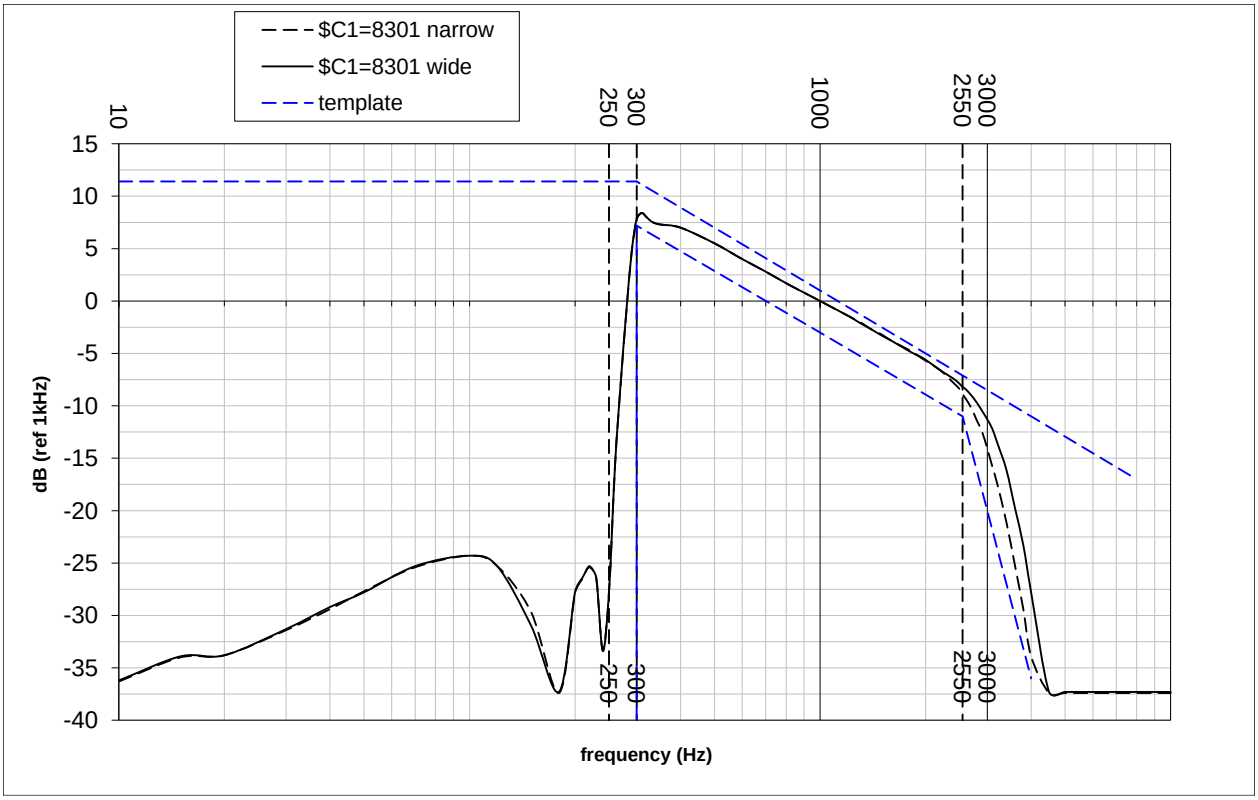


Figure 28 Rx Audio Response

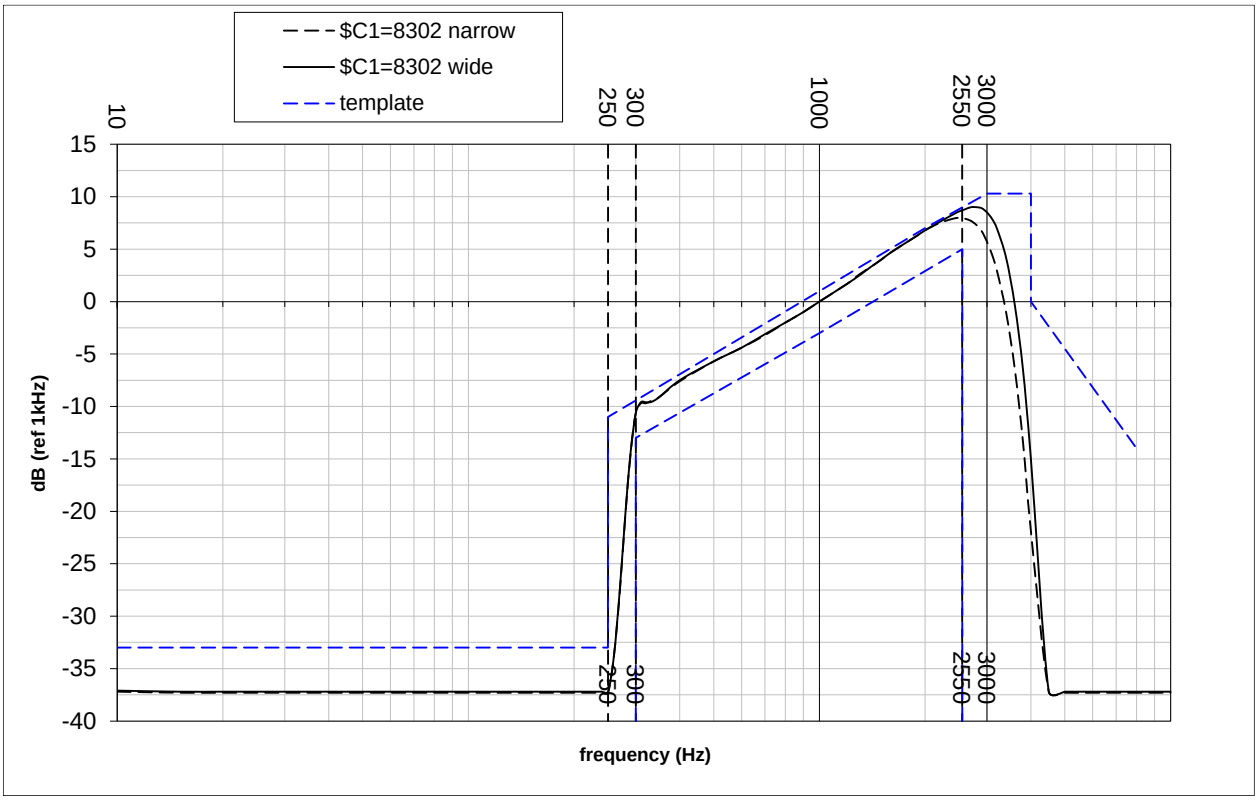


Figure 29 Tx Audio Response

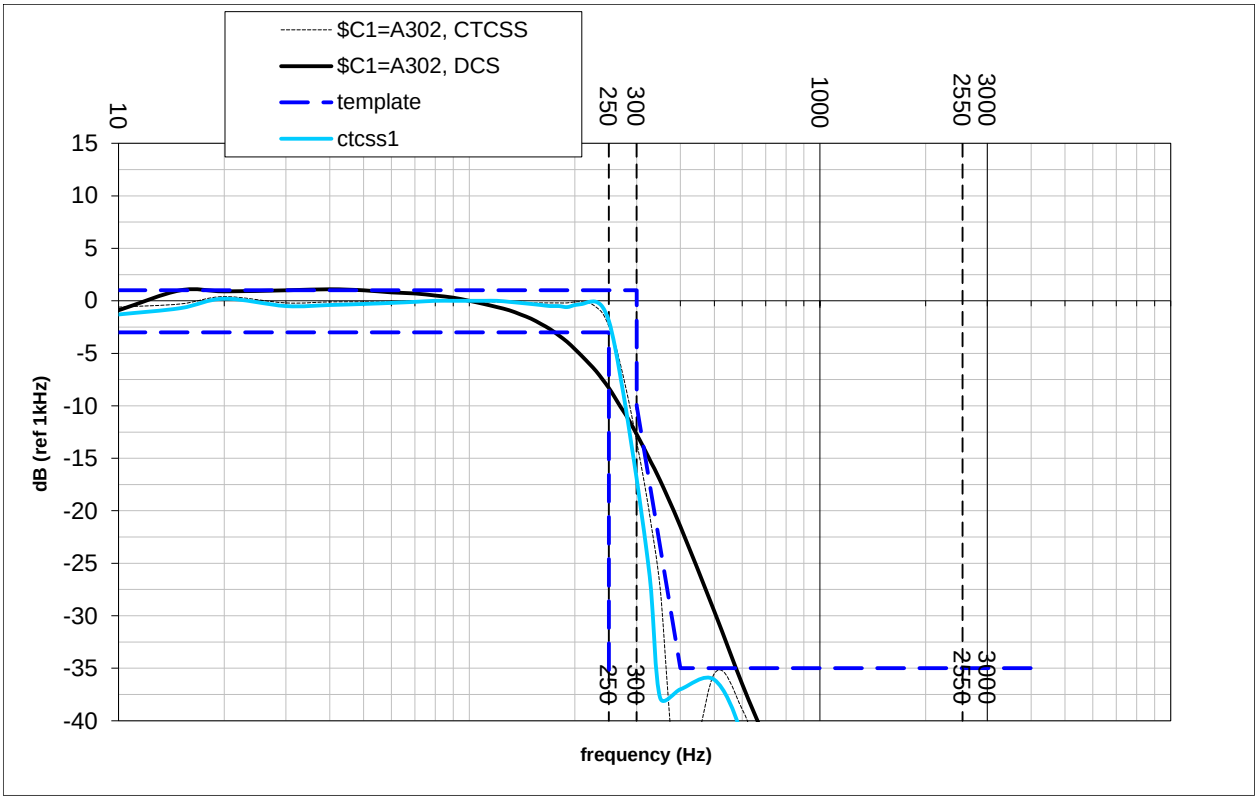


Figure 30 CTCSS and DCS filters

Table 21 DCS codes and values

	Register Value					Register Value			
DCS Code	**true**		**inverted**		**DCS Code**	**true**		**inverted**	
	Decimal	Hex	Decimal	Hex		Decimal	Hex	Decimal	Hex
no code	0	00	100	64	**311**	42	2A	142	8E
23	1	01	101	65	**315**	43	2B	143	8F
25	2	02	102	66	**331**	44	2C	144	90
26	3	03	103	67	**343**	45	2D	145	91
31	4	04	104	68	**346**	46	2E	146	92
32	5	05	105	69	**351**	47	2F	147	93
43	6	06	106	6A	**364**	48	30	148	94
47	7	07	107	6B	**365**	49	31	149	95
51	8	08	108	6C	**371**	50	32	150	96
54	9	09	109	6D	**411**	51	33	151	97
65	10	0A	110	6E	**412**	52	34	152	98
71	11	0B	111	6F	**413**	53	35	153	99
72	12	0C	112	70	**423**	54	36	154	9A
73	13	0D	113	71	**431**	55	37	155	9B

	Register Value					Register Value			
DCS Code	**true**		**inverted**		**DCS Code**	**true**		**inverted**	
	Decimal	Hex	Decimal	Hex		Decimal	Hex	Decimal	Hex
74	14	0E	114	72	**432**	56	38	156	9C
114	15	0F	115	73	**445**	57	39	157	9D
115	16	10	116	74	**464**	58	3A	158	9E
116	17	11	117	75	**465**	59	3B	159	9F
125	18	12	118	76	**466**	60	3C	160	A0
131	19	13	119	77	**503**	61	3D	161	A1
132	20	14	120	78	**506**	62	3E	162	A2
134	21	15	121	79	**516**	63	3F	163	A3
143	22	16	122	7A	**532**	64	40	164	A4
152	23	17	123	7B	**546**	65	41	165	A5
155	24	18	124	7C	**565**	66	42	166	A6
156	25	19	125	7D	**606**	67	43	167	A7
162	26	1A	126	7E	**612**	68	44	168	A8
165	27	1B	127	7F	**624**	69	45	169	A9
172	28	1C	128	80	**627**	70	46	170	AA
174	29	1D	129	81	**631**	71	47	171	AB
205	30	1E	130	82	**632**	72	48	172	AC
223	31	1F	131	83	**654**	73	49	173	AD
226	32	20	132	84	**662**	74	4A	174	AE
243	33	21	133	85	**664**	75	4B	175	AF
244	34	22	134	86	**703**	76	4C	176	B0
245	35	23	135	87	**712**	77	4D	177	B1
251	36	24	136	88	**723**	78	4E	178	B2
261	37	25	137	89	**731**	79	4F	179	B3
263	38	26	138	8A	**732**	80	50	180	B4
265	39	27	139	8B	**734**	81	51	181	B5
271	40	28	140	8C	**743**	82	52	182	B6
306	41	29	141	8D	**754**	83	53	183	B7
					user defined	84	54	184	B8

Table 22 CTCSS codes and values

Register Value		CTCSS tone		Register Value		CTCSS tone
Decimal	Hex	Frequency		Decimal	Hex	Frequency
200	C8	Tx: no tone Rx: Tone Clone		228	E4	173.8
201	C9	67.0		229	E5	179.9
202	CA	71.9		230	E6	186.2
203	CB	74.4		231	E7	192.8
204	CC	77.0		232	E8	203.5
205	CD	79.7		233	E9	210.7
206	CE	82.5		234	EA	218.1
207	CF	85.4		235	EB	225.7
208	D0	88.5		236	EC	233.6
209	D1	91.5		237	ED	241.8
210	D2	94.8		238	EE	250.3
211	D3	97.4		239	EF	69.3
212	D4	100.0		240	F0	62.5
213	D5	103.5		241	F1	159.8
214	D6	107.2		242	F2	165.5
215	D7	110.9		243	F3	171.3
216	D8	114.8		244	F4	177.3
217	D9	118.8		245	F5	183.5
218	DA	123.0		246	F6	189.9
219	DB	127.3		247	F7	196.6
220	DC	131.8		248	F8	199.5
221	DD	136.5		249	F9	206.5
222	DE	141.3		250	FA	229.1
223	DF	146.2		251	FB	254.1
224	E0	151.4		252	FC	user defined
225	E1	156.7		253	FD	Phase change
226	E2	162.2		254	FE	DCS turn-off
227	E3	167.9		255	FF	invalid tone

CTCSS detector thresholds and bandwidth are selectable using P2.4. Use of the “split tones” (239 to 251) will require a smaller bandwidth to be used, otherwise the adjacent tone frequency may be detected instead.
CTCSS phase changes (greater than +/- 90 degrees) are indicated by code $FD, and generated by writing to $C3 whilst the CTCSS generator is active. The phase change detector is enabled using P2.0:b2.

6.11 FFSK Data Modem

The device supports 1200 baud FFSK data mode suitable for use with MPT1327 or similar systems.
Selection of the FFSK mode is performed by bit 8 of the Mode register ($C1). Detection of the selected In-band signalling mode can be performed in parallel with voice reception.

See:

- Modem Control - $C1 write

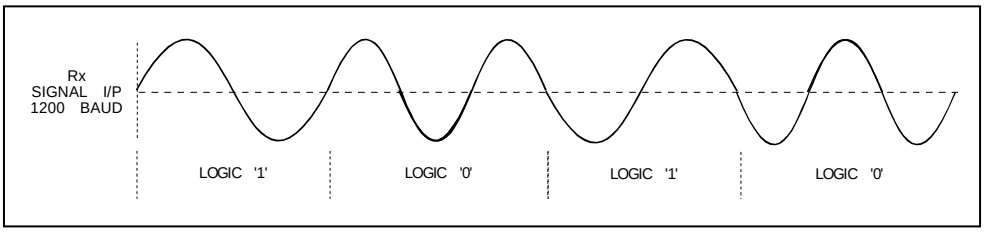


Figure 31 Modulating Waveforms for 1200 MSK/FFSK Signals

The table below shows the combinations of frequencies and number of cycles to represent each bit of data, for both baud rates.

Table 23 Data Frequencies for MPT1327 mode

Baud Rate	Data	Frequency	Number of Cycles
1200baud	1	1200Hz	one
	0	1800Hz	one and a half

Note: FFSK may be transmitted in conjunction with a CTCSS or DCS sub-audio component.

6.11.1 Receiving FFSK Signals

The device can decode incoming FFSK signals at 1200 and 2400 baud data rates. The desired rates can be configured by setting the Rx Mode in the FFSK Modem Format via the Analogue Level Control register ($C3:Bxxx). The form of FFSK signals is shown in Figure 31. An FFSK transmission begins with a preamble sequence followed by a 16-bit Sync sequence and then the user data.

The received signal is filtered and data is extracted with the aid of a PLL to recover the clock from the serial data stream. The recovered data is stored in a 2 byte buffer and an interrupt issued to indicate received data is ready. Data is transferred over the C-BUS under host µC control. If this data is not read before the next data is decoded it will be overwritten and it is up to the user to ensure that the data is transferred at an adequate rate following data ready being flagged. The FFSK bit clock is not output externally.

The extracted data is compared with the 16-bit programmed Frame Sync pattern (default is $CB23). An in-band IRQ will be flagged when the programmed Frame Sync pattern is detected. Once a valid Frame Sync pattern has been detected, the frame sync search algorithm is disabled; it may be re-started by the host disabling the FFSK bit of the Modem Control register ($C1:b8) and then re-enabling it (taking note of the C-BUS latency time).

Separate sync sequences are available, SynC, SynD, SynT and SynX. SynT is automatically derived as the inverse of the SynC sequence. All other sync sequences are user programmable. Sync detects are reported with an in-band event IRQ and a code in the Analogue Status / Pon Checksum 1Hi register ($B8). The FFSK RxRate bit in this register can be read to determine whether the detection was at 1200 or 2400 baud.
After frame synchronisation has been achieved, the following user data is made available in the RxData FIFO with burst type 0001_b, along with a DataRdy IRQ indication.

FFSK may be transmitted in conjunction with a CTCSS or DCS sub-audio component. The device will handle the sub-audio signals as previously described. If a sub-audio signal turns off during reception of FFSK, it is up to the host µC to turn off the decoding as the device will continue receiving and processing the incoming signal until commanded otherwise by the host µC.

The host µC must keep track of the message length or otherwise determine the end of reception (e.g. by using sub-audio information to check for signal presence) and disable the demodulator at the appropriate time.

6.11.2 Transmitting FFSK Signals

When enabled, the modulator will begin transmitting the preamble data (defined in P4.23), followed by the selected sync sequence as defined in P4.24 to P4.26 and selected by b11-8 of the Analogue Mode register ($B5). Therefore, these registers should be programmed to the required values before transmission is enabled.
The modulation rate will be determined by the setting of Tx Mode in the FFSK Modem Format field of the Analogue Level Control register ($C3 = $Bxxx). Changes to this setting will not be applied until the next time the modem is enabled. The level of the FFSK signal generated can be controlled using the Audio Tone Tx Level field of the Analogue Level Control register ($C3 = $6xxx).

The device will issue a Tx FIFO RDY IRQ, which the host should respond to by loading the user data it wishes to transmit through the Tx FIFO.

The device generates its own internal data clock and converts the binary data into the appropriately phased frequencies, as shown in Figure 31 and Table 23. The binary data is taken from Tx Data FIFO with burst type 0001_b, most significant bit first. The following data words must be provided over the C-BUS in response to the Tx FIFO RDY IRQ. The FFSK transmission will terminate when the Tx FIFO is starved, after which it will indicate that the final data bit has left the chip by raising the TxDone IRQ, after which the host may power-down the RF circuitry and return the device to Idle mode as required.

6.12 Selcall Signalling

The device supports both Selcall and user-programmable in-band tones between 288Hz and 3000Hz. Note that if tones below 400Hz are used, sub-audio signalling should be disabled and the 300Hz HPF disabled.

By default, the device will load the CCIR Selcall tone set, however this may be over-written by the host with any valid set of tones within its operational range by use of Program Block 4. This ensures that the device can remain compatible with all available tone systems in use. The device does not implement automatic repeat tone insertion or deletion: it is up to the host to correctly implement the appropriate Selcall protocol.

Selection of the Selcall mode is performed by bit 10 of the Mode register ($C1). Detection of the selected in-band signalling mode can be performed in parallel with voice reception.
See:

- Modem Control - $C1 write
- Analogue Mode - $B5 write
- Analogue Status / Pon Checksum 1 Hi - $B8 read

6.12.1 Receiving and Decoding Selcall Tones

Selcall tones can be used to flag the start of a call or to confirm the end of a call. If they occur during a call the tone may be audible at the receiver. When enabled, an interrupt will be issued when a signal matching a valid in-band tone changes state (i.e. on, off or a change to different tone).

The device implements the EEA tone set. Other addressing and data formats can be implemented by loading the Program Blocks with the appropriate values. The frequency of each tone is defined in the Programming registers P4.0 to P4.15

In receive mode the device scans through the tone table sequentially. The code reported will be the first one that matches the incoming frequency and b3 of the IRQ Status register, $C6, will be asserted.

Adjustable decoder bandwidths and threshold levels are programmable via the Programming register. These allow certainty of detection to be traded against signal to noise performance when congestion or range limits the system performance.

Table 24 Selcall Tones

$B8:b15-13 (Rx)	$B8:b12 – 8 (Rx) $B6:b4-0 (Tx)			Freq. (Hz)	Program Block
Binary		Dec	Hex		
100	00000	0	0	1981	P4.0
100	00001	1	1	1124	P4.1
100	00010	2	2	1197	P4.2
100	00011	3	3	1275	P4.3
100	00100	4	4	1358	P4.4
100	00101	5	5	1446	P4.5
100	00110	6	6	1540	P4.6
100	00111	7	7	1640	P4.7
100	01000	8	8	1747	P4.8
100	01001	9	9	1860	P4.9
100	01010	10	A	2400	P4.10
100	01011	11	B	930	P4.11
100	01100	12	C	2247	P4.12
100	01101	13	D	991	P4.13
100	01110	14	E	2110	P4.14
100	01111	15	F	1055	P4.15
100	10000	16	10	Null tone	-
100	11111	31	1F	Unknown tone (Rx only)	-

Notes:

Normally, tone 14 is the repeat tone. This code must be used in transmit mode when the new code to be sent is the same as the previous one. e.g. to send '333' the sequence '3R3' should be sent, where 'R' is the repeat tone. When receiving Selcall tones, the device will indicate the repeat tone when it is received. It is up to the host to interpret and decode the tones accordingly.

6.12.2 Transmitting Selcall Tones

In Tx mode, only one in-band signalling mode may be selected at a time. The Selcall tone to be generated is loaded into the Analogue In-band Signalling ($B6) using bits 4-0 – see Table 24. The Selcall tone level is set using the Analogue Level Control register ($C3 = $6xxx) using the Audio Tone Tx Level field.

6.12.3 Alternative Selcall Tone Sets

These may be loaded via the Programming register to locations P4.0 to P4.15. See section 8.3.5.

Table 25 Alternative Selcall Tone Sets

	Frequency (Hz)				
Tone Number	**EIA**	**EEA**	**CCIR**	**ZVEI 1**	**ZVEI 2**
0	600	1981	1981	2400	2400
1	741	1124	1124	1060	1060
2	882	1197	1197	1160	1160
3	1023	1275	1275	1270	1270
4	1164	1358	1358	1400	1400
5	1305	1446	1446	1530	1530
6	1446	1540	1540	1670	1670
7	1587	1640	1640	1830	1830
8	1728	1747	1747	2000	2000
9	1869	1860	1860	2200	2200
A	2151	1055	2400	2800	885
B	2435	930	930	810	810
C	2010	2247	2247	970	740
D	2295	991	991	885	680
E	459	2110	2110	2600	970
F	NoTone	2400	1055	680	2600

6.13 DTMF Signalling

The device provides both DTMF encode and decode functions using the tone combinations shown in Table 26. Selection of DTMF mode is performed by bit 9 of the Modem Control register ($C1). Detection of the selected in-band signalling mode can be performed in parallel with voice reception.

6.13.1 Reception and Decoding of DTMF

When a DTMF tone has been detected, b3 of the IRQ Status register ($C6) will be set and the tone code will be available in:Analogue Status / Pon Checksum 1 Hi - $B8 read– see Table 26. This value will over-write any existing in-band tone value that may be present.

6.13.2 Transmission of DTMF

In Tx mode, only one in-band signalling mode may be selected at a time, DTMF is selected by setting b9 in the Modem Control register ($C1). The DTMF signals to be generated are loaded into the Analogue In-band Signalling register ($B6) using bits 3-0 – see Table 26.

Single tone mode ($B6:b4) generates only a single tone of the DTMF pair. The underlined value in Table 26 indicates which of the tones will be generated when this bit is enabled.

The DTMF level is set with the Analogue Level Control register, using the AudioTone Tx Level field ($C3 = $6xxx) with optional twist set using $B6:b6,5 – see Table 27.

Setting $B6:b7 (No Tone) will mute the output of the DTMF generator. This can be used to generate a pause period between tones, thereby minimising the number of C-BUS writes required when generating a string of DTMF digits.

Table 26 DTMF Tone Pairs

$B8:b15-13 (Rx)	$B8:b12–8 (Rx) $B6:b3-0 (Tx)			Freq. Low (Hz)	Freq. High (Hz)
Binary		Key	Hex		
010	00000	D	0	941	1633
010	00001	1	1	697	1209
010	00010	2	2	697	1336
010	00011	3	3	697	1477
010	00100	4	4	770	1209
010	00101	5	5	770	1336
010	00110	6	6	770	1477
010	00111	7	7	852	1209
010	01000	8	8	852	1336
010	01001	9	9	852	1477
010	01010	0	A	941	1336
010	01011	*	B	941	1209
010	01100	#	C	941	1447
010	01101	A	D	697	1663
010	01110	B	E	770	1663
010	01111	C	F	852	1663
010	10000	x	x	Null tone (Rx only)	

Table 27 DTMF Twist

b6,5	Twist - dB
00	0
01	-2
10	-4
11	-6

6.14 Squelch Operation

Many limiter/discriminator chips provide a noise-quieting squelch circuit around an op-amp configured as a filter. This signal is conventionally passed to a comparator to provide a digital squelch signal, which can be routed directly to one of the CMX7241/7341's GPIO pins or to the host. However with the CMX7241/7341, the comparator and threshold operations can be replaced by one of the AuxADCs with programmable thresholds and hysteresis functions.
See:

- IRQ Status - $C6 read
- Program Block Address - $C7 write.

Note: This functionality is not necessary in I/Q mode as squelch detection is within CMX7241/7341 signal processing however the AuxADC functionality remains available.

6.15 GPIO Pin Operation

The CMX7241/7341 provides four GPIO pins: RXENA, TXENA, GPIOA and GPIOB.

RXENA and TXENA are configured to reflect the Tx/Rx state of the Mode register under control of the Tx Sequencer. These lines should be pulled to their inactive state by 47kΩ resistors. This will ensure that the signals are in an inactive state whilst the FI loads, and also allows the FI to determine if they should be driven active high (CMX994A compatible) or active low (for backwards compatibility with the 7141 series).

Note that RXENA and TXENA will not change state until the relevant mode change has been executed by the CMX7241/7341. This is to allow the host sufficient time to load the relevant data buffers and the CMX7241/7341 time to encode the data required prior to its transmission. There is a fixed time delay between the GPIO pins changing state and the modulation signal appearing at the MOD output pins. During the power-on sequence (until the FI has completed its load sequence) these pins have only a weak pull-up applied to them, so care should be taken to ensure that any loading during this period does not adversely affect the operation of the unit.

GPIOA and GPIOB can either be used as serial clock and data signals when separate serial ports are required (see Section 8.1.29), can be host programmable for input or output using the P6.0, or can be assigned as part of the Tx Sequencer operation (CMX7241 only).

6.16 Auxiliary ADC Operation

The inputs to the two auxiliary ADCs can be independently routed from any of the signal input pins under control of the AuxADC Control register, $93. Conversions will be performed as long as a valid input source is selected. To stop the ADCs, the input source should be set to 'off'. Register $C0:b6, BIAS, must be enabled for auxiliary ADC operation.

Averaging can be applied to the ADC readings by selecting the relevant bits in the AuxADC Control register, $93, the length of the averaging is determined by the value in the C-BUS registers $93, and defaults to a value of 0. This is a rolling average system such that a proportion of the current data will be added to the last average value. For an average value of:

0 = 50% of the current value will be added to 50% of the last average value,
1 = 25% of the current value will be added to 75% of the last average value,
2 = 12.5% etc.
--- etc
7 = 0.78125% of input sample + 99.21875% of saved average
The maximum value of this field is 7.

High and Low thresholds may be independently applied to both ADC channels (the comparison is applied after averaging, if this is enabled) and an IRQ generated the first time a rising edge passes the High threshold or a falling edge passes the Low threshold, see Figure 32. A high threshold IRQ re-arms the low threshold interrupt and vice-versa. The thresholds are programmed using registers $94-$97 See Figure 32.

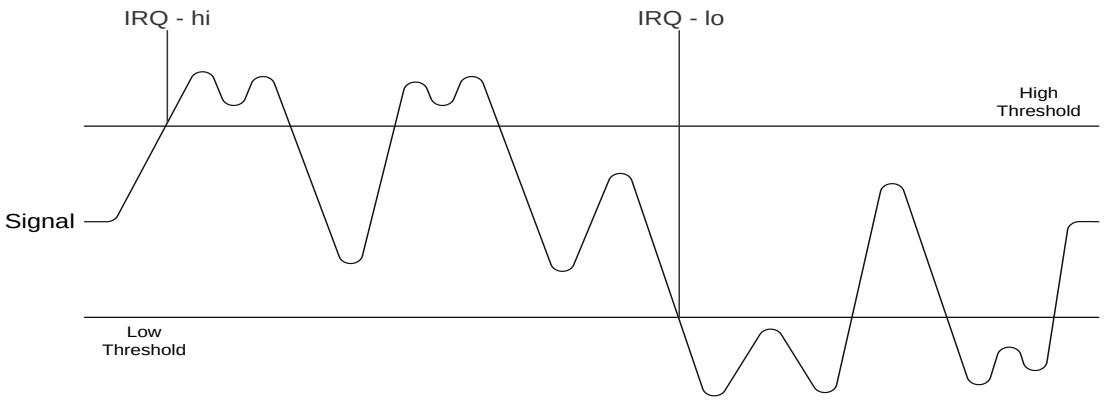


Figure 32 AuxADC IRQ Operation

Auxiliary ADC data is read back in the AuxADC1 / AuxADC2 Data registers ($D6 and $D7) and includes the threshold status as well as the actual conversion data (subject to averaging, if enabled).
See:

- Pon Checksum 2 Hi - $A9 read
- AuxADC1 and 2 Data - $D6 and $D7 read
- Aux Config – Powersave and RSSI Threshold - $CD write

6.17 Auxiliary DAC/RAMDAC Operation

The four auxiliary DAC channels are programmed via the AuxDAC Data registers, $30 to $33.

AuxDAC channel 1 is allocated to the RAMDAC function, which will automatically output a pre-programmed profile at a programmed rate under control of the Tx Sequencer when TxENA is active. The default profile is a raised cosine (see Table 29), but this may be overwritten with a user-defined profile by writing to Programming register P7.0 to 63. The gain of the profile may be adjusted by writing to the RAMDAC Level ($84) and a fixed offset may be applied using the RAMDAC Offset ($85). RAMDAC operations can be automatically controlled using the Tx Sequencer, or manually using $A8.

The RAMDAC operation is only available when TxENA is active and, to avoid glitches in the ramp profile, it is important not to change to Tx Off/Rx Off or Rx mode whilst the RAMDAC is still ramping. An external R-C network maybe required to remove any “step” noise from the output.
When TxENA is not active, AuxDAC channel 1 is available for manual control using AuxDAC Data register $30.

The AuxDAC outputs hold the user-programmed level during a powersave operation if left enabled, otherwise they will return to zero. Updating an AuxDAC is performed by writing to the relevant AuxDAC Data register ($30 to $33).

See:

- Aux Function Control - $A8 write.
- AuxDAC1-4 Data - $30 to $33 write

6.18 Digital System Clock Generators

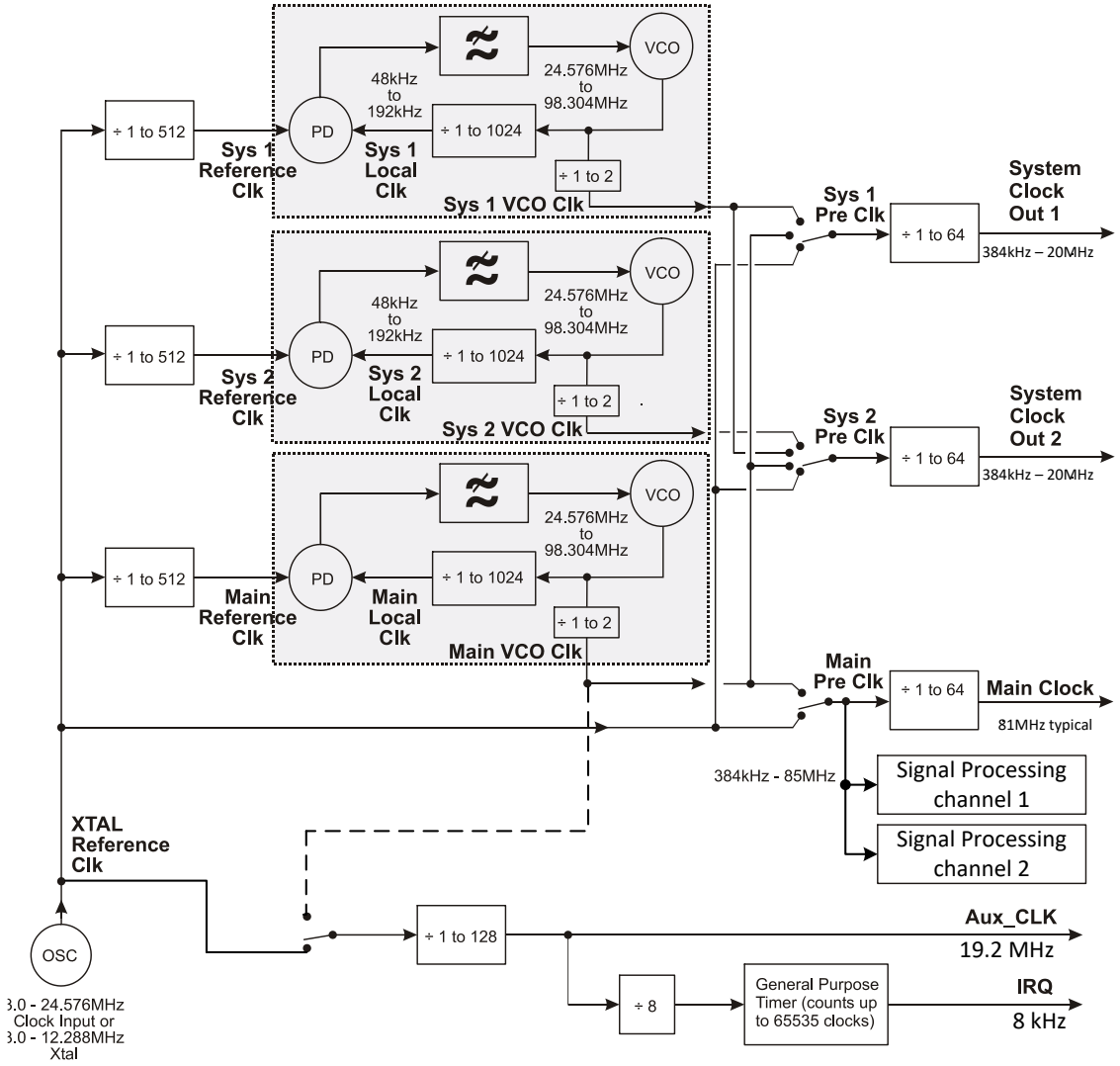


Figure 33 Digital Clock Generation Schemes

The CMX7241/7341 includes a two-pin crystal oscillator circuit. This can either be configured as an oscillator, as shown in Section 4.1 or the XTAL input can be driven by an externally generated clock. The crystal (Xtal) source frequency can go up to 12.288MHz (clock source frequency up to 24.576MHz), however, a 19.2MHz oscillator is assumed by default for the functionality provided in this Function Image.

6.18.1 Main Clock Operation

A digital PLL is used to create the Main Clock (nominally 81.1008MHz) for the internal sections of the CMX7241/7341. At the same time, other internal clocks are generated by division of either the XTAL Reference Clock or the Main Clock. These internal clocks are used for determining the sample rates and conversion times of A-to-D and D-to-A converters and the signal processing blocks. The CMX7241/7341 defaults to the settings appropriate for a 19.2MHz oscillator.

SYSCLK1 output is available to drive additional circuits, as required. This phase locked loop (PLL) clock can be programmed via the System Clock registers with suitable values chosen by the user. The SYSCLK 1 PLL Data ($AB) controls the values of the VCO Output divider and Main Divide registers, while the SYSCLK 1 PLL Ref register ($AC) controls the values of the Reference Divider and signal routing configurations. A spreadsheet to help derive the values for these registers is available from CML Customer Support. The default state is to output the XTAL signal on this pin, it may be disabled to save power using the $AB register.

Alternatively, the SYSCLK1 pin may be re-configured as an External LNA Enable, for use in Rx I/Q AGC operation. See section 8.3.7.

SYSCLK2 is used to output a Slot/frame timing signal in this FI and is not available for user configuration.
See:

- SYSCLK 1 and SYSCLK 2 PLL Data - $AB, $AD write
- SYSCLK 1 and SYSCLK 2 PLL REF - $AC, $AE write.

6.19 Signal Level Optimisation

The internal signal processing of the CMX7241/7341 will operate with wide dynamic range and low distortion only if the signal level at all stages in the signal processing chain is kept within the recommended limits. For a device working from a 3.3V ±10% supply, the maximum signal level which can be accommodated without distortion is [(3.3 x 90%) - (2 x 0.3V)] Volts pk-pk = 838mV rms, assuming a sine wave signal. This should not be exceeded at any stage. In particular, any over-loading of the ADC inputs should be avoided if the device is to work to specification.

6.19.1 Transmit Path Levels

For the maximum signal out of the MOD1 and MOD2 attenuators, the signal level at the output of the Modem block is set to be 0dB, The Fine Output adjustment ($80)[5] has a maximum attenuation of 1.8dB and no gain, whereas the Coarse Output adjustment ($B0) has a variable attenuation of up to 12dB and no gain.

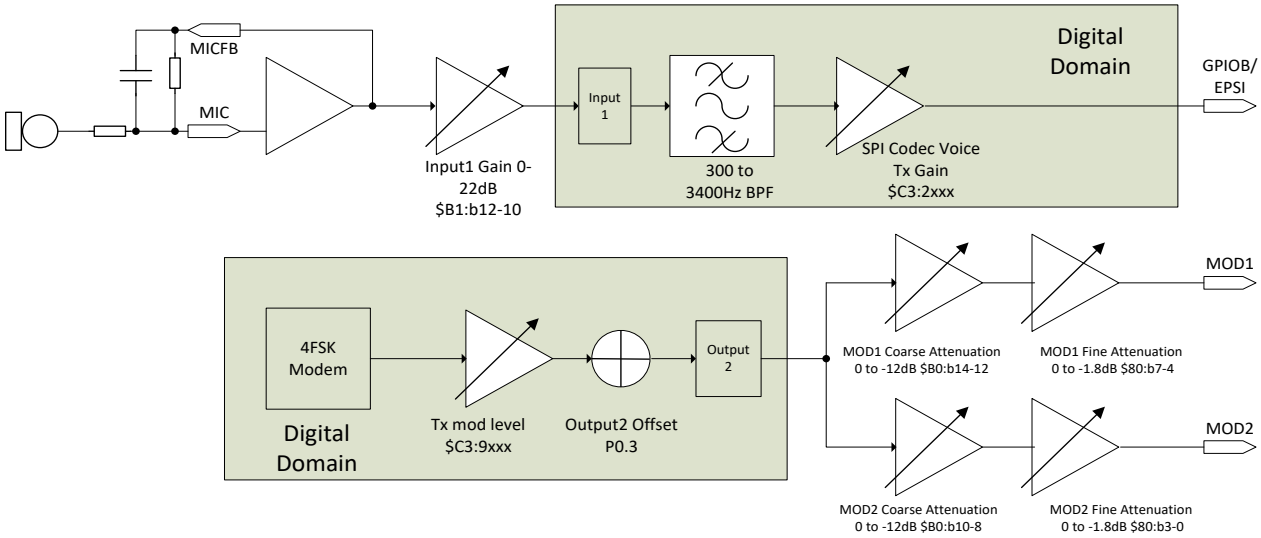


Figure 34 Tx Levels

6.19.2 Receive Path Levels

The Coarse Input adjustment ($B1) has a variable gain of 0 to +22.4 dB and no attenuation. In LD mode with the lowest gain setting (0dB), the maximum allowable input signal level at the DISCFB pin would be 838mV rms. This signal level is an absolute maximum, which should not be exceeded.

[5] Note that C-BUS register $80 is an 8-bit register.

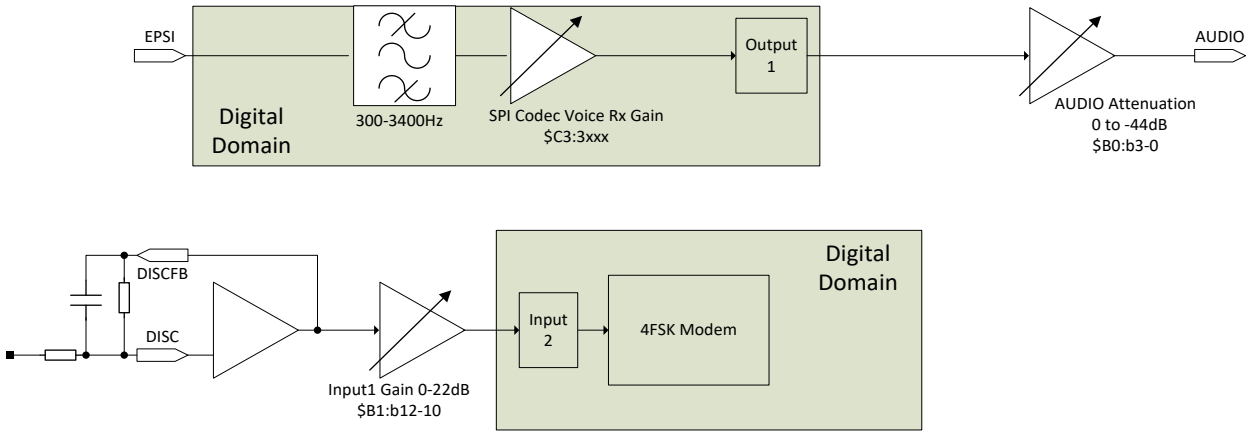


Figure 35 Rx Levels (LD mode)

In I/Q mode CMX7241/7341 automatically manages the gain control settings of Input 1 and Input 2 to optimise signal levels.

6.20 Tx Spectrum Plots

Using the test system shown in Figure 36 the CMX7241 FI-2 internal PRBS generator was used to modulate the RF FM signal generator. Some typical results are shown in Figure 37. The desired deviation was achieved by adjusting the deviation control on the RF signal generator.

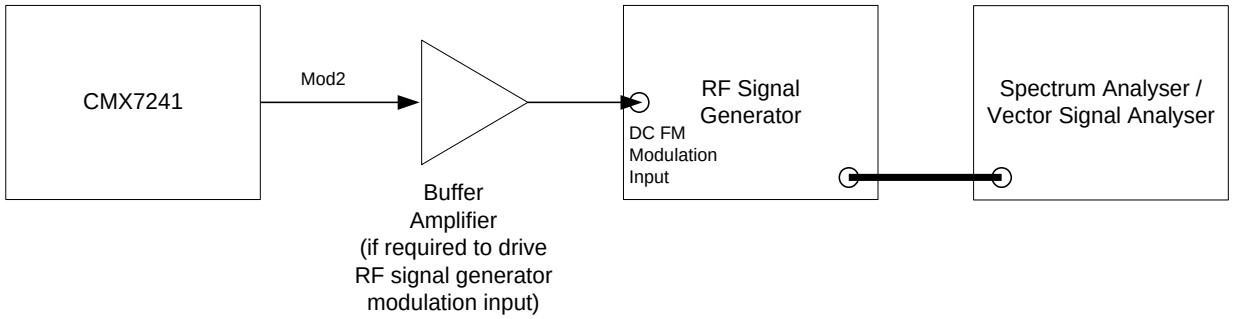


Figure 36 Tx Spectrum and Modulation Measurement Configuration for Two-point Modulation

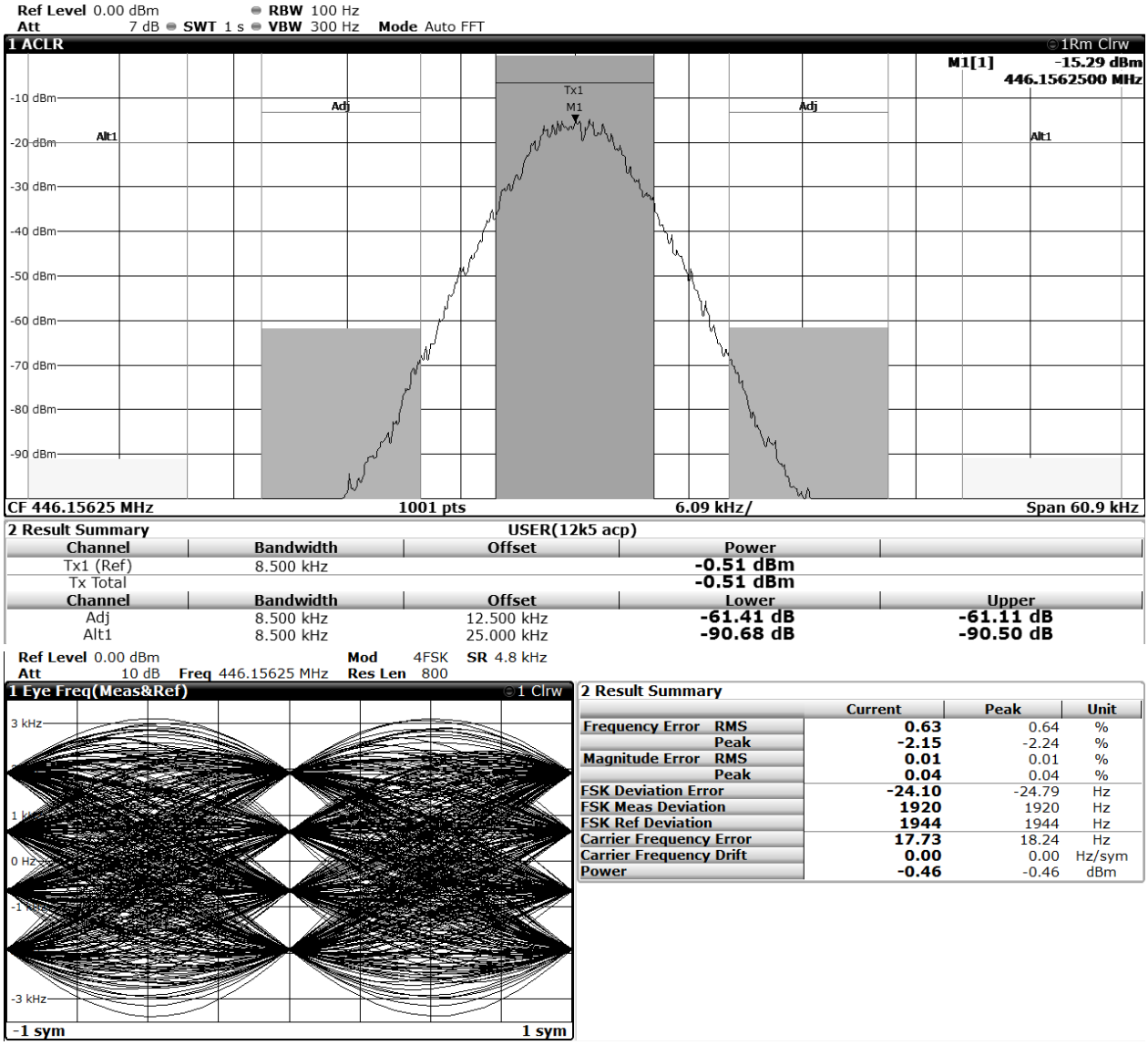


Figure 37 Tx Modulation Spectra (4-FSK, 9.6 kbps, RRC – 0.2)

7 Performance Specification

7.1 Electrical Performance

7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply: DV_{DD}- DV_{SS}	−0.3	4.5	V
AV_{DD}- AV_{SS}	−0.3	4.5	V
Voltage on any pin to DV_{SS}	−0.3	DV_{DD} + 0.3	V
Voltage on any pin to AV_{SS}	−0.3	AV_{DD} + 0.3	V
Current into or out of any power supply pin (excluding BIAS) (i.e. VDEC, AVDD, AVSS, DVDD, DVSS)	−30	+30	mA
Current into or out of any other pin	−20	+20	mA
Voltage differential between power supplies:			
DV_{DD} and AV_{DD}	0	0.3	V
DV_{SS} and AV_{SS}	0	50	mV

L4 Package (48-pin LQFP)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1600	mW
... Derating	–	16	mW/°C
Storage Temperature	−55	+125	°C
Operating Temperature	−40	+85	°C

Q3 Package (48-pin VQFN)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1750	mW
... Derating	–	17.5	mW/°C
Storage Temperature	−55	+125	°C
Operating Temperature	−40	+85	°C

7.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Unit
Supply Voltage:				
$DV_{DD} – DV_{SS}$		3.0	3.6	V
$AV_{DD} – AV_{SS}$		3.0	3.6	V
$V_{DEC} – DV_{SS}$	2	1.8	1.8	V
Operating Temperature		−40	+85	°C
XTAL/CLK Frequency (using an Xtal)	1	3.0	12.288	MHz
XTAL/CLK Frequency (using an external clock)	1	3.0	24.576	MHz

Notes: 1 This FI is designed to operate using a 19.2MHz clock (CMOS logic level).
To meet DMR requirements for TDMA direct mode, 1 ppm tolerance is required.

2 The V_{DEC} supply is automatically derived from DV_{DD} by the on-chip voltage regulator.

7.1.3 Operating Characteristics

Details in this section represent design target values and are not currently guaranteed.

For the following conditions unless otherwise specified:

External components as recommended in Figure 2 and Figure 3. Maximum load on digital outputs = 30pF.

Oscillator Frequency = 19.2MHz ±0.0002% (2 ppm); T_{AMB} = –40°C to +85°C.

$AV_{DD} = DV_{DD}$ = 3.0 V to 3.6 V.

V_{DEC} = 2.5 V.

Reference Signal Level = 308mVrms at 1kHz with AV_{DD} = 3.3V.

Signal levels track with supply voltage, so scale accordingly.

Signal to Noise Ratio (SNR) in bit rate bandwidth.

Input stage gain = 0 dB. Output stage attenuation = 0 dB.

Current consumption figures quoted in this section apply to the device when loaded with 7241/7341FI-2.x only. The use of other CMX7241/7341 Function Images can modify the current consumption of the device.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current	21				
All Powersaved					
DI_{DD}		–	8	100	µA
AI_{DD}		–	4	20	µA
Tx Idle/Rx Idle Mode	22				
DI_{DD}		–	4.7	–	mA
AI_{DD}	23	–	2.5	–	mA
Rx Mode (LD Mode)	22				
DI_{DD} (search for FS)		–	TBA	–	mA
DI_{DD} (FS found)		–	TBA	–	mA
AI_{DD}		–	TBA	–	mA
Rx Mode (I/Q Mode)	22				
DI_{DD} (search for FS)		–	11.7	–	mA
DI_{DD} (FS found)		–	12.8	–	mA
AI_{DD}		–	3.9	–	mA
Tx Mode	22				
DI_{DD} (two-point)		–	7.4	–	mA
DI_{DD} (I/Q)		–	9.3	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	4.1	–	mA

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Additional Current for each Auxiliary System Clock (output running at 4MHz)					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)	26	–	250	–	µA
Additional Current for each Auxiliary ADC					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	50	–	µA
Additional Current for each Auxiliary DAC					
AI_{DD} (AV_{DD} = 3.3V)		–	200	–	µA
XTAL/CLK Input	24				
Input Logic 1		70%	–	–	DV_{DD}
Input Logic 0		–	–	30%	DV_{DD}
Input Current (Vin = DVDD)		–	–	40	µA
Input Current (Vin = DVSS)		−40	–	–	µA
C-BUS Interface and Logic Inputs					
Input Logic 1		70%	–	–	DV_{DD}
Input Logic 0		–	–	30%	DV_{DD}
Input Leakage Current (Logic 1 or 0)		−1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
C-BUS Interface and Logic Outputs					
Output Logic 1 (I_{OH} = 2mA)		90%	–	–	DV_{DD}
Output Logic 0 (I_{OL} = -5mA		–	–	10%	DV_{DD}
'Off' State Leakage Current		–	–	10	µA
IRQN (Vout = DVDD)		−1.0	–	+1.0	µA
REPLY_DATA (output HiZ)		−1.0	–	+1.0	µA
V_{BIAS}	25				
Output Voltage Offset wrt AVDD/2 (IOL < 1µA)		–	±2%	–	AV_{DD}
Output Impedance		–	22	–	kΩ

Notes:
21 T_{AMB} = 25°C: not including any current drawn from the device pins by external circuitry.
22 System Clocks: auxiliary circuits disabled, but all other digital circuits (including the Main Clock PLL) enabled.
23 May be further reduced by power-saving unused sections
24 Characteristics when driving the XTAL/CLK pin with an external clock source.
25 Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor as shown in Figure 2.
26 At power-on, SYSCLK1 defaults to XTAL out, 19.2MHz, so will consume 250/4 * 19.2µA = 1.2mA

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AC Parameters		Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input						
'High' Pulse Width		31	15	–	–	ns
'Low' Pulse Width		31	15	–	–	ns
Input Impedance (at 6.144MHz)						
Powered-up	Resistance		–	150	–	kΩ
	Capacitance		–	20	–	pF
Powered-down	Resistance		–	300	–	kΩ
	Capacitance		–	20	–	pF
Xtal Start-up Time (from powersave)			–	20	–	ms
System Clk 1/2 Outputs						
XTAL/CLK input to CLOCK_OUT timing:						
(in high to out high)		32	–	15	–	ns
(in low to out low)		32	–	15	–	ns
'High' Pulse Width		33	76	81.38	87	ns
'Low' Pulse Width		33	76	81.38	87	ns
V_{BIAS}						
Start-up Time (from powersave)			–	30	–	ms
Microphone, Alternative and Discriminator Inputs (MIC, ALT, DISC)						
Input Impedance		34	–	>10	–	MΩ
Maximum Input Level (pk-pk)		35	–	–	80%	AV_{DD}
Load Resistance (feedback pins)			80	–	–	kΩ
Amplifier Open Loop Voltage Gain						
(I/P = 1mVrms at 100Hz)			–	80	–	dB
Unity Gain Bandwidth			–	1.0	–	MHz
Programmable Input Gain Stage		36				
Gain (at 0dB)		37	−0.5	0	+0.5	dB
Cumulative Gain Error						
(wrt attenuation at 0dB)		37	−1.0	0	+1.0	dB

Notes:
31 Timing for an external input to the XTAL/CLK pin.
32 XTAL/CLK input driven by an external source.
33 6.144MHz XTAL fitted and 6.144MHz output selected (scale for 19.2MHz).

34 With no external components connected, measured at DC.

35 Centred about $AV_{DD}/2$; after multiplying by the gain of input circuit (with external components connected).

36 Gain applied to signal at output of buffer amplifier: DISCFB, ALTFB or MICFB.

37 Design Value. Overall attenuation input to output has a tolerance of 0dB ±1.0dB.

AC Parameters	Notes	Min.	Typ.	Max.	Unit
Modulator Outputs 1/2 and Audio Output (MOD 1, MOD 2, AUDIO)					
Power-up to Output Stable	41	–	50	100	µs
Modulator Attenuators					
Attenuation (at 0dB)	43	−1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		−0.6	0	+0.6	dB
Output Impedance ⎫ Enabled	42	–	600	–	Ω
Output Impedance ⎭ Disabled	42	–	500	–	kΩ
Output Current Range (AV_{DD} = 3.3V)		–	–	±125	µA
Output Voltage Range	44	0.5	–	AV_{DD} –0.5	V
Load Resistance		20	–	–	kΩ
Audio Attenuator					
Attenuation (at 0dB)	43	−1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		−1.0	0	+1.0	dB
Output Impedance ⎫ Enabled	42	–	600	–	Ω
Output Impedance ⎭ Disabled	42	–	500	–	kΩ
Output Current Range (AV_{DD} = 3.3V)		–	–	±125	µA
Output Voltage Range	44	0.5	–	AV_{DD} –0.5	V
Load Resistance		20	–	–	kΩ

Notes:
41 Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the XTAL and C-BUS interface, to be in placed in powersave mode.
42 Small signal impedance, at AV_{DD} = 3.3 V and T_{AMB} = 25°C.
43 With respect to the signal at the feedback pin of the selected input port.
44 Centred about $AV_{DD}/2$; with respect to the output driving a 20kΩ load to $AV_{DD}/2$.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Auxiliary Signal Inputs (Aux ADC 1 to 4)					
Source Output Impedance	51	–	–	24	kΩ
Auxiliary 10 Bit ADCs					
Resolution		–	10	–	Bits
Maximum Input Level (pk-pk)	54	–	–	80%	AV_{DD}
Conversion Time	52	–	250	–	µs
Input Impedance					
Resistance	57	–	>10	–	MΩ
Capacitance		–	5	–	pF
Zero Error	55	0	–	±10	mV
Integral Non-linearity		–	–	±3	LSBs
Differential Non-linearity	53	–	–	±1	LSBs
Auxiliary 10 Bit DACs					
Resolution		–	10	–	Bits
Maximum Output Level (pk-pk), no load	54	80%	–	–	AV_{DD}
Zero Error	56	0	–	±10	mV
Resistive Load		5	–	–	kΩ
Integral Non-linearity		–	–	±4	LSBs
Differential Non-linearity	53	–	–	±1	LSBs

Notes:
51 Denotes output impedance of the driver of the auxiliary input signal, to ensure <1 bit additional error under nominal conditions.
52 With an auxiliary clock frequency of 6.144MHz.
53 Guaranteed monotonic with no missing codes.
54 Centred about $AV_{DD}/2$.
55 Input offset from a nominal V_{BIAS} input, which produces a $0200 ADC output.
56 Output offset from a $0200 DAC input, measured with respect to nominal V_{BIAS} output.
57 Measured at dc.

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7.1.4 Parametric Performance

For the following conditions unless otherwise specified:

External components as recommended in Figure 2 and Figure 3. Maximum load on digital outputs = 30 pF.

Oscillator Frequency = 19.2MHz ±0.0002% (2ppm); T_{AMB} = −40°C to +85°C.

AV_{DD} = DV_{DD} = 3.0 V to 3.6 V. Reference Signal Level = 308mVrms at 1kHz with AV_{DD} = 3.3V.

Signal levels track with supply voltage, so scale accordingly.

Signal-to-Noise Ratio (SNR) in bit rate bandwidth.

Input stage gain = 0 dB, Output stage attenuation = 0 dB.

All figures quoted in this section apply to the device when loaded with FI-2.x only. The use of other CMX7241/7341 Function Images can modify the parametric performance of the device.

DMR Modem	Notes	Min.	Typ.	Max.	Unit
Modem Symbol Rate		–	4800	–	sym/s
Modulation			4FSK		
Filter (RC) Alpha		–	0.2	–	
Tx Output Level (MOD1, MOD2, two-point)	60	–	2.88	–	Vpk-pk
Tx Output Level (MOD1, MOD2, I/Q)	60	–	2.20	–	Vpk-pk
Tx Adjacent Channel Power (MOD1, MOD2, prbs)	61, 63	-60	–	–	dB
Rx Co-channel Rejection	61, 63	15	12	–	dB
Rx Input Level		–	–	838	mVrms
Rx Input DC Offset		0.5	–	AV_{DD}-0.5	V

Notes:

60 Transmitting continuous default preamble.

61 See user manual section 6.20

62 Measured at baseband – radio design will affect ultimate product performance.

63 For a 12.5kHz/9.6 kbps channel.

Analogue I/Q Performance	Notes	Min.	Typ.	Max.	Unit
Rx Sensitivity (12dB SINAD)	74,75	–	-122	–	dBm
Rx Adjacent Channel Rejection	74,75		47.5	–	dB
Rx Adjacent Channel Rejection	75,76	–	69		dB
Rx Alternate Channel Rejection	75,76		71		dB
Rx Blocking	74,75		95		dB
Rx Intermodulation	75,76	–	67		dB

Audio Performance	Notes	Min.	Typ.	Max.	Unit
Audio Tone Generator					
Frequency Range		288	–	3000	Hz
Tone Frequency Accuracy		–	–	±0.3	%
Tone Amplitude Tolerance	81	–1.0	0	+1.0	dB
Total Harmonic Distortion	80	–	2.0	4.0	%
Analogue Channel Audio Filtering					
Pass-band (nominal bandwidth):					
12.5kHz Channel	83	300	–	2550	Hz
25kHz Channel	83	300	–	3000	Hz
Pass-band Gain (at 1.0kHz)		–	0	–	dB
Pass-band Ripple (wrt gain at 1.0kHz)		–2.0	0	+0.5	dB
Stop-band Attenuation		33.0	–	–	dB
Residual Hum and Noise Tx	84	–	–47	–	dBm
Residual Hum and Noise Rx	84	–	–44	–	dBm
Pre-emphasis	83	–	+6	–	dB/oct
De-emphasis	83	–	–6	–	dB/oct

CTCSS Detector	Notes	Min.	Typ.	Max.	Unit
SINAD Opening	74	–	4	–	dB
Sensitivity	74	–	−124	–	dBm
Response Time (Composite Signal)	73	–	225	250	ms
Dropout Immunity	73	–	160	–	ms
Falsing	73	–	1	–	
Frequency Range		60	–	260	Hz
Tone Frequency Accuracy		–	–	±0.3	%
Tone Amplitude Tolerance	81	−1.0	0	+1.0	dB
Total Harmonic Distortion		–	2.0	4.0	%

CTCSS Encoder	Notes	Min.	Typ.	Max.	Unit
Frequency Range		60.0	–	260	Hz
Tone Frequency Accuracy		–	–	±0.3	%
Tone Amplitude Tolerance	81	−1.0	0	+1.0	dB
Total Harmonic Distortion	82	–	2.0	4.0	%

DCS Decoder	Notes	Min.	Typ.	Max.	Unit
SINAD Opening			10		dB
Sensitivity		–	–	–	
Response Time (Composite Signal)		–	295	–	ms
Bit-Rate Sync Time		–	2	–	edges
Bit Rate		–	134.4	–	bps
Amplitude Tolerance		−1.0	0	+1.0	dB

DCS Encoder	Notes	Min.	Typ.	Max.	Unit
Bit Rate		–	134.4	–	bps
Amplitude Tolerance	81	−1.0	0	+1.0	dB

Selcall Tone Detector	Notes	Min.	Typ.	Max.	Unit
Sensitivity	(Pure Tone)	–	–26	–	dB
Response Time	(Good Signal)	–	35	–	ms
De-response Time	(Good Signal)	–	–	45	ms
Drop-out Immunity		–	–	20	ms
Frequency Range		288	–	3000	Hz

Selcall Tone Encoder		Min.	Typ.	Max.	Unit
Frequency Range		288	–	3000	Hz
Tone Frequency Accuracy		–	–	±0.3	%
Tone Amplitude Tolerance		–1.0	0	+1.0	dB
Total Harmonic Distortion		–	2.0	4.0	%

DTMF Decoder	Notes	Min.	Typ.	Max.	Unit
Sensitivity		–	-22	+3	dB
Response Time		–	35	–	ms
De-response Time		–	–	45	ms
Falsing Rate (per 30min Voice input)		–	10	–	
Frequency Tolerance		–	±2.5	–	%
Twist		-10	–	+10	dB

DTMF Encoder	Notes	Min.	Typ.	Max.	Unit
Output Signal Level (2dB twist)		–	360	775	mVrms
Output Level Variation					dB
Output Distortion		–	–	5	%

FFSK Modem	Notes	Min.	Typ.	Max.	Unit
Modem Symbol Rate		–	1200/2400	–	symbols/s
Logic 1 frequency		1198	1200	1202	Hz
Logic 0 frequency – 1200 baud		1798	1800	1802	Hz
Logic 0 frequency – 2400 baud		2398	2400	2402	Hz
Isochronous Distortion (0 to 1 and 1 to 0)		–	–	40	µs
3rd Harmonic Distortion		–	–	3	%
Rx Co-channel Rejection	70, 72	15	12	–	dB
Bit Error Rate (SNR = 20dB)	73	–	<1	–	10^{-8}
Probability of bit 16 being correct		–	>99.9	–	%

Notes:

70 Transmitting continuous default preamble.

72 For a 12.5kHz channel.

73 Combined performance of CMX7241/CMX7341 and CMX994 connected as shown in Figure 6 using EV9942 and PE0403 measurement method from EN 301 166.

74 Test Method TIA-603-C.

75 For a 12.5kHz channel; Combined performance of CMX7241/CMX7341 and CMX994 connected as shown in Figure 6 using EV9942 and PE0201.

76 Test Method EN 300 086.

80 Measured at MOD 1 or MOD 2 output.

81 AV_{DD} = 3.3V and Tx Sub-Audio Level set to 88mV p-p (31mVrms).

83 See Figure 28 and Figure 29.

85 Internal signal.

7.2 C-BUS Timing

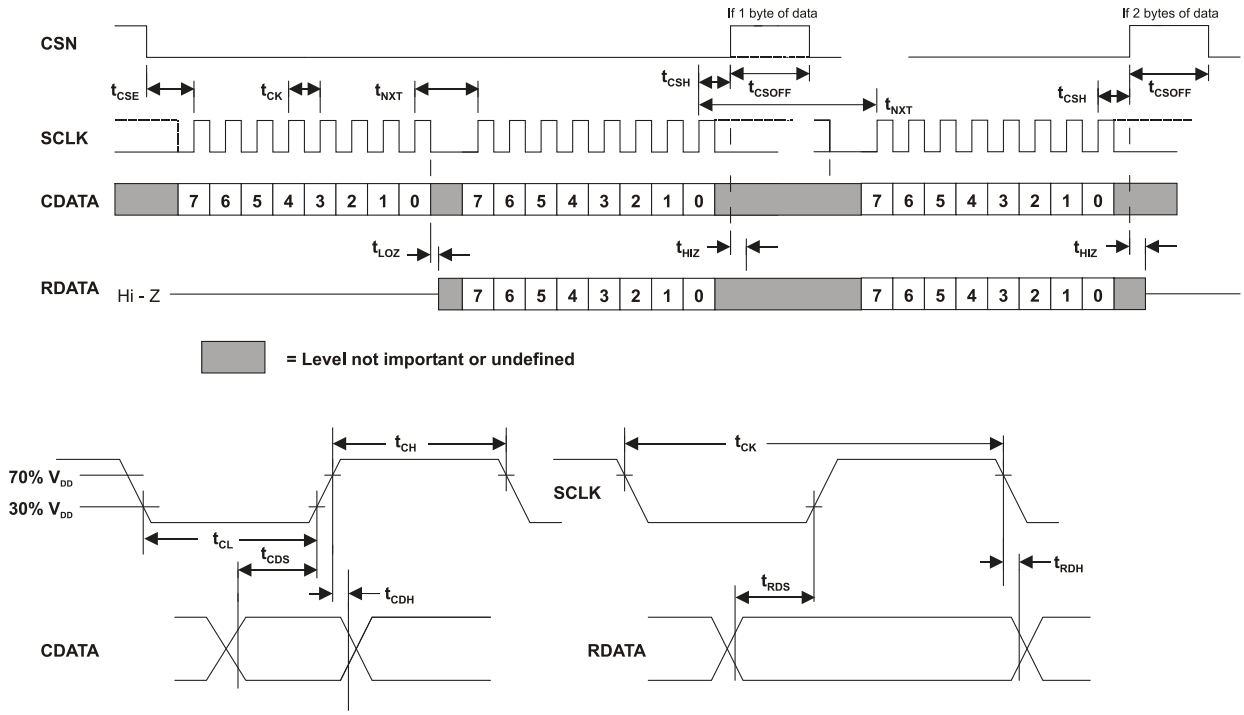


Figure 38 C-BUS Timing

C-BUS Timing		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	CSN Enable to SCLK high time		100	–	–	ns
t_{CSH}	Last SCLK high to CSN high time		100	–	–	ns
t_{LOZ}	SCLK low to RDATA Output Enable Time		0.0	–	–	ns
t_{HIZ}	CSN high to RDATA high impedance		–	–	1.0	µs
t_{CSOFF}	CSN high time between transactions		1.0	–	–	µs
t_{NXT}	Inter-byte time		0	–	–	ns
t_{CK}	SCLK frequency		-	–	10	MHz
t_{CH}	SCLK high time		50	–	–	ns
t_{CL}	SCLK low time		50	–	–	ns
t_{CDS}	CDATA setup time		75	–	–	ns
t_{CDH}	CDATA hold time		25	–	–	ns
t_{RDS}	RDATA setup time		50	–	–	ns
t_{RDH}	RDATA hold time		0	–	–	ns

Notes: 1. Depending on the command, 1 or 2 bytes of CDATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. RDATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.

2. Data is clocked into the peripheral on the rising SCLK edge.

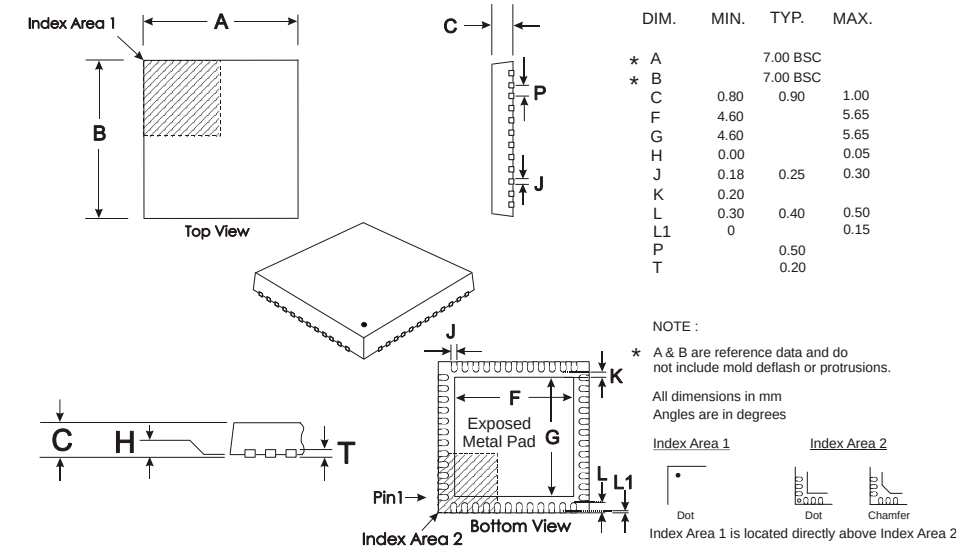
3. Commands are acted upon at the end of each command (rising edge of CSN).

4. To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with SCLK pulses starting and ending at either polarity.

5. Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than earlier C-BUS timing specification. The CMX7241/7341 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

7.3 Packaging.



Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 39 Mechanical Outline of 48-lead VQFN (Q3)

Order as part no. CMX7241Q3 or CMX7341Q3

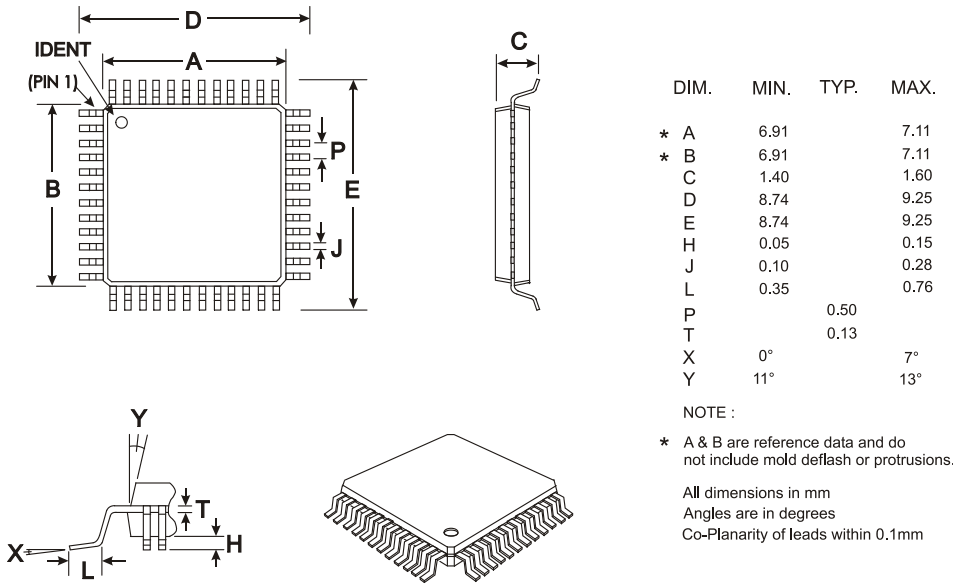


Figure 40 Mechanical Outline of 48-pin LQFP (L4)

Order as part no. CMX7241L4

As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the About Us/Packaging Information page of the CML website: [www.cmlmicro.com].

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