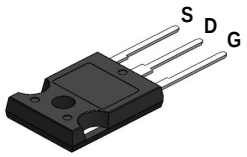
RoHS HAL PB Green

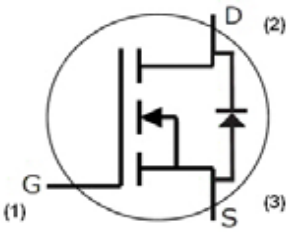
Silicon Carbide Power MOSFET N-Channel Enhancement Mode

Features

- 3rd generation SiC MOSFET technology
- High blocking voltage with low on-resistance
- High speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant



TO-247-3



ORDERING INFORMATION

HT120N650ADZ

T_A = -40° to 175° C for all packages

Typical Applications

- EV charging
- Solar PV inverters
- UPS
- SMPS
- DC/DC converters

Benefits

- Higher system efficiency
- Reduced cooling requirements
- Increased power density
- Increased system switching frequency
- Easy to parallel and simple to drive
- Enable new hard switching PFC topologies (Totem-Pole)

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			650	V	T_C = 25°C	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+19		Transient	
Operational Gate-Source Voltage	$V_{GS\,op}$		-4/15			Static	Note 1
DC Continuous Drain Current	I_D			120	A	V_{GS} = 15 V, T_C = 25 °C, T_J ≤175 °C	Fig. 19 Note 2
				96		V_{GS} = 15 V, T_C = 100 °C, T_J ≤175 °C	
Pulsed Drain Current	I_{DM}			418		t_{Pmax} limited by T_{jmax} V_{GS} = 15V, T_C = 25 °C	Fig. 22
Power Dissipation	P_D			416	W	T_C = 25 °C, T_J = 175 °C	Fig. 20
Operating Junction and Storage Temperature	T_J, T_{stg}			-40 to +175	°C		
Solder Temperature	T_L			260		According to JEDEC J-STD-020	
Mounting Torque	M_D			1 8.8	Nm lbf-in	M3 or 6-32 screw	

Note (1): Recommended turn-on gate voltage is 15V with ±5% regulation tolerance, see Application Note PRD-04814 for additional details
Note (2): Verified by design

Electrical Characteristics (T_C = 25 °C Unless Otherwise Specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	650			V	V_{GS} = 0 V, I_D = 100 µA	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.3	3.6		V_{DS} = V_{GS}, I_D = 15.5 mA	Fig. 11
			1.9			V_{DS} = V_{GS}, I_D = 15.5 mA, T_J = 175 °C	
Zero Gate Voltage Drain Current	I_{DSS}		1	50	µA	V_{DS} = 650 V, V_{GS} = 0 V	
Gate-Source Leakage Current	I_{GSS}		10	250	nA	V_{GS} = 15 V, V_{DS} = 0 V	
Drain-Source On-State Resistance	$R_{DS(on)}$	10.5	15	21	mΩ	V_{GS} = 15 V, I_D = 55.8 A	Fig. 4,5,6
			20			V_{GS} = 15 V, I_D = 55.8 A, T_J = 175 °C	
Transconductance	g_{fs}		42		S	V_{DS} = 20 V, I_{DS} = 55.8 A	Fig. 7
			40			V_{DS} = 20 V, I_{DS} = 55.8 A, T_J = 175 °C	
Input Capacitance	C_{iss}		5011		pF	V_{GS} = 0 V, V_{DS} = 400 V f = 100 khz V_{AC} = 25 mV	Fig. 17,18
Output Capacitance	C_{oss}		289				
Reverse Transfer Capacitance	C_{rss}		31				
Effective Output Capacitance (Energy Related)	$C_{o(er)}$		357				Note 3
Effective Output Capacitance (Time Related)	$C_{o(tr)}$		516				
C_{oss} Stored Energy	E_{oss}		29		µJ		Fig. 16
Turn-On Switching Energy (Body Diode)	E_{ON}		1500		µJ	V_{DS} = 400 V, V_{GS} = -4 V/15 V, I_D = 55.8 A, $R_{G(ext)}$ = 5 Ω, L = 57.6 µH, T_J = 175 °C FWD = Internal Body Diode of MOSFET	Fig. 25
Turn Off Switching Energy (Body Diode)	E_{OFF}		700				
Turn-On Switching Energy (External Diode)	E_{ON}		1200		µJ	V_{DS} = 400 V, V_{GS} = -4 V/15 V, I_D = 55.8 A, $R_{G(ext)}$ = 5 Ω, L = 57.6 µH, T_J = 175 °C FWD = External SiC DIODE	Fig. 25
Turn Off Switching Energy (External Diode)	E_{OFF}		1000				
Turn-On Delay Time	$t_{d(on)}$		22		ns	V_{DD} = 400 V, V_{GS} = -4 V/15 V I_D = 55.8 A, $R_{G(ext)}$ = 5 Ω, L = 57.6 µH Timing Relative to V_{DS} Inductive Load	Fig. 26
Rise Time	t_r		125				
Turn-Off Delay Time	$t_{d(off)}$		58				
Fall Time	t_f		25				
Internal Gate Resistance	$R_{G(int)}$		1.5		Ω	f = 1 MHz, V_{AC} = 25 mV	
Gate to Source Charge	Q_{gs}		54		nC	V_{DS} = 400 V, V_{GS} = -4 V/15 V I_D = 55.8 A Per IEC60747-8-4 pg 21	Fig. 12
Gate to Drain Charge	Q_{gd}		62				
Total Gate Charge	Q_g		188				

Note (3): $C_{o(er)}$, a lumped capacitance that gives same stored energy as coss while V_{DS} is rising from 0 to 400 V.
$C_{o(tr)}$, a lumped capacitance that gives same charging time as coss while V_{DS} is rising from 0 to 400 V.

Reverse Diode Characteristics

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Note
Diode Forward Voltage	V_{SD}	4.7		V	V_{GS} = -4 V, I_{SD} = 27.9 A, T_J = 25 °C	Fig. 8, 9, 10
		4.2			V_{GS} = -4 V, I_{SD} = 27.9 A, T_J = 175 °C	
Continuous Diode Forward Current	I_S		79	A	V_{GS} = -4 V, T_C= 25 °C	
Diode Pulse Current	I_{SM}		418		V_{GS} = -4 V, Pulse Width t_P Limited by T_{jmax}	
Reverse Recovery Time	t_{rr}	85		ns	V_{GS} = -4 V, I_{SD} = 55.8 A , V_R = 400 V dif/dt = 1500 A/µs, T_J = 175 °C	
Reverse Recovery Charge	Q_{rr}	667		nC		
Peak Reverse Recovery Current	I_{rrm}	17		A		
Reverse Recovery Time	t_{rr}	74		ns	V_{GS} = -4 V, I_{SD} = 55.8 A , V_R = 400 V dif/dt = 1000 A/µs, T_J = 175 °C	
Reverse Recovery Charge	Q_{rr}	562		nC		
Peak Reverse Recovery Current	I_{rrm}	14		A		

Thermal Characteristics

Parameter	Symbol	Typ.	Unit	Test Conditions	Note
Thermal Resistance from Junction to Case	$R_{\theta JC}$	0.35	°C/W		Fig. 21
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	40			

Typical Performance

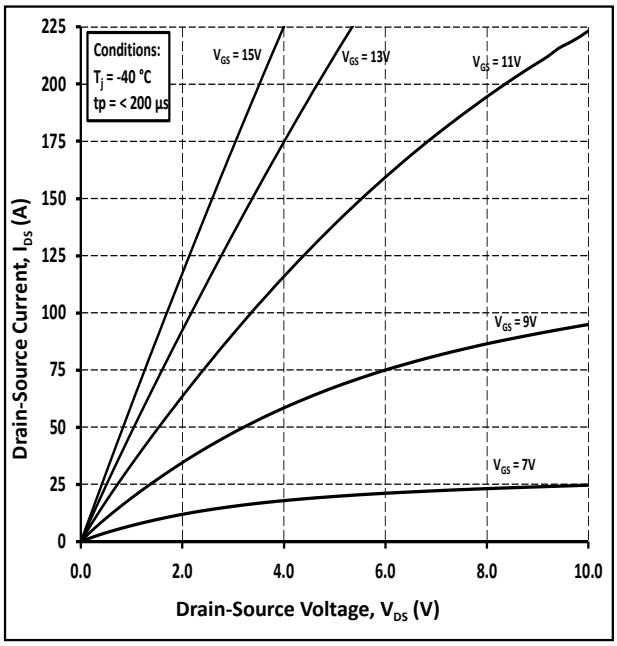


Figure 1. Output Characteristics T_J = -40 °C

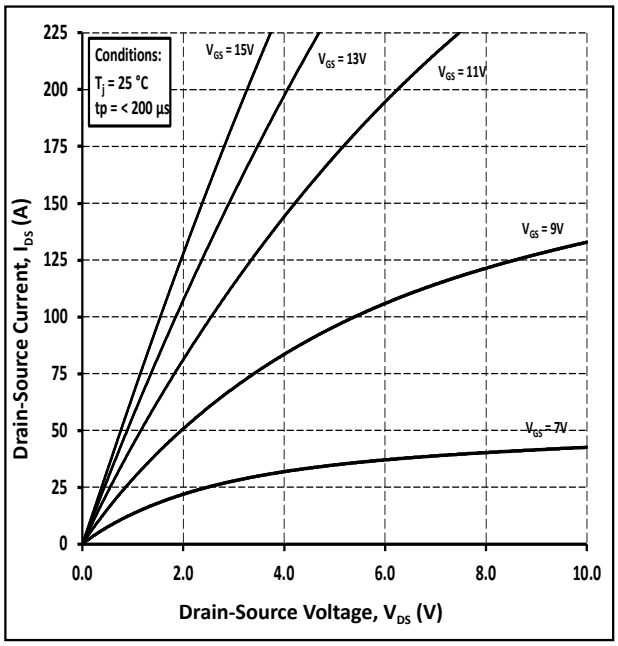


Figure 2. Output Characteristics T_J = 25 °C

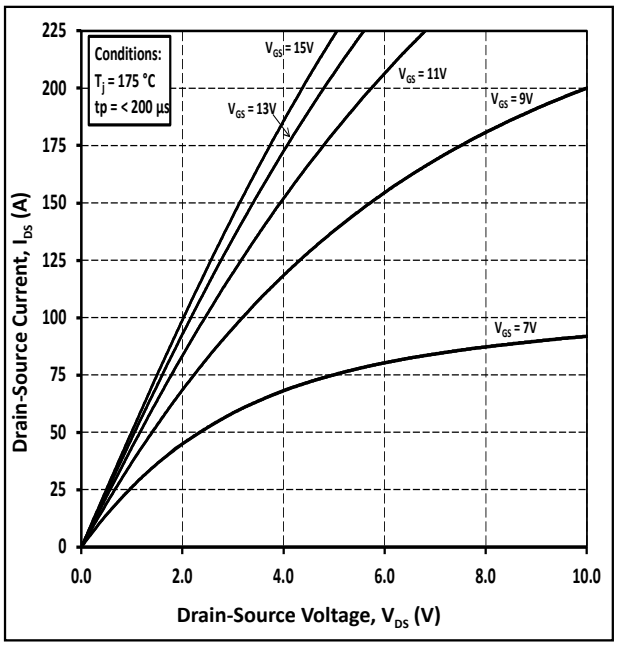


Figure 3. Output Characteristics T_J = 175 °C

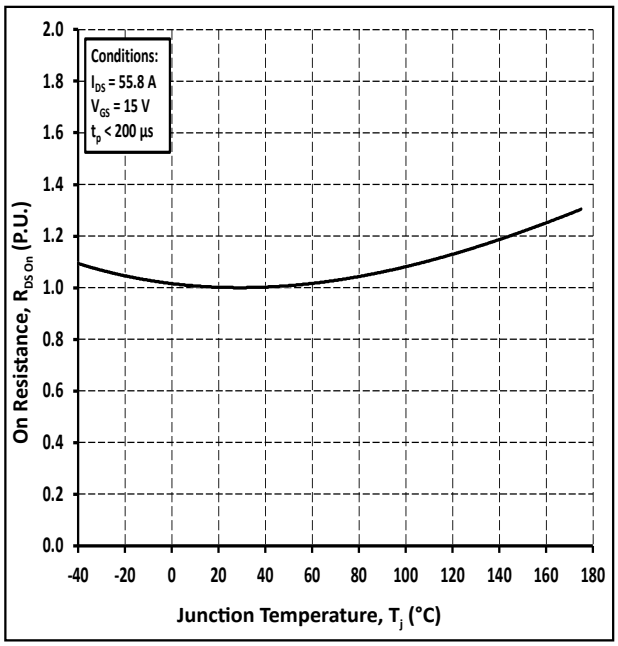


Figure 4. Normalized On-Resistance vs Temperature

Typical Performance

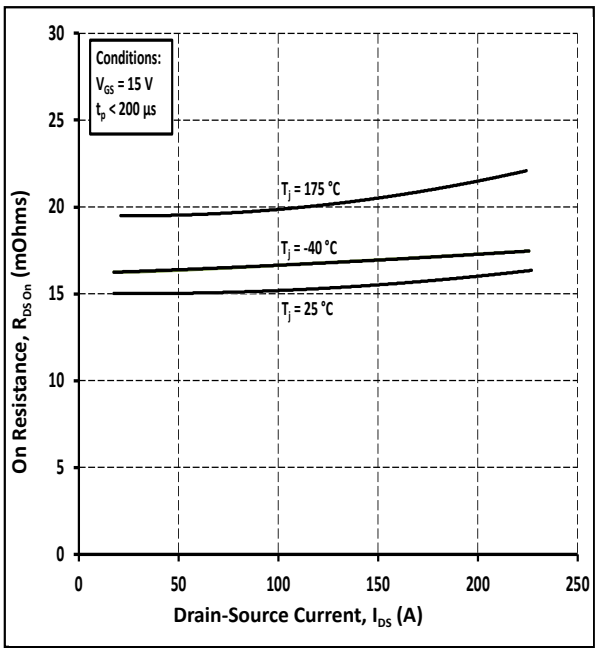


Figure 5. On-Resistance vs Drain Current for Various Temperatures

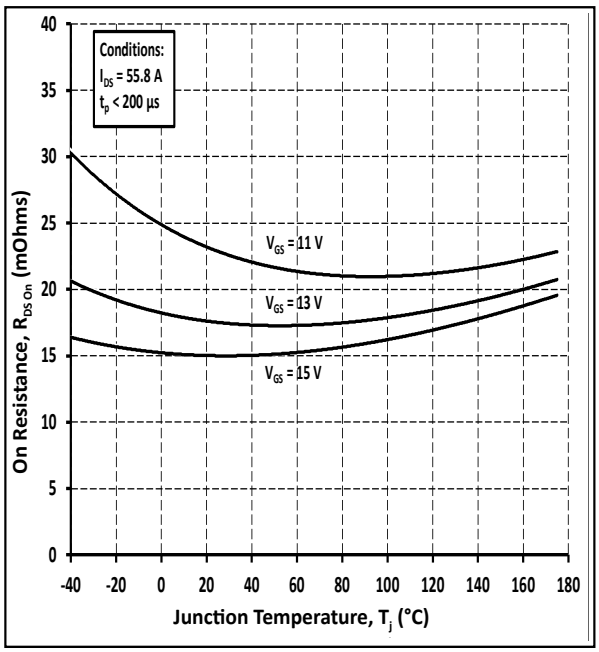


Figure 6. On-Resistance vs Temperature for Various Gate Voltage

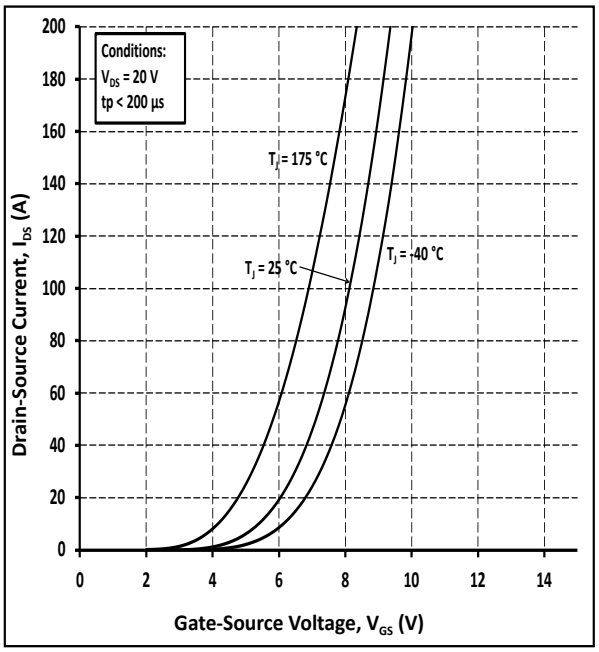


Figure 7. Transfer Characteristic for Various Junction Temperatures

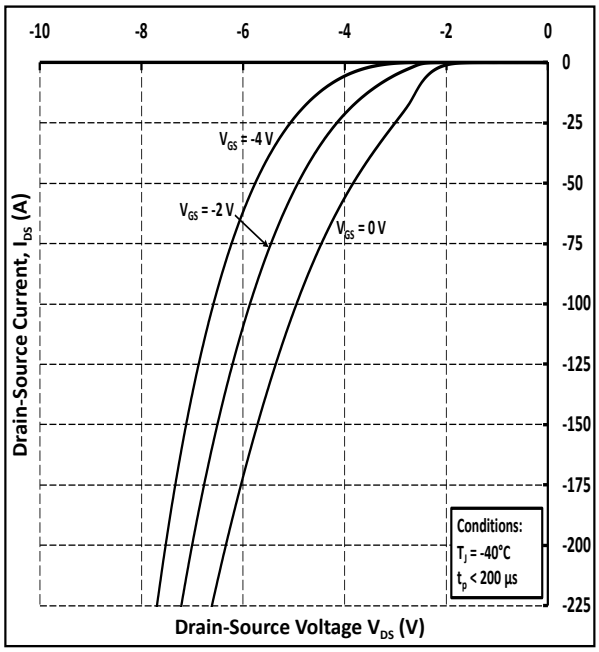


Figure 8. Body Diode Characteristic at -40 °C

Typical Performance

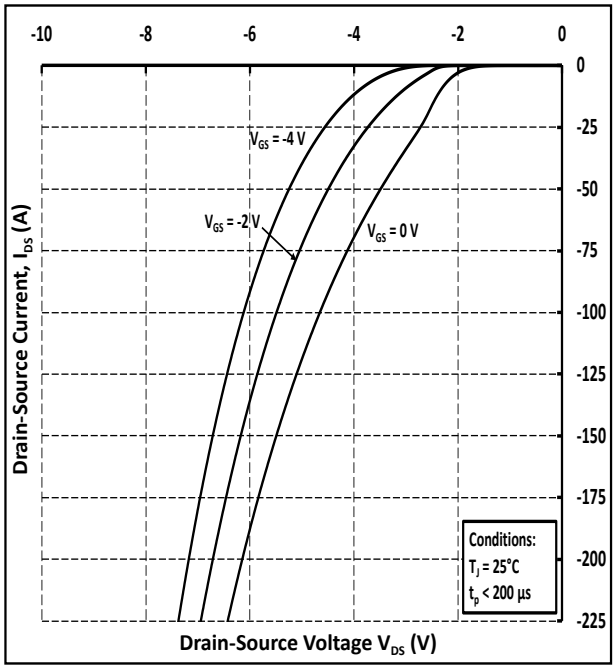


Figure 9. Body Diode Characteristic at 25 °C

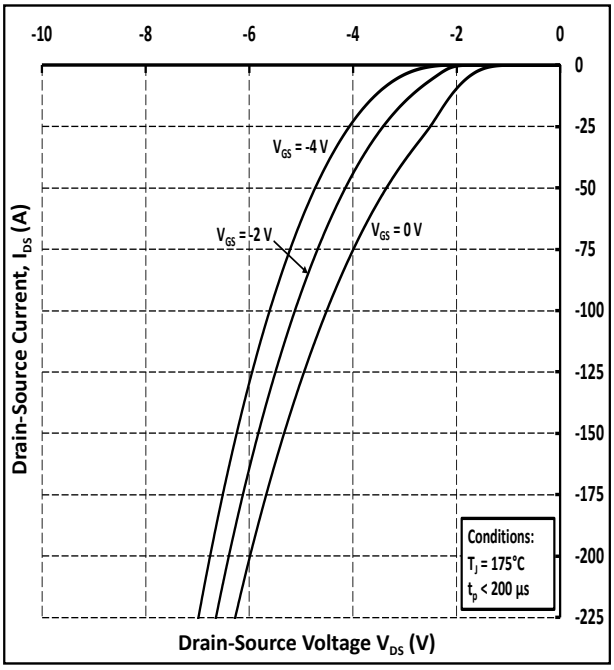


Figure 10. Body Diode Characteristic at 175 °C

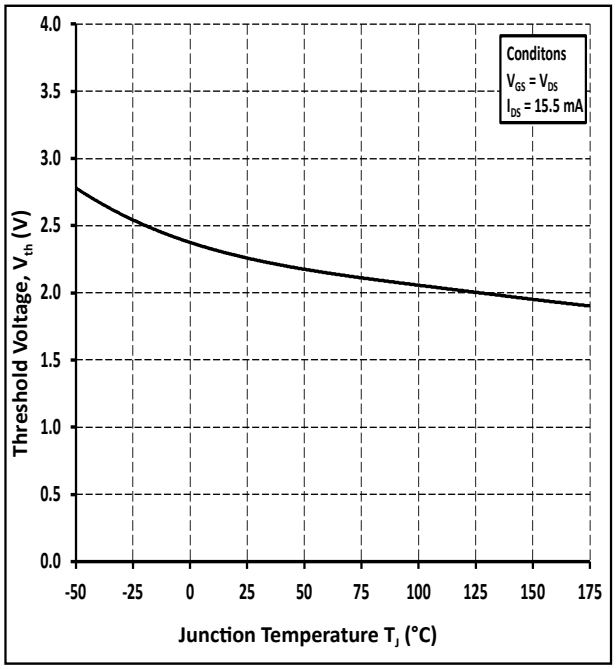


Figure 11. Threshold Voltage vs Temperature

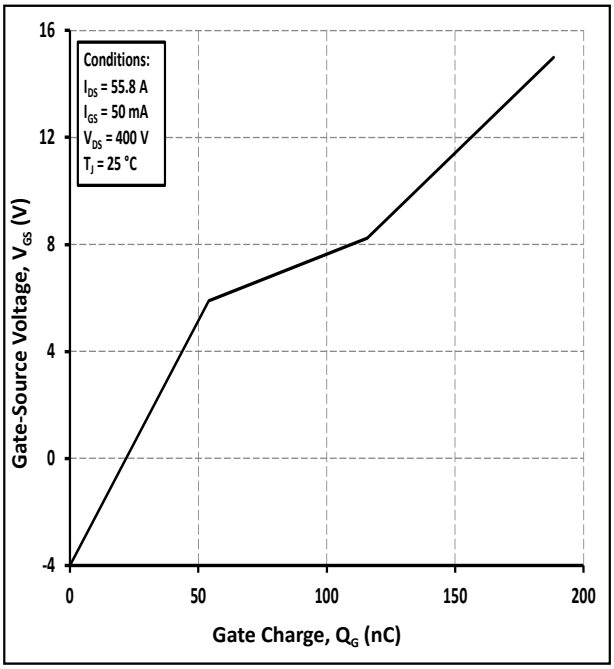


Figure 12. Gate Charge Characteristic

Typical Performance

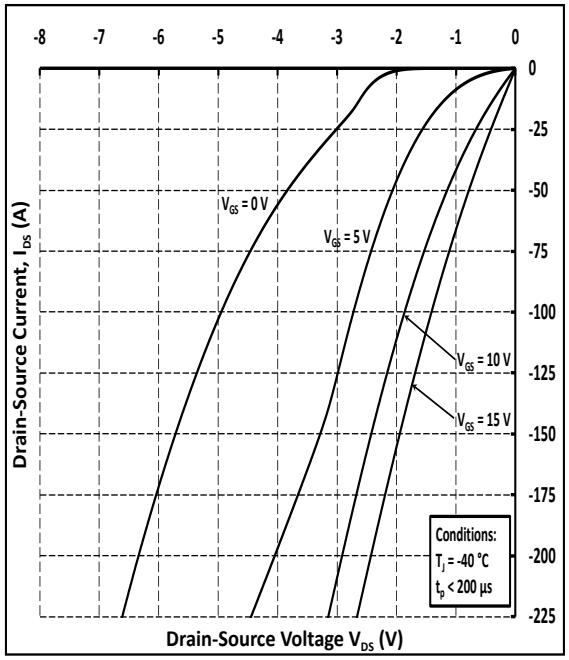


Figure 13. 3rd Quadrant Characteristic at -40 °C

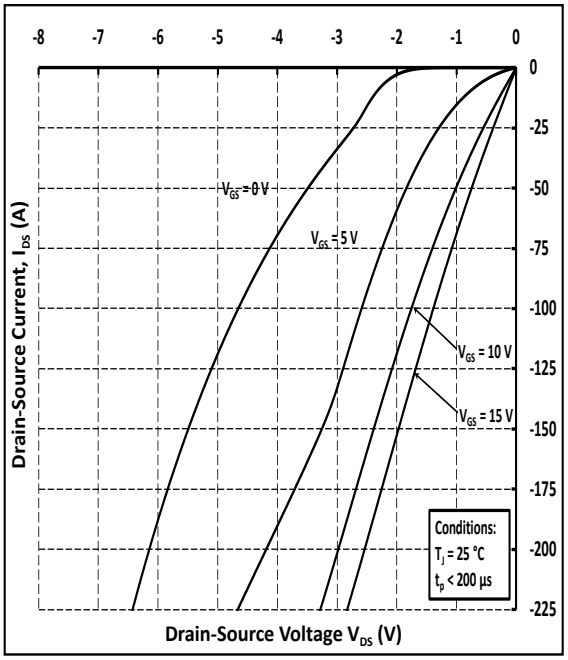


Figure 14. 3rd Quadrant Characteristic at 25 °C

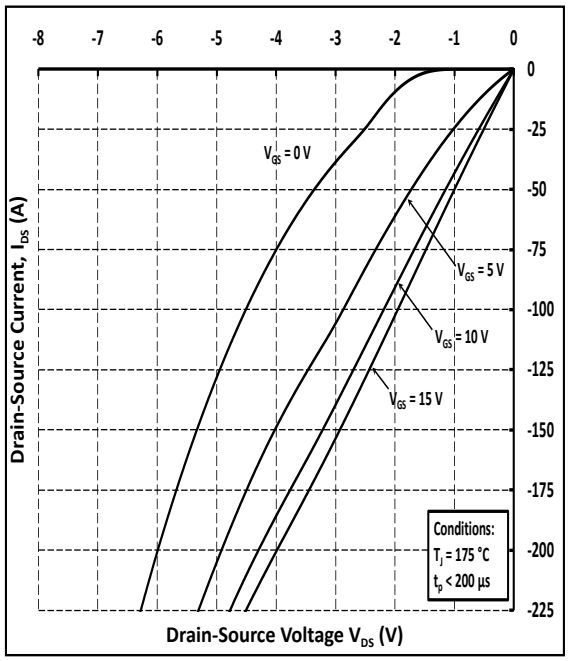


Figure 15. 3rd Quadrant Characteristic at 175 °C

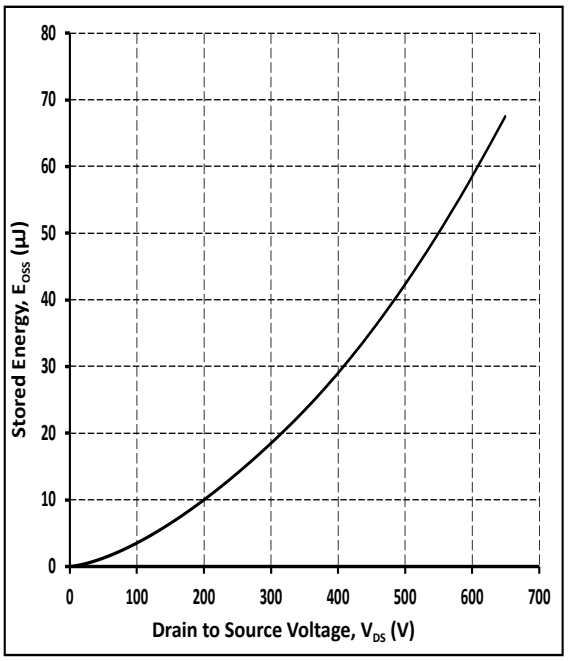


Figure 16. Output Capacitor Stored Energy

Typical Performance

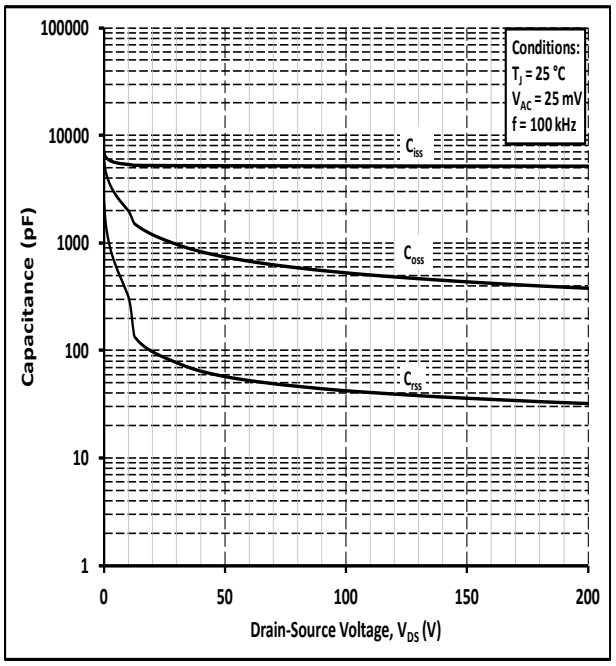


Figure 17. Capacitances vs Drain-Source Voltage (0-200 V)

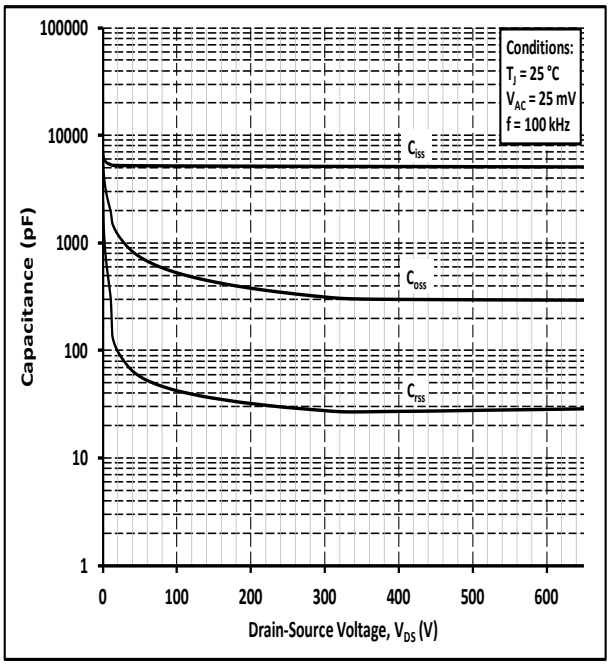


Figure 18. Capacitances vs Drain-Source Voltage (0-650 V)

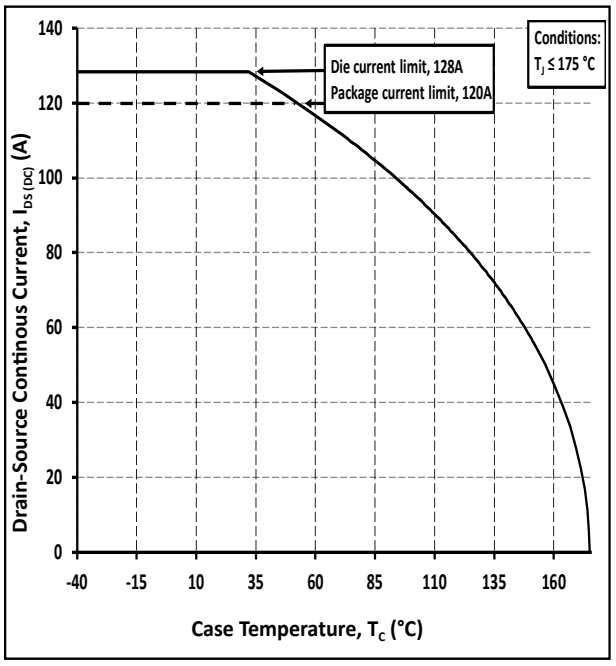


Figure 19. Continuous Drain Current Derating vs Case Temperature

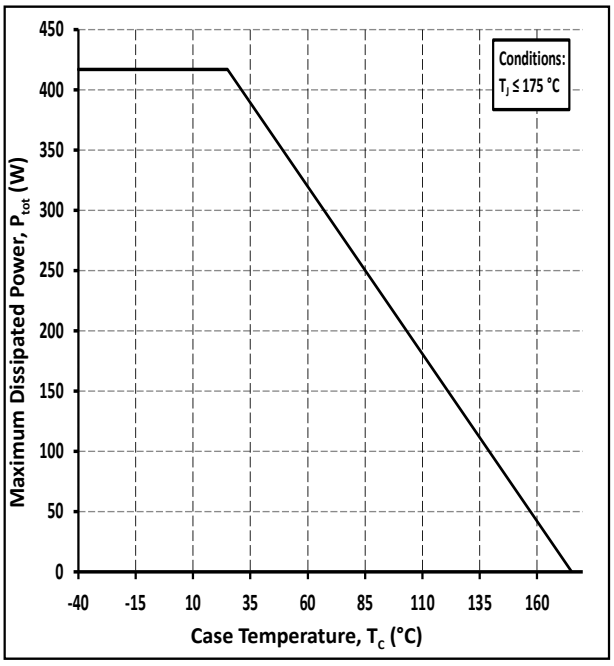


Figure 20. Maximum Power Dissipation Derating vs Case Temperature

Typical Performance

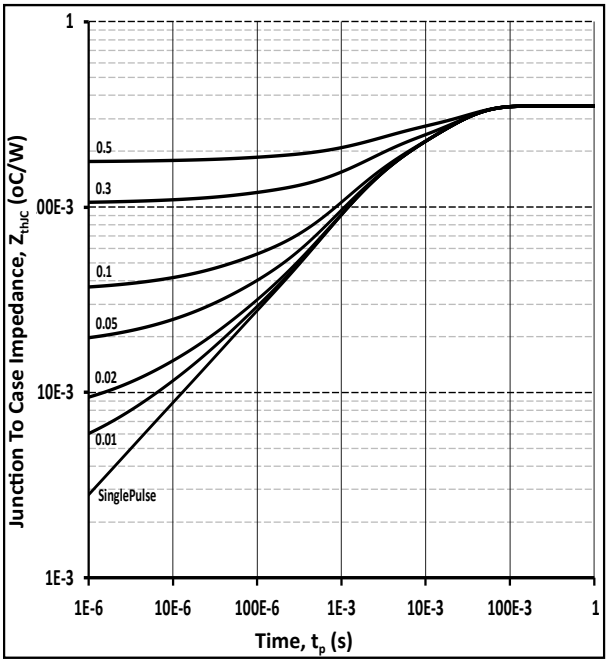


Figure 21. Transient Thermal Impedance (Junction - Case)

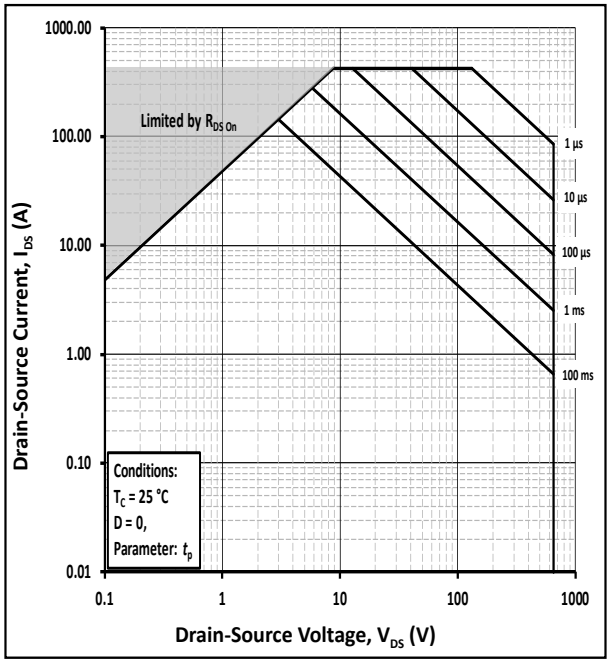


Figure 22. Safe Operating Area

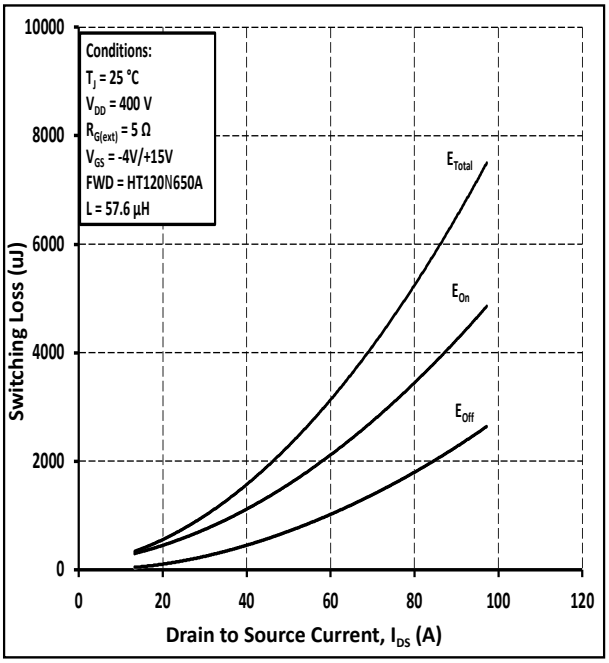


Figure 23. Clamped Inductive Switching Energy vs Drain Current (V_{DD} = 400 V)

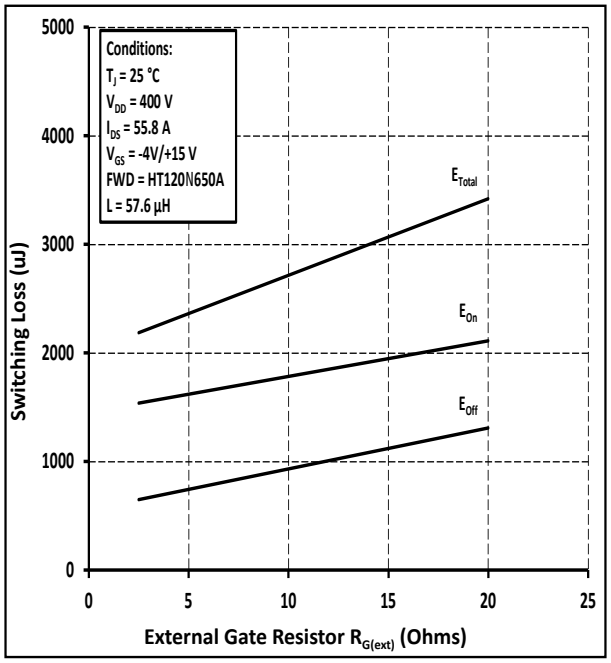


Figure 24. Clamped Inductive Switching Energy vs $R_{G(ext)}$

Typical Performance

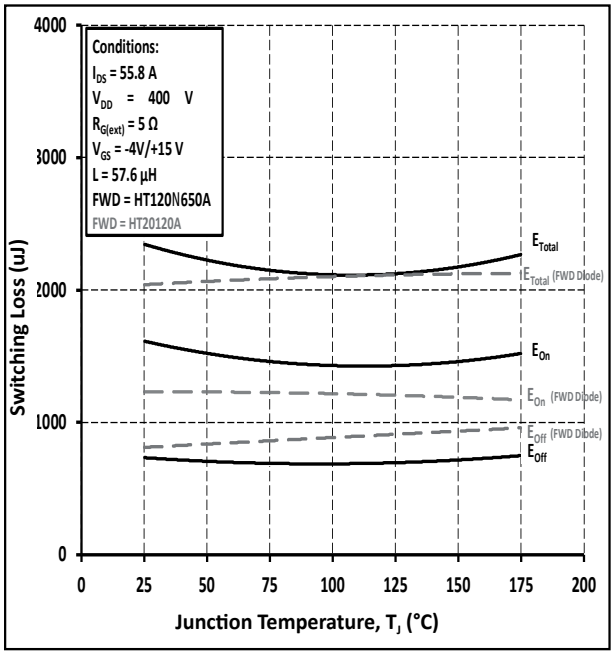


Figure 25. Clamped Inductive Switching Energy vs Temperature

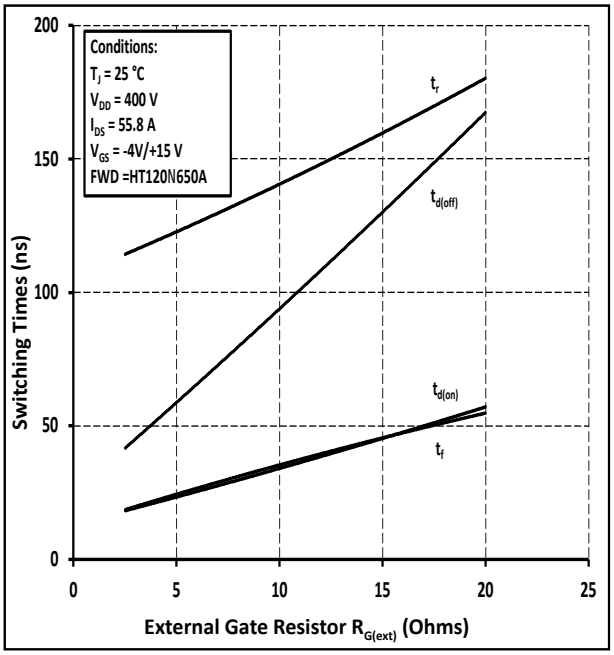


Figure 26. Switching Times vs $R_{G(ext)}$

Test Circuit Schematic

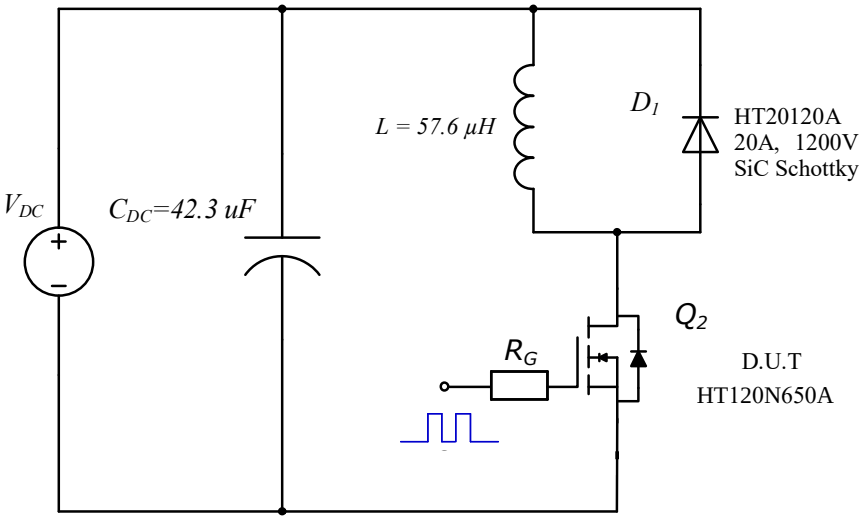


Figure 27. Clamped Inductive Switching Waveform Test Circuit

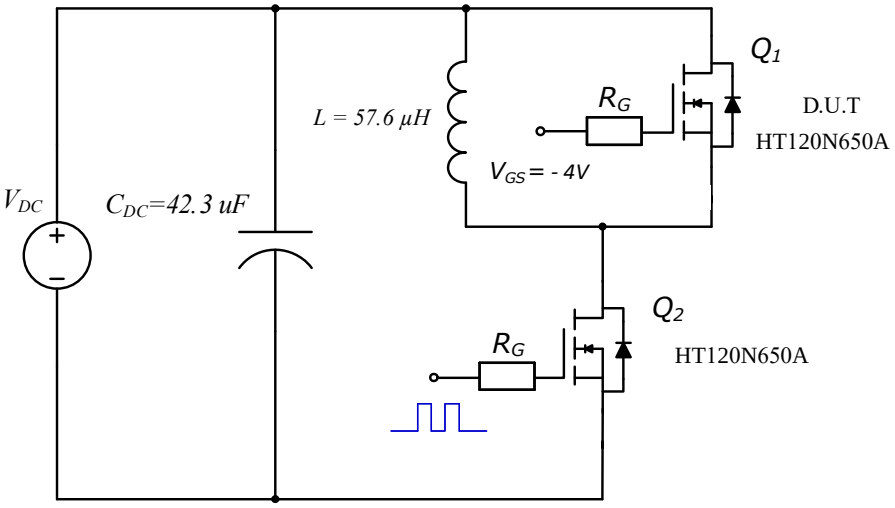
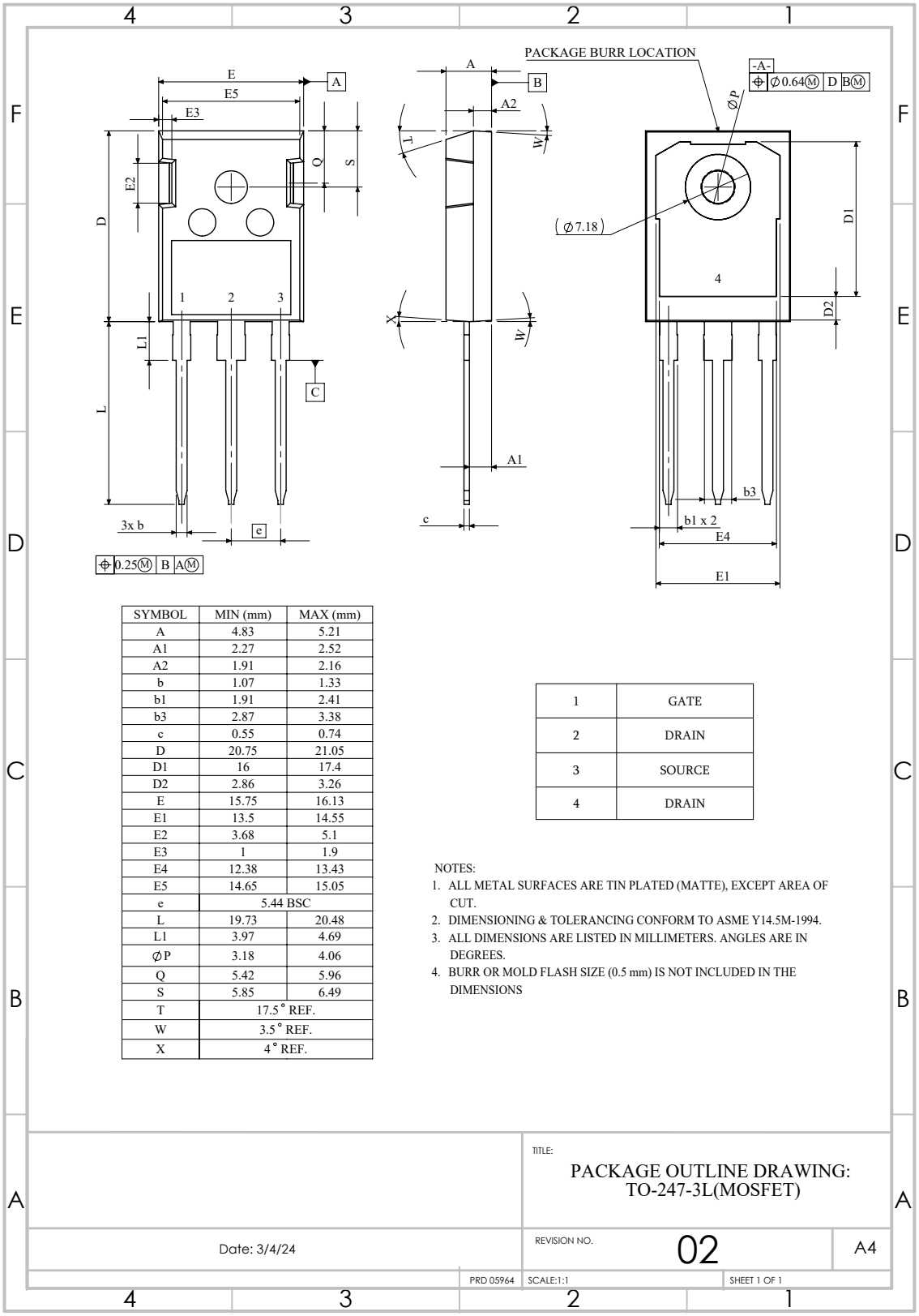


Figure 28. Body Diode Recovery Test Circuit

Package Dimensions

Package: TO-247-3



SYMBOL	MIN (mm)	MAX (mm)
A	4.83	5.21
A1	2.27	2.52
A2	1.91	2.16
b	1.07	1.33
b1	1.91	2.41
b3	2.87	3.38
c	0.55	0.74
D	20.75	21.05
D1	16	17.4
D2	2.86	3.26
E	15.75	16.13
E1	13.5	14.55
E2	3.68	5.1
E3	1	1.9
E4	12.38	13.43
E5	14.65	15.05
e	5.44 BSC	
L	19.73	20.48
L1	3.97	4.69
ØP	3.18	4.06
Q	5.42	5.96
S	5.85	6.49
T	17.5° REF.	
W	3.5° REF.	
X	4° REF.	

1	GATE
2	DRAIN
3	SOURCE
4	DRAIN

NOTES:
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. BURR OR MOLD FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

TITLE: PACKAGE OUTLINE DRAWING: TO-247-3L(MOSFET)

Date: 3/4/24 | REVISION NO. 02 | A4

PRD 05964 | SCALE:1:1 | SHEET 1 OF 1

Recommended Solder Pad Layout